

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE8295AD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

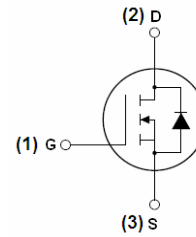
General Features

- $V_{DS} = 82V, I_D = 95A$
 $R_{DS(ON)} < 8.0 \text{ m}\Omega @ V_{GS} = 10V$ (Typ: 6.6m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Special designed for convertors and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

100% UIS TESTED!
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE8295AD	NCE8295AD	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	82	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	95	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	67	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	170	W
Derating factor		1.13	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	529	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.88	$^\circ\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

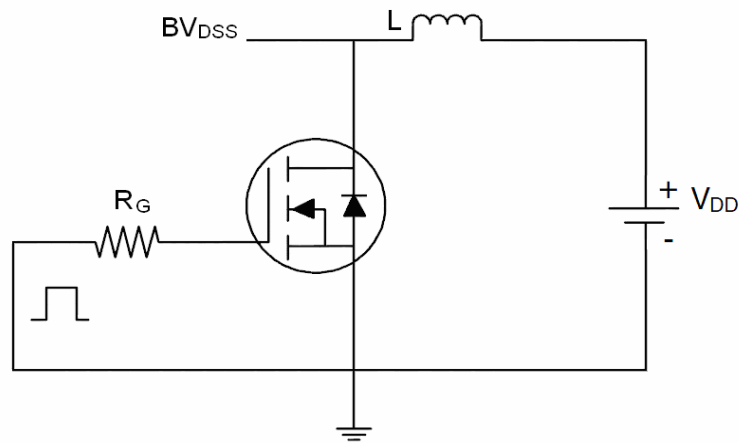
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	82	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=82V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	2.9	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	6.6	8.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	-	50	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	6800	-	PF
Output Capacitance	C_{oss}		-	353	-	PF
Reverse Transfer Capacitance	C_{rss}		-	261	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40V, R_L=15\Omega$ $R_G=2.5\Omega, V_{GS}=10V$	-	18	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	56	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	$V_{DS}=40V, I_D=50A,$ $V_{GS}=10V$	-	109.3	-	nC
Gate-Source Charge	Q_{gs}		-	35.1	-	nC
Gate-Drain Charge	Q_{gd}		-	25.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=95A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	95	A
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}\text{C}, I_F=100A$ $di/dt=100A/\mu s$ (Note 3)	-		37	nS
Reverse Recovery Charge	Q_{rr}		-		58	nC

Notes:

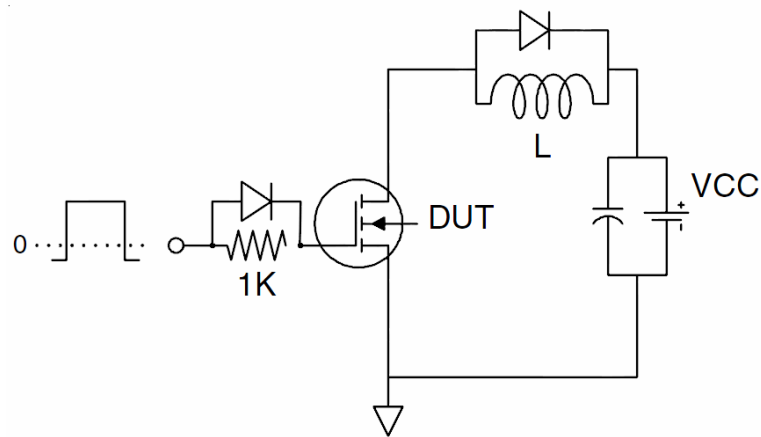
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=40V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

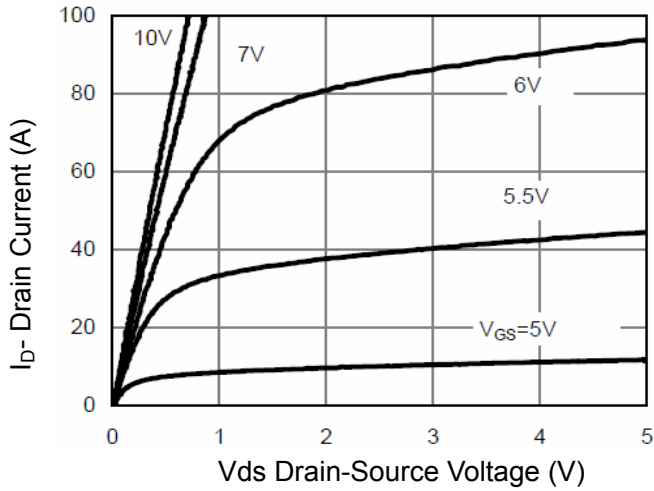


Figure 1 Output Characteristics

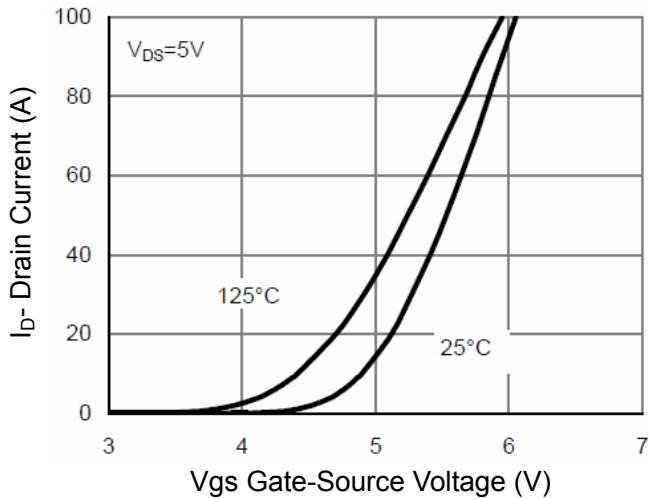


Figure 2 Transfer Characteristics

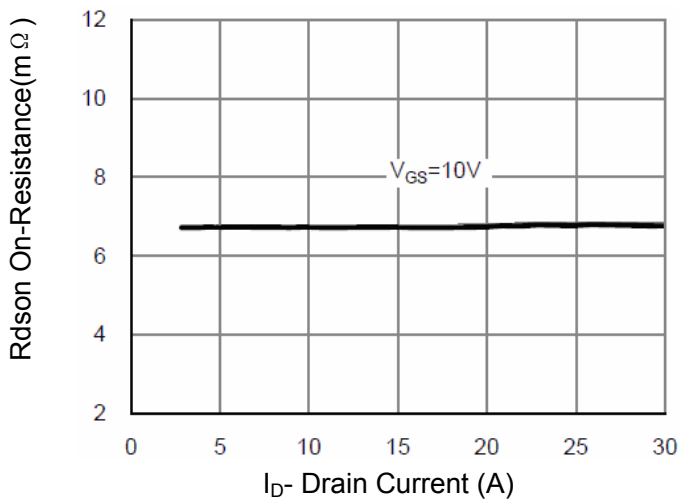


Figure 3 Rdson- Drain Current

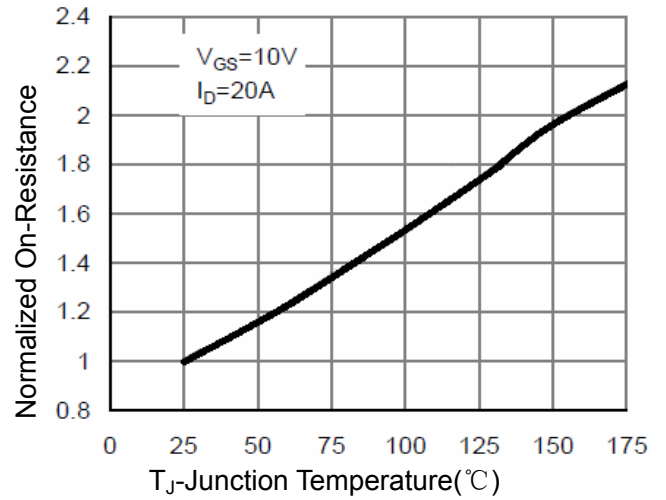


Figure 4 Rdson-Junction Temperature

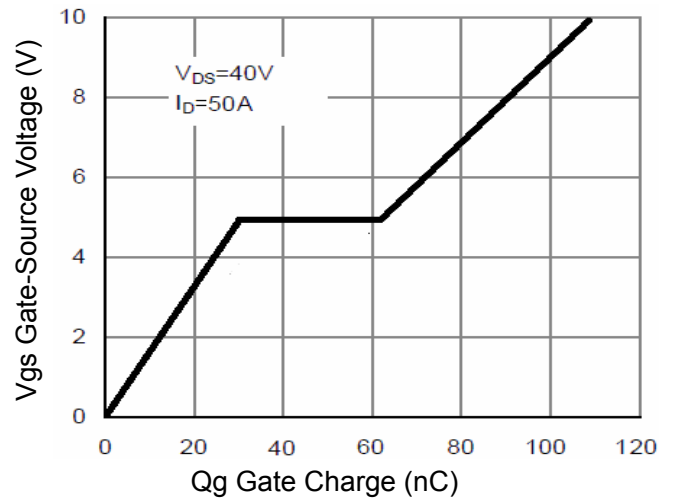


Figure 5 Gate Charge

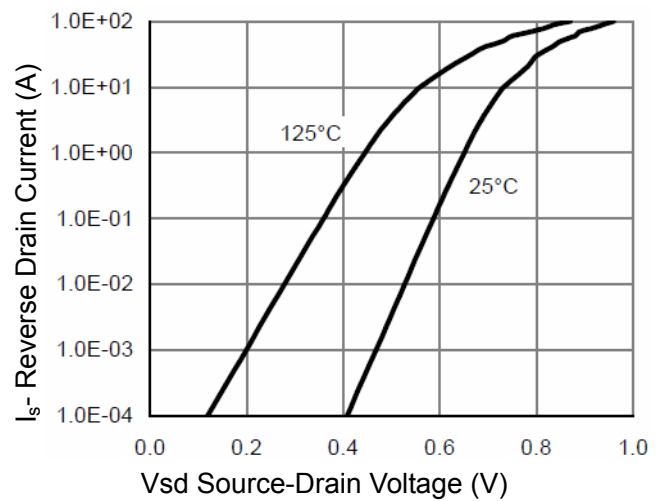


Figure 6 Source- Drain Diode Forward

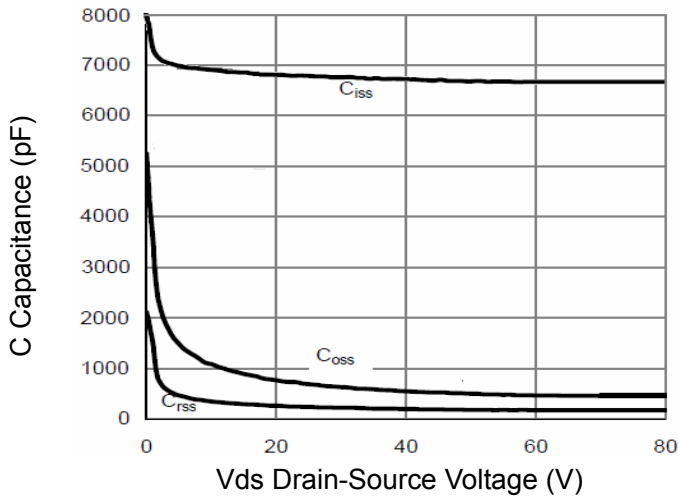


Figure 7 Capacitance vs Vds

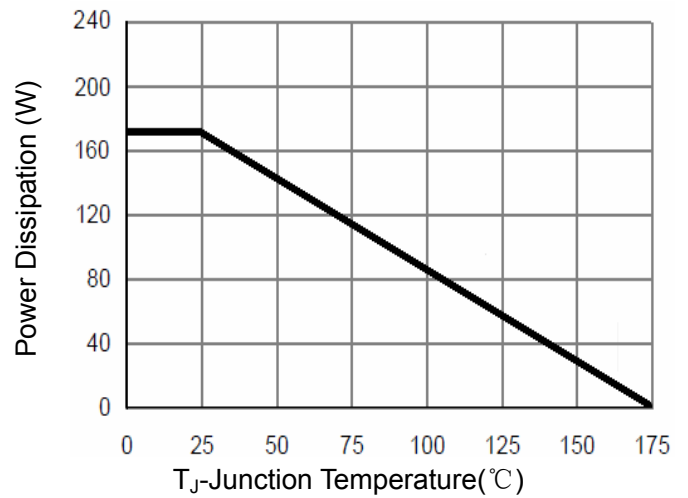


Figure 9 Power De-rating

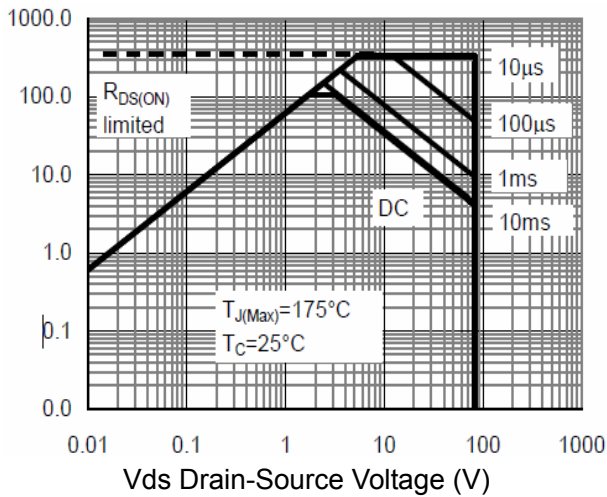


Figure 8 Safe Operation Area

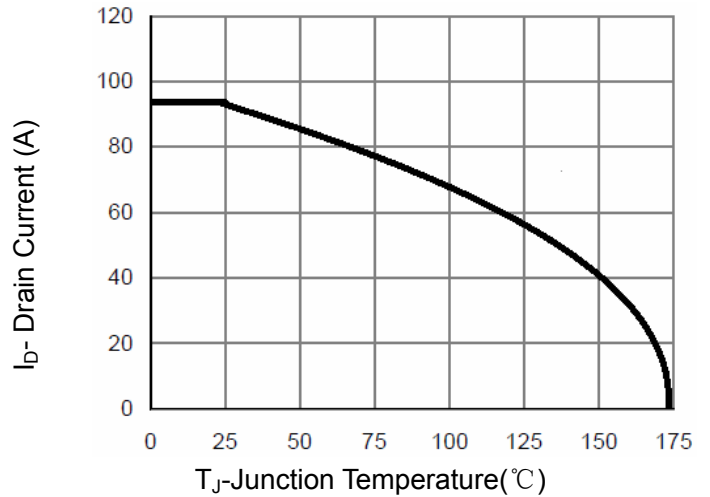


Figure 10 ID Current De-rating

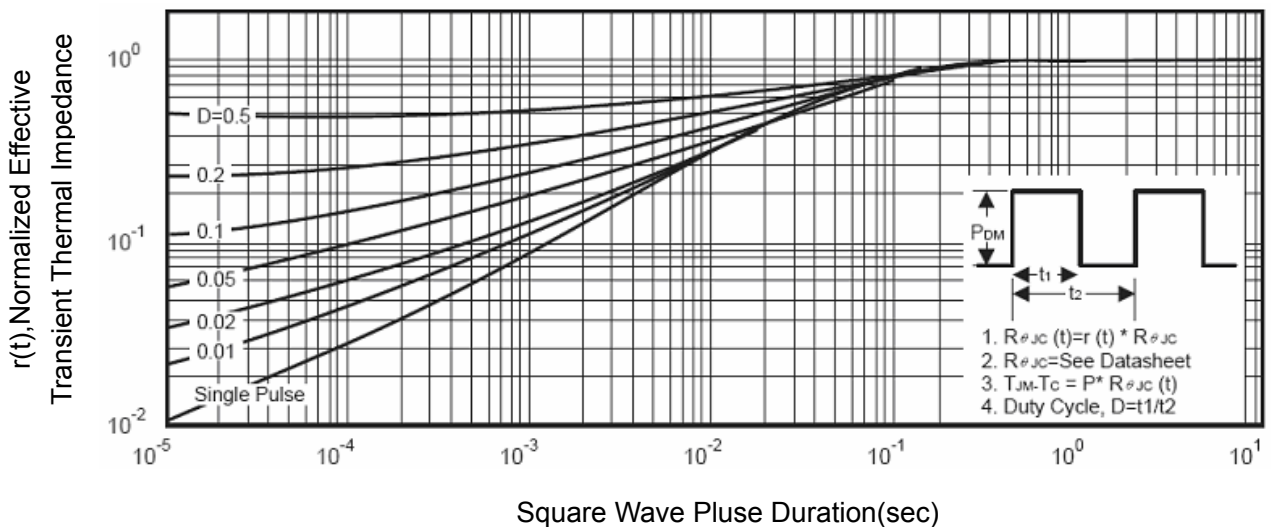
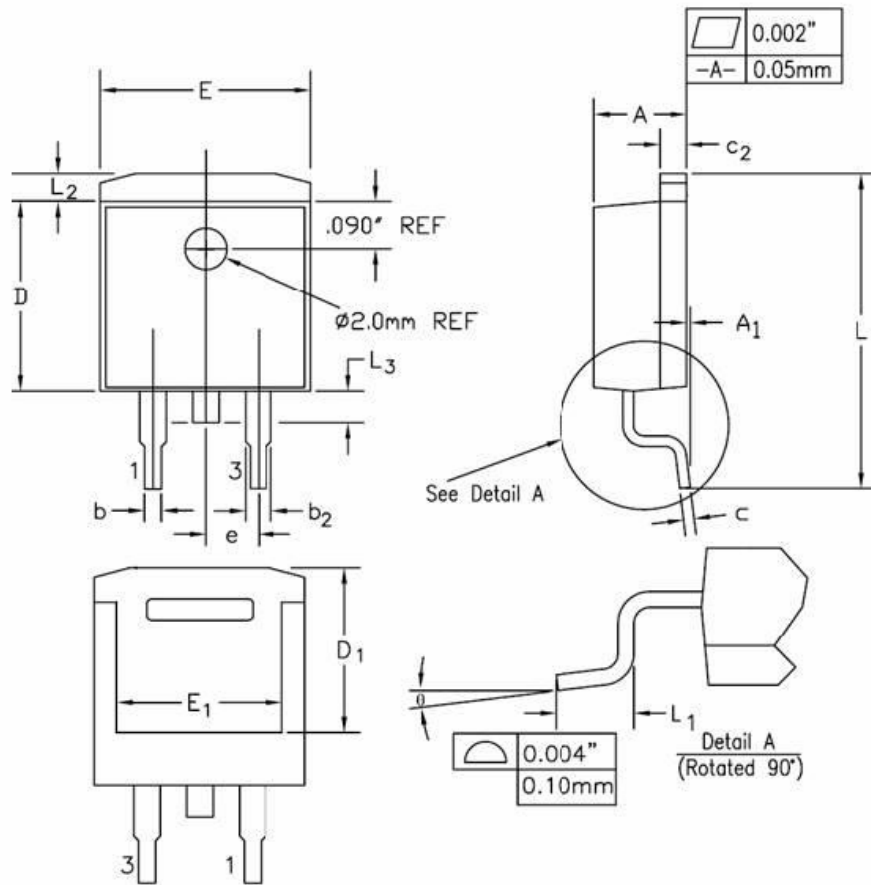


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	
A1	-	0.010	-	0.25	
b	0.028	0.037	0.71	0.94	
b2	0.045	0.055	1.15	1.40	
c	0.018	0.024	0.46	0.61	
c2	0.048	0.055	1.22	1.40	
D	0.350	0.370	8.89	9.40	
D1	0.315	0.324	8.01	8.23	
E	0.395	0.405	10.04	10.28	
E1	0.310	0.318	7.88	8.08	
e	0.100 BSC.		2.54 BSC.		
L	0.580	0.620	14.73	15.75	
L1	0.090	0.110	2.29	2.79	
L2	0.045	0.055	1.15	1.39	
L3	0.050	0.070	1.27	1.77	
θ	0°	8°	0°	8°	

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