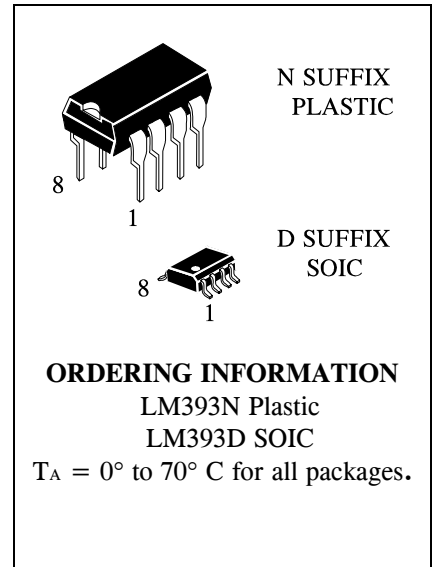


Low Power Low Offset Voltage Dual Comparators

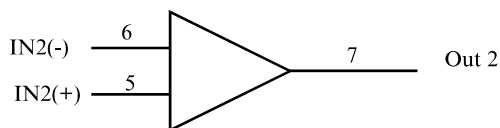
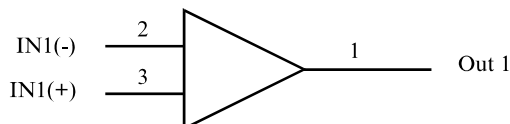
The LM393 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates.

- Single or Split Supply Operation
- Low Input Bias Current
- Low Input Offset Current
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage
- TTL and CMOS Compatible

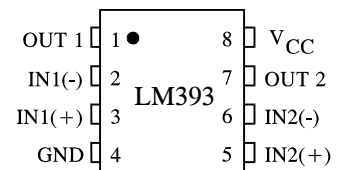


LOGIC DIAGRAM



PIN 8 = V_{CC}
PIN 4 = GND

PIN ASSIGNMENT



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Power Supply Voltages		
	Single Supply	36	V
	Split Supplies	±18	
V _{IDR}	Input Differential Voltage Range	36	V
V _{ICR}	Input Common Mode Voltage Range (1)	-0.3 to V _{CC}	V
I _{SC}	Output Short Circuit to Ground	Continuous	
I _{IN}	Input Current, per pin (2)	50	mA
T _J	Junction Temperature		
	Plastic Packages	150	°C
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1mm from Case for 10 Seconds	260	°C
P _D	Power Dissipation @T _A =25°C		
	Plastic Package	570	μW
	Derate above 25°C	5.7	mW/°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Notes:

1. Split Power Supplies.
2. V_{IN} < -0.3V. This input current will only exist when voltage at any of the input leads is driven negative.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	±2.5 or 5.0	±15 or 30	V
T _A	Operating Temperature, All Package Types	0	+70	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS($T_A=0$ to $+70^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Guaranteed Limit			Unit
			Min	Typ	Max	
V_{IO}	Input Offset Voltage	$V_0=1.4\text{V}$ $V_{CC}=5.0\text{-}30\text{V}; R_S \leq 100\Omega$ $V_{ICR}=0\text{V} - (V_{CC}-1.5)\text{V}$	-		9.0	mV
I_{IB}	Input Bias Current	$V_0=1.4\text{V}$ $V_{CC}=5.0\text{-}30\text{V}$ $V_{ICR}=0\text{V} - (V_{CC}-1.5)\text{V}$	-		400	nA
I_{IO}	Input Offset Current	$V_0=1.4\text{V}$ $V_{CC}=5.0\text{-}30\text{V}$ $V_{ICR}=0\text{V} - (V_{CC}-1.5)\text{V}$	-		± 150	nA
V_{ICR}	Input Common Mode Voltage Range	$V_{CC}=5.0\text{-}30\text{V}$	0		$V_{CC}-2.0\text{V}$	V
I_{CC}	Supply Current	$R_L=\infty, V_{CC}=5.0$ $R_L=\infty, V_{CC}=30\text{V}$	-		1.0* 2.5*	mA
A_{VOL}	Voltage Gain	$V_{CC}=15\text{V}, R_L=15\text{K}\Omega$	-	200*	-	V/mV
t_1	Large Signal Response Time	$V_{IN}=\text{TTL Logic Swing},$ $V_{ref}=1.4\text{V}, V_{CC}=5.0\text{V},$ $R_L=5.1\text{K}\Omega, V_{RL}=5.0\text{V}$	-	300*	-	ns
t_2	Response Time (Note 6)	$V_{CC}=5.0\text{V}, R_L=5.1\text{K}\Omega,$ $V_{RL}=5.0\text{V}$	-	1.3*	-	μs
I_{sink}	Output Sink Current	$V_{I(-)}=1.0\text{V}, V_{I(+)}=0\text{V},$ $V_0 \leq 1.5\text{V}, V_{CC}=5.0\text{V}$	6.0*	-	-	mA
V_{sat}	Saturation Voltage	$V_{I(-)}=1.0\text{V}, V_{I(+)}=0\text{V},$ $I_{sink} \leq 4.0\text{mA}, V_{CC}=5.0\text{V}$	-	-	700	mV
I_{OL}	Output Leakage Current	$V_{I(+)}=1.0\text{V}, V_{I(-)}=0\text{V},$ $V_0=5.0\text{V}$ $V_0=30\text{V}$		0.1*	1000	nA
V_{IDR}	Differential Input Voltage Range	All $V_{IN} \geq \text{GND}$ or V-Supply (if used)			V_{CC}	V

 *= $@25^\circ\text{C}$

TYPICAL PERFORMANCE CHARACTERISTICS

($V_{CC}=1.5V$, $T_A=+25^{\circ}C$, (each comparator))

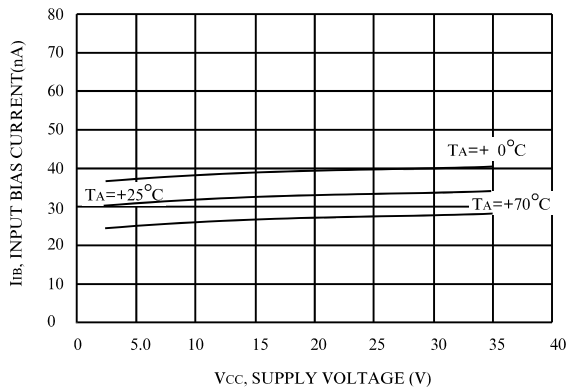


Figure 1. Input Bias Current versus Power Supply Voltage

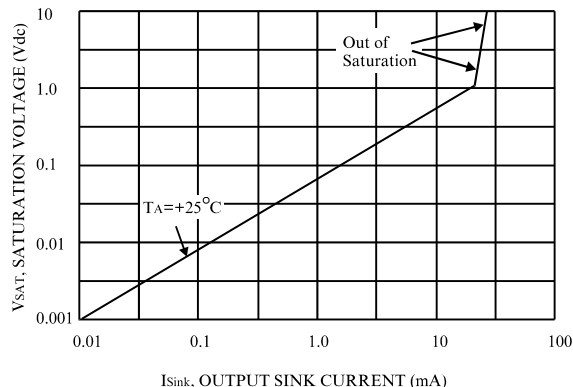


Figure 2. Output Saturation Voltage versus Output Sink Current

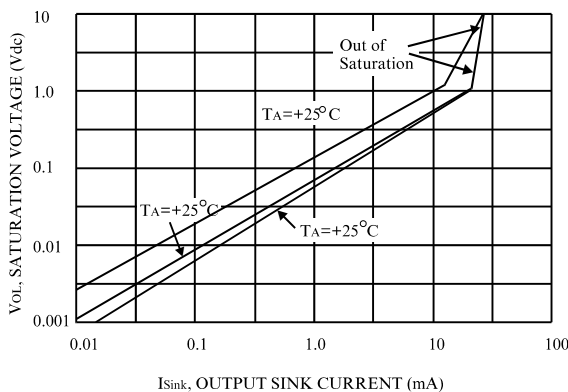


Figure 3. Output Saturation Voltage versus Output Sink Current

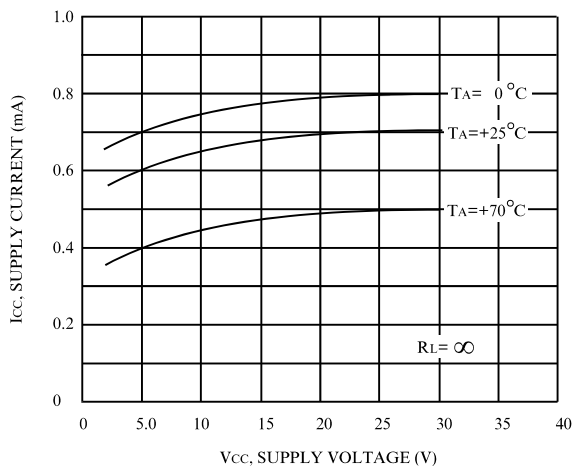


Figure 4. Power Supply Current versus Power Supply Voltage

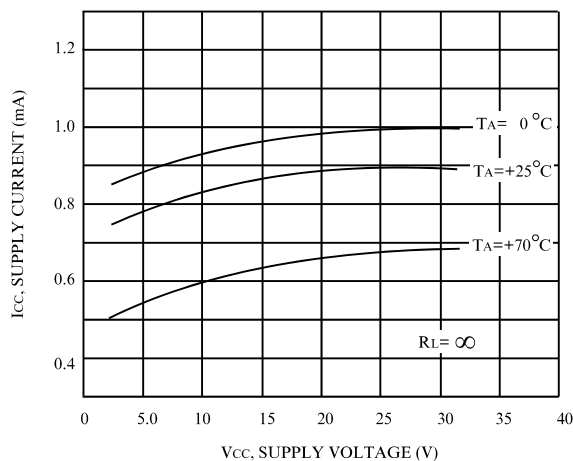


Figure 5. Power Supply Current versus Power Supply Voltage

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