SiI9292 MHL to HDMI Bridge

Data Sheet

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Patents

The subject matter described herein contains one or more inventions claimed in patents and/or patents pending owned by Silicon Image, Inc., including but not limited to the inventions claimed in US patents #6,914,637, #6,151,334, #6,026,124, #5,974,464 and #5,825,824.

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Revision History

Revision	Date	Comment
A	2/2011	Minor content update; first Production release.
B	3/2011	Update description of pin 19.

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General Description

The SiI9292 MHL to HDMI Bridge facilitates the design of low-pin count, low-power mobile-to-standard HDMI®-interoperable applications. The Silicon Image Mobile High-definition Link (MHL™) technology carries formatted video and audio from compatible transmitters, using only 3 signal lines, power, and ground (5 pins total) compared to the 19 pins required for the standard High Definition Multimedia Interface (HDMI®).

The SiI9292 bridge uses a minimum number of parts to convert MHL source devices, such as adapters, smart cables, and docking stations, to existing HDMI devices.

Silicon Image MHL products use the latest generation of Transition Minimized Differential Signaling (TMDS™) core technology. With this solution, HD camcorders, digital still cameras, and personal mobile devices can connect to a large installed base of HDMI TVs.

Together, the SiI923*x* and SiI9244 MHL transmitters and the SiI9292 bridge enable a fully compliant HDMI link solution and are pre-certified to pass HDMI compliance testing.

Features

- The MHL receiver part of the bridge receives data over a single differential pair instead of four
- To reduce bridge device cost, a microcontroller is not required if CEC support is not required.
- A single-wire control bus supports all sideband signaling for DDC, Remote Control, and Hot Plug Detect (HPD)
- The bridge converts data received in the MHL format to standard HDMI, and supports all resolutions between 25-75 MHz
- I^2C interface for configuration by local microcontroller.
- HDMI and DVI 1.0 transmitter compatibility
- Low power 1.2 V core
- 40-pin QFN, 6 mm x 6 mm body size
- Extended commercial temperature range (–20 C to +85 °C).

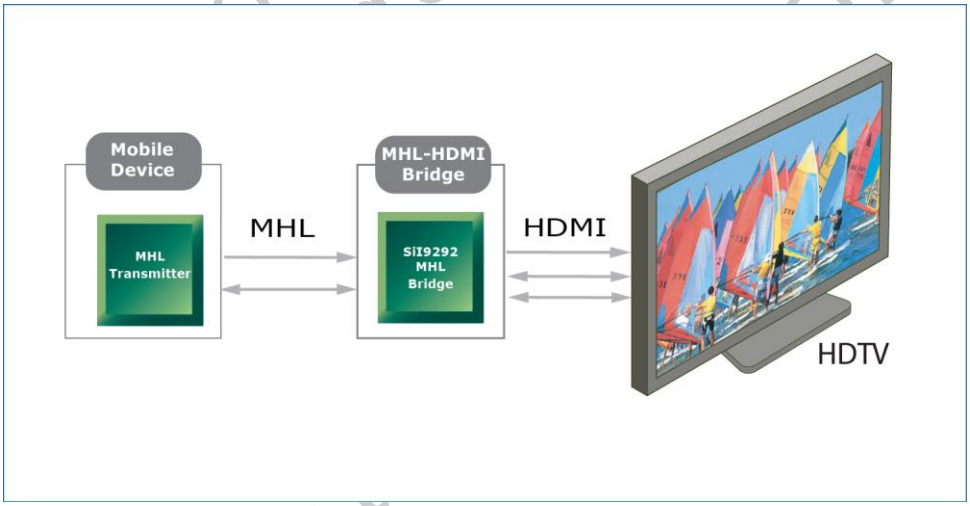


Figure 1. Typical Application as an MHL-to-HDMI Bridge

Pin Mapping

Figure 2 shows the pin diagram for the SiI9292 bridge. A description of the pin functions begins on page 10.

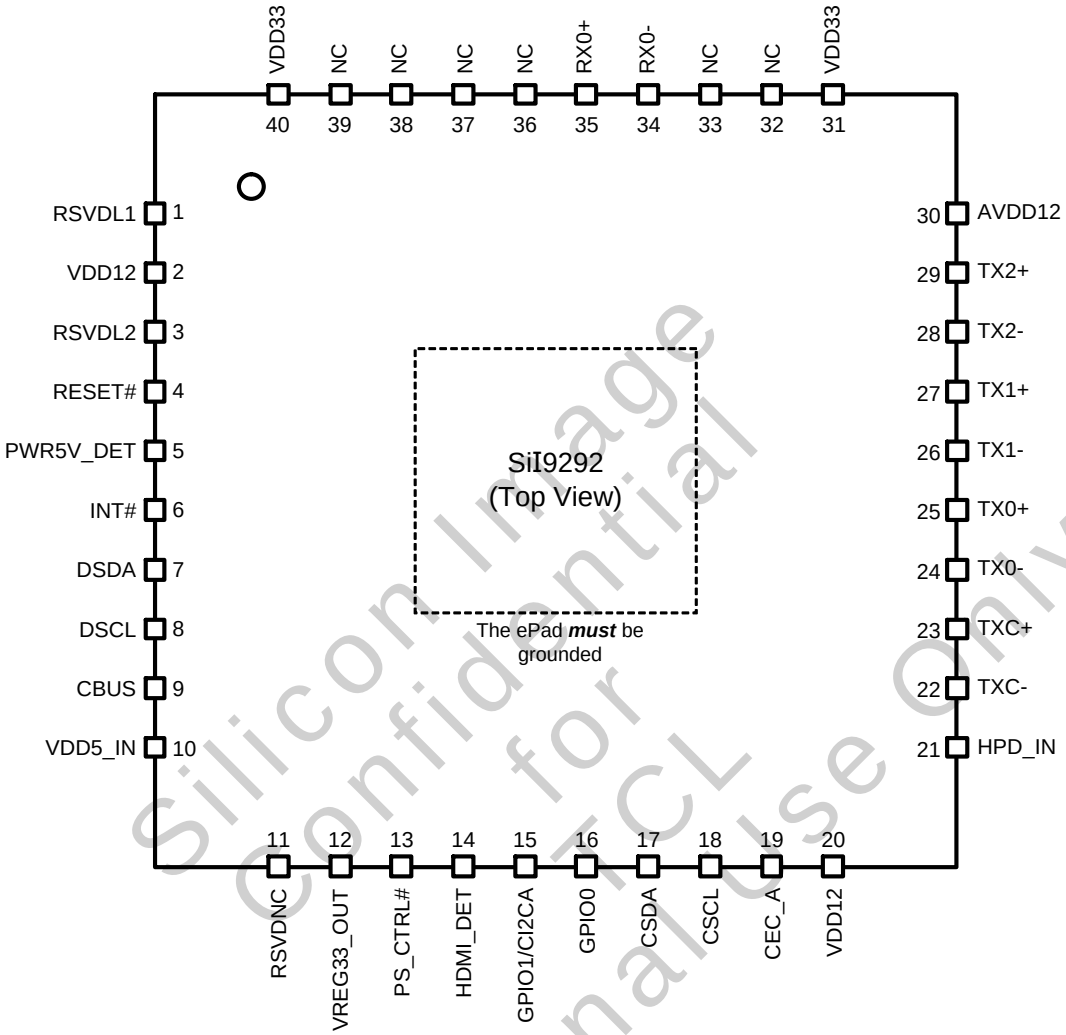


Figure 2. Pin Mapping

Functional Description

The SiI9292 bridge takes the MHL common mode clock operating at the pixel clock frequency, and the data channel running at 3 times the pixel clock rate, and generates a standard HDMI output.

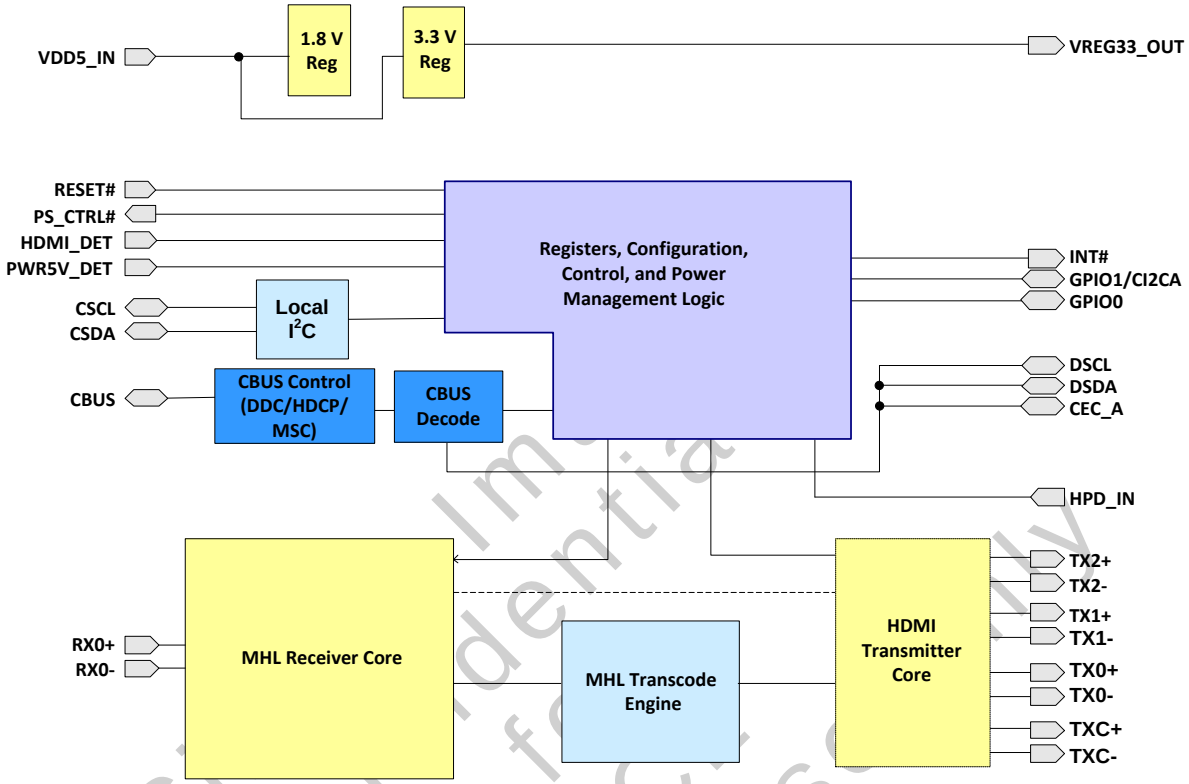


Figure 3. Functional Block Diagram

As shown in Figure 3, the bridge consists of these major blocks:

- MHL Receiver with automatic termination and equalization controls
- MHL Transcode Engine
- HDMI Transmitter with internal source termination
- CBUS Interface
- CBUS Decode and HDMI DDC and CEC interface
- Local I^2C interface
- Configuration registers, control and Interrupt logic block
- On-chip voltage regulators

MHL Receiver Block

The MHL receiver block consists of a single pair MHL standard interface. In MHL mode, the source video and audio is formatted as MHL protocol. The TMDS receiver circuitry recovers the data and passes it on for conversion back to the three-lane HDMI.

MHL Transcode Engine

The MHL Transcode Engine changes the recovered MHL data, which has a single data lane running at 3 times the HDMI rate, into HDMI format. Format conversion repacks this data into the standard 1x video rate, three-lane format associated with standard HDMI.

HDMI Transmitter Block

The transmitter block sends an HDMI stream that is based on the content of the original stream from the source. Internal source termination eliminates the requirement for external RC components for signal shaping.

CBUS Interface

The CBUS signal handles the MHL Control Bus Interface. The MHL transmitter and receiver follow a specific communication and arbitration protocol to exchange EDID, Control, and HDCP information that would normally pass over the DDC clock and data wires. In addition, device remote control commands and hot plug status is also exchanged. All of the communication is managed transparently, so the source and bridge logic operate as if they had discrete DDC, control, and HPD signals.

CEC Interface Block

The Consumer Electronics Control (CEC) Interface, which is part of the CBUS Decode block, sends and receives CEC-compliant signals using the CEC_A signal. A host microcontroller translates RCP (Remote Control Protocol) commands from the host MHL device over the CBUS to CEC commands using the CPI programming interface. The CEC controller in turn sends and receives commands. Using the CEC interface is optional and is used to translate between the RCP and CEC protocols in dongle applications.

Downstream Sink Hot Plug

The HPDIN (Hot Plug) signal is used to detect the connection status of the HDMI sink device. The power management state machine uses this information, and it is also available to the MHL source device over the CBUS.

Downstream Sink DDC Interface

The Downstream DDC Interface is part of the CBUS Decode block and is used to read HDCP and EDID information from the downstream sink device in MHL mode. The DDC interface is encoded and decoded by the Control bus decode block and sent over the CBUS interface to the MHL source device.

Configuration, Local I^2C, POR, and Interrupt Logic Block

The Configuration block is used to configure and control the operation of the device, which can operate in either I^2C mode (*smart* dongle mode with microcontroller) or *standalone* mode (basic bridge or dongle mode). During local register reads only sequential I^2C read mode is supported by SiI9292 bridge. The Power-On Reset (POR) circuit is also contained in this block. POR provides an on-chip reset function that is primarily to eliminate the need for an external power on reset circuit. The power-on default is the basic dongle mode. Refer to the Programmer's Reference for more information on configuration for smart dongle mode.

On-Chip Regulators

The chip contains two regulators that provide the internal CBUS 1.8 V and external 3.3 V power sources derived from the VDD5_IN (5 V input) to the chip. The on-chip regulators provide a lower cost system implementation by eliminating the need for external voltage regulator.

Example System Block Diagram

Figure 4 shows an example of a system block diagram with an external 5 V charging adapter and microcontroller option.

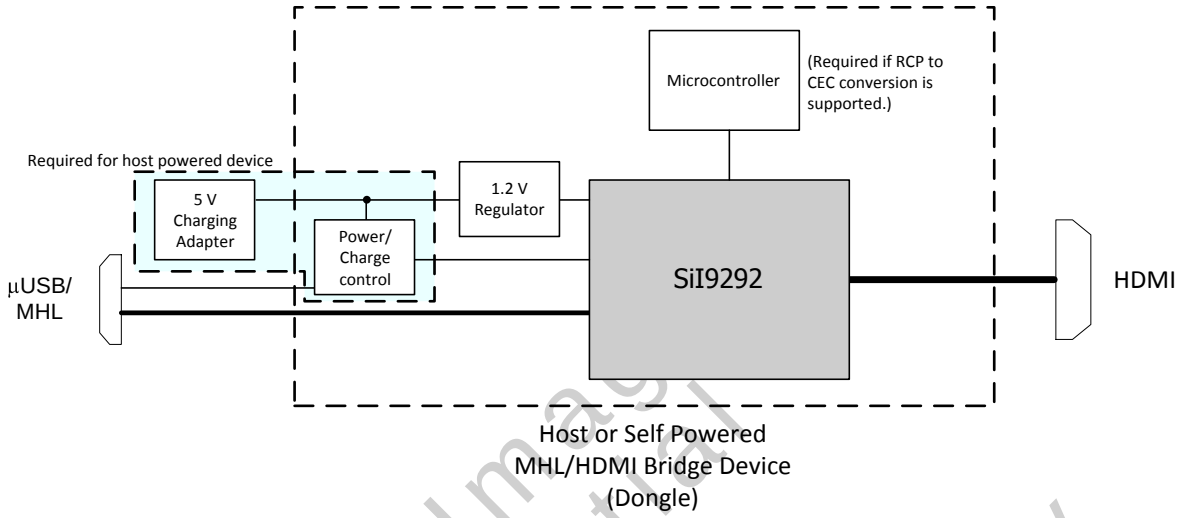


Figure 4. MHL to HDMI Bridge Mode

Electrical Specifications

Table 1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD5V_IN	Primary on-chip regulator supply voltage	−0.5	—	5.7	V	1, 2, 3
VDD12	Core Supply Voltage	−0.3	—	2.0	V	1, 2
VDD33	TMDS I/O Supply Voltage	−0.3	—	4.0	V	1, 2
AVDD12	Analog I/O Supply Voltage	−0.3	—	2.0	V	1, 2
VREG33_OUT	On-Chip regulator output voltage	−0.3	—	4.0	V	1, 2
V_I	Input voltage	−0.3	—	VDD33 + 0.3	V	1, 2
V_O	Output voltage	−0.3	—	VDD33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input voltage on 5 V-tolerant pins	−0.3	—	5.5	V	—
T_J	Junction temperature	—	—	125	°C	—
T_{STG}	Storage temperature	−65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.

Table 2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD5V_IN	Primary on-chip regulator supply voltage	4.3	5.0	5.5	V	—
VDD33	TMDS I/O supply voltage	3.15	3.3	3.45	V	1
VDD12	Core supply voltage	1.08	1.2	1.32	V	—
AVDD12	Analog I/O Supply Voltage	1.08	1.2	1.32	V	—
VREG33_OUT	On-Chip regulator output voltage	3.15	3.3	3.45	V	—
V_{DDN}	Supply voltage noise	—	—	100	$mV_{P\text{-}P}$	2
T_A	Ambient temperature (with power applied)	-20	+25	+85	°C	—
Θ_{ja}	Ambient thermal resistance (Theta JA)	—	—	32	°C/W	3
Θ_{jc}	Junction to case resistance (Theta JC)	—	—	24	°C/W	3

Notes:
1. The HDMI Specification requires termination voltage (VDD33) to be controlled to 3.3 V ±5%.
2. The supply voltage noise is measured at test point VDDTP as shown in Figure 5. The ferrite bead provides filtering of power supply noise.
3. Airflow at 0 m/s, 4-layer PCB.

See the Power Supply Decoupling section on page 14 for the recommended decoupling for power supplies.

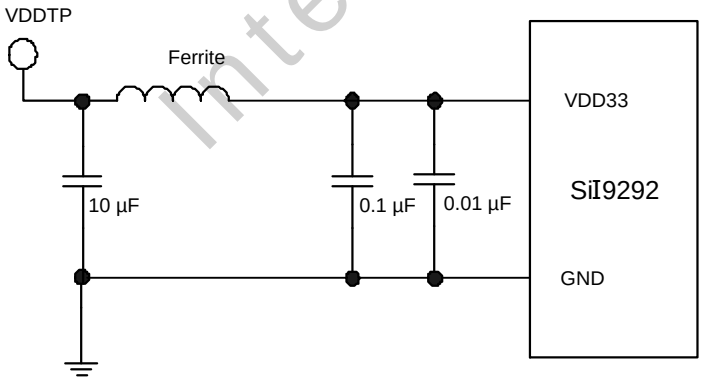


Figure 5. Test Point VDDTP for VDD Noise Tolerance Specification

DC Specifications

Table 3. DC Power Supply Specifications

Symbol	Parameter	HDMI Output Frequency	VDD33 Source*	Typ			Max			Units
				VDD5_IN	VDD33	VDD12 AVDD12	VDD5_IN	VDD33	VDD12 AVDD12	
I_{DDSB}	Standby current	—	External	2	0.5	2	3	3	14	mA
	MHL Input									
I_{DDFP}	Full operation state current	25 MHz	External	2.2	32	80	3.7	36	96	mA
		75 MHz	External	2.2	32	153	3.7	36	165	mA
			Internal	37	—	153	40	—	165	mA

***Note:** For VDD Internal Source, connect VREG33_OUT to VDD33. For VDD External source, connect an external 3.3 V source to VDD33.

Table 4. Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	Conditions[2]	Min	Typ	Max	Units	Note
V_{TH+DDC}	LOW to HIGH threshold	Schmitt trigger $_{DDC}$	—	3.0	—	—	V	8
V_{TH-DDC}	HIGH to LOW threshold	Schmitt trigger $_{DDC}$	—	—	—	1.5	V	8
V_{TH+CEC_A}	LOW to HIGH threshold, CEC_A pin	Schmitt trigger$_{CEC_A}$	—	2.0	—	—	V	—
V_{TH-CEC_A}	HIGH to LOW threshold, CEC_A pin	Schmitt trigger$_{CEC_A}$	—	—	—	0.8	V	—
V_{TH+}	LOW to HIGH threshold	Schmitt trigger	—	1.75	—		V	6, 7
V_{TH-}	HIGH to LOW threshold	Schmitt trigger	—		—	1.1	V	6, 7
I_{Oz}	Output leakage current	—	High impedance	−10	—	10	µA	—
I_{IL}	Input leakage current	—	—	−10	—	10	µA	—
V_{ID}	Differential input voltage	—	—	75	250	1000	mV	4
V_{OD}	Differential output single-ended swing amplitude	TMDS	RLOAD = 50 Ω	400	500	600	mV	—
V_{DOH}	Differential HIGH level output voltage	TMDS	—	—	3.3	—	V	—
I_{DOS}	Differential output short-circuit current	TMDS	VOUT = 0 V	—	—	5	µA	—
I_{OD8}	General digital output drive	Output	V_{OH} = 2.4 V	7.5	—	—	mA	1, 6, 7
			V_{OL} = 0.4 V		—	—	mA	1, 6, 7
I_{ODDDC}	I^2C digital output drive	Output	V_{OL} = 0.5 V	3.0	—	—	mA	1, 6, 8
I_{ODCEC_A}	CEC_A digital output drive	Output	V_{OH} = 2.4 V	4.0	—	—	mA	9
			V_{OL} = 0.4 V					

Notes:

1. These limits are guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading C_L = 10 pF.
3. Refer to Pin Descriptions section (beginning on page 10) for pin type designations for all package pins.
4. Differential input voltage is a single-ended measurement, according to the DVI Specification.
5. Only these Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively and are guaranteed by design.
6. Minimum output drive specified at ambient = 70 °C and VDD33 = 3.0 V. Typical output drive specified at ambient = 25°C and VDD33 = 3.3 V. Maximum output drive specified at ambient = −20 °C and VDD33 = 3.6 V.
7. I_{OD8} Output applies to all pins defined as LVTTL and LVTTL/Schmitt trigger.
8. I_{ODDDC} Output applies to all pins defined as Schmitt trigger$_{DDC}$.
9. I_{ODCEC_A} Output applies to CEC_A pin.

Table 5. Digital CBUS I/O Specifications

V_{IH_CBUS}	LOW to HIGH threshold, CBUS pin	CBUS	—	1.0	—	—	V	—
V_{IL_CBUS}	HIGH to LOW threshold, CBUS pin	CBUS	—	—	—	0.6	V	—
V_{OH_CBUS}	Output HIGH Voltage, CBUS pin	CBUS	IOVCC18 = 1.8 V, 85 °C	1.5	—	1.9	V	—
V_{OL_CBUS}	Output LOW Voltage, CBUS pin	CBUS	IOVCC18 = 1.8 V, 85 °C	—	—	0.2	V	—
I_{OH_CBUS}	HIGH output drive current	CBUS	VOH = 1.5 V	2	—	—	mA	—
I_{OL_CBUS}	LOW output drive current	CBUS	VOL = 0.2 V	300	—	—	µA	—
$I_{IL/IIH}$	Input Leakage Current	CBUS	High impedance	–1.0	—	1.0	µA	—
$Z_{CBUS\_SINK\_DISCOVER}$	Pull down resistance - discovery	CBUS	—	800	1000	1200	Ω	—
$Z_{CBUS\_SINK\_ON}$	Pull down resistance - ON	CBUS	—	90	100	110	kΩ	—

AC Specification

Table 6. TMDS Input Timings

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Units	Notes
F_{RXC2}	Common-mode input clock frequency	MHL Mode	25	—	75	MHz	2
T_{RXC2}	Common-mode input clock period	MHL Mode	13.33	—	40	ns	—

Notes:
1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. MHL Mode, 1X clock 3X data rate.

Table 7. TMDS Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
F_{CYC}	Clock frequency	MHL Input	25	—	75	MHz	—
T_{CYC}	Clock period	MHL Input	13.33	—	40	ns	—
S_{LHT}	Differential swing LOW-to-HIGH transition time	—	75	—	490	ps	—
S_{HLT}	Differential swing HIGH-to-LOW transition time		75	—	490	ps	—

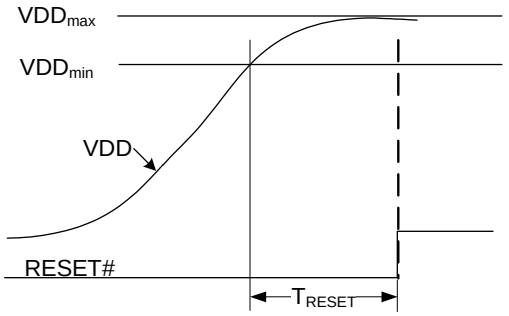
Table 8. Miscellaneous Timings

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	Delay from falling edge of I^2C clock that I^2C data is valid	C_L = 400 pF	—	—	700	ns	—	—
F_{DDC}	Speed on HDMI DDC port	C_L = 400 pF	—	—	100	kHz	—	2
F_{I2C}	Speed on local I^2C port	C_L = 400 pF	—	—	400	kHz	—	3
T_{RESET}	RESET# signal LOW time for valid reset	—	10	—	—	ms	Figure 6	—

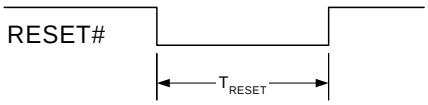
Notes:
1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. DDC port is limited to 100 kHz by the HDMI Specification, and meets I^2C Standard mode timings.
3. Local I^2C port (CSCL/CSDA) meets Standard mode I^2C timing requirements to 400 kHz.

Timing Diagrams

Power sequencing is not required for the SiI9292 device. However to ensure a proper RESET, the rules mentioned under the diagrams in Figure 6 must be followed.



VDD must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET# is HIGH.



When using the external reset function, RESET# must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET# LOW until T_{RESET} after stable power (as shown at left); **or** by pulling RESET# LOW from a HIGH state (as shown above) for at least T_{RESET}.

Figure 6. RESET# Minimum Timing

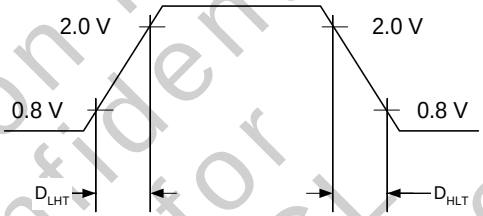


Figure 7. Digital Output Transition Times

Pin Descriptions

MHL/HDMI Receiver Port Pins

Pin Name	Pin	Type	Dir	Description
RX0+	35	TMDS	Input	MHL Input Port Data pair. Series termination resistors are required for each pin. See the High-Speed TMDS Signals section on page 14 for details.
RX0-	34	TMDS	Input	
CBUS	9	Custom CBUS Schmitt 5-V tolerant	Input/ Output	In MHL mode this pin is the Control Bus signal. The CBUS signal is for communication between the MHL transmitter and receiver using a 1.8 V signal level.

HDMI Transmitter Port Pins

Pin Name	Pin	Type	Dir	Description
TX0+	25	TMDS	Output	TMDS data pair 0.
TX0-	24	TMDS	Output	
TX1+	27	TMDS	Output	TMDS data pair 1.
TX1-	26	TMDS	Output	
TX2+	29	TMDS	Output	TMDS data pair 2.
TX2-	28	TMDS	Output	
TXC+	23	TMDS	Output	TMDS clock pair.
TXC-	22	TMDS	Output	
HPD_IN	21	Schmitt 5 V tolerant	Input	TX Hot Plug Detection input. An external 10 kΩ pulldown resistor is required on this pin.
CEC_A	19	CEC compliant	Input/ Output	Interface to CEC devices. Interface to CEC devices. CEC electrical spec compliant signal. Powered by VDD33. Only use this pin with a microcontroller. When used in standalone mode or dongle configuration, this pin must be left unconnected. This pin has an internal pullup; therefore an external 27 kΩ resistor is not required.
DSCL	8	I^2C compliant Open drain 5 V tolerant	Input/ Output	DDC Clock and Data for transmitter (I^2C Master). These pins implement true open-drain circuits; external pullup (1.8 kΩ ±10% typical) resistors to DDC 5 V are required. These are 5 V tolerant pins.
DSDA	7	I^2C compliant, Open drain, 5 V tolerant	Input/ Output	

Control and Configuration Pins

Pin Name	Pin	Type	Dir	Description
RESET#	4	LVTTL Schmitt 5 V tolerant	Input	External Reset pin. (Active low). This pin has an Internal pullup; it can be left open when external reset is not required.
CSCL	18	LVTTL Schmitt Open drain 5 V tolerant	Input/ Output	Local I^2C Clock. This pin is true open drain, so it does not pull to ground if power is not applied. An external pullup resistor to 3.3 V is required.
CSDA	17	LVTTL Schmitt Open drain 5 V tolerant	Input/ Output	Local I^2C Data. This pin is true open drain, so it does not pull to ground if power is not applied. An external pullup resistor to 3.3 V is required
PS_CTRL#	13	LVTTL/ Open Drain 5 V tolerant	Output	Power Supply Control Output. Active LOW output used to control an external MOSFET power switch to enable VBUS back to the host after MHL discovery has been completed.
INT#	6	LVTTL Open drain 5 V tolerant	Output	Active LOW interrupt output to host controller. This is an open drain output and requires an external pullup resistor.
GPIO0	16	LVTTL Schmitt 5 V tolerant	Input/ Output	General Purpose Input/Output 0. See the Programmer's Reference for more details.
GPIO1 CI2CA	15	LVTTL Schmitt 5 V tolerant	Input/ Output	General Purpose Input/Output 1/CI2CA. This pin defaults to an input and is sampled once at reset to select the local I^2C target address ranges, as follows: LOW = 0xD0, 0xC0, 0xC8 HIGH = 0xD4, 0xC4, 0xCC See the Programmer's Reference for more details.
HDMI_DET	14	LVTTL Schmitt 5 V tolerant	Input	Pull this pin LOW through a 10 kΩ resistor to ground.
PWR5V_DET	5	LVTTL Schmitt 5 V tolerant	Input	Senses External 5 V charger input to change power provisioning. Connect this pin to the local 5 V power supply when using self-powered dongle configurations.

Power and Ground Pins

Pin Name	Pin	Type	Description
GND	ePad	Ground	Ground. All ground connections to the device are through the ePad; therefore it ***must*** be soldered to the board and the pad must have a low resistance connection to the board ground plane.
VDD12	2, 20	Power	Digital Core VDD from external regulator.
AVDD12	30	Power	Analog Core VDD from external regulator.
VDD33	31, 40	Power	Receiver termination 3.3 V analog supply input. Connect to an external 3.3 V regulator or to VREG33_OUT as described below.
VDD5V_IN	10	Power	Connect this pin to the HDMI +5 V input or VBUS +5 V input from a MHL Source.
VREG33_OUT	12	Power	Internal 3.3 V regulator output. When this on-chip regulator is used, it should be externally connected to VDD33 (pins 31 and 40). Additional decoupling capacitors are required; see the Power Supply Decoupling section on page 14 for an example circuit. When an external 3.3 V regulator is used to supply power to VDD33, this pin must be left open.

Reserved Pins

Name	Pin	Type	Description
RSVDL1	1	Reserved	This pin must be connected to GND in normal operation.
RSVDL2	3	Reserved	This pin must be connected to GND in normal operation.
RSVDNC	11	Reserved	This pin must be left unconnected in normal operation.

System Design Guidelines

The tolerance of all resistors shown in this section is ±5% unless otherwise noted.

Adapter Application

In the adapter application, there are two modes, bus-powered and self-powered. In the self-powered mode, the external power supply control circuitry is shown in Figure 8. In the VBUS powered mode, external CBUS circuitry is required to isolate the unpowered device loading and also to provide the 1 kΩ detection resistance to the source device as shown in Figure 9.

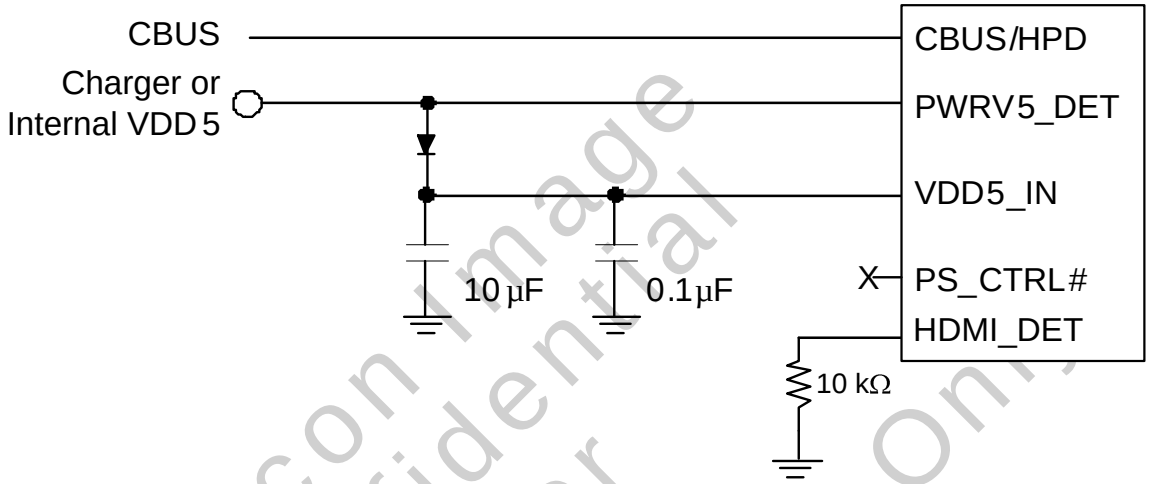


Figure 8. Self-Powered Dongle

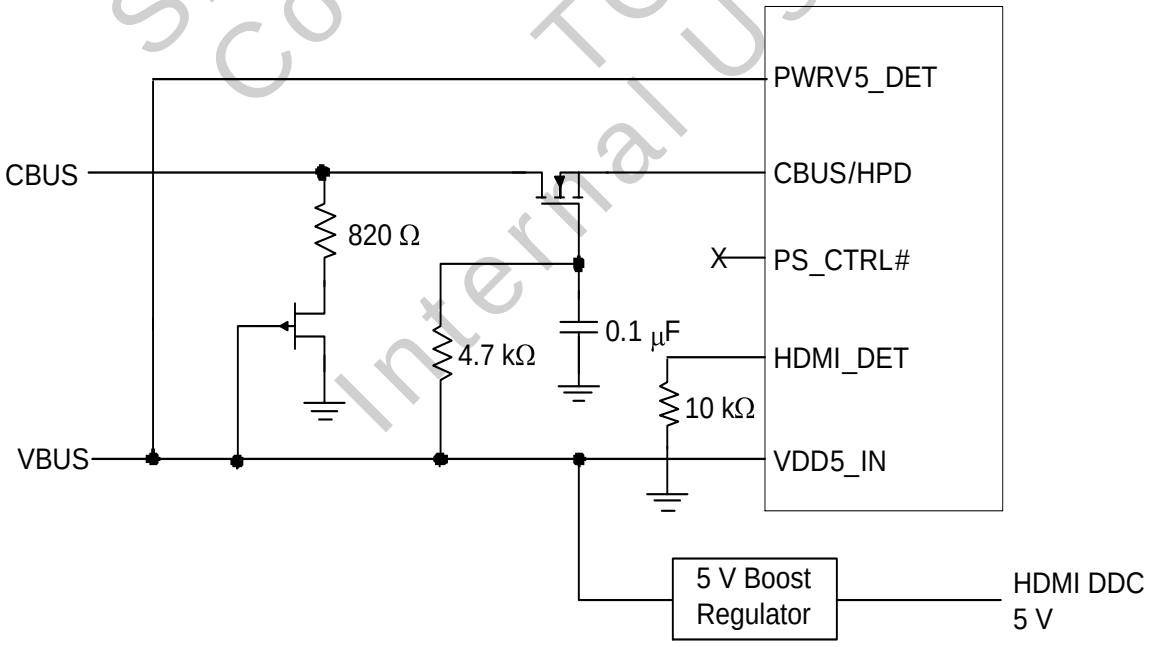


Figure 9. BUS-Powered Dongle with Isolation Circuit

Power Supply Decoupling

Silicon Image recommends that designers include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 10. Place these components as close as possible to the SiI9292 device pins and avoid routing traces through vias, if possible. An example of this layout configuration is shown in Figure 11. Pins in each of the VDD12 and VDD33 groups can share C2, C3, and L1, with each pin having a separate C1 placed as close as possible to the pin. Suggested values for C1, C2 and C3 are 0.01 µF, 0.1 µF, and 10 µF, respectively. The recommended impedance of the ferrite is 10 Ω or more in the frequency range of 1–2 MHz for all power supplies.

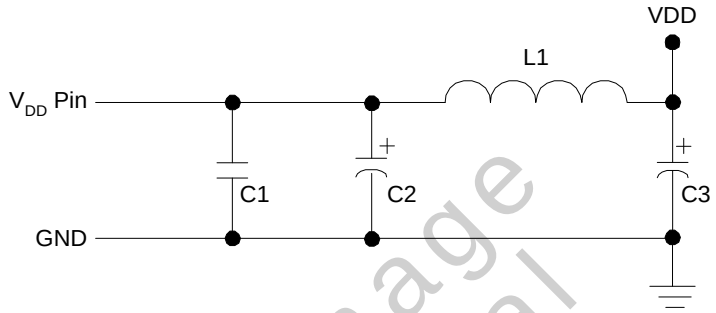


Figure 10. Decoupling and Bypass Schematic

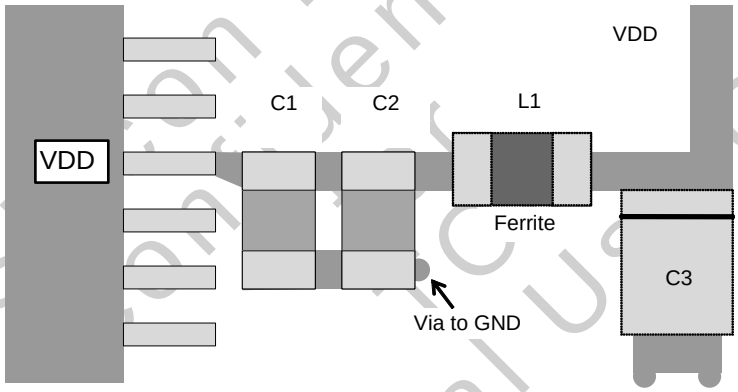


Figure 11. Decoupling and Bypass Capacitor Placement

High-Speed TMDS Signals

Layout Guidelines

The layout guidelines below help to ensure signal integrity, and Silicon Image strongly encourages the board designer to follow the guidelines below.

- Place the input and output connectors that carry the TMDS signals as close as possible to the chip.
- Place a 5.1 Ω ± 5% or better series resistor as close as possible to each TMDS receiver pin (see the Termination Requirement section on page 15 for details).
- Route the differential lines as directly as possible from the connector to the device when using industry-standard HDMI connectors.
- Route the two traces of each differential pair together.
- Minimize the number of vias through which the signal lines are routed.
- Lay out the MHL input pin traces with a controlled differential impedance of 100 Ω and a common mode impedance of 30 Ω. The differential impedance of the HDMI output pins must be designed within ±15% of 100 Ω.
- Serpentine traces are not recommended to compensate for inter-pair trace skew.

Termination Requirement

A 5.1 Ω resistor, shown as *R* in Figure 12, must be placed in series with the SiI9292 Rx0± pins. In addition, the distance from the resistor to the MHL receiver pins, designated as *d* in the figure, must be within 1 cm or 393 mils, to ensure the impedance does not deviate from the limits allowed by the MHL 1.0 Specification.

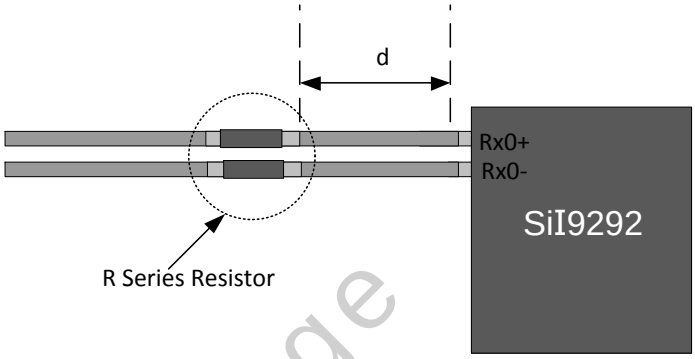


Figure 12. TMDS Signal Termination

ESD Protection

The SiI9292 bridge can withstand electrostatic discharges due to handling during manufacture. In applications where higher protection levels are required, ESD-limiting components can be placed on the differential lines of the chip. These components typically have a capacitive effect that reduces the signal quality at higher clock frequencies. Use the lowest capacitance devices possible. ESD components must be placed after the series termination resistors and as close as possible to the input or output connector. In no case can the capacitance value of these components exceed 1 pF.

EMI Considerations

Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines, except the common-mode chokes and ESD protection described earlier. The differential signaling used in HDMI is inherently low in EMI if the routing recommendations noted in the Layout Guidelines section are followed.

The PCB ground plane should extend unbroken under as much of the bridge chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

Packaging

ePad Requirements

The SiI9292 chip is packaged in a 40-pin QFN package with an Exposed Pad™ (ePad™), used both for electrical connectivity and for improved thermal transfer characteristics. The ePad dimensions are shown on the following page. Soldering of the ePad is ***required*** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground.

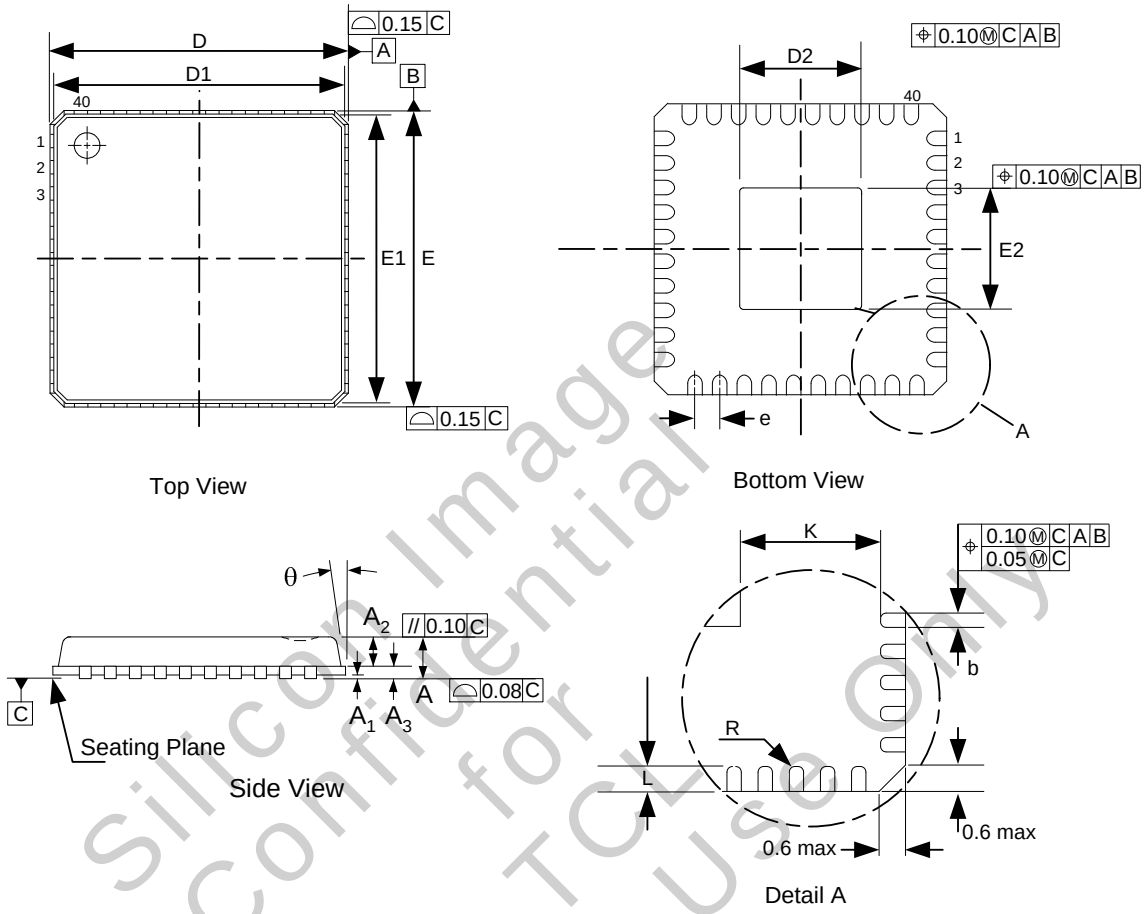
Note: The ePad must be soldered to the PCB ground. Provide a landing area on the PCB with dimensions and location corresponding to the ePad within the footprint of the package. The size of this landing area can be larger than the ePad on the package but should be at least the same as the maximum size of exposed pad of the package (2.50 mm x 2.50 mm). If any circuit traces are within the area of the maximum size of the ePad, the trace may short to the pad if the package has a pad with the maximum dimensions.

The thermal land area on the PCB can use thermal vias to improve heat removal from the package. These thermal vias can double as ground connections, attaching internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, Silicon Image recommends that the via diameter be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel be plated with 1-ounce copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off is also a consideration. For a nominal stand-off of approximately 0.1 mm (see dimension A1), the stencil thickness of 5 mils to 8 mils provide a good solder joint between the ePad and the thermal land.

Package Dimensions

Package drawings are not to scale.



JEDEC Package Code MO-220

Item	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A_1	Stand-off	0.00	0.02	0.05
A_2	Body thickness	0.60	0.65	0.70
A_3	Base thickness		0.20 REF	
D	Body size	5.90	6.00	6.10
E	Body size	5.90	6.00	6.10
D_1	Footprint		5.75 BSC	
E_1	Footprint		5.75 BSC	

Item	Description	Min	Typ	Max
D_2	ePad size	2.35	2.50	2.65
E_2	ePad size	2.35	2.50	2.65
b	Plated lead width	0.18	0.23	0.30
e	Lead pitch		0.50 BSC	
L	Lead foot length	0.30	0.40	0.50
θ	Mold angle	0°	—	12°
R	Lead tip radius	0.09	—	—
K	Lead to ePad clearance	0.20	—	—

Figure 13. 40-pin QFN Package Diagram

Marking Specification

Marking drawing is not to scale.

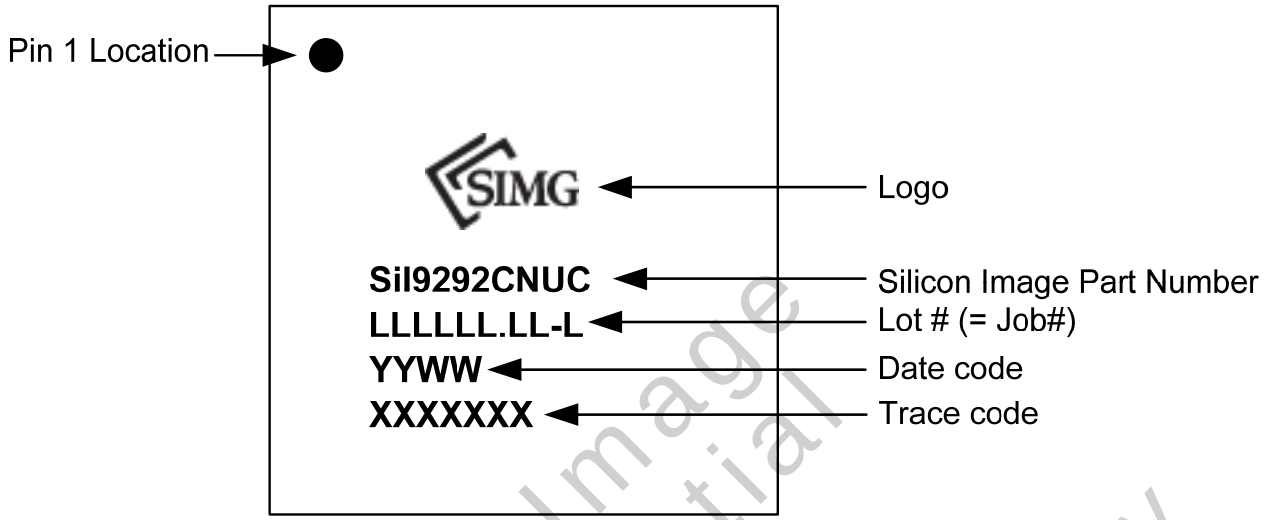


Figure 14. Marking Diagram

Ordering Information

Production Device Type	Device Number
Universal	SiI9292CNUC

The universal package can be used in lead-free and ordinary process lines.

References

Standards Documents

Table 9 lists the abbreviations used in this document. Contact the responsible standards groups listed in Table 10 for more information on these specifications.

Table 9. Referenced Documents

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface, Revision 1.4a*, HDMI Consortium, March 2010
HCTS	*HDMI Compliance Test Specification, Revision 1.4a*, HDMI Consortium, March 2010
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group, April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA, Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, March 2001
CEA-861-D	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, Draft 020328, EIA/CEA, July 2006
EDDC	*Enhanced Display Data Channel Standard, Version 1.1*, VESA, March 2004
I^2C	*The I^2C Bus Specification*, Version 2.1, Philips Semiconductors, January 2000
MHL	*MHL (Mobile High-definition Link) Specification*, Version 1.0, MHL, LLC, June 2010

Table 10. Standards Groups Contact Information

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
I^2C	http://www.nxp.com	—	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—
MHL	http://www.mhlconsortium.org	Customerservice@mhlconsortium.org	408-962-4269

Silicon Image Documents

Table 11 lists Silicon Image documents that are available from your Silicon Image sales representative.

Table 11. Silicon Image Publications

Document	Title
SiI-PR-1049	*SiI1292 and SiI9292 MHL/HDMI-to-HDMI Bridge*

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