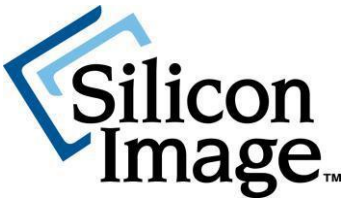

SiI9687A Port Processor

Data Sheet

Document # SiI-DS-1140-A

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Revision History

Revision	Date	Comment
A	12/10/2012	First production release.

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General Description

The SiI9687A HDMI port processor delivers four HDMI inputs with fast InstaPort™ S port switching to DTVs and other consumer electronic devices. One HDMI input can automatically detect and switch between HDMI and Mobile High-definition Link (MHL™) mode. The SiI9687A also supports InstaPrevue™, which provides real-time previews of the HDMI/DVI/MHL input ports overlaid on top of the selected main video.

The SiI9687A device supports the MHL 2 Specification on any one input port. The port processor features all MHL 2 required and conditional 3D video modes including 1920 x 1080p 24 Hz 3D Frame Sequential, It supports the UTF-8 character protocol subcommands. The SiI9687A device supports HDMI frequencies up to 300 MHz, which enables 4K x 2K @ 30 Hz and 1080p 3D @ 60 Hz.

The port processor supports the Audio Return Channel (ARC) described in the HDMI 1.4b Specification, which transmits an S/PDIF audio signal from an HDMI sink to an HDMI source in the opposite direction of the TMDS data flow. ARC simplifies audio connectivity and switching for the consumer.

HDMI Inputs and Output

- Four HDMI input ports and one output port
- HDMI, HDCP, and DVI compatibility
- TMDS™ cores run up to 3.0 Gbp/s
- Video resolutions up to 4K x 2K @ 30Hz, 1080p @ 120 Hz, and 1080P 3D @ 60 Hz
- MHL 2 on any one input port
- 21 x 9 aspect ratio support
- Pre-programmed with HDCP keys
- Single mode ARC

Performance Improvement Features

- InstaPrevue technology adds a preview image of the background ports to the video of the main port
- InstaPort™ S viewing technology allows HDMI input port switching in about one second
- Adaptive equalizer provides long cable support
- Built-in pattern generator to speed design, test, and manufacturing
- AVI, Audio InfoFrame, and video input resolution detection for all input ports, accessible port-by-port
- Hardware-based HDCP error detection and recovery minimizes firmware intervention
- Automatic output mute and unmute based on link stability, such as cable connect/detach

Control Capability

- Integrated EDID and DDC support for the HDMI/VGA ports using a 512-byte NVRAM shared between ports that loads into separate 256-byte SRAM for each of four HDMI ports and 128-byte SRAM for VGA EDID
- Individual control of Hot Plug Detect (HPD) for each port
- Controllable by the local I^2C bus

Packaging

- 76-pin, 9 mm x 9 mm, 0.4 mm pitch MQFN package with enhanced ePad™

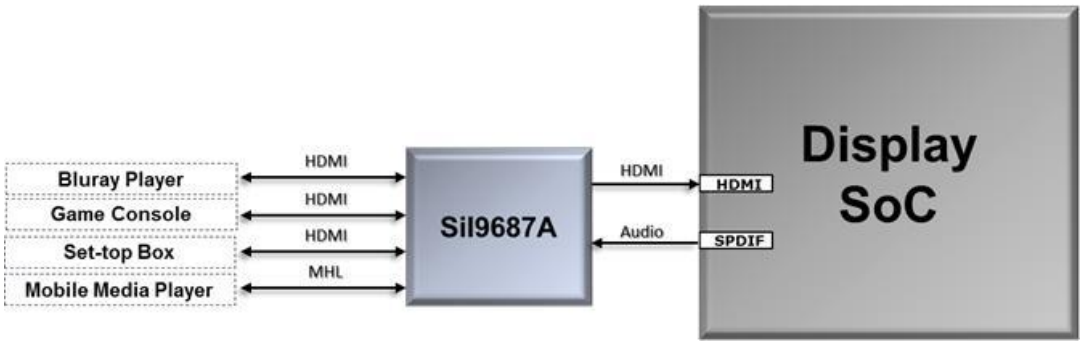


Figure 1. Port Processor Application

Pin Diagram

Figure 2 shows the pin assignments of the SiI9687A port processor. A description of the pin functions is in the Pin Descriptions section beginning on page 13. The package is a 9 mm x 9 mm 76-pin MQFN with an ePad, which ***must*** be connected to ground.

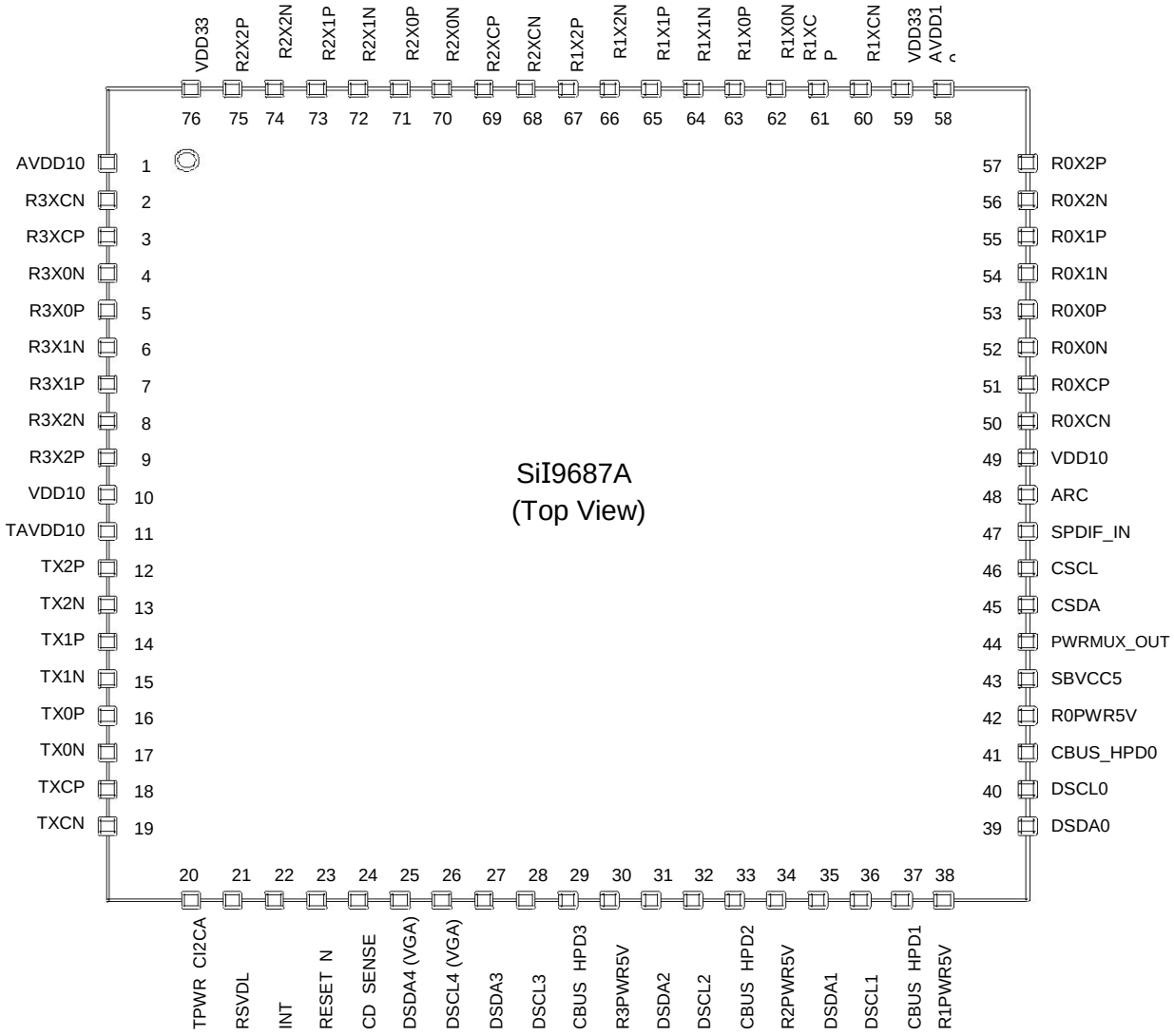


Figure 2. Pin Diagram (Top View)

Functional Description

Figure 3 shows the block diagram of the SiI9687A port processor.

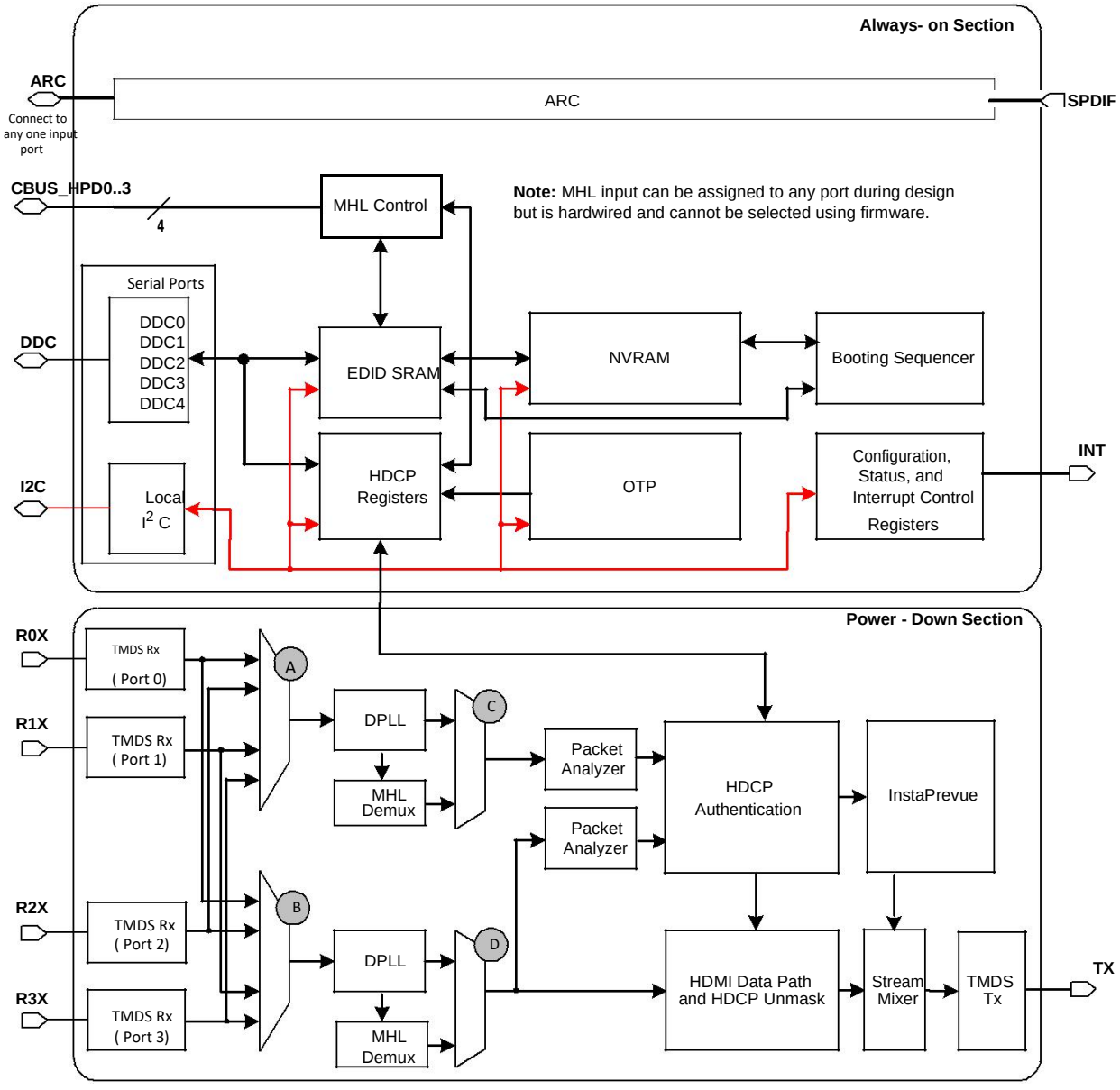


Figure 3. Functional Block Diagram

Always-on Section

The Always-On Section contains the low speed control parts of the HDMI connection, and includes the I^{2}C interfaces, internal memory blocks, and the registers that control the blocks of the Power-Down Section.

Serial Ports Block

The Serial Ports Block provides six I^{2}C serial interfaces: 4 DDC ports to communicate with the HDMI or DVI hosts, 1 VGA DDC port, and one local I^{2}C port for initialization and control by a local microcontroller in the display. Each interface is 5 V tolerant. Figure 4 shows the connection of the local I^{2}C port to the system microcontroller.

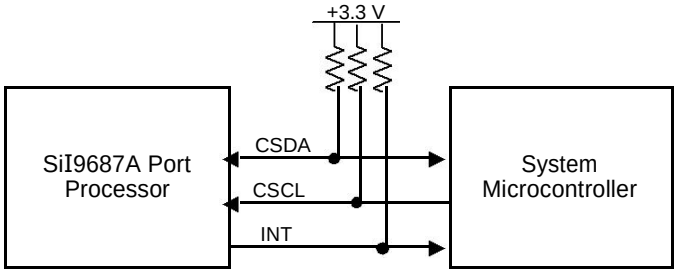


Figure 4. I^{2}C Control Mode Configuration

The five DDC interfaces (DDC 0–4) on the SiI9687A port processor are slave interfaces. Each HDMI DDC interface connects to one E-DDC bus and is used to read the integrated EDID and HDCP authentication information. These ports are accessible on the E-DDC bus at device addresses 0xA0 for the EDID and 0x74 for HDCP control. This feature complies with the HDCP 1.4 Specification. The VGA DDC port is only accessible on the E-DDC bus at device address 0xA0 for the EDID.

Refer to the Local I2C section on page 24 for information about the I^{2}C addresses and the use of the CI2CA pin.

Static RAM Block

The EDID Static RAM (SRAM) Block contains 1280 bytes of RAM. Each port is allocated a 256-byte block for DDC; this allows all ports to be read simultaneously from four different sources connected to the SiI9687A device. A 128-byte block is available for the VGA EDID, 64 bytes are used for the Auto-boot feature, and 64 bytes are reserved. The SRAM can be written to and read from using the local I^{2}C interface and it can be read through the DDC interface. The memory can be read without main TV power (VDD33), using 5 V power from the HDMI or VGA connector (R*n*PWR5V or SBVCC5). See the EDID Memory section on page 23 for information about how the SRAM and NVRAM work together.

NVRAM Block

The port processor contains 512 bytes of NVRAM, 256 of which is used to store common EDID data used by each of the ports, 128 of which is used for VGA DDC, and 64 of which is used by the Auto-Boot feature. (64 bytes are reserved.) Both the NVRAM EDID data and NVRAM Auto-Boot data should be initialized by software using the local I^{2}C bus at least once during the time of manufacture.

HDCP Register Block

The HDCP Register block controls the necessary logic to decrypt the incoming audio and video data. The decryption process is controlled entirely by the host side microcontroller using a set sequence of register reads and writes through the DDC channel. The decryption process uses pre-programmed HDCP keys and Key Selection Vector (KSV) stored in the on-chip non-volatile memory.

OTP ROM Block

The OTP ROM Block is programmed at the factory and contains the pre-programmed HDCP keys. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. All purchasing, programming,

and security for the HDCP keys is handled by Silicon Image. The pre-programmed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed.

Booting Sequencer

The Booting Sequencer boots up the required data, such as EDID, initial HPD status, and MHL port selection from NVRAM during power on.

Configuration, Status, and Interrupt Control Registers Block

The Configuration, Status, and Interrupt Control Registers block incorporates the registers required for configuring and managing the features of the SiI9687A port processor. These registers are used to perform audio/video/auxiliary format processing, CEA-861E InfoFrame Packet format, and power-down control. The registers are accessible from the local I^2C port. This block also handles interrupt operations.

MHL Control Block

The MHL Control Block handles CBUS conversion of DDC signals for the HDCP interface and EDID blocks.

Power-down Section

The Power-down section contains HDMI high-speed data paths, including the analog TMDS input and output blocks and the digital logic for HDMI data and HDCP processing.

TMDS Receiver Blocks

The receiver ports, defined as Port 0, Port 1, Port 2, and Port 3 are terminated separately, equalized under the control of the receiver digital block, and controlled by the local I^2C bus.

4:1 Input Multiplexer Blocks

4:1 Input Multiplexer Blocks A and B select one of the four inputs. Multiplexer Block A sequentially selects one of the three inactive inputs and sends its data over the roving pipe to the DPLL block and the MHL demux block. Multiplexer Block B selects the active input and sends its data over the main pipe to be processed.

MHL Demultiplexer Blocks

If the signal received from the DPLL block only appears in one of the three lanes, the input is an MHL signal. The Demultiplexer block distributes the single-lane RGB serial data blocks over the three parallel RGB lanes of video data.

2:1 HDMI/MHL Multiplexer Blocks

2:1 HDMI/MHL Multiplexer Blocks C and D select either the HDMI from the DPLL block or the MHL converted to HDMI by the MHL Demultiplexer. Block C transfers data from the roving pipe, and block D transfers data from the main pipe.

Packet Analyzer Blocks

The packet analyzer blocks extract the control signals from the HDMI control packets that are needed to control the HDCP decryption process in the main and the roving pipe. HDCP decryption is controlled by register information.

HDCP Authentication Block

The active receiver port switched to the main pipe is permanently connected to its HDCP decryption block. The remaining three ports share the roving pipe. Each of the decryption blocks are sequentially switched to its input port for a period long enough to get the control information from the HDMI packets needed for the pre-authentication process. There is a small probability of missing important information in the roving process because of the unpredictable

occurrence of control packets. The missed information is detected and leads to a full re-authentication of the corresponding HDCP path.

MP and RP HDMI Receive Data Path and HDCP Unmask Blocks

HDMI data from the Main Pipe (MP) and Roving Pipe (RP) are sent to and processed by the respective HDMI Receive Data Path and HDCP Unmask blocks. The appropriate decryption key for the main port and the input port currently connected to the roving pipe is applied to the XOR mask in these blocks to descramble the video, audio, and auxiliary packets.

InstaPrevue Block

The InstaPrevue block merges downscaled images from the roving pipe into the preview positions of main image coming from the main pipe. DeepColor processing, color space conversion, pixel repetition, interleaving, and 3D processing (for 720p and 1080p FramePacking only) are handled properly by the InstaPrevue core. The downscaled image is converted to match the format of the main pipe.

AV Mute Block

The AV mute block controls audio and video mute, using two methods. Software mute is controlled by register settings. When hardware mute is enabled, audio and video are automatically muted and unmuted if an ECC error occurs.

TMDS Transmitter Block

The transmitter block delivers an HDMI content stream, based on the content of the original stream from the selected source. Internal source termination eliminates the need to use external R-C components for signal shaping. The internal source termination can be disabled.

ARC Block

The Audio Return Channel (ARC) block allows digital S/PDIF data received from the sink device to be transmitted in the direction opposite to the TMDS input port signal. The block embeds the audio data, in single mode format, in the same lines connected to the Utility pin of the HDMI connector.

Electrical Specifications

Absolute Maximum Conditions

Table 1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDD33	Supply voltage	−0.3	—	4.0	V	1, 2
SBVCC5	Supply voltage	−0.3	—	5.7	V	1, 2
R*n*PWR5V	5V input from power pin of HDMI connector	−0.3	—	5.7	V	1, 2
AVDD10	TMDS receiver core supply voltage	−0.3	—	1.5	V	1, 2
TAVDD10	TMDS transmitter core supply voltage	−0.3	—	1.5	V	1, 2
VDD10	Digital core supply voltage	−0.3	—	1.5	V	1, 2
V_I	Input voltage	−0.3	—	VDD33 + 0.3	V	1, 2
V_O	Output voltage	−0.3	—	VDD33 + 0.3	V	1, 2
T_J	Junction temperature	0	—	125	°C	—
T_{STG}	Storage temperature	−65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section below.

Table 2. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Note
Latch up	ESD Latch up	± 200	—	—	mA	1, 2
HBM	Human Body Model	± 4	—	—	kV	3
MM	Machine Model	± 200	—	—	V	4
CDM	Charged Device Model	± 1	—	—	kV	5
V_{ESD}	ESD voltage per IEC 61000-4-2 (Contact)	± 8	—	—	kV	6
	ESD voltage per IEC 61000-4-2 (Air)	± 8	—	—	kV	6

Notes:
1. At 70 °C.
2. Measured as per JESD78B standard.
3. Measured as per JESD22-A114 standard.
4. Measured as per JESD22-A115 standard,
5. Measured as per JESD22-C101 standard.
6. System level tests at HDMI connectors.

Normal Operating Conditions

Table 3. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDD33	Supply voltage	3.14	3.3	3.46	V	—
SBVCC5	Supply voltage	4.3	5.0	5.5	V	2, 3
R*n*PWR5V	5V input from power pin of HDMI connector	4.3	5.0	5.5	V	2
AVDD10	TMDS receiver core supply voltage	0.95	1.0	1.05	V	—
TAVDD10	TMDS transmitter core supply voltage	0.95	1.0	1.05	V	—
VDD10	Digital core supply voltage	0.95	1.0	1.05	V	—
V_{DD33N}	3.3 V Supply voltage noise	—	—	100	mV_{P-P}	1
V_{DD10N}	1.0 V Supply voltage noise	—	—	50	mV_{P-P}	1
T_A	Ambient temperature (with power applied)	0	+25	+70	°C	—
Θja	Ambient thermal resistance (Theta JA)	—	—	28	°C/W	4,5
$Θ_{jc}$	Junction to case resistance (Theta JC)	—	—	14.4	°C/W	5

Notes:

1. The supply voltage noise is measured at test point VDDTP shown in Figure 5. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VDD pins as well.
2. The MHL VBUS voltage requirements may be more stringent than the 5 V power supply requirements for the port processor itself.
3. SBVCC5 Voltage is measured at SBVCC5TP as shown in Figure 6.
4. Airflow at 0 m/s.
5. The thermal resistance figures are based on a 4-layer PCB.

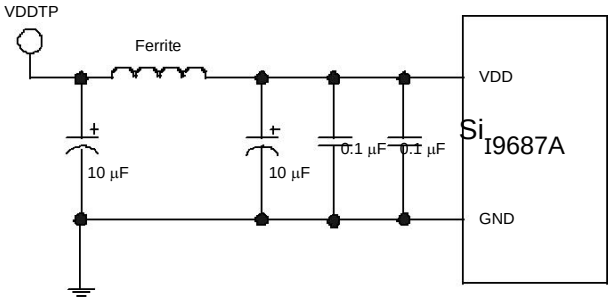


Figure 5. Test Point VDDTP for VDD Noise Tolerance Spec

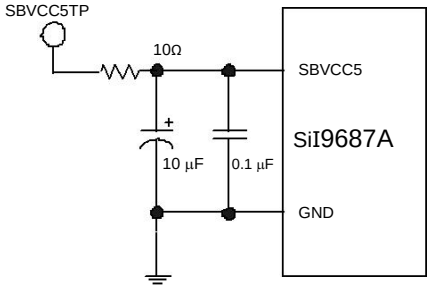


Figure 6. Test Point SBVCC5TP for SBVCC5 Measurement

DC Specifications

Table 4. Digital I/O Specifications

Symbol	Parameter	Pin Type[1]	Conditions	Min	Typ	Max	Units	Note
V_{IH}	HIGH-level Input Voltage	LVTTL	—	2.0	—	—	V	2
V_{IL}	LOW-level Input Voltage	LVTTL	—	—	—	0.8	V	2
Vth+ RESET#	LOW-to-HIGH threshold RESET # pin	Schmitt		2.0			V	—
Vth- RESET#	HIGH-to-LOW threshold RESET# pin	Schmitt				0.8	V	—
V_{TH+DDC}	LOW-to-HIGH Threshold, DDC Bus	Schmitt	—	3.0	—	—	V	3
V_{TH-DDC}	HIGH-to-LOW Threshold, DDC Bus	Schmitt	—	—	—	1.5	V	3
V_{TH+I2C}	LOW-to-HIGH Threshold, I^2C Bus	Schmitt	—	2.0	—	—	V	—
V_{TH-I2C}	HIGH-to-LOW Threshold, I^2C Bus	Schmitt	—	—	—	0.8	V	—
V_{OH}	HIGH-level Output Voltage	LVTTL	I_{OH} = 4 mA	2.4	—	—	V	4
V_{OL}	LOW-level Output Voltage	LVTTL	I_{OL} = –4 mA	—	—	0.4	V	4
V_{OL_DDC}	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	3
V_{OL_I2C}	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
V_{OL_INT}	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
I_{IL}	Input Leakage Current	LVTTL	High Impedance	−10	—	10	µA	—
I_{OL}	Output Leakage Current	LVTTL	High Impedance	−10	—	10	µA	—
I_{OD}	4 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4 V	4	—	—	mA	4
			V_{OUT} = 0.4 V	4	—	—	mA	4

Notes:
1. Refer to the Pin Descriptions section on page 13 for pin type designations for all package pins.
2. Applies to the GPIO, SPDIF, and TPWR_CI2CA signal pins.
3. Applies to the DDC interface.
4. Applies to the GPIO and TPWR_CI2CA signal pins.

Table 5. Power Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{AVDD10}	Supply Current for Receiver Analog VDD10	—	100	165	mA	1
$I_{TAVDD10}$	Supply Current for Transmitter Analog VDD10	—	10	15	mA	1
I_{VDD33}	Supply Current for VDD33	—	210	240	mA	1
I_{VDD10}	Supply Current for Digital VDD10	—	95	155	mA	1
$I_{SBVCC5SB}$	Supply Current for SBVCC5 during standby	—	8	13	mA	—
$I_{SBVCC5OP}$	Supply Current for SBVCC5 during operation	—	12	15	mA	1
$I_{RnPWR5V}$	Supply Current for RnPWR5V during operation	—	—	4	mA	1, 2
Total	Total Power	—	960	1265	mW	1

Notes:
1. Maximum supply currents are measured at maximum operating voltages, with all input and output ports switching at 297 MHz.
2. The power provided by $I_{RnPWR5V}$ is not included in the Total Power row.

Table 6. TMDS Input DC Specifications—HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Voltage	—	AVDD33 – 400	—	AVDD33 – 37.5	mV

Table 7. TMDS Input DC Specifications—MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	AVDD33 – 1200	—	AVDD33 – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min(720, 0.85 V_{IDF})	mV

Table 8. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SWING}	Single-ended Output Swing Voltage	R_{LOAD} = 50 Ω	400	—	600	mV
V_H	Single-ended High-level Output Voltage	—	AVDD33 – 200	—	AVDD33 + 10	mV
V_L	Single-ended Low-level Output Voltage	—	AVDD33 – 700	—	AVDD33 – 400	mV

Table 9. Single Mode Audio Return Channel DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
V_{el}	Operating DC Voltage	—	0	—	5	V	—
$V_{el\ swing}$	Swing Amplitude	—	400	—	600	mV	—

Table 10. CBUS DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
V_{IH_CBUS}	High-level Input Voltage	—	1.0	—	—	V	—
V_{IL_CBUS}	Low-level Input Voltage	—	—	—	0.6	V	—
V_{OH_CBUS}	High-level Output Voltage	I_O = 100 µA	1.5	—	—	V	—
V_{OL_CBUS}	Low-level Output Voltage	I_O = 100 µA	—	—	0.2	V	—
Z_{DSC_CBUS}	Pull-down Resistance – Discovery	—	800	1000	1200	Ω	—
Z_{ON_CBUS}	Pull-down Resistance – Active	—	90	100	110	kΩ	—
I_{IL_CBUS}	Input Leakage Current	High-Impedance	—	—	1	µA	—
C_{CBUS}	Capacitance	Power Off	—	—	30	pF	—

AC Specifications

Table 11. TMDS Input Timing AC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
$T_{INTRA-PAIR\_SKEW}$	Input Intra-Pair Skew	—	—	—	0.4	T_{BIT}	—
$T_{INTER-PAIR\_SKEW}$	Input Inter-Pair Skew	—	—	—	$0.2T_{PIXEL}$ + 1.78	ns	—
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz	—
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns	—
T_{IJIT}	Differential Input Clock Jitter Tolerance	300 MHz	—	—	0.3	T_{BIT}	—

Table 12. TMDS Input Timing AC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SKEW_DF}	Input Differential Intra-Pair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common-mode Intra-Pair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	75	MHz
T_{RXC}	Differential Input Clock Period	—	13.33	—	40	ns
T_{CLOCK_JIT}	Common-mode Clock Jitter Tolerance	—	—	—	$0.3T_{BIT}$ + 200	ps
T_{DATA_JIT}	Differential Data Jitter Tolerance	—	—	—	$0.4T_{BIT}$ + 88.88	ps

Table 13. TMDS Output Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
T_{TXDPS}	Intra-Pair Differential Output Skew	—	—	—	0.15	T_{BIT}	—
T_{TXRT}	Data/Clock Rise Time	20%–80%	75	—	144	ps	—
T_{TXFT}	Data/Clock Fall Time	20%–80%	75	—	120	ps	—
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz	—
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns	—
T_{DUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}	—
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}	—

Table 14. Single Mode Audio Return Channel AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
T_{ASMRT}	Rise Time	10%–90%	—	—	60	ns	—
T_{ASMFT}	Fall Time	10%–90%	—	—	60	ns	—
T_{ASMJIT}	Jitter Max	—	—	—	0.05	UI*	—
F_{ASMDEV}	Clock Frequency Deviation	—	–1000	—	1000	ppm	—

***Note:** Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF specification.

Table 15. S/PDIF Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
F_{I_SPDIF}	Sample Rate	To ARC	32	—	48	kHz	—
T_{I_SPCYC}	Cycle Time	—	—	—	1.0	UI*	—
T_{I_SPDUTY}	Duty Cycle	—	90	—	110	%UI*	—

***Note:** Proportional to unit time (UI), according to sample rate. Refer to S/PDIF specification.

Table 16. CBUS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{BIT_CBUS}	Bit Time	1 MHz clock	0.8	—	1.2	µs
T_{BJIT_CBUS}	Bit-to-Bit Jitter	—	–1%	—	+1%	T_{BIT_CBUS}
T_{DUTY_CBUS}	Duty Cycle of 1 Bit	—	40%	—	60%	T_{BIT_CBUS}
T_{R_CBUS}	Rise Time	0.2 V–1.5 V	5	—	200	ns
T_{F_CBUS}	Fall Time	0.2 V–1.5 V	5	—	200	ns
ΔT_{RF}	Rise to Fall Time Difference	—	—	—	100	ns

Table 17. I^2C Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Figure
F_{I2C}	I^2C frequency range	—	—	—	400	kHz	—
T_{HDDAT}	I^2C data hold time*	0–400 KHz	0	—	—	ns	—

***Note:** This minimum hold time is required by CSCL and CSDA pins as an I^2C slave. The 300ns internal delay for CSDA can be enabled by NVRAM configuration

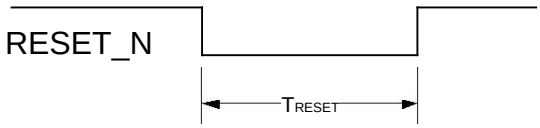
Miscellaneous Timing

Table 18. Miscellaneous Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Figure	Notes
T_{RESET}	RESET_N signal LOW time for valid reset	—	1	—	—	ms	Figure 7	—
T_{RESET_VDD10}	Time required for RESET_N high before VDD10*	50% RESET_N to 90% VDD10	1	—	—	µs	Figure 8	—
$T_{SBVCC5RT}$	Rise Time	10%–90%	—	—	1	ms	—	—

***Note: This time is required due to internal Power-on Reset.**

Reset Timings



RESET_N must be pulled LOW for T_{RESET} before accessing registers. This is done by pulling RESET_N LOW from a HIGH state (shown above) for at least T_{RESET}.

Figure 7. RESET_N Minimum Timing

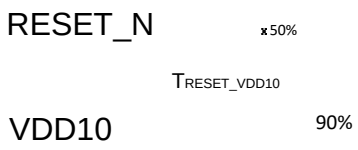


Figure 8. RESET_N to VDD10 Timing

Pin Descriptions

HDMI and MHL Receiver Port Pins

Pin Name	Pin	Type	Dir	Description
R0X0P	53	TMDS	Input	TMDS input Port 0 data pairs.
R0X0N	52			
R0X1P	55			
R0X1N	54			
R0X2P	57			
R0X2N	56			
R0XCP	51	TMDS	Input	TMDS input Port 0 clock pair.
R0XCN	50			
R1X0P	63	TMDS	Input	TMDS input Port 1 data pairs.
R1X0N	62			
R1X1P	65			
R1X1N	64			
R1X2P	67			
R1X2N	66			
R1XCP	61	TMDS	Input	TMDS input Port 1 clock pair.
R1XCN	60			
R2X0P	71	TMDS	Input	TMDS input Port 2 data pairs.
R2X0N	70			
R2X1P	73			
R2X1N	72			
R2X2P	75			
R2X2N	74			
R2XCP	69	TMDS	Input	TMDS input Port 2 clock pair.
R2XCN	68			
R3X0P	5	TMDS	Input	TMDS input Port 3 data pairs.
R3X0N	4			
R3X1P	7			
R3X1N	6			
R3X2P	9			
R3X2N	8			
R3XCP	3	TMDS	Input	TMDS input Port 3 clock pair.
R3XCN	2			

Note: For the port that has been configured as a MHL input, the R*n*X0P and R*n*X0N pins carry the MHL signal. All eight TMDS lines require 5.1 ohm series resistors to meet the impedance requirements of both the MHL and HDMI Specifications. HDMI-only ports do not require 5.1 Ω series resistors on the TMDS lines.

Audio Pins

Pin Name	Pin	Type	Dir	Description
ARC	48	Analog	Output	Audio Return Channel. This pin is used to transmit an IEC60958-1 audio stream, received on the SPDIF_IN input pin, upstream to a compatible source or repeater device, using single-mode ARC.
SPDIF_IN	47	LVTTL	Input	S/PDIF input from the SoC. Pull-down if not used.

HDMI Transmitter Port Pins

Pin Name	Pin	Type	Dir	Description
TX0P	16	TMDS	Output	HDMI Transmitter Output Port Data. TMDS Low Voltage Differential Signal output data pairs.
TX0N	17			
TX1P	14			
TX1N	15			
TX2P	12			
TX2N	13			
TXCP	18	TMDS	Output	HDMI Transmitter Output Port Clock. TMDS Low Voltage Differential Signal output clock pair.
TXCN	19			

System Switching Pins

Pin Name	Pin	Type	Dir	Description
DSDA0	39	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I^2C Data for respective port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor. Pull-up if not used.
DSDA1	35			
DSDA2	31			
DSDA3	27			
DSDA4(VGA)	25			
DSCL0	40	LVTTL Schmitt Open-drain 5 V tolerant	Input	DDC I^2C Clock for respective port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor. Pull-up if not used.
DSCL1	36			
DSCL2	32			
DSCL3	28			
DSCL4(VGA)	26			
R0PWR5V	42	Power	Input	5 V Port detection input for respective port. Connect to 5 V signal from HDMI input connector. These pins require a 10 Ω series resistor, a 5.1 kΩ pull-down resistor, and at least a 1 µF capacitor to ground. Pull-down if not used.
R1PWR5V	38			
R2PWR5V	34			
R3PWR5V	30			
CBUS_HPD0	41	Schmitt 5 V tolerant Analog pad	Input/ Output	Hot Plug Detect Output for the respective port. In MHL mode, these pins serve as the respective CTRL bus. Pull-down if not used.
CBUS_HPD1	37			
CBUS_HPD2	33			
CBUS_HPD3	29			

Control Pins

Pin Name	Pin	Type	Dir	Description
CSCL	46	LVTTL 5 V tolerant Schmitt	Input	Local Configuration/Status I^2C Clock. Chip configuration/status is accessed via this I^2C port. This pin is true open drain, so it doesn't pull to ground if power is not applied.
CSDA	45	LVTTL 5 V tolerant Schmitt	Input/ Output	Local Configuration/Status I^2C Data. Chip configuration/status is accessed via this I^2C port. This pin is true open drain, so it doesn't pull to ground if power is not applied. See Figure 4 on page 4.
CD_SENSE	24	LVTTL 5 V tolerant Schmitt	Input	MHL cable detection pin. This pin requires a 300 kΩ pull-down resistor, which the MHL specification requires for CD_SENSE. This pin can be configured as a GPIO if MHL is not used. Pull-down if not used.
RESET_N	23	LVTTL 5 V Tolerant Schmitt	Input	External reset. Active LOW. Must be pulled-up to the ―Always-on‖ 3.3 V domain.. The microcontroller GPIO that is connected to this pin should be HIGH by default. Apply an external reset only when the internal Power-on Reset does not work properly. Refer to the Programmer's Reference for more details about the external reset sequence.

Configuration Pins

Pin Name	Pin	Type	Dir	Description
TPWR_CI2CA	20	LVTTL 5 V tolerant Schmitt	Input/ Output	I^2C Slave Address input / Transmit Power Sense Output. During chip reset, either by internal power-on-reset (POR) or the RESET_N signal, this pin is used as an input to latch the I^2C sub-address. The level on this pin is latched when the POR transitions from the asserted state to the de-asserted state or on a LOW-to-HIGH transition of the RESET_N signal. After completion of reset, this pin is used as the TPWR output, showing the R*n*PWR status of the selected port. A register setting can change this pin to show if the active port is receiving a TMDS clock. This pin must be tied to ground for the 0xB0 I^2C address through a 4.7 kΩ resistor. For the 0xB2 I^2C address, this pin must be pulled up to PWRMUX_OUT through a 4.7 kΩ resistor.
INT	22	Open-drain 5 V tolerant Schmitt	Output	Interrupt Output.

Power and Ground Pins

Pin Name	Pin	Type	Description
VDD33	59, 76	Power	TMDS Core VDD. In order to prevent reverse leakage from source device through TMDS input pins, VDD33 should be isolated from other system power. Must be supplied at 3.3 V.
PWRMUX_OUT	44	Output	Power Output. This pin requires a 10 µF capacitor to ground.
SBVCC5	43	Power	Local Power from TV. Must be set to 5 V. This pin requires a 10 Ω series resistor.
AVDD10	1, 58	Power	TMDS Receiver Core. Must be supplied at 1.0 V.
TAVDD10	11	Power	TMDS Transmitter Core Must be supplied at 1.0 V.
VDD10	10, 49	Power	Digital Core. Must be supplied at 1.0 V.
GND	ePad	Ground	The ePad ***must*** be soldered to ground, as this is the only ground connection for the device.

Reserved Pins

Pin Name	Pin	Type	Description
RSVDL	21	Reserved	Reserved, must be tied to ground.

Unused Pins

Table 19 below summarizes how to connect pins in case their associated functions are not used.

Table 19. Required Connection for Unused Pins

Unused Pin Name	Connection
TPWR/CI2CA	Must always be pulled-up or pulled-down to select I^2C address
RSVDL	Reserved, Must be tied to ground
INT	Output, Leave unconnected
RESET_N	Must be pulled-up
CD_SENSE	Must be pulled-down
DSDA*n*	Must be pulled-up
DSCL*n*	Must be pulled-up
CBUS_HPD*n*	Must be pulled-down
R*n*PWR5V	Must be pulled-down
SPDIF_IN	Must be pulled-down
ARC	Output, Leave unconnected
TMDS inputs (R*n*X*m*N / R*n*X*m*P)	Leave unconnected

Feature Information

Standby and HDMI Port Power Supplies

The SiI9687A port processor incorporates a 5-volt standby power supply pin (SBVCC5). SBVCC5 can be used to supply power to the EDID portions of the device when all other power supplies are turned off. This arrangement allows the EDID to be readable. Table 20 summarizes the power modes available in the processor. Figure 9 shows a block diagram of the standby power supply sources and the always-on power island.

Table 20. Description of Power Modes

Power mode	Description	SBVCC5	R*n*PWR5V	VDD33	VDD10
Power-On mode 5 V Standby. ARC supported.	All power supplies to the SiI9687A chip are on. All functions are available. The standby power supply is 5 V.	5 V	Don't Care	3.3 V	1.0 V
Standby power mode. 5 V standby.	The always-on power domain is on, supplied from the internal power MUX; all other supplies are off. The standby power supply is 5 V. In this mode, EDID is functional, but both video and audio processing is not performed and all outputs are off.	5 V	Don't Care	Off	Off
HDMI/VGA Port only power.	Power is off to the device. HDMI +5 V from the HDMI cable is the only power source. For example, if the TV is unplugged from AC wall outlet, the EDID is functional in this mode.	Muxed with VGA power	5 V on any input	Off	Off

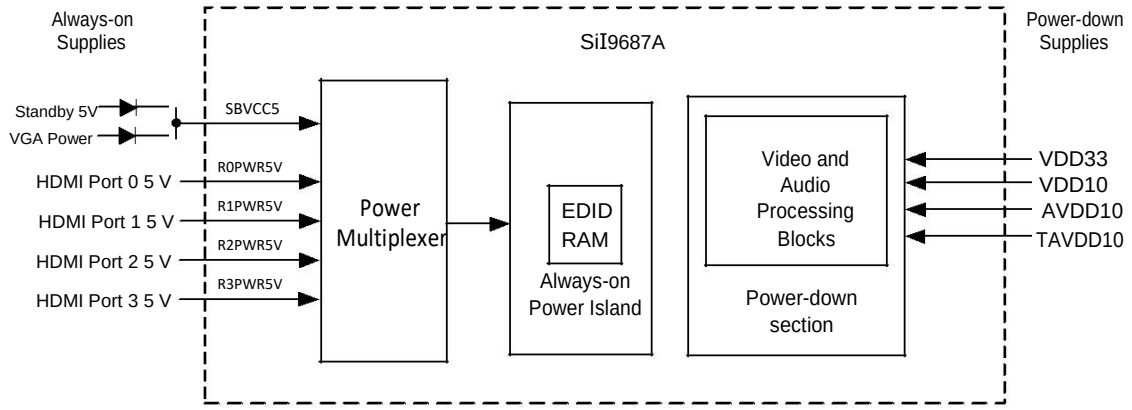


Figure 9. Standby Power Supply Diagram

If all power is off to the device (for example, if the TV is unplugged from the AC electrical outlet), the EDID can still be read from the source by using power from the HDMI connector +5 V signal. In this case, the internal power MUX will automatically switch to the HDMI connector power to use it for powering the EDID logic. In this mode, only the EDID block is functional, with all other functions of the device in power-off mode. No damage will occur to the device in this mode.

Hardware Reset

Silicon Image recommends applying a hardware reset through RESET_N pin only when a Power-on Reset problem is detected by the indicating register (Refer to the SiI9687A Programmer's Reference). The connection for RESET_N should meet the following conditions:

1. RESET_N must be pulled up to the Always-on 3.3 V domain.
2. RESET_N must be pulled HIGH at all times, except when it is necessary to be toggled.
3. The microcontroller GPIO that is connected to RESET_N should be HIGH by default when microcontroller boots up, and should not toggle RESET_N.
4. Ensure that RESET_N goes HIGH earlier than VDD10 when the system powers up as shown in Figure 8 on page 13.

After a hardware reset, the SiI9687A device latches the level on the TPWR_CI2CA pin to set the device I^2C address, restores all registers to default values, and reloads the EDID data and Auto-boot data from NVRAM. Hardware reset also toggles Hot Plug.

Built-in Pattern Generator

The SiI9687A port processor contains a built-in pattern generator that supports the eight different built-in patterns shown in Table 21 at a resolution of 1280 x 720 pixels. An internal oscillator with a part-to-part accuracy of ±10% or a 74.25 MHz external clock with higher accuracy can be used as the clock source for the pattern generator. These patterns are invoked using the I^2C interface. See the SiI9687A Programmer's Reference for details about how to activate the pattern generator.

Table 21. Built-in Pattern List

Pattern	RGB Description	Example Picture
Solid Red	255, 0, 0	
Solid Green	0, 255, 0	
Solid Blue	0, 0, 255	
Solid Black	0, 0, 0	
Solid White	255, 255, 255	
256 Grey Ramp	256 Vertical bars, 5 pixels wide, Value of first bar: RGB (0, 0, 0) Value of last bar: RGB (255, 255, 255) Increment of each bar: One RGB value (1, 1, 1), (2, 2, 2), etc.	
Checkerboard	8 x 6 black/white squares No border Value of white: RGB (0, 0, 0) Value of black: RGB (255, 255, 255)	
RGB Color Bars	8 Vertical Bars White: 255, 255, 255, Yellow: 255, 255, 0 Cyan: 0, 255, 255, Green: 0, 255, 0 Magenta: 255, 0, 255, Red: 255, 0, 0 Blue: 0, 0, 255, Black: 0, 0, 0	

3D Video Formats

The SiI9687A port processor supports the pass-through of 3D video modes described in the HDMI 1.4b and MHL 2 Specifications. All HDMI modes support RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color formats and 8-, 10-, and 12-bit data-width per color component. DeepColor (10-bit and 12-bit) modes are supported for resolutions where the required link clock rate does not exceed 300 MHz for HDMI or 75 MHz for MHL. Table 22 shows only the maximum possible resolution with a given frame rate; for example, Side-by-Side (Half) mode is defined for 1080p, 60 Hz, which implies that 720p, 60 Hz and 480p, 60 Hz are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

Pass-through of the HDMI/MHL Vendor Specific InfoFrame, which carries 3D information to the receiver, is supported by the SiI9687A device. It also supports extraction of the HDMI/MHL Vendor Specific InfoFrame, which allows the 3D information contained in the InfoFrame to be passed to the host system over the I^2C port.

Table 22. Supported HDMI 3D Video Formats

HDMI 3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	50/60	297
Side-by-Side	full			
Line Alternative	—			
L+ Depth	—			
Frame Packing	—	1080p	24/30	148.5
		720p/1080i	50/60	
Side-by-Side	Full	1080p	24/30	
		720p/1080i	50/60	
	Half	1080p	50/60	
Top-and-Bottom	—	1080p	50/60	
		1080p	24/30	74.25
		720p/1080i	50/60	
Line Alternative	—	1080p	24/30	148.5
		720p/1080i	50/60	
Field Alternative	—	1080i	50/60	
L + depth	—	1080p	24/30	
		720p/1080i	50/60	

For the supported MHL 3D formats listed in Table 23, the MHL 3D format is converted to the corresponding HDMI 3D format before being output by the SiI9687A port processor. The 3D MHL Vendor Specific InfoFrame is passed through and the output is unchanged along with the 3D HDMI Audio/Video. However, the extracted MHL Vendor Specific InfoFrame is also converted to an HDMI Vendor Specific InfoFrame, which can be accessed by reading registers in the port processor.

Table 23. Supported MHL 3D Video Formats

MHL 3D Format	Corrisponding HDMI Format	Resolution	Frame Rate (Hz)	Input Link Clock for 8-bit color (MHz)
Top-Bottom	Top-and-Bottom	1080p	50/60	74.25 (PackedPixel)
		720p/1080i	50/60	74.25
		1080p	24/30	
Left-Right	Side-by-Side (Half)	1080p	50/60	74.25 (PackedPixel)
		720p/1080i	50/60	74.25
		1080p	24/30	74.25
Frame Sequential	Frame Packing	720p/1080i	50/60	74.25 (PackedPixel)
		1080p	24/30	

InstaPrevue Format Support

The InstaPrevue feature of the SiI9687A port processor supports all 2D formats and certain 3D formats up to 225 MHz for the main display and preview windows. Refer to Table 24 below to determine which combinations of formats are supported.

Table 24. InstaPrevue Supported Formats

Main Display Format	InstaPrevue Window Format	Supported?
All supported 2D Resolutions	All supported 2D Resolutions	YES
	720p and 1080p 3D Frame Packing	YES
	480p and 1080i 3D Frame Packing	NO
	3D Side-by-Side (Half)	NO
	3D Side-by-Side (Full)	NO
	3D Top-and-Bottom	NO
720p and 1080p 3D Frame Packing	All supported 2D Resolutions	YES
	720p and 1080p 3D Frame Packing	YES
	480p and 1080i 3D Frame Packing	NO
	3D Side-by-Side (Half)	NO
	3D Side-by-Side (Full)	NO
	3D Top-and-Bottom	NO
480p and 1080i 3D Frame Packing	All Formats	NO
3D Top-and-Bottom		
3D Side-by-Side (Half)		
3D Side-by-Side (Full)		

Input Video Resolution Detection and InfoFrame Extraction

InfoFrame extraction and input video resolution detection are supported for the main and roving port and are accessible port-by-port. This feature helps the microcontroller reduce switching time by predetermining the resolution and InfoFrame before switching.

MHL PackedPixel Mode

MHL PackedPixel mode is a method of encoding pixel data. The YCbCr 4:2:2 pixel data is encoded with the PackedPixel format, which allows 16 bits of data to be encoded and transmitted rather than the 24 bits per pixel as in the other pixel encoding modes. The incoming pixel clock rate may be as high as 150 MHz in this mode, with a link clock rate of half of the pixel clock, which allows MHL to support 1080p @ 60 Hz video. The maximum link clock rate still remains 75 MHz in PackedPixel mode.

Audio Return Channel

ARC is transmitted in single mode by using the ARCP (Utility) line. When using ARC single-mode transmission, a standard HDMI cable can be used. *Utility* is a new name for the *Reserved* pin described in earlier versions of the HDMI Specification (The SiI9687A port processor doesn't support ARC common-mode.)

The way the S/PDIF backchannel is used depends on the application. For example, in a TV application, an S/PDIF audio signal from the TV can be sent to an HDMI source device such as an A/V receiver over the Audio Return Channel.

ARC simplifies system setup because the consumer does not need to run an S/PDIF cable from the TV to the AVR. ARC also automates connectivity. When the TV input is switched to an analog source or the TV tuner, the TV can use the CEC protocol to indicate to the AVR that it should switch to playback of the ARC input.

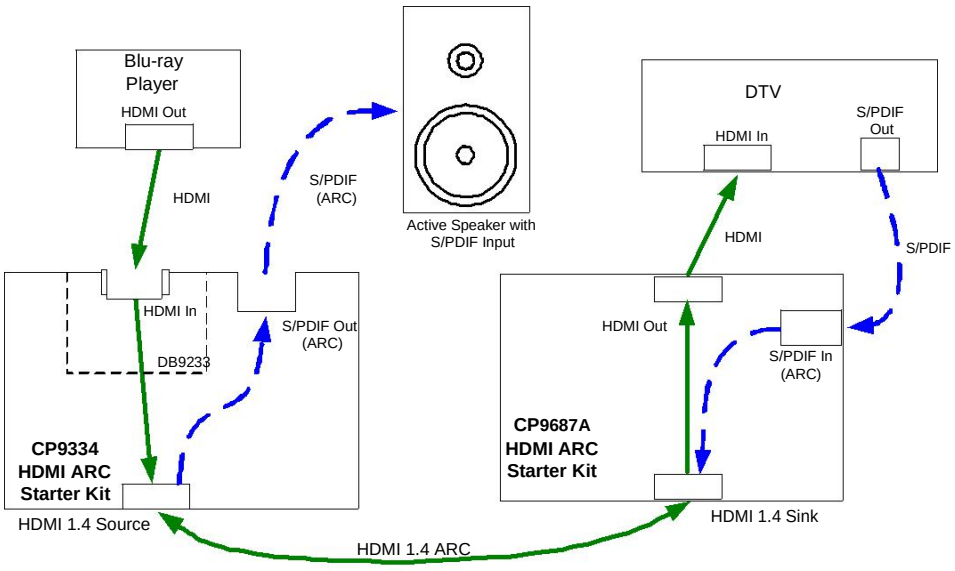


Figure 10. Audio Return Channel Example Application

EDID Memory

The port processor contains 512 bytes of NVRAM that stores common EDID data used by each of the ports and information used by the Auto-Boot feature. The Auto-Boot feature initializes some of the registers used to enable the EDID for the respective port, as well as asserts Hot Plug Detect (HPD) after the EDID has loaded properly into the SRAM. For example, by changing the data in the NVRAM Auto-boot portion, EDID load and HPD state can be set HIGH in three of the HDMI ports while disabling this feature in the fourth port. See the associated Programmer's Reference for more detail about the format of the NVRAM Auto-boot feature. Each port has a 256-byte block of SRAM for EDID data, which allows all ports to be read simultaneously from four different sources connected to the SiI9687A device. In addition, a 128-byte block of NVRAM is reserved for the VGA EDID. Figure 11 shows how the NVRAM is initialized using the local I^2C slave and the shadow SRAM during manufacture, and how data is loaded into the SRAM blocks from the NVRAM during normal operation.

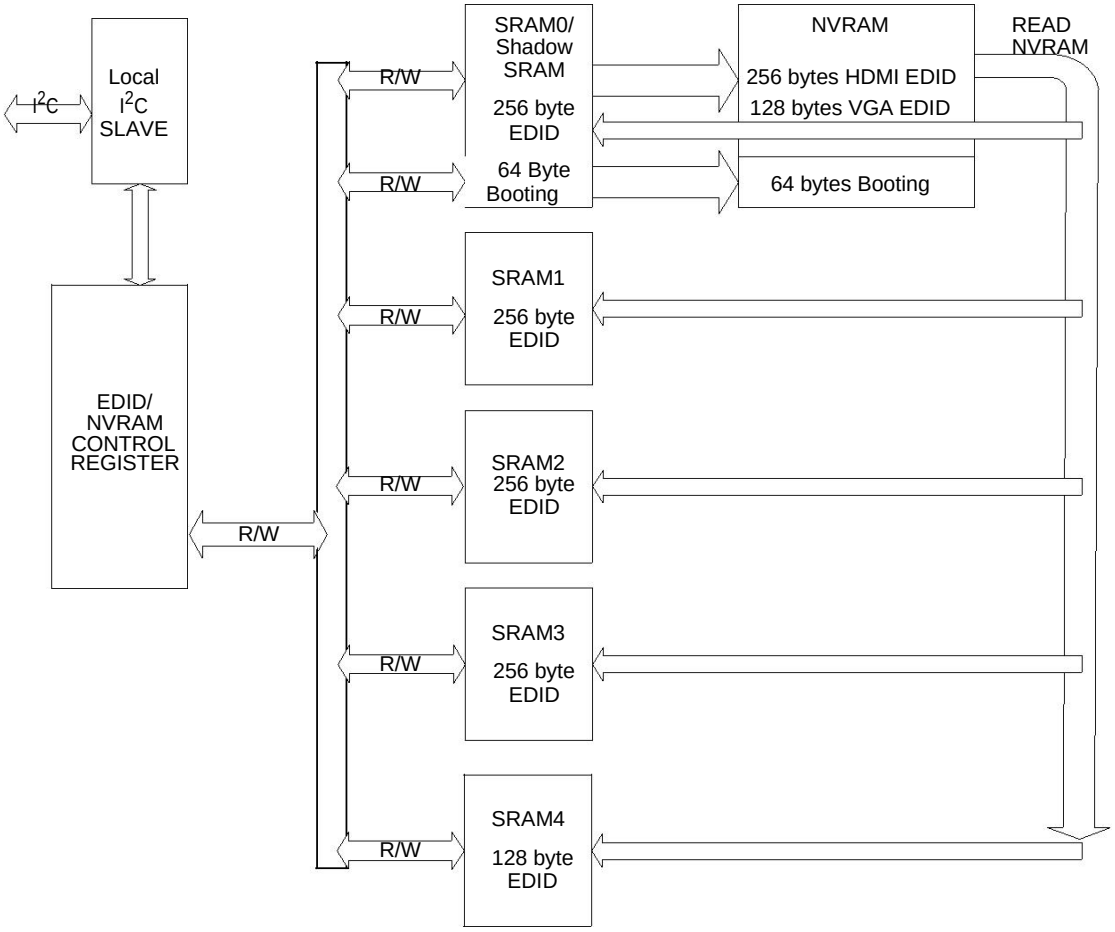


Figure 11. EDID Block Diagram

Local I²C Port

The local I²C slave port on the SiI9687A port processor (pins CSCL and CSDA) is capable of running up to 400 kHz. This port is used to configure the port processor by reading from and writing to necessary registers.

The local I²C port consists of ten separate I²C slave addresses. Therefore, the port processor appears as ten separate devices on the I²C local bus. The address for accessing the system control registers is fixed, and can only be set to one of two values by using the CI2CA pin. The remaining nine addresses have an I²C register-programmable address mapped into the system control register space so that they can be changed to any free addresses in the system. Refer to the Programmer's Reference for complete information.

Table 25. I²C Register Address Groups

I²C Slave Address	Through	Register Programmable	Blocks
0x74	DDC	No	HDCP
0xA0	DDC	No	EDID
0x64	Local I²C	Yes	Rx TMDS
0x68	Local I²C	Yes	Reserved
0x50	Local I²C	Yes	Pre-authentication, page 0
0x52	Local I²C	Yes	Pre-authentication, page 1
0x54	Local I²C	Yes	Pre-authentication, page 2
0x90	Local I²C	Yes	Tx TMDS /ARC
0xB0/0xB2	Local I²C	No	System Control
0xE0	Local I²C	Yes	EDID/NVRAM/MHL
0xE6	Local I²C	Yes	CBUS
0xFA	Local I²C	Yes	InstaPrevue

Design Recommendations

Audio Return Channel Design

Figure 12 shows a sample design circuit for using the Audio Return Channel feature. Any one of the five input ports can be wired for ARC use; connection to Port 1 for ARC is shown in the figure.

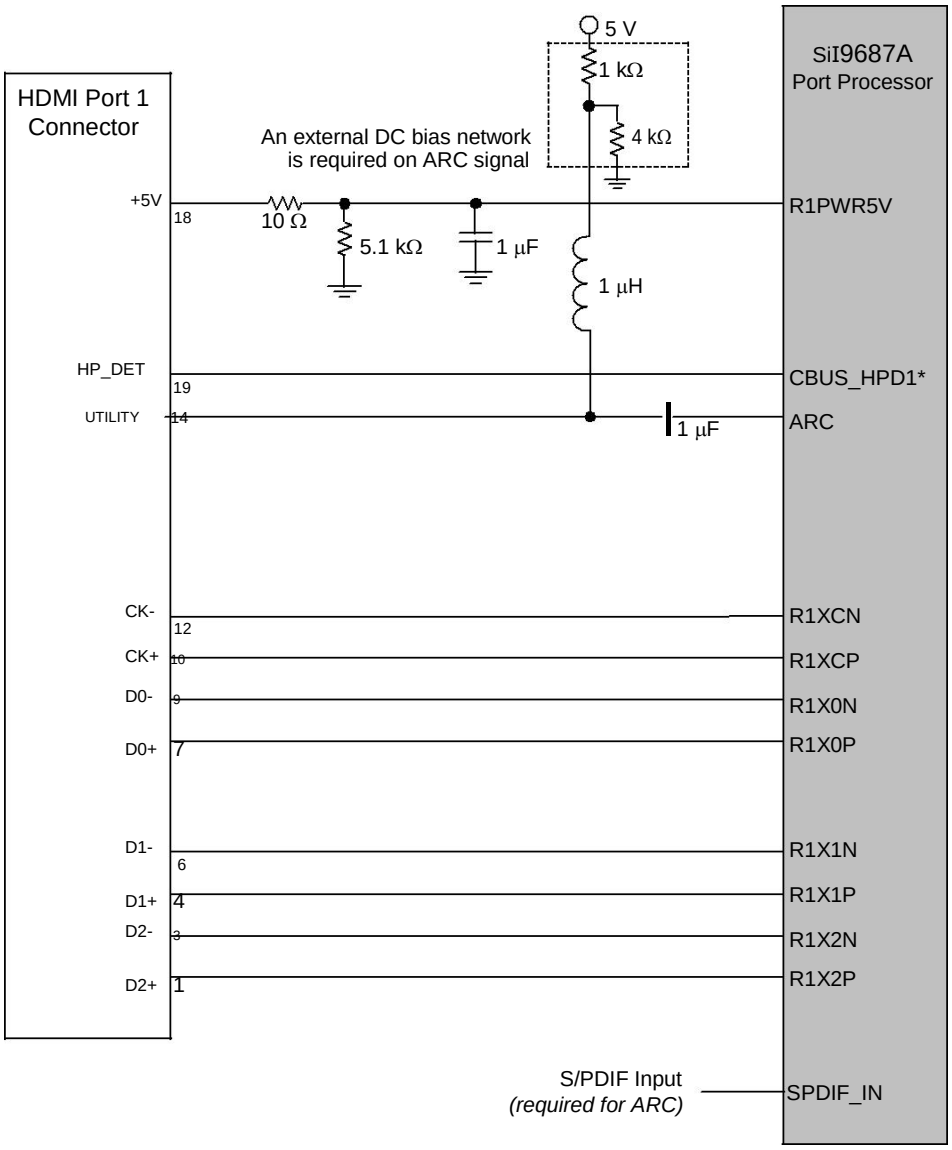


Figure 12. Connection of ARC to HDMI Port

MHL Power and Cable Detect Design

Figure 13 on the next page shows a sample design circuit for an MHL and HDMI combined port. All eight TMDS connections require 5.1 Ω series resistors for ports that are wired for both MHL and HDMI. Any one of the input ports can be wired for MHL; connection to Port 3 for combined HDMI and MHL is shown in the figure.

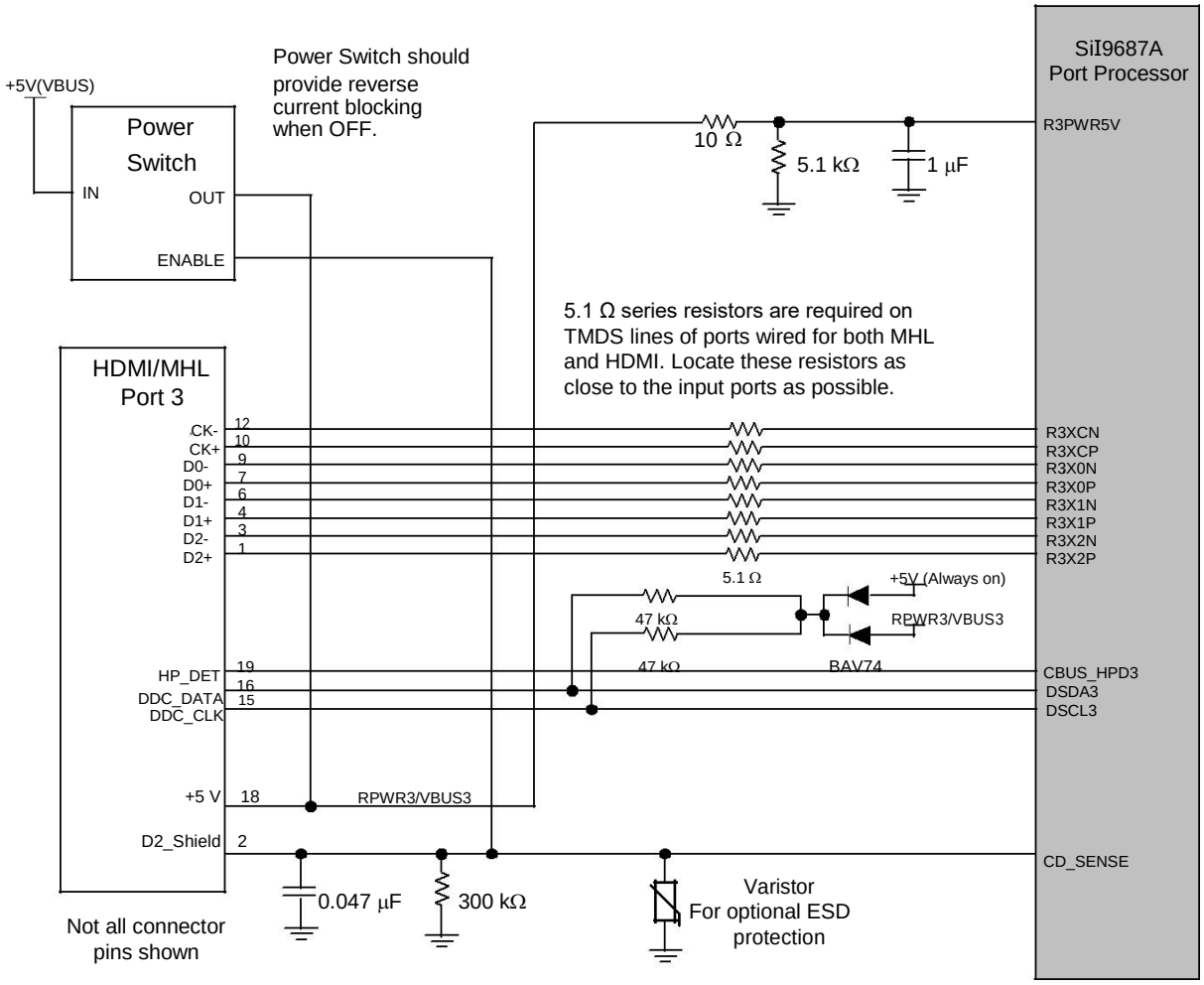


Figure 13. Connection of MHL and HDMI Combined Port

Power Supply Decoupling

Designers should include decoupling and bypass capacitors at each power signal in the layout. These are shown schematically in Figure 14. Connections in one group (such as VDD33) can share C2, C3, and the ferrite, with each pin having a separate C1 placed as close to the pin as possible. Figure 15 on the next page is representative of the various types of power connections on the port processor.

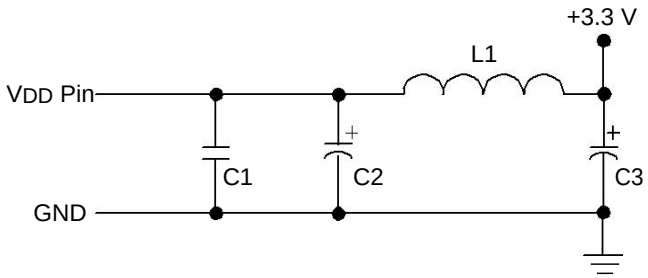


Figure 14. Decoupling and Bypass Schematic

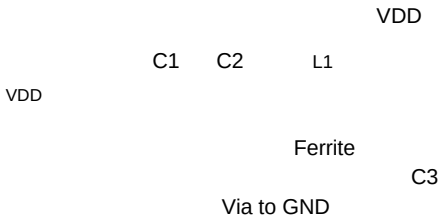


Figure 15. Decoupling and Bypass Capacitor Placement

Power Supply Sequencing

All power supplies in the SiI9687A port processor are independent, but identical supplies must come on at the same time; for example, power to all VDD33 pins must come on together. During power up, the SBVCC5 rise time (from 10% to 90% of 5 V) should be less than 1 ms.

Package Information

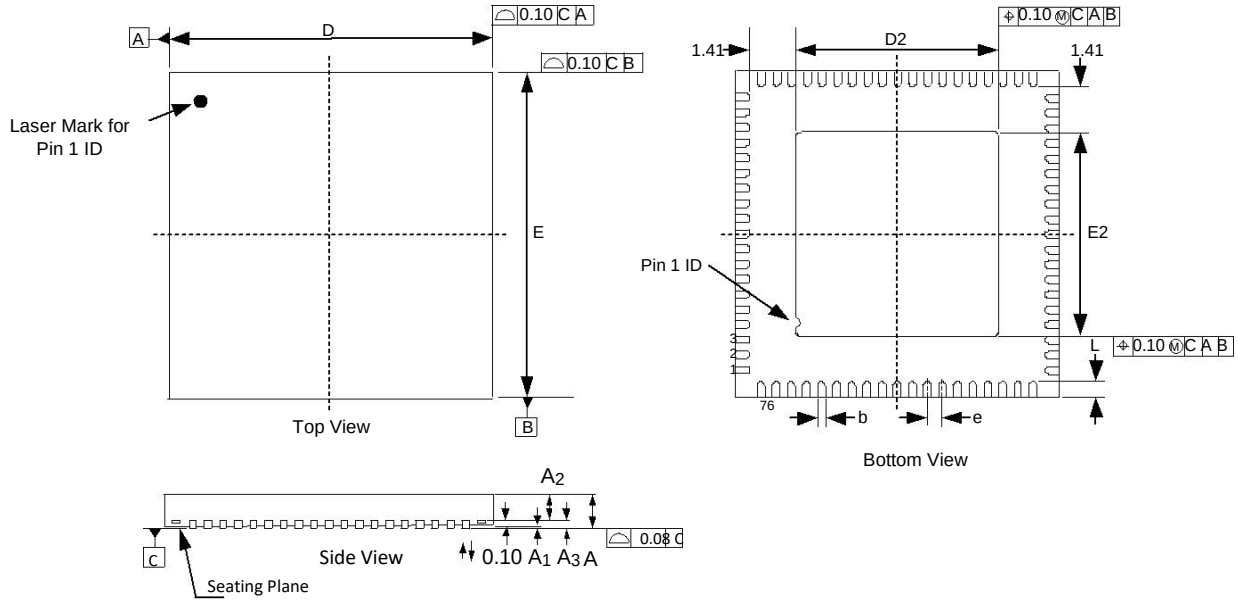
ePad Requirements

The SiI9687A Port Processor chip is packaged in a 76-pin, 9 mm x 9 mm MQFN package with an ExposedPad™ (ePad™) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 5.38 mm × 5.38 mm (±0.15 mm). Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. As a general guideline, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

Figure 16 shows the package dimensions of the SiI9687A port processor.

Package Dimensions

These drawings are not to scale. All dimensions are in millimeters.



JEDEC Package Code MO-220

Symbol	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	—	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D		9.00 BSC	

Symbol	Min	Typ	Max
D2	5.23	5.38	5.53
E		9.00 BSC	
E2	5.23	5.38	5.53
L	0.30	0.40	0.50
e		0.40 BSC	

Figure 16. Package Diagram

Marking Specification

Figure 17 shows the markings of the SiI9687A port processor package. This drawing is not to scale.

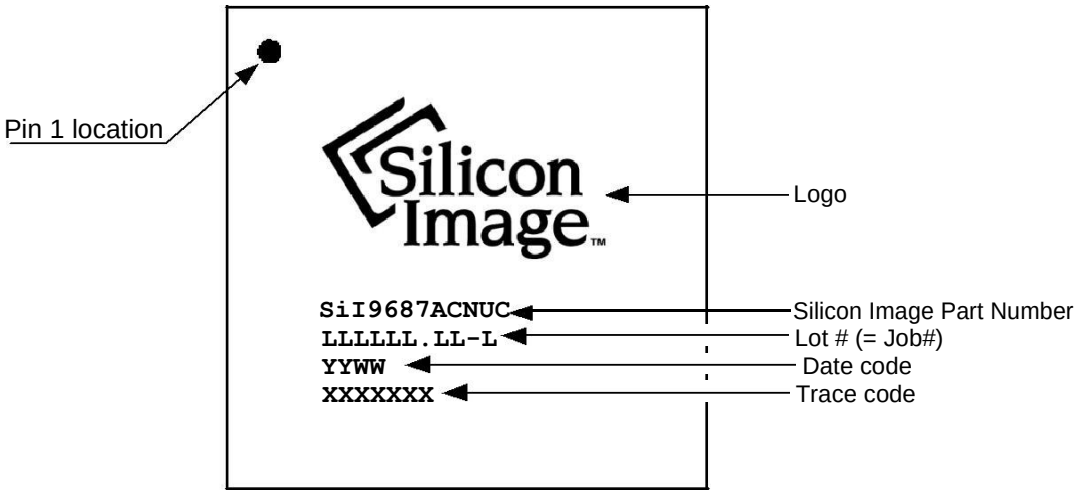


Figure 17. Marking Diagram

Ordering Information

Production Part Numbers:

Device	Part Number
SiI9687A Port Processor	SiI9687ACNUC

References

Standards Documents

Table 26 lists the abbreviations used in this document. Contact the responsible standards groups listed in Table 27 for more information on these specifications.

Table 26. Referenced Documents

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface*, Revision 1.4b, HDMI Licensing, LLC, October 2011
HCTS	*HDMI Compliance Test Specification*, Revision 1.4b, HDMI Licensing, LLC, October 2011
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.4, Digital Content Protection, LLC, July 2009
DVI	*Digital Visual Interface*, *Revision 1.0*, Digital Display Working Group, April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA, Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, June 2001
CEA-861-E	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, EIA/CEA, March 2008
EDDC	*Enhanced Display Data Channel Standard*, Version 1.1, VESA, September 1999
MHL	*MHL (Mobile High-definition Link) Specification*, Version 2.0, MHL, LLC, February 2012

Table 27. Standards Groups Contact Information

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
MHL	http://www.mhlconsortium.org	info@mhlconsortium.org	408-962-4269

Silicon Image Documents

Table 28 lists Silicon Image documents that are available from your Silicon Image sales representative.

Table 28. Silicon Image Publications

Document	Title
SiI-PR-1078	*SiI9687A Port Processor Programmer's Reference*

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