

FQB10N50CF

N-Channel QFET® FRFET® MOSFET

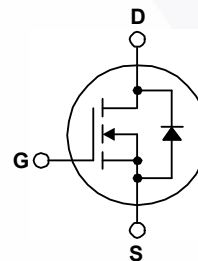
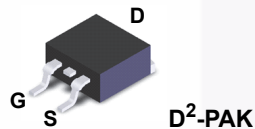
500 V, 10 A, 610 mΩ

Features

- 10 A, 500 V, $R_{DS(on)} = 610 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$
- Low gate charge (Typ. 45 nC)
- Low C_{rss} (Typ. 17.5 pF)
- 100% avalanche tested
- Fast recovery body diode

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB10N50CFM_WS	Unit
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	10
		- Continuous ($T_C = 100^\circ\text{C}$)	6.35
I_{DM}	Drain Current	- Pulsed (Note 1)	40
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	825
I_{AR}	Avalanche Current	(Note 1)	10
E_{AR}	Repetitive Avalanche Energy	(Note 1)	14.3
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	2.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	143
		- Derate above 25°C	1.14
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQB10N50CFM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.87	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in ² pad of 2 oz copper), Max.	40	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB10N50CF	FQB10N50CFM_WS	D2-PAK	330mm	24mm	800

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.5	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$	-	-	10	μA
		$V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 5\text{A}$	-	0.51	0.61	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 5\text{A}$	-	105	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1660	2210	pF
C_{oss}	Output Capacitance		-	182	240	pF
C_{rss}	Reverse Transfer Capacitance		-	17.5	26	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 10\text{A}$ $V_{GS} = 10\text{V}$ (Note 4)	-	45	60	nC
Q_{gs}	Gate to Source Gate Charge		-	8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	19	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 10\text{A}$ $R_G = 25\Omega$ (Note 4)	-	25	60	ns
t_r	Turn-On Rise Time		-	47	105	ns
$t_{d(off)}$	Turn-Off Delay Time		-	138	285	ns
t_f	Turn-Off Fall Time		-	55	120	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	10	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	40	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 10\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 10\text{A}$ $di_F/dt = 100\text{A}/\mu\text{s}$	-	91	-	ns
Q_{rr}	Reverse Recovery Charge		-	220	-	nC

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 16.5\text{mH}, I_{AS} = 10\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 10\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

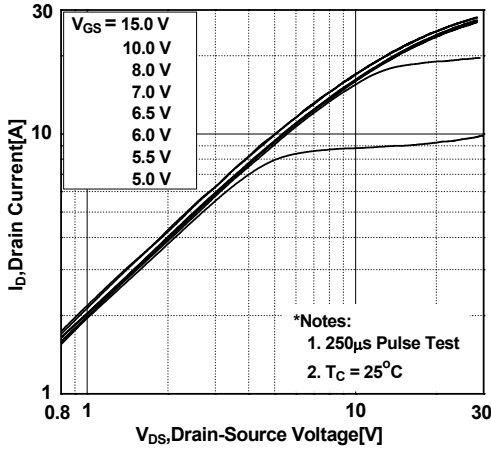


Figure 2. Transfer Characteristics

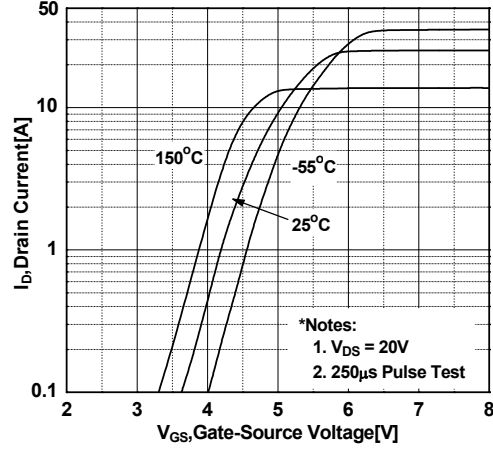


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

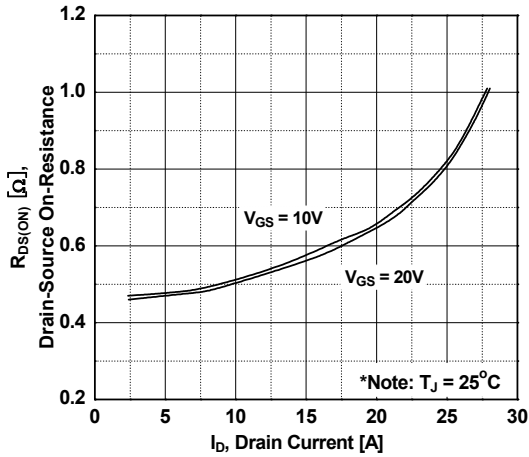


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

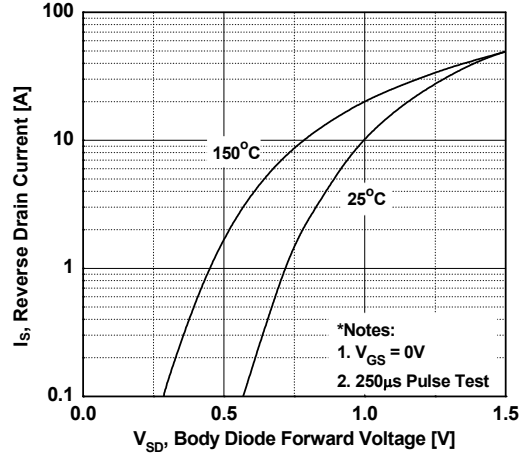


Figure 5. Capacitance Characteristics

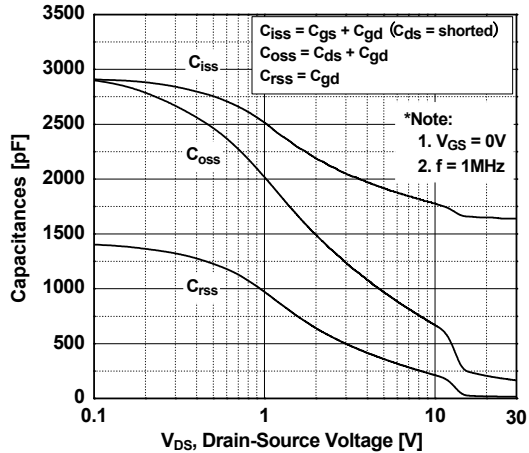
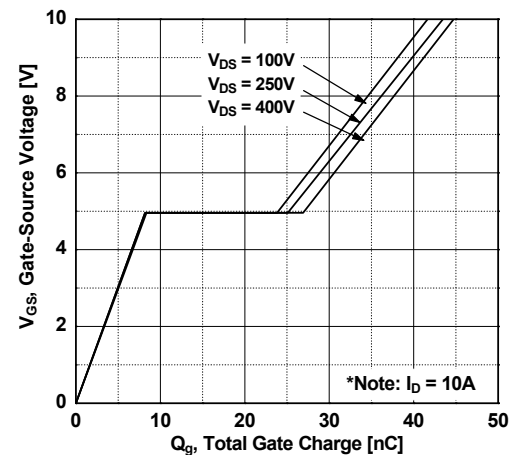


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

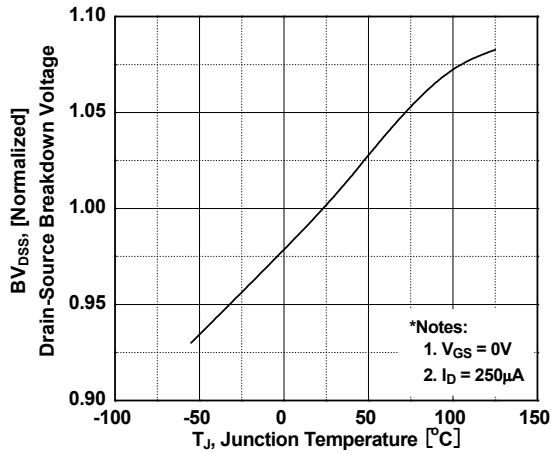


Figure 8. On-Resistance Variation vs. Temperature

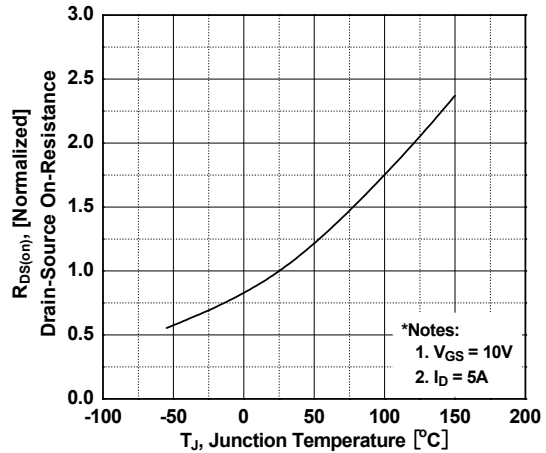


Figure 9. Maximum Safe Operating Area

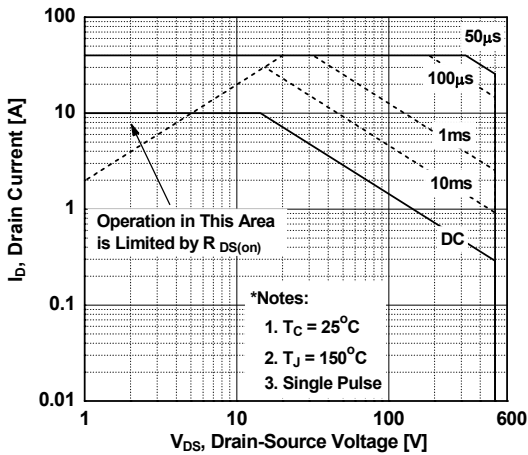


Figure 10. Maximum Drain Current vs. Case Temperature

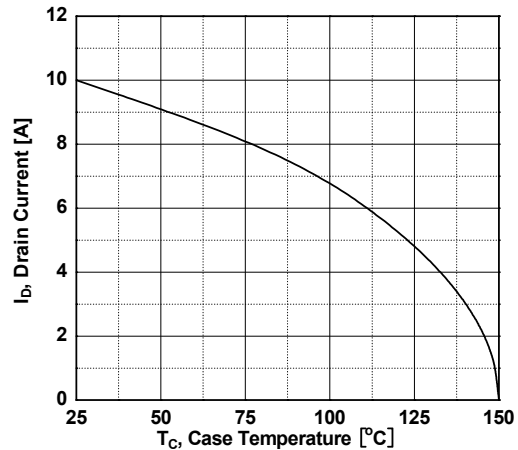


Figure 11. Transient Thermal Response Curve

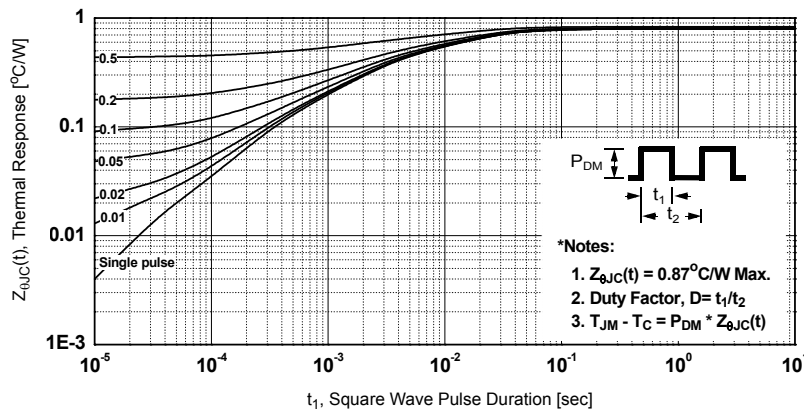


Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

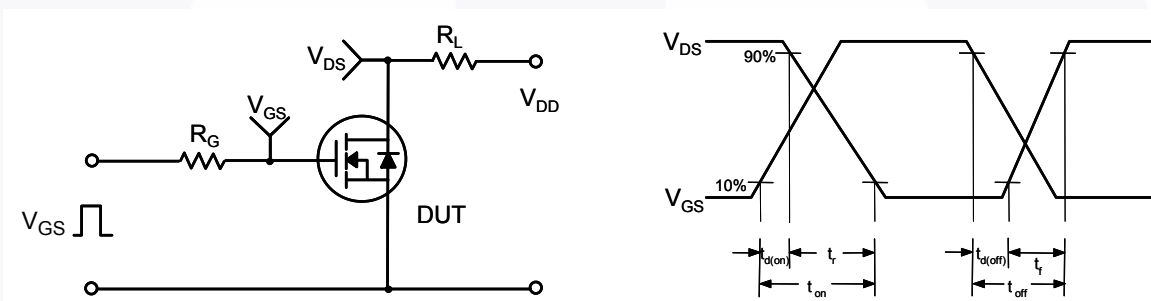


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

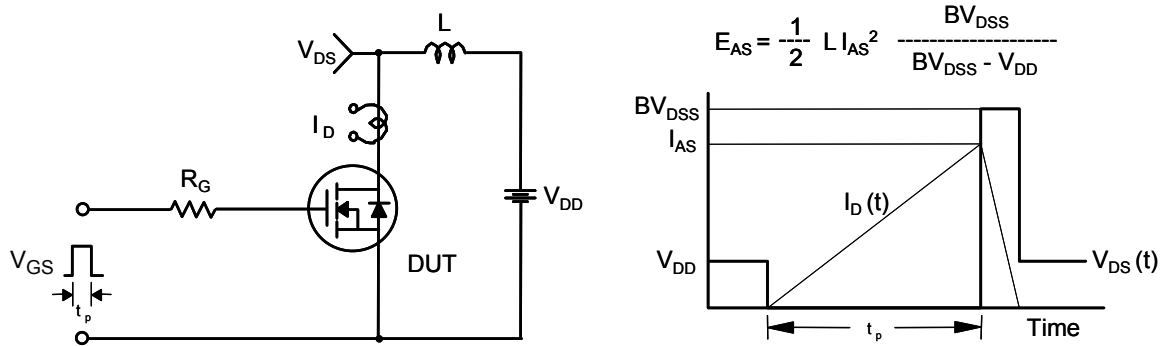
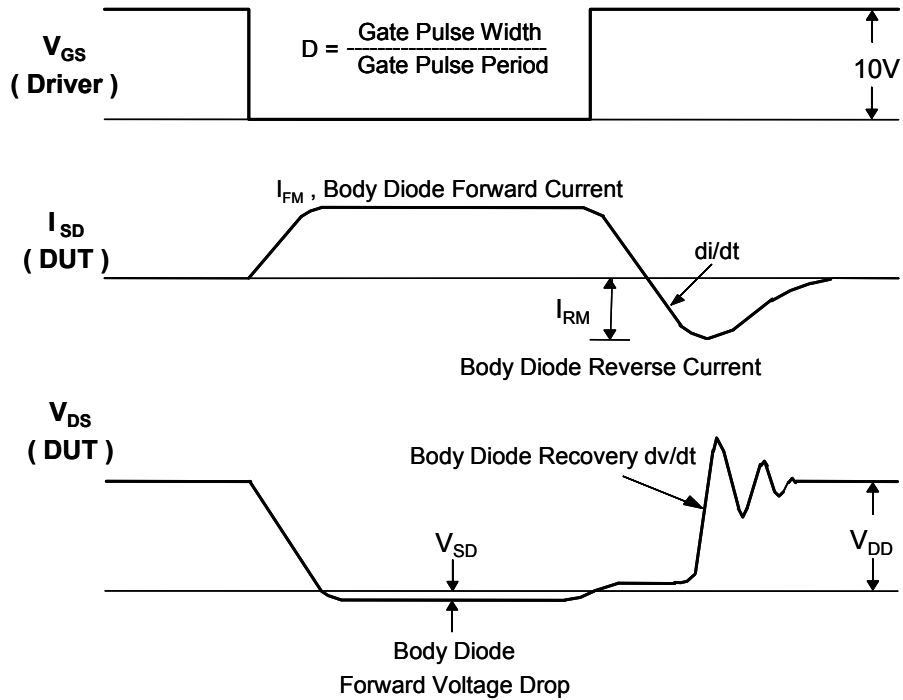
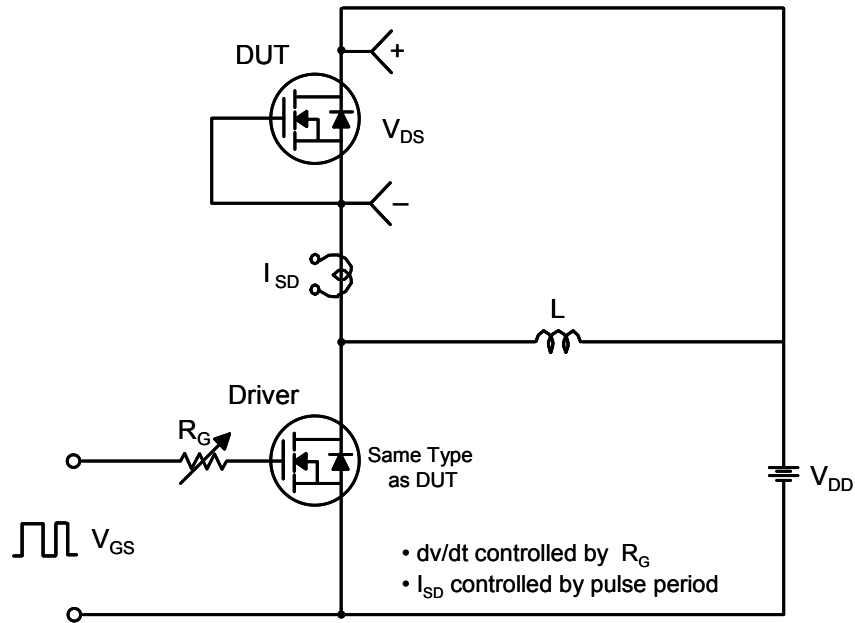


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-263 2L (D²PAK)

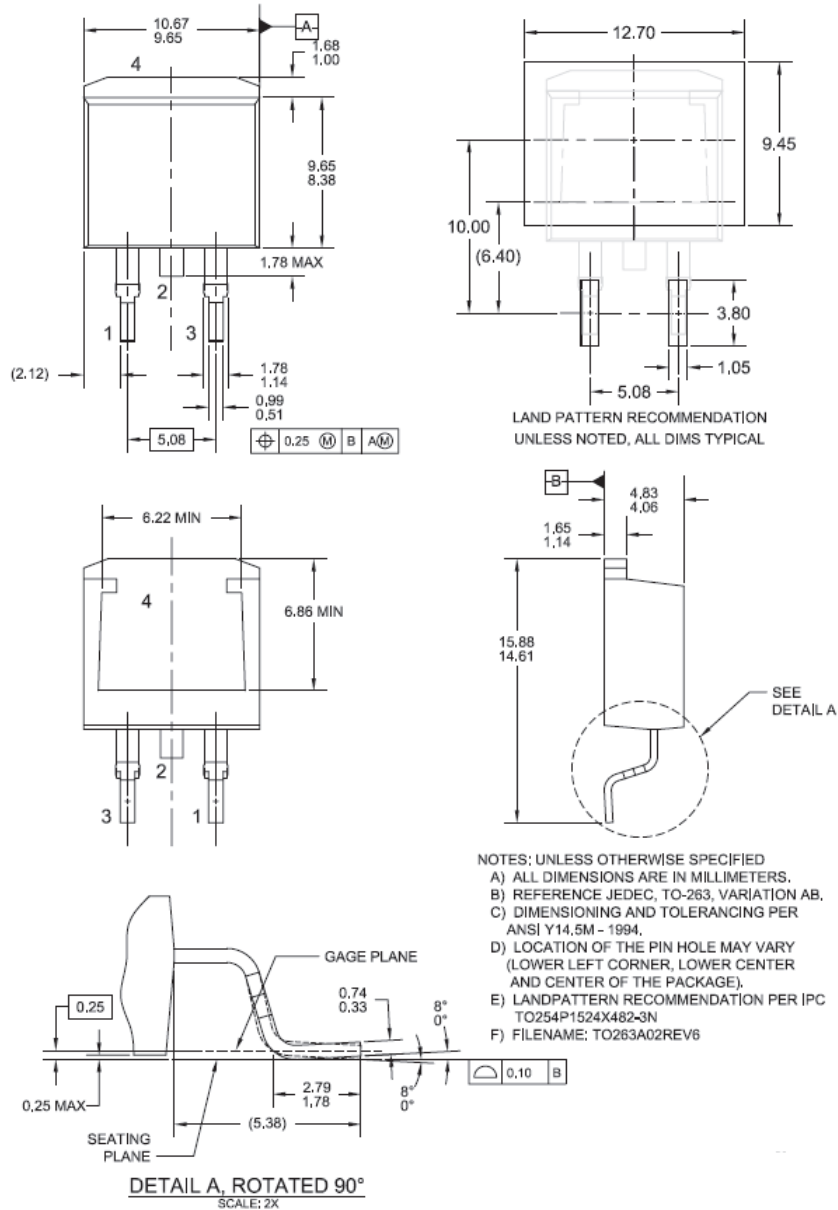


Figure 16. 2LD, TO263, Surface Mount

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Dimension in Millimeters

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