

October 2013

# FQB10N50CF

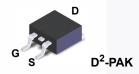
# N-Channel QFET $^{\circledR}$ FRFET $^{\circledR}$ MOSFET 500 V, 10 A, 610 m $_{\Omega}$

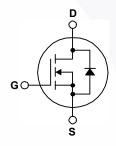
### **Features**

- 10 A, 500 V,  $R_{DS(on)}$  = 610 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 5 A
- Low gate charge (Typ. 45 nC)
- Low Crss (Typ. 17.5 pF)
- 100% avalanche tested
- · Fast recovery body diode

# **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.





# **MOSFET Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted

Symbol		Parameter	Parameter		Unit
$V_{DSS}$	Drain to Source Voltage			500	V
$V_{GSS}$	Gate to Source Voltage			±30	V
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)		10 6.35	Α
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	40	Α
E <sub>AS</sub>	Single Pulsed Avalanch	e Energy	(Note 2)	825	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	10	Α
E <sub>AR</sub>	Repetitive Avalanche Er	nergy	(Note 1)	14.3	mJ
dv/dt	Peak Diode Recovery de	v/dt	(Note 3)	2.0	V/ns
D	Dawar Dissipation	(T <sub>C</sub> = 25°C)		143	W
$P_{D}$	Power Dissipation	- Derate above 25°C		1.14	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage	Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Tempera 1/8" from Case for 5 Sec	ature for Soldering Purpose, conds		300	°C

## **Thermal Characteristics**

Symbol	Parameter	FQB10N50CFTM_WS	Unit
$R_{\thetaJC}$	Thermal Resistance, Junction to Case, Max	0.87	
В	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> pad of 2 oz copper), Max.	40	

# Package Marking and Ordering Information T<sub>C</sub> = 25°C unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB10N50CF	FQB10N50CFTM_WS	D2-PAK	330mm	24mm	800

# **Electrical Characteristics**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
$BV_DSS$	Drain to Source Breakdown Voltage	$I_D = 250\mu A, V_{GS} = 0V, T_J = 25^{\circ}C$	500	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	-	0.5	-	V/°C
I	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V , V <sub>GS</sub> = 0V	-	-	10	μА
I <sub>DSS</sub> Zero Gate voltage Drain Current		$V_{DS} = 400V, T_{C} = 125^{\circ}C$	-	-	100	μΛ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	±100	nA

# **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5A	-	0.51	0.61	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 20V, I_{D} = 5A$	-	105	ı	S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	\\ - 25\\ \\ - 0\\		-	1660	2210	pF
Coss	Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V$ f = 1MHz		-	182	240	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 111112	j	-\	17.5	26	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V			- \	45	60	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DS} = 400V, I_{D} = 10A$	j	-	8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	V <sub>GS</sub> = 10V	(Note 4)	-	19	-	nC

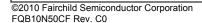
# **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			-	25	60	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 250V, I_{D} = 10A$		-	47	105	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$R_G = 25\Omega$	Ī	- /	138	285	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	-	55	120	ns

## **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	10	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	40	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 10A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 10A	-	91	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	220	-	nC

- **Notes:**1. Repetitive Rating: Pulse width limited by maximum junction temperature 2: L = 16.5mH,  $I_{AS}$  = 10A,  $V_{DD}$  = 50V,  $R_G$  = 250, Starting  $T_J$  = 25°C 3:  $I_{SD} \le$  10A, di/dt  $\le$  200A/ $\mu$ s,  $V_{DD} \le$  BV $_{DSS}$ , Starting  $T_J$  = 25°C 4: Essentially Independent of Operating Temperature Typical Characteristics



# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

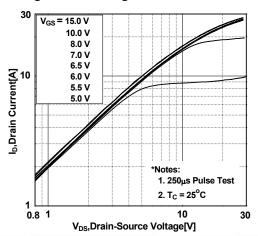


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

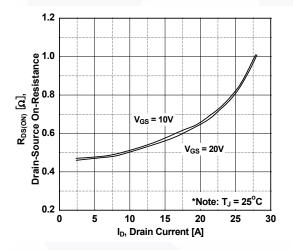


Figure 5. Capacitance Characteristics

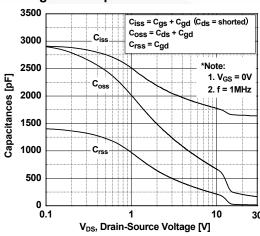


Figure 2. Transfer Characteristics

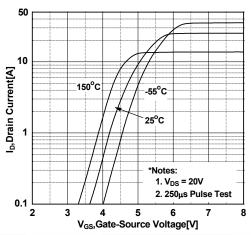


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

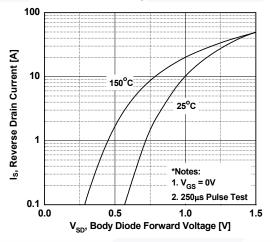
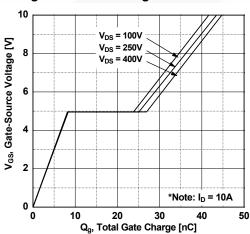


Figure 6. Gate Charge Characteristics



# **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

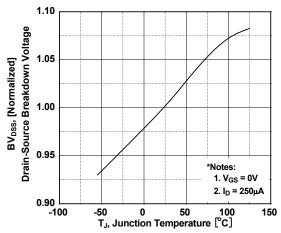


Figure 8. On-Resistance Variation vs. Temperature

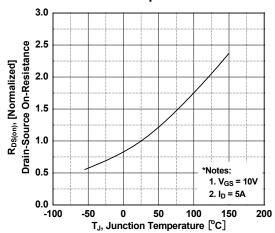


Figure 9. Maximum Safe Operating Area

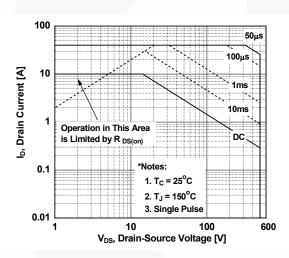


Figure 10. Maximum Drain Current vs. Case Temperature

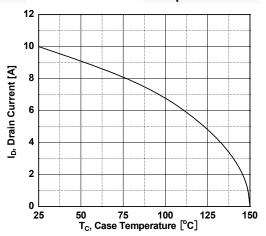


Figure 11. Transient Thermal Response Curve

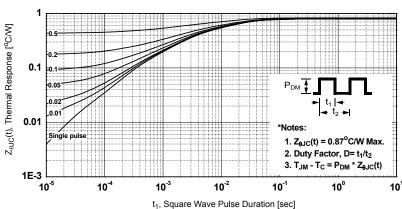


Figure 12. Gate Charge Test Circuit & Waveform

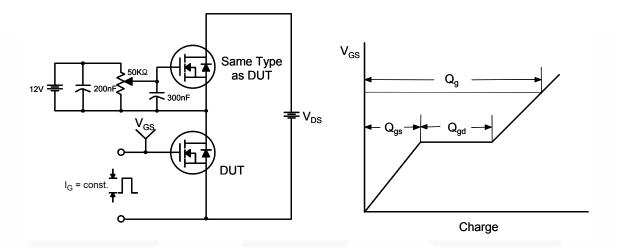


Figure 13. Resistive Switching Test Circuit & Waveforms

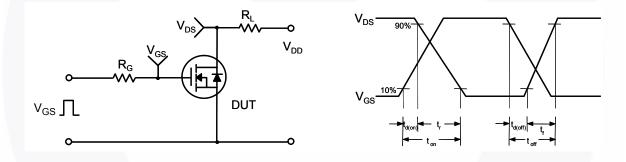
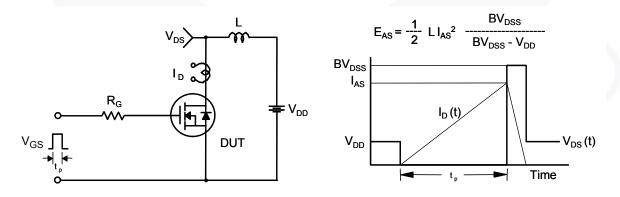


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



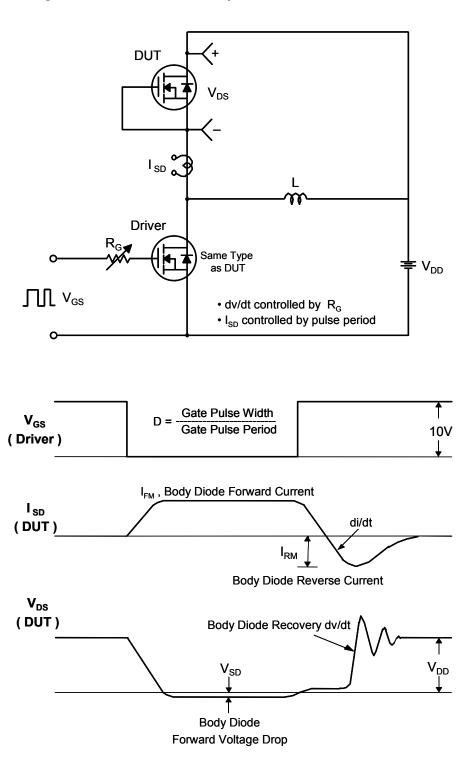


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

# **Mechanical Dimensions**

# TO-263 2L (D<sup>2</sup>PAK)

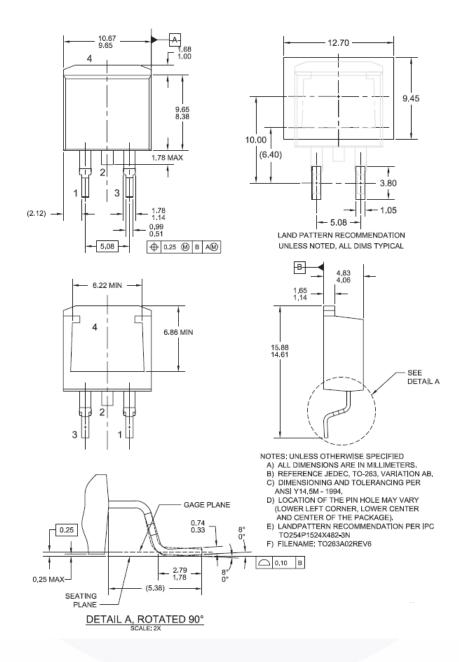


Figure 16. 2LD, TO263, Surface Mount

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Dimension in Millimeters





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