Zero-Drift Operational Amplifier

FEATURES

- *Guaranteed* Max Offset: 5μV
- *Guaranteed* Max Offset Drift: 0.05μV/°C
- Typ Offset Drift: 0.01μV/°C
- Excellent Long Term Stability: 100nV/√Month
- *Guaranteed* Max Input Bias Current: 30pA
- Over Operating Temperature Range:
  - *Guaranteed* Min Gain: 120dB
  - *Guaranteed* Min CMRR: 120dB
  - *Guaranteed* Min PSRR: 120dB
- Single Supply Operation: 4.75V to 16V (Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V^- with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

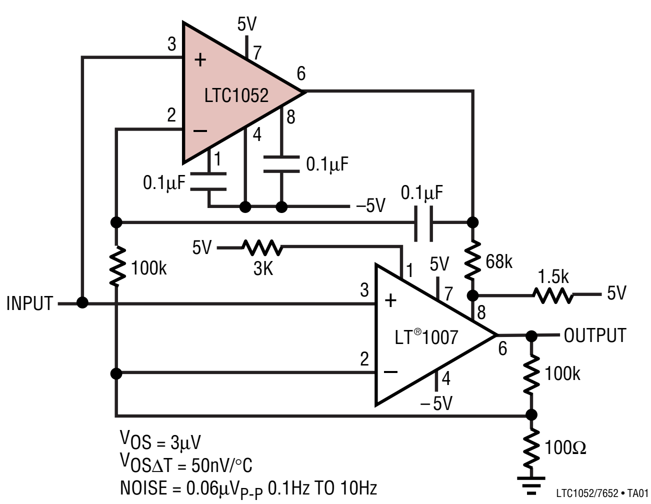
The LTC®1052 and LTC7652 are low noise zero-drift op amps manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common mode voltage are corrected. This, coupled with picoampere input currents, gives these amplifiers unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample-and-hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin and 16-pin versions to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

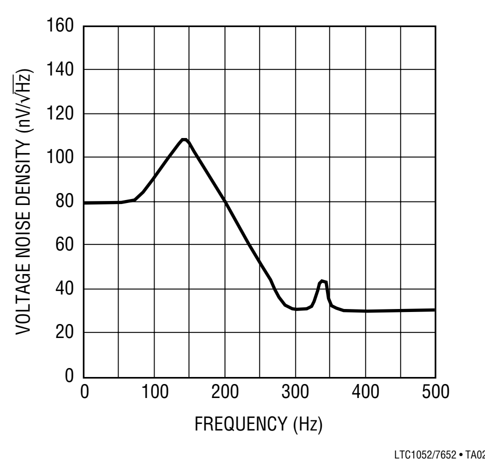
TYPICAL APPLICATION

Ultralow Noise, Low Drift Amplifier



V_{OS} = 3μV
$V_{OS}\Delta T$ = 50nV/°C
NOISE = 0.06μV_{P-P} 0.1Hz TO 10Hz

Noise Spectrum

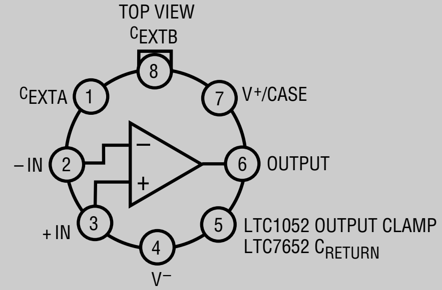


ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage .... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short Circuit Duration .... Indefinite
Storage Temperature Range .... –55°C to 150°C

Operating Temperature Range
LTC1052C/LTC7652C .... –40°C to 85°C
LTC1052M **(OBSOLETE)**..................... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

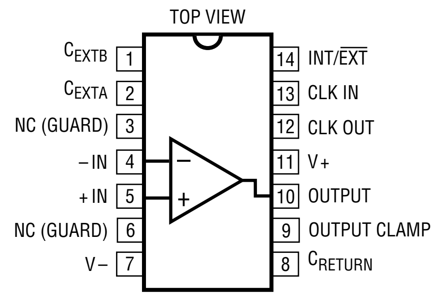
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

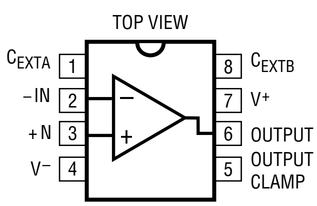
ORDER PART NUMBER	REPLACES
LTC7652CH	ICL7652CTV ICL7652ITV ICL7650CTV-1 ICL7650ITV-1
LTC1052CH	ICL7650CTV ICL7650ITV
LTC1052MH	ICL7650MTV



N PACKAGE, 14-LEAD CERDIP
T_{JMAX} = 110°C, θ_{JA} = 130°C/W

J PACKAGE, 14-LEAD CERDIP
OBSOLETE PACKAGE
Consider the N14 Package for Alternate Source

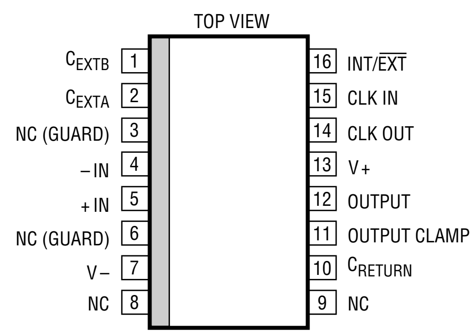
ORDER PART NUMBER	REPLACES
LTC1052CN	ICL7652CPD ICL7650CPD
LTC1052CJ	ICL7652IJD ICL7650IJD
LTC1052MJ	ICL7650MJD



N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 150°C/W

J8 PACKAGE, 8-LEAD CERDIP
OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

ORDER PART NUMBER	REPLACES
LTC1052CN8	ICL7650CPA
LTC1052CJ8 LTC1052MJ8	ICL7650IJA



SW PACKAGE
16-LEAD PLASTIC (WIDE) SO
T_{JMAX} = 110°C, θ_{JA} = 150°C/W

ORDER PART NUMBER	REPLACES
LTC1052CSW	LTC1052CS

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_S = \pm5V$, test circuit TC1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1052M MIN	LTC1052M TYP	LTC1052M MAX	LTC1052C/LTC7652C MIN	LTC1052C/LTC7652C TYP	LTC1052C/LTC7652C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 3)			±0.5	±5		±0.5	±5	µV
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Drift	(Note 3)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
$\Delta V_{OS}/\Delta Time$	Long-Term Offset Voltage Stability				100			100		$nV/\sqrt{Month}$
I_{OS}	Input Offset Current		 ●		±30	±90 ±2000		±30	±90 ±350	pA pA
I_B	Input Bias Current		 ●		±1	±30 ±1000		±1	±30 ±175	pA pA
e_{nP-P}	Input Noise Voltage	$R_S = 100\Omega$, DC to 10HZ, TC3 $R_S = 100\Omega$, DC to 1HZ, TC3			1.5 0.5			1.5 0.5		μV_{P-P} μV_{P-P}
I_n	Input Noise Current	f = 10Hz (Note 5)			0.6			0.6		$fA/\sqrt{Hz}$
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to 2.7V	●	120	140		120	140		dB
PSRR	Power Supply Rejection Ratio	$V_{SUPPLY} = \pm2.375V$ to $\pm8V$	●	120	150		120	150		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = \pm4V$	●	120	150		120	150		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 10k$ $R_L = 100k$	●	±4.7	±4.85 ±4.95		±4.7	±4.85 ±4.95		V V
SR	Slew Rate	$R_L = 10k$, $C_L = 50pF$			4			4		V/µs
GBW	Gain Bandwidth Product				1.2			1.2		MHz
I_S	Supply Current	No Load	 ●		1.7	2.0 3.0		1.7	2.0 3.0	mA mA
f_S	Internal Sampling Frequency				330			330		Hz
	Clamp On Current	$R_L = 100k$	●	25	100		25	100		µA
	Clamp Off Current	$-4V < V_{OUT} < 4V$	 ●		10	100 2		10	100 1	pA nA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+, or less than V^-, may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052/LTC7652.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of the voltage levels in high speed automatic testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB}, A_{VOL}, CMRR and PSRR are measured to insure proper operation of the nulling loop to ensure meeting the V_{OS} and V_{OS} drift specifications. See Package-Induced V_{OS} in the Applications Information section.

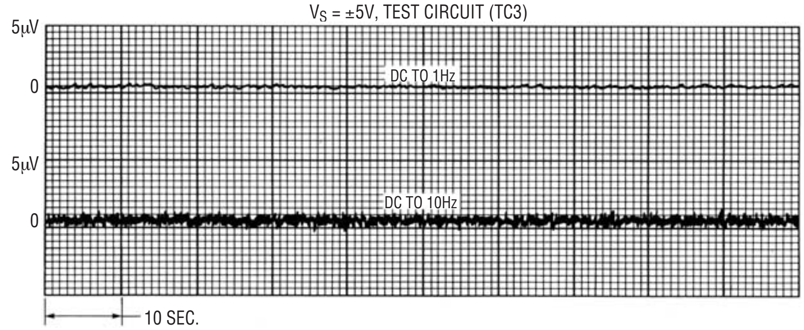
Note 4: Output clamp not connected.

Note 5: Current noise is calculated from the formula: $i_n = (2q\ I_B)^{1/2}$, where $q = 1.6 \cdot 10^{-19}$ coulomb.

TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise Voltage

$V_S = \pm5V$, TEST CIRCUIT (TC3)



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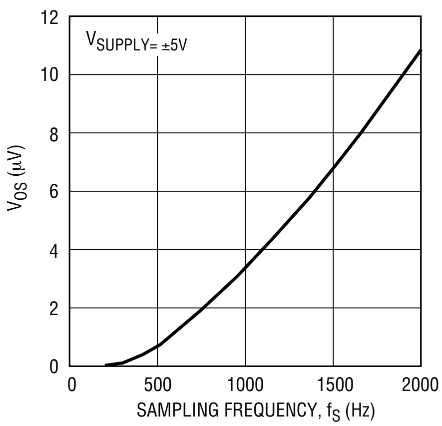
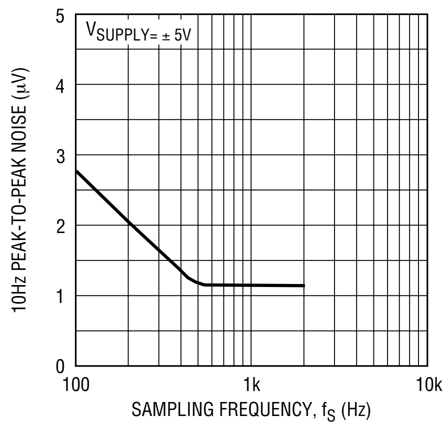
TYPICAL PERFORMANCE CHARACTERISTICS

Offset Voltage vs Sampling Frequency



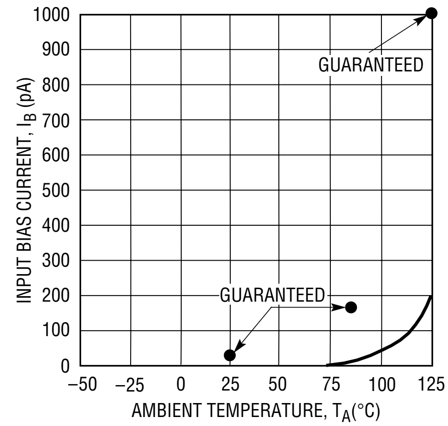
LTC1052/7652 • TPC01

10Hz P-P Noise vs Sampling Frequency



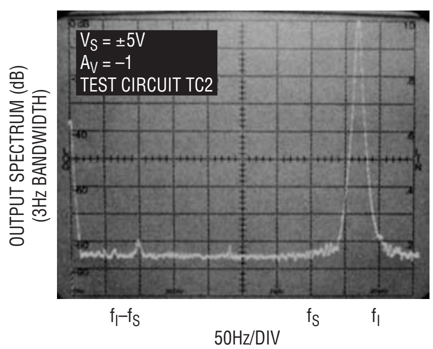
LTC1052/7652 • TPC02

Input Bias Current vs Temperature

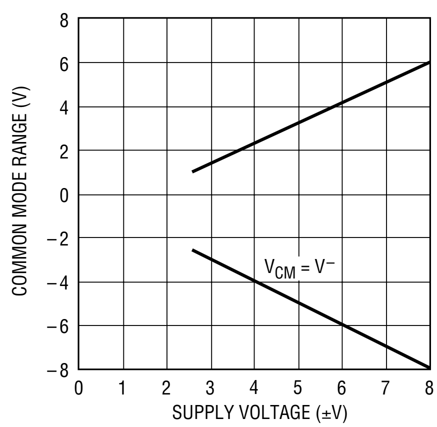


LTC1052/7652 • TPC03

Aliasing Error

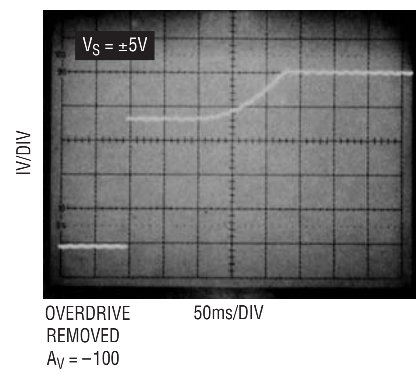


Common Mode Input Range vs Supply Voltage

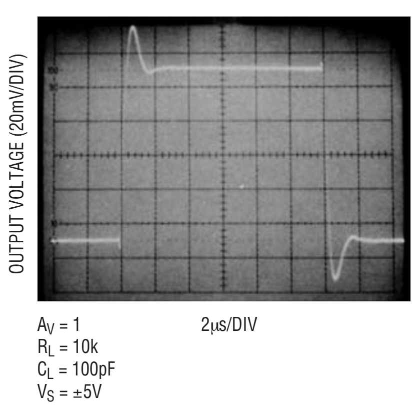


LTC1052/7652 • TPC04

Overload Recovery (Output Clamp Not Used)

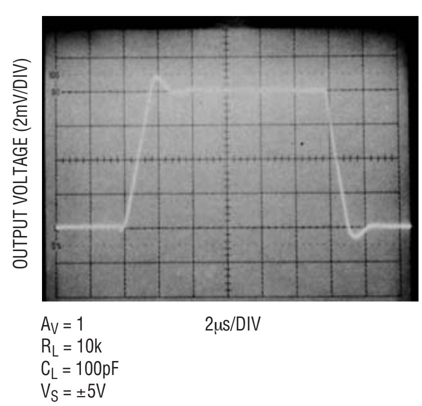


Small-Signal Transient Response*

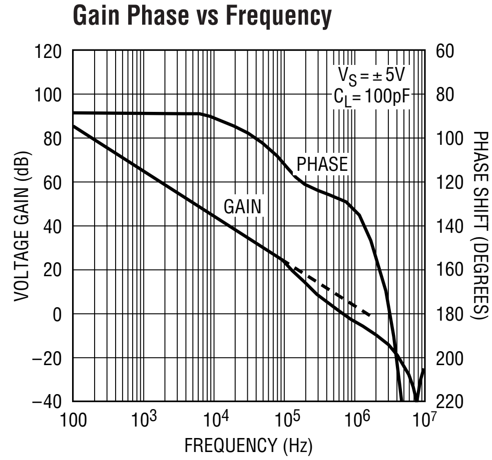


*RESPONSE IS NOT DEPENDENT ON PHASE OF CLOCK

Large-Signal Transient Response*



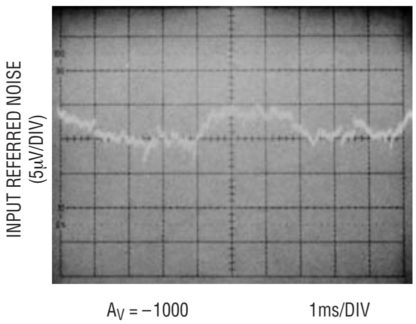
Gain Phase vs Frequency



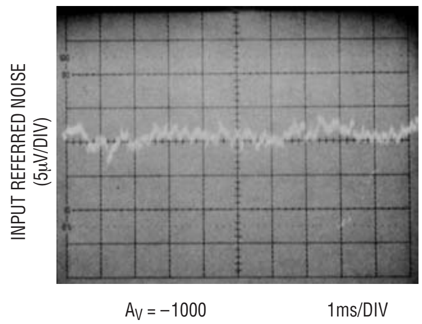
LTC1052/LTC7652 • TPC06

TYPICAL PERFORMANCE CHARACTERISTICS

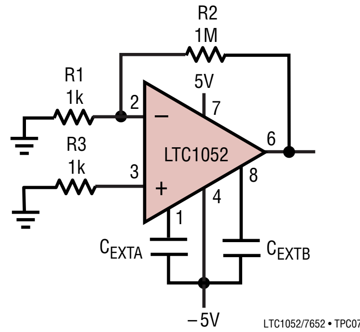
Broadband Noise, C_{EXT} = 0.1µF



Broadband Noise, C_{EXT} = 1.0µF

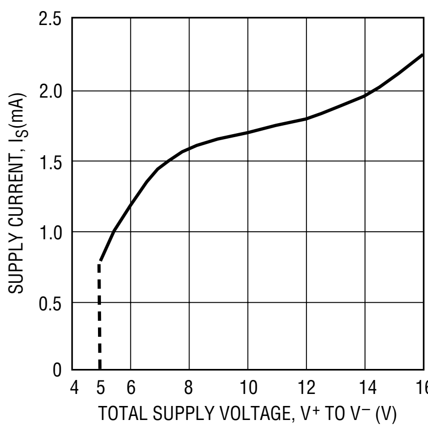


Broadband Noise Test Circuit (TC2)



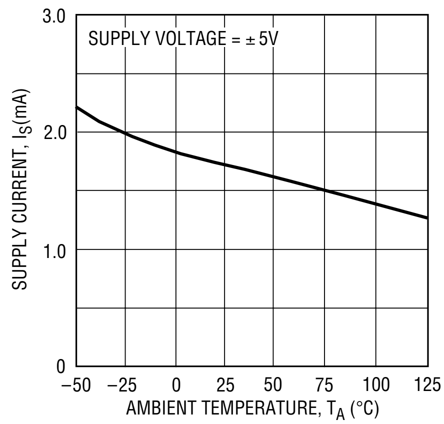
LTC1052/7652 • TPC07

Supply Current vs Supply Voltage



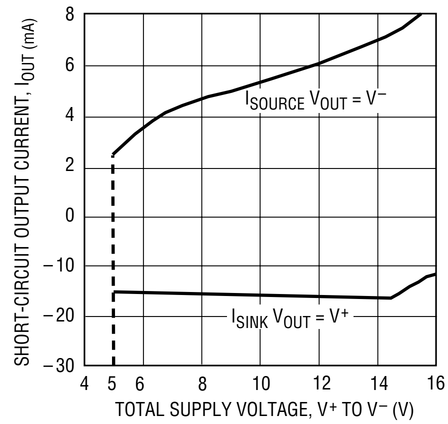
LTC1052/LTC7652 • TPC08

Supply Current vs Temperature



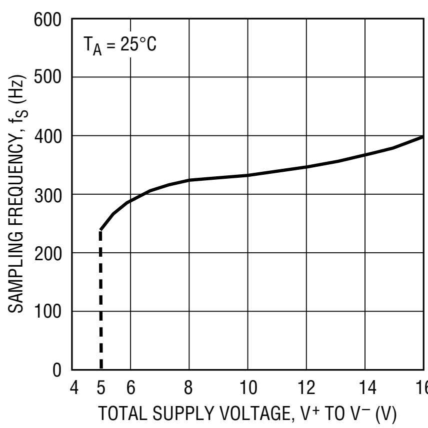
LTC1052/LTC7652 • TPC09

Output Short-Circuit Current vs Supply Voltage



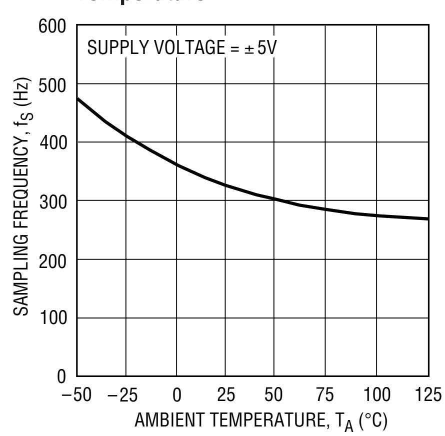
LTC1052/LTC7652 • TPC10

Sampling Frequency vs Voltage



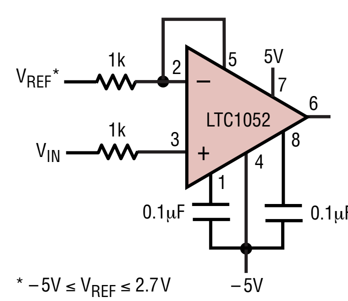
LTC1052/LTC7652 • TPC11

Sampling Frequency vs Temperature



LT1052/LTC7652 • TPC12

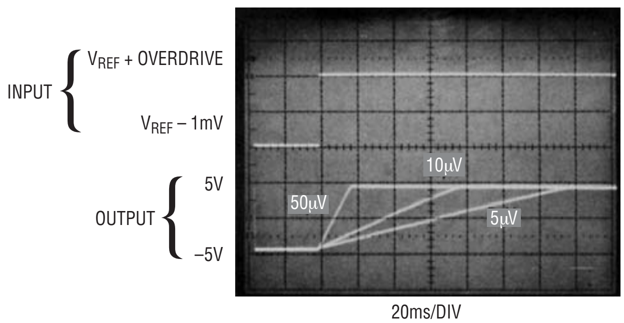
Comparator Operation



LTC1052/7652 • TPC13

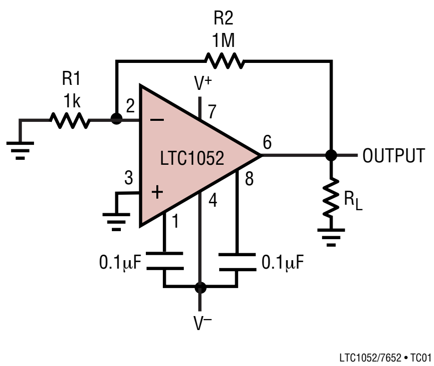
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time vs Overdrive

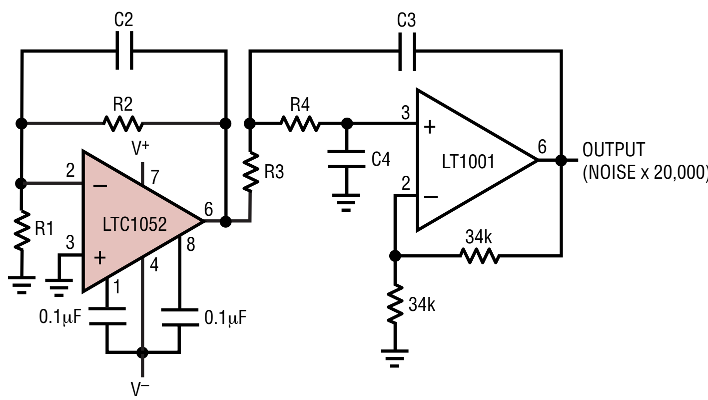


TEST CIRCUITS

Electrical Characteristics Test Circuit (TC1)



DC to 10Hz and DC to 1HZ Noise Test Circuit (TC3)



BANDWIDTH	R1	R2	R3	R4	C2	C3	C4
10Hz	16.2Ω	162k	16.2k	16.2k	0.1μF	1.0μF	1.0μF
1Hz	16.2Ω	162k	162k	162k	1.0μF	1.0μF	1.0μF

LTC1052/7652 • TC02

THEORY OF OPERATION

DC OPERATION

The shaded portion of the LTC1052 block diagram (Figure 1a) entirely determines the amplifier's DC characteristics. During the auto zero portion of the cycle, the g_{m1} inputs are shorted together and a feedback path is closed around the input stage to null its offset. Switch S2 and capacitor C_{EXTA} act as a sample-and-hold to store the nulling voltage during the next step—the sampling cycle.

In the sampling cycle, the zeroed amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S2 act as a sample-and-hold to store the amplified input signal during the auto zero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the auto zero cycle the g_{m1} inputs are not only shorted together, but are also shorted to the inverting input. This forces nulling with the common mode voltage present and accounts for the extremely high CMRR of the LTC1052. In the same fashion, variations in

THEORY OF OPERATION

power supply are also nulled. For nulling to take place, the offset voltage, common mode voltage and power supply must not change at a frequency which is high compared to the frequency response of the nulling loop.

AC OPERATION AND ALIASING ERRORS

So far, the DC performance of the LTC1052 has been explained. As the input signal frequency increases, the problem of aliasing must be addressed. Aliasing is the spurious formation of low and high frequency signals caused by the mixing of the input signal with the sampling frequency, f_S. The frequency of the error signals, f_E, is:

$$f_E = f_S \pm f_I$$

where f_I = input signal frequency.

Normally it is the difference frequency ($f_S - f_I$) which is of concern because the high frequency ($f_S + f_I$) can be easily filtered. As the input frequency approaches the sampling frequency, the difference frequency approaches zero and will cause DC errors—the exact problem that the zero-drift amplifier is meant to eliminate.

The solution is simple; filter the input so the sampling loop never sees any frequency near the sampling frequency.

At a frequency well below the sampling frequency, the LTC1052 forces I_1 to equal I_2 (see Figure 1b). This makes δI zero, thus the gain of the sampling loop zero at this and higher frequencies (i.e., a low pass filter). The corner frequency of this low pass filter is set by the output stage pole ($1/R_{L4}\, g_{m5}\, R_{L5}\, C2$).

For frequencies above this pole, I_2 is:

$$I_2 = V_{IN}\, g_{m6} \bullet \frac{1}{SC2} \bullet SC1$$

and

$$I_1 - I_2 = V_{IN}\, g_{m1} - V_{IN}\, g_{m6} \bullet \frac{C1}{C2}$$

The LTC1052 is very carefully designed so that $g_{m1} = g_{m6}$ and C1 = C2. Substituting these values in the above equation shows $I_1 - I_2 = 0$.

The g_{m6} input stage, with Cl and C2, not only filters the input to the sampling loop, but also acts as a high frequency path to give the LTC1052 good high frequency response. The unity-gain cross frequencies for both the DC path and high frequency path are identical

$$\left[f3dB = \frac{1}{2\pi}(g_{m1}/C1) = \frac{1}{2\pi}(g_{m6}/C2)\right]$$

thereby making the frequency response smooth and continuous while eliminating sampling noise in the output as the loop transitions from the high gain DC loop to the high frequency loop.

The typical curves show just how well the amplifier works. The output spectrum shows that the difference frequency ($f_I - f_S$ = 100Hz) is down by 80dB and the frequency response curve shows no abnormalities or perturbations. Also note the well-behaved small and large-signal step responses and the absence of the sampling frequency in the output spectrum. If the dynamics of the amplifier (i.e., slew rate and overshoot), depend on the sampling clock, the sampling frequency will appear in the output spectrum.

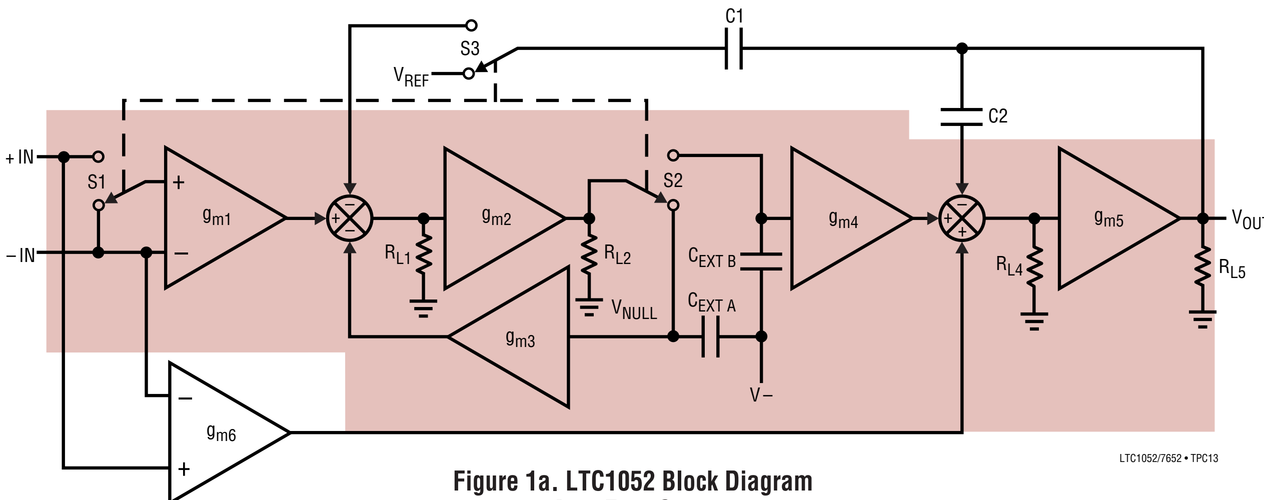


Figure 1a. LTC1052 Block Diagram Auto Zero Cycle

THEORY OF OPERATION

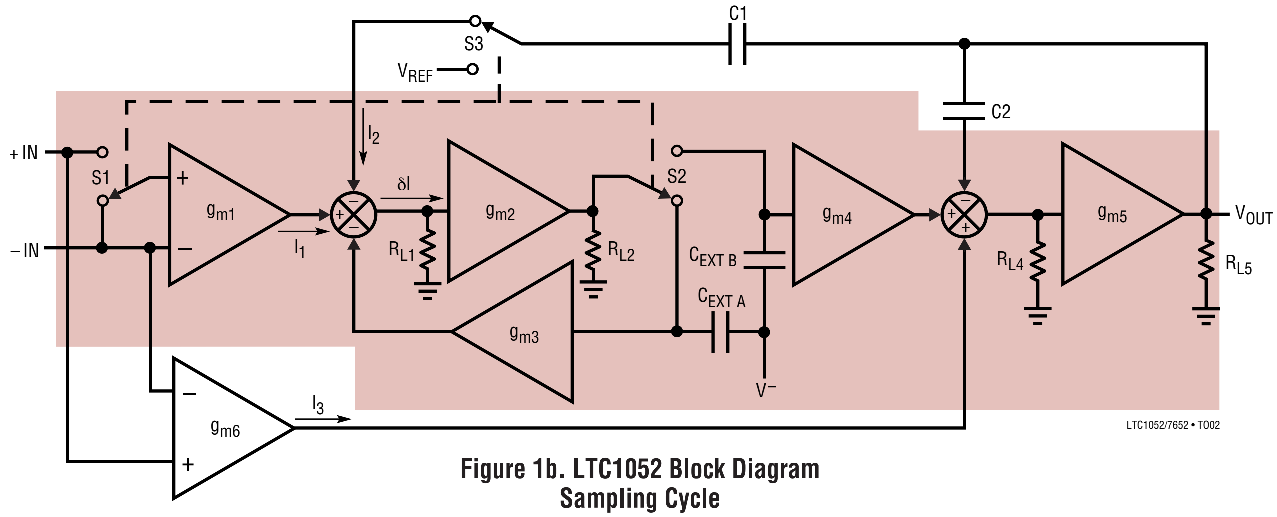


Figure 1b. LTC1052 Block Diagram Sampling Cycle

APPLICATIONS INFORMATION

EXTERNAL CAPACITORS

C_{EXTA} and C_{EXTB} are the holding elements of a sample-and-hold circuit. The important capacitor characteristics are leakage current and dielectric absorption. A high quality film-type capacitor such as mylar or polypropylene provides excellent performance. However, low grade capacitors such as ceramic are suitable in many applications.

Capacitors with very high dielectric absorption (ceramic) can take several seconds to settle after power is first turned on. This settling appears as clock ripple on the output and, as the capacitor settles, the ripple gradually disappears. If fast settling after power turn-on is important, mylar or polypropylene is recommended.

Above 85°C, leakage, both from the holding capacitors and the printed circuit board, becomes important. To maintain the capabilities of the LTC1052 it may be necessary to use Teflon™ capacitors and Teflon standoffs when operating at 125°C (see Achieving Picoampere/Microvolt Performance).

C_{EXTA} and C_{EXTB} are normally in the range of 0.1μF to 1.0μF. All specifications are guaranteed with 0.1μF and the broadband noise (refer to Typical Performance Characteristics) is only very slightly degraded with 0.1μF. Output clock ripple is not present for capacitors of 0.1μF or greater at any temperature.

On competitive devices, connecting C_{EXTA} and C_{EXTB} to V^- causes an increase in amplifier noise. Design changes have eliminated this problem on the LTC1052. On the 14-pin LTC1052 and 8-pin LTC7652, the capacitors can be returned to V^- or C_{RETURN} with no change in noise performance.

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

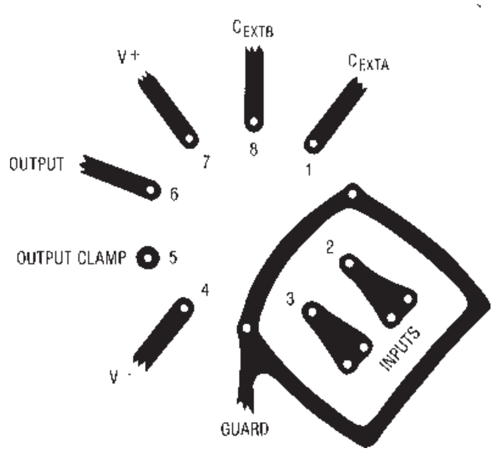
In order to realize the picoampere level of accuracy of the LTC1052, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary—particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations, the guard ring should be tied to ground; in noninverting

Teflon is a trademark of Dupont.

APPLICATIONS INFORMATION

connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.



Microvolts

Thermocouple effects must be considered if the LTC1052's ultralow drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C—4 times the maximum drift specification of the LTC1052. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35µV/°C−700 times the maximum drift specification of the LTC1052.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 2 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

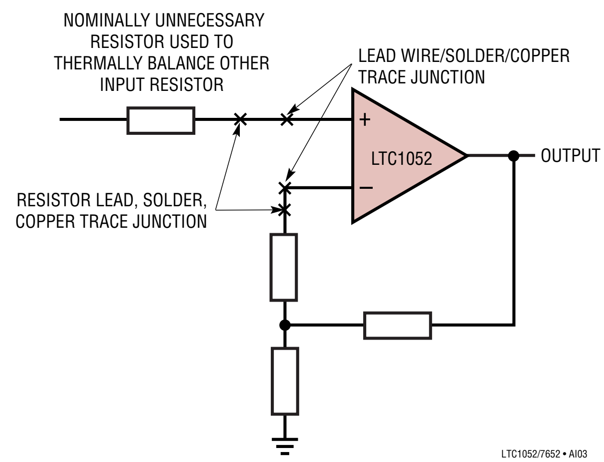


Figure 2

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

Table 1. Resistor Thermal EMF

RESISTOR TYPE	THERMAL EMF/°C GRADIENT
Tin Oxide	~mV/°C
Carbon Composition	~450µV/°C
Metal Film	~20µV/°C
Wire Wound	
Evenohm	~2µV/°C
Manganin	~2µV/°C

APPLICATIONS INFORMATION

When all of these errors are considered, it may seem impossible to take advantage of the extremely low drift specifications of the LTC1052. To show that this is not the case, examine the temperature test circuit of Figure 3. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity and thermal resistance each input sees is balanced because of the symmetrical connection of resistors and their identical size. Thermal EMF-induced shifts are equal in phase and amplitude, thus cancellation occurs.

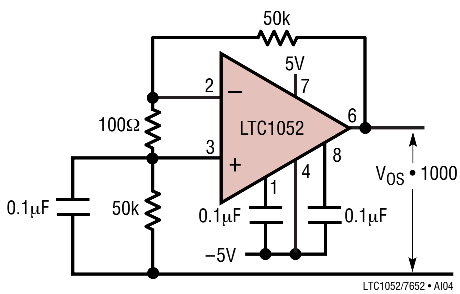


Figure 3. Offset Drift Test Circuit

Figure 4 shows the response of this circuit under temperature transient conditions. Metal film resistors and an 8-pin DIP socket were used. Care was taken in the construction to thermally balance the inputs to the amplifier. The units were placed in an oven and allowed to stabilize at 25°C. The recording was started and after 100 seconds the oven, preset to 125°C, was switched on. The test was first performed on an 8-pin plastic package and then was repeated for a TO-5 package plugged into the same test board. It is significant that the change in V_{OS}, even under these severe thermal transient conditions, is quite good. As temperature stabilizes, note that the steady-state change of V_{OS} is well within the maximum ±0.05μV/°C drift specification.

Very slight air currents can still affect even this arrangement. Figure 5 shows strip charts of output noise both with the circuit covered and with no cover in "still" air. This data illustrates why it is often prudent to enclose the LTC1052 and its attendant components inside some form of thermal baffle.

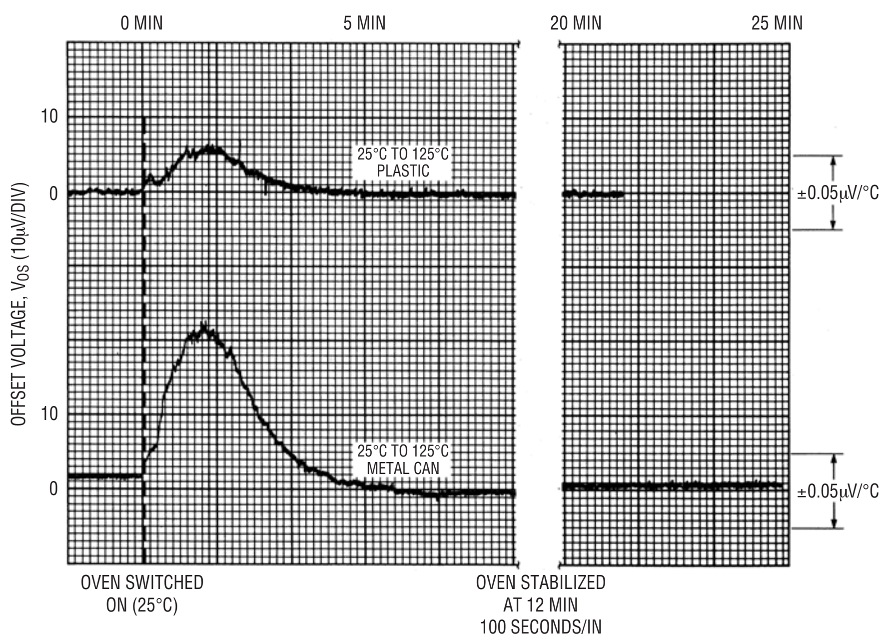


Figure 4. Transient Response of Offset Drift Test Circuit with 100°C Temperature Step

APPLICATIONS INFORMATION

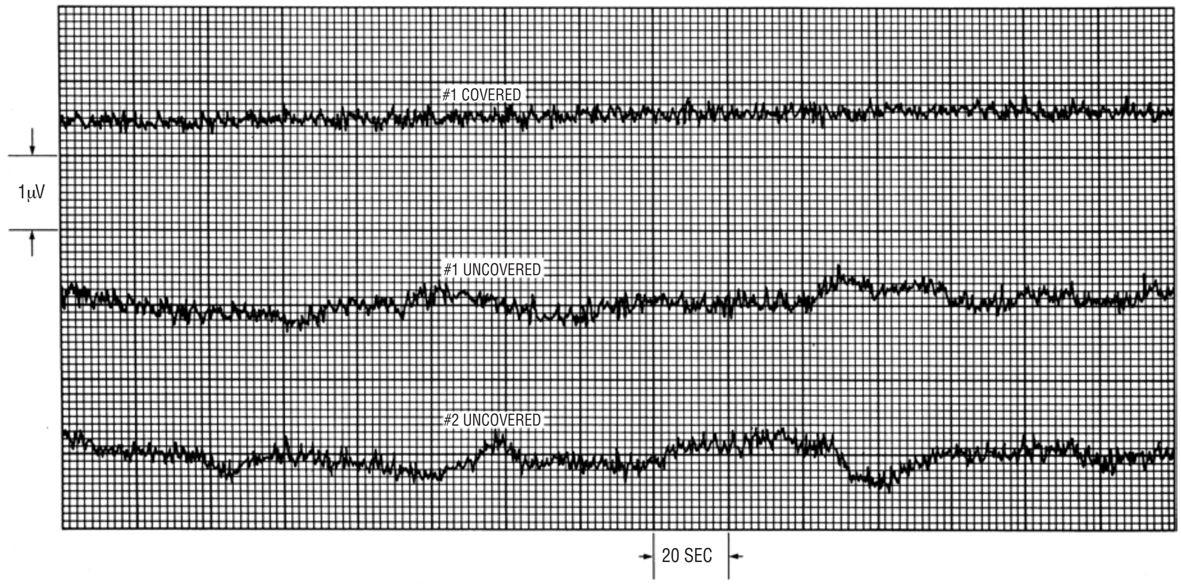


Figure 5. DC to 1Hz (Test Circuit TC3)

PACKAGE-INDUCED OFFSET VOLTAGE

Since the LTC1052 is constantly fixing its own offset, it may be asked why there is any error at all, even under transient temperature conditions. The answer is simple. The LTC1052 can only fix offsets inside its own nulling loop. There are many thermal junctions outside this loop that cannot be distinguished from legitimate signals.

Some have been discussed previously, but the package thermal EMF effects are an important source of errors.

Notice the difference in the thermal response curves of Figure 4. This can only be attributed to the package since everything else is identical. In fact, the V_{OS} specification is set by the package-induced warm-up drift, not by the LTC1052. TO-99 metal cans exhibit the worst warm-up drift and Linear Technology sample tests TO-99 lots to minimize this problem.

Two things make 100% screening costly: (1) The extreme precision required on the LTC1052 and (2) the thermal time constant of the package is 0.5 to 3 minutes, depending on package type. The first precludes the use of automatic handling equipment and the second takes a long time. Bench test equipment is available to 100% test for warmed-up drift if offsets of less than ±5μV are required.

CLOCK

The LTC1052 has an internal clock, setting the nominal sampling frequency at 330Hz. On 8-pin devices, there is no way to control the clock externally. In some applications it may be desirable to control the sampling clock and this is the function of the 14-pin device.

CLK IN, CLK OUT and INT/$\overline{EXT}$ are provided to accomplish this. With no external connection, an internal pull-up holds INT/$\overline{EXT}$ at the V^+ supply and the 14-pin device self-oscillates at 330Hz. In this mode there is a signal on the CLK IN pin of 660Hz (2 times sampling frequency) with a 30% duty cycle. A divide-by-two drives the CLK OUT pin and sets the sampling frequency.

To use an external clock, connect INT/$\overline{EXT}$ to V^- and the external clock to CLK IN. The logic threshold of CLK IN is 2.5V below the positive supply; this allows CMOS logic to drive it directly with logic supplies of V^+ and ground. CLK IN can be driven from V^+ to V^- if desired. The duty cycle of the external clock is not particularly critical but should be kept between 30% and 60%.

Capacitance between CLK IN and CLK OUT (pins 13 and 12) can cause the divide-by-two circuit to malfunction. To avoid this, keep this capacitance below 5pF.

APPLICATIONS INFORMATION

OUTPUT CLAMP

If the LTC1052 is driven into saturation, the nulling loop, attempting to force the differential input voltage to zero, will drive C_{EXTA} and C_{EXTB} to a supply rail. After the saturating drive is removed, the capacitors take a finite time to recover—this is the overload recovery time. The overload recovery is longest when the capacitors are driven to the negative rail (refer to Overload Recovery in the Typical Performance Characteristics section). The overload recovery time in this case is typically 225ms. In the opposite direction (i.e., C_{EXTA} and C_{EXTB} at positive rail), it is about ten times faster (25ms). The overload recovery time for the LTC1052 is much faster than competitive devices; however, if a faster overload recovery time is necessary, the output clamp function can be used.

When the output clamp is connected to the negative input it prevents the amplifier from saturating, thus keeping C_{EXTA} and C_{EXTB} at their nominal voltages. The output clamp is a switch that turns on when the output gets to within approximately 1V of either supply rail. This switch is in parallel with the amplifier's feedback resistor. As the output moves closer to the rail, the switch on resistance decreases, reducing the closed loop gain. The output swing is reduced when the clamp function is used.

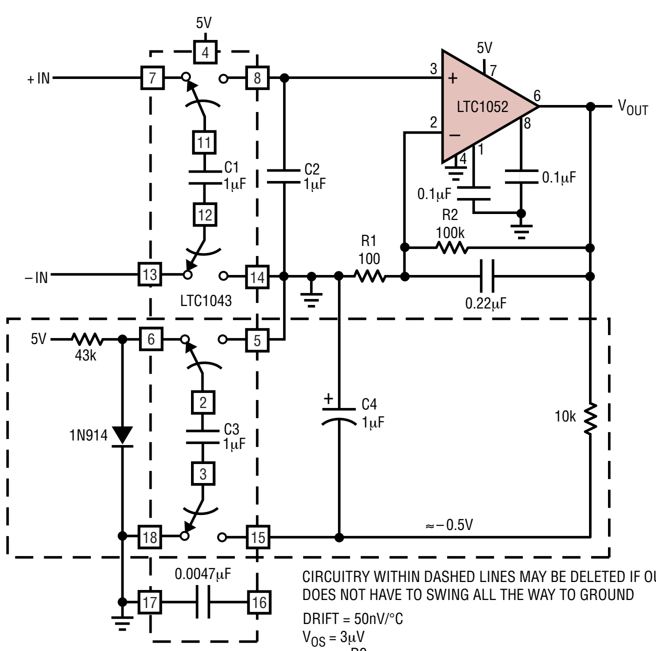
How much current the output clamp leaks when off is important because, when used, it is connected to the amplifier's negative input. Any current acts like input bias current and will degrade accuracy. At the other extreme, the maximum current the clamp conducts when on determines how much overdrive the clamp will take, and still keep the amplifier from saturating. Both of these numbers are guaranteed in the Electrical Characteristics section.

LOW SUPPLY OPERATION

The minimum supply voltage for proper operation of the LTC1052 is typically 4.0V (±2.0V). In single supply applications, PSRR is guaranteed down to 4.7V (±2.35V). This assures proper operation down to the minimum TTL specified voltage of 4.75V.

TYPICAL APPLICATIONS

5V Powered Ultraprecision Instrumentation Amplifier

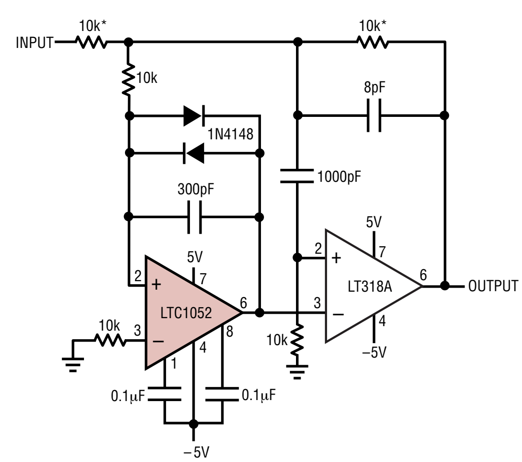


CIRCUITRY WITHIN DASHED LINES MAY BE DELETED IF OUTPUT DOES NOT HAVE TO SWING ALL THE WAY TO GROUND

DRIFT = 50nV/°C
V_{OS} = 3µV
GAIN = $\frac{R2}{R1}$ + 1
CMRR = >120dB DC – 20kHz
BANDWIDTH = 10Hz

LTC1052/7652 • TA03

Fast Precision Inverter



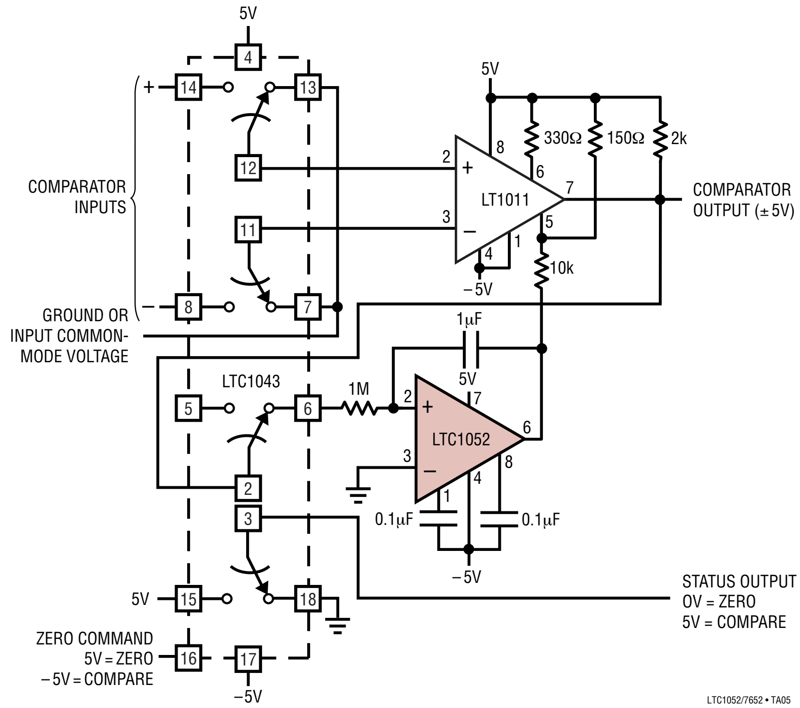
*1% METAL FILM
FULL POWER BANDWIDTH = 2MHz
SLEW RATE = 40V/µs
SETTLING (10V STEP) = 12µs TO 0.01%
BIAS CURRENT DC = 30pA
OFFSET DRIFT = 50nV/°C
OFFSET VOLTAGE = 5µV

LTC1052/7652 • TA04

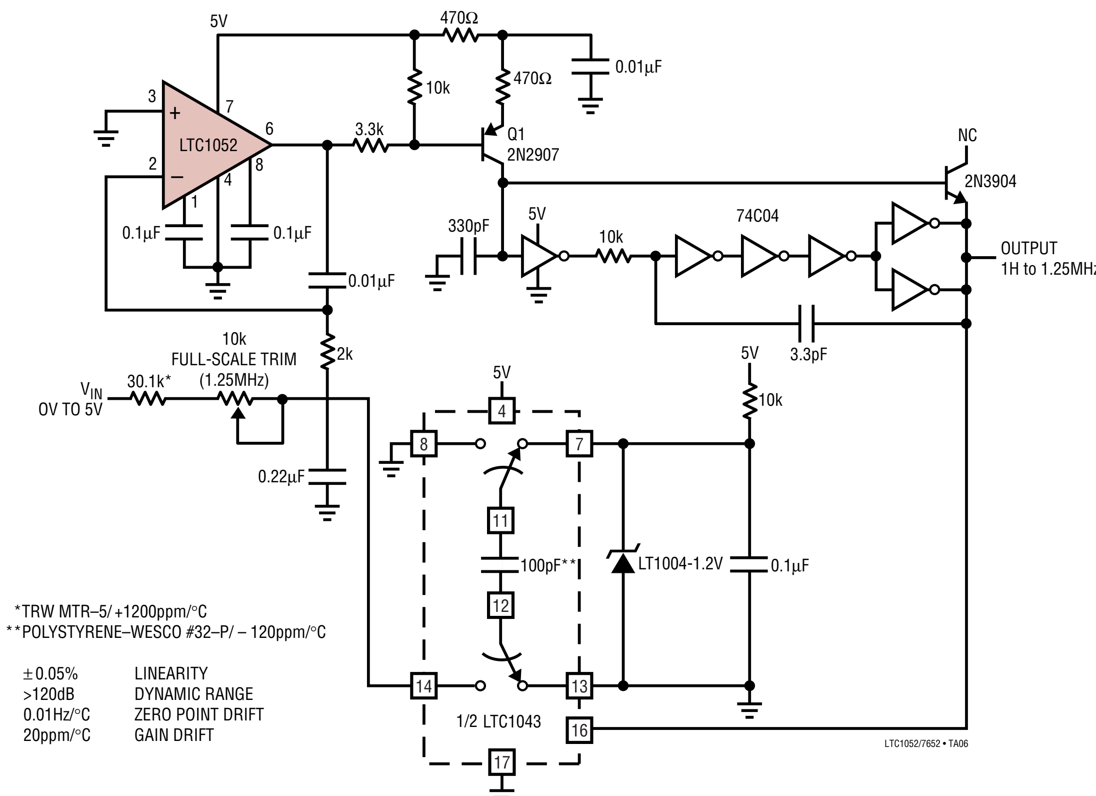
1052fa

TYPICAL APPLICATIONS

Offset Stabilized Comparator

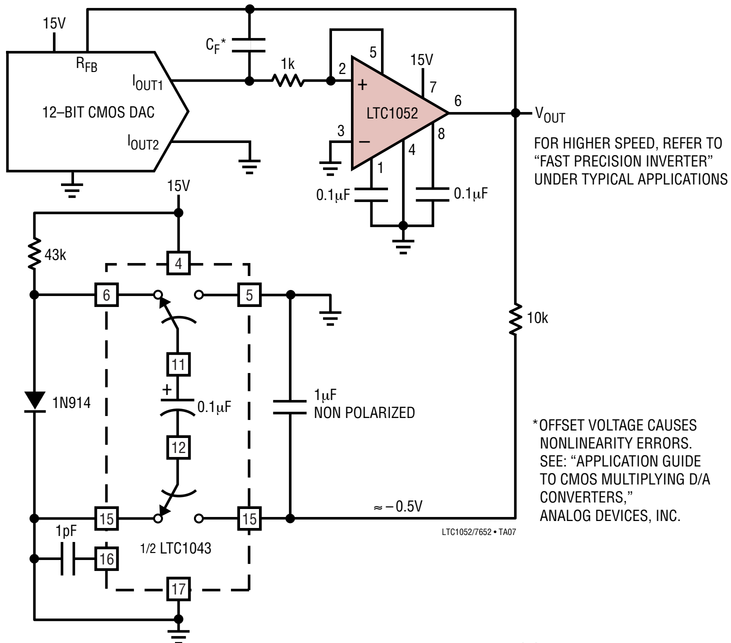


1HZ to 1.25MHz Voltage-to-Frequency Converter (5V Supply)

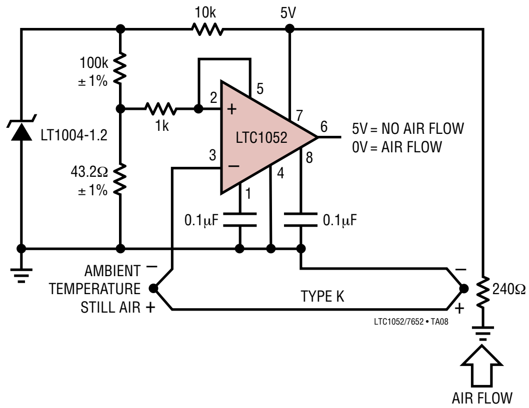


TYPICAL APPLICATIONS

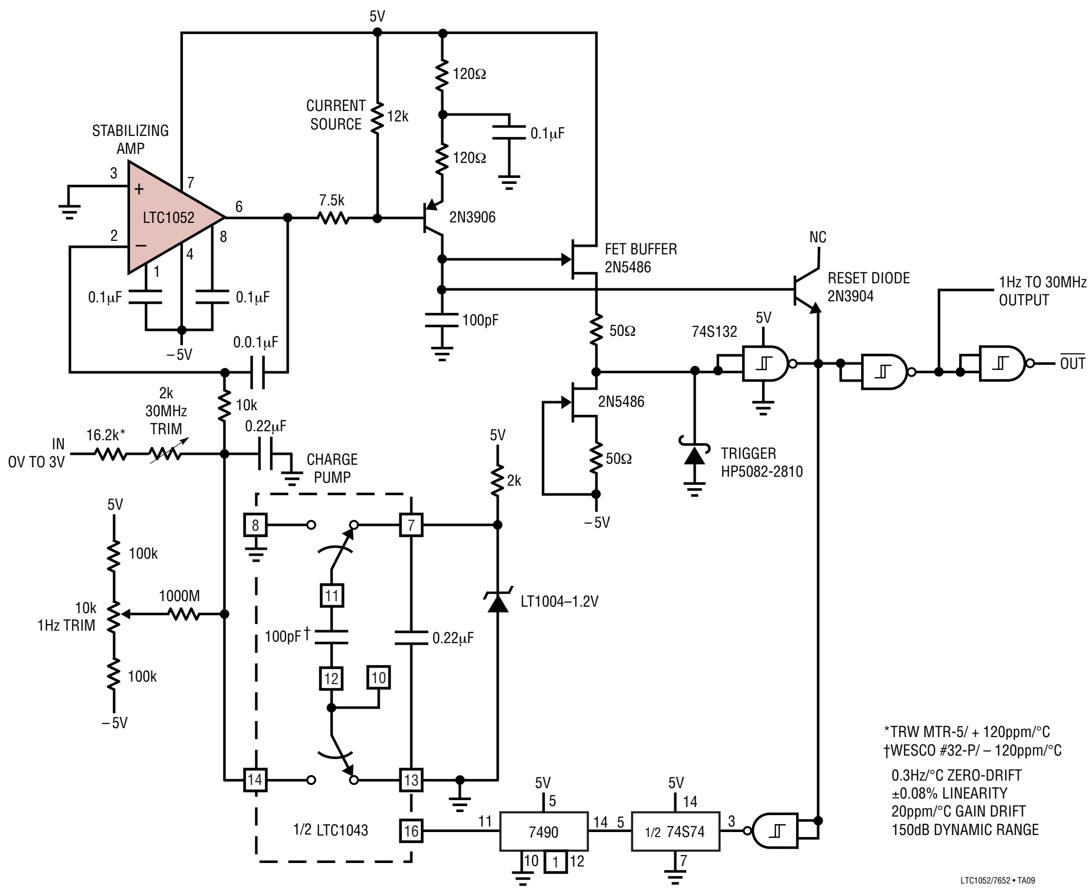
No V_{OS} Adjust* CMOS DAC Buffer—Single Supply



Air Flow Detector

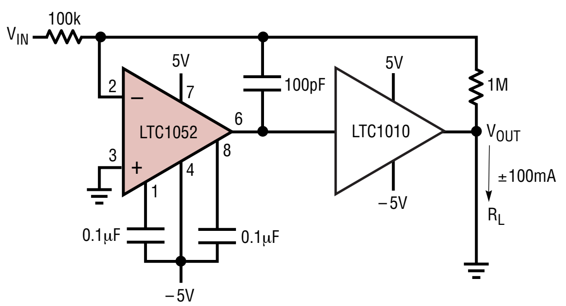


1Hz to 30MHz Voltage-to-Frequency Converter



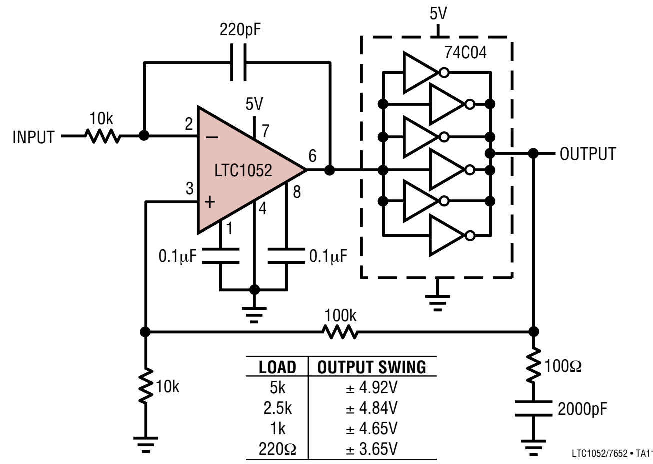
TYPICAL APPLICATIONS

±100mA Output Drive



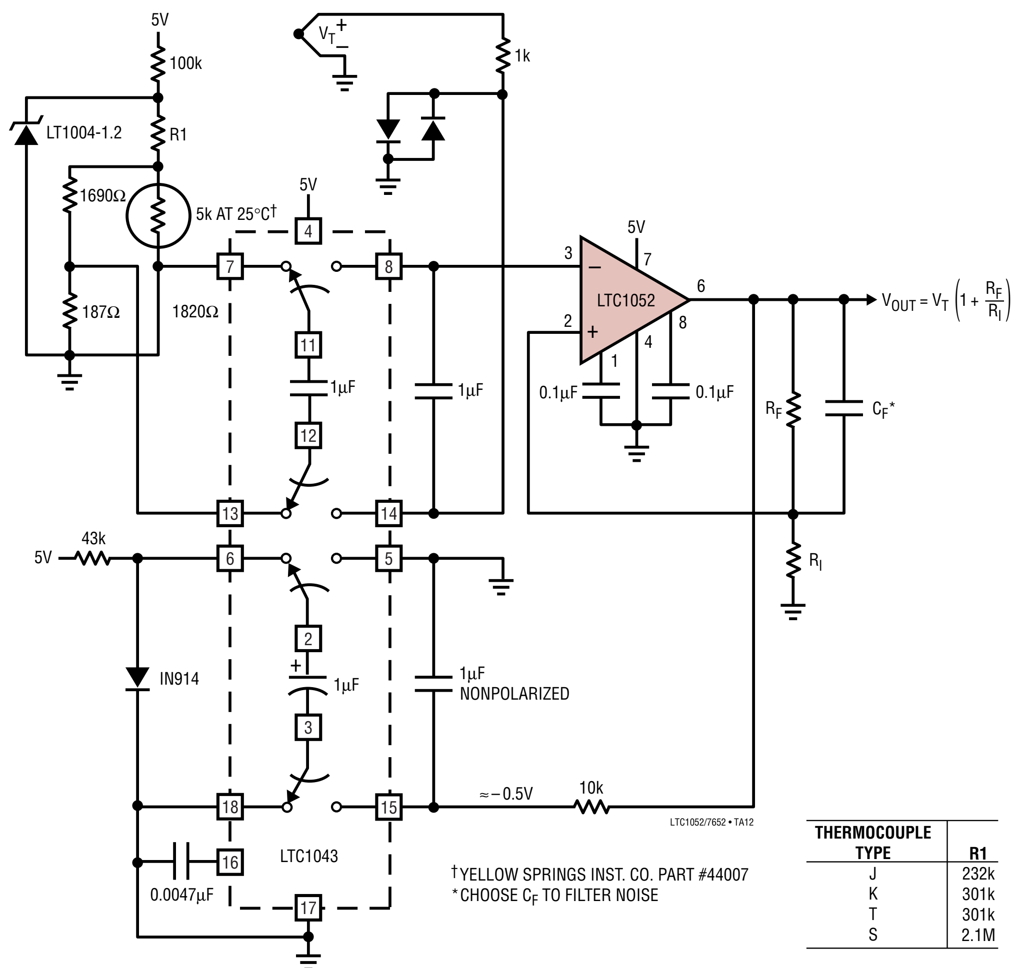
V_{OS} = 5µV
$V_{OS}/\Delta T$ = 50µV/°C
GAIN = 10
FULL POWER BANDWIDTH = 1kHz

Increasing Output Current



LOAD	OUTPUT SWING
5k	± 4.92V
2.5k	± 4.84V
1k	± 4.65V
220Ω	± 3.65V

Single 5V Thermocouple Amplifier with Cold Junction Compensation

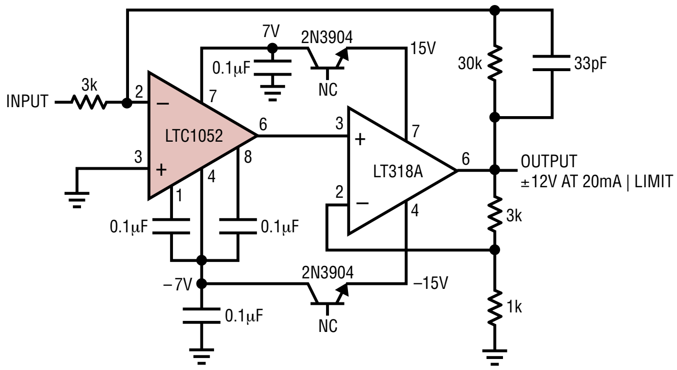


†YELLOW SPRINGS INST. CO. PART #44007
*CHOOSE C_F TO FILTER NOISE

THERMOCOUPLE TYPE	R1
J	232k
K	301k
T	301k
S	2.1M

TYPICAL APPLICATIONS

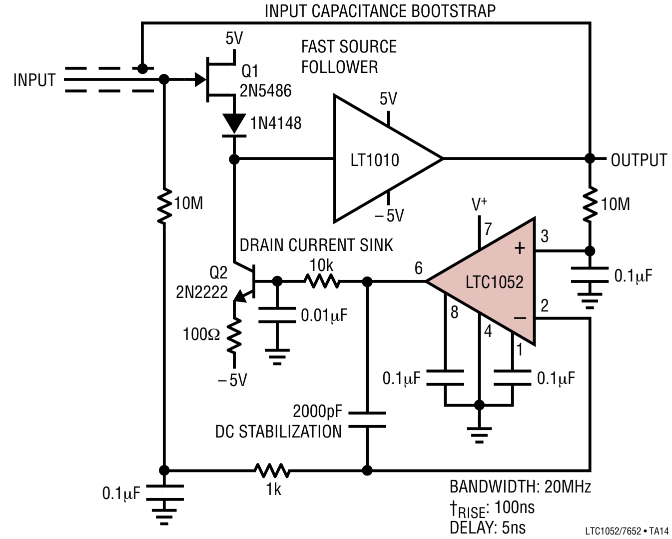
Increasing Output Current and Voltage ($V_{SUPPLY} = \pm 15V$)



STABLE FOR ALL GAINS, INVERTING AND NONINVERTING, OBSERVE LTC1052 COMMON MODE INPUT LIMITS

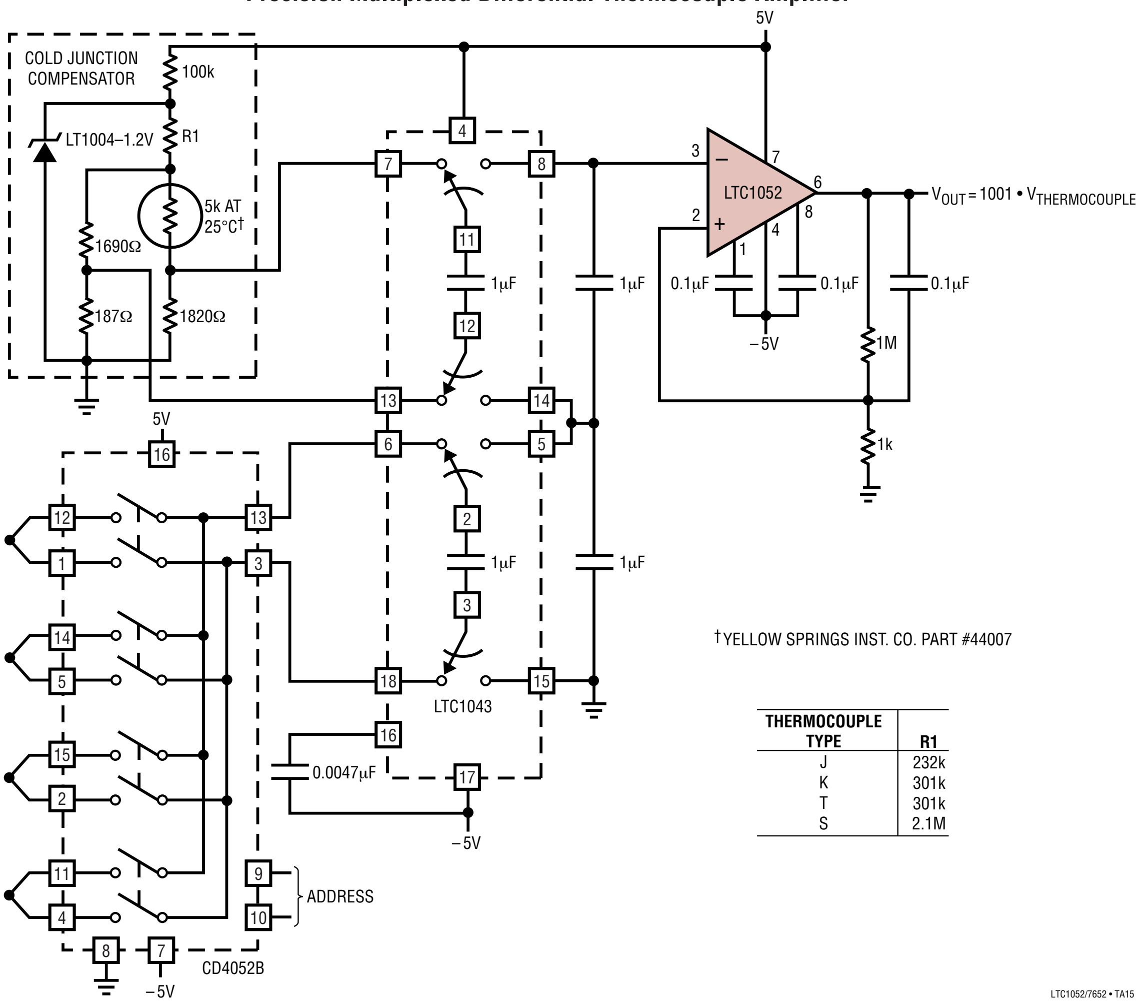
LTC1052/7652 • TA13

DC Stabilized FET Probe



LTC1052/7652 • TA14

Precision Multiplexed Differential Thermocouple Amplifier



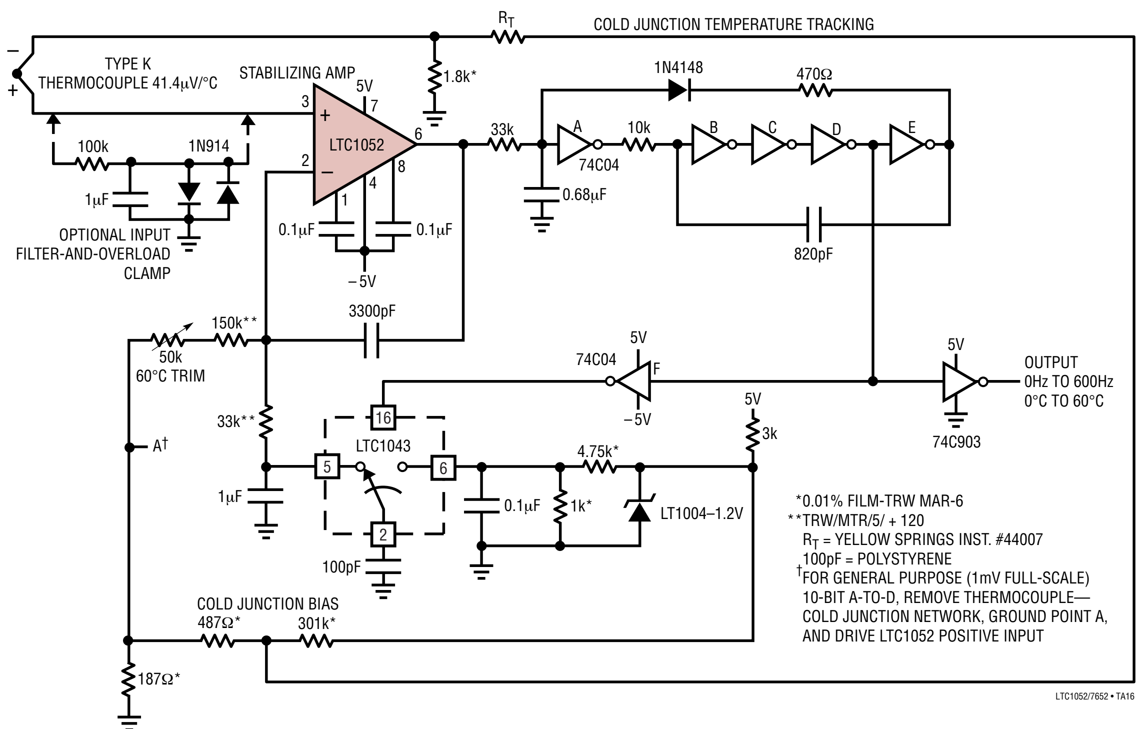
†YELLOW SPRINGS INST. CO. PART #44007

THERMOCOUPLE TYPE	R1
J	232k
K	301k
T	301k
S	2.1M

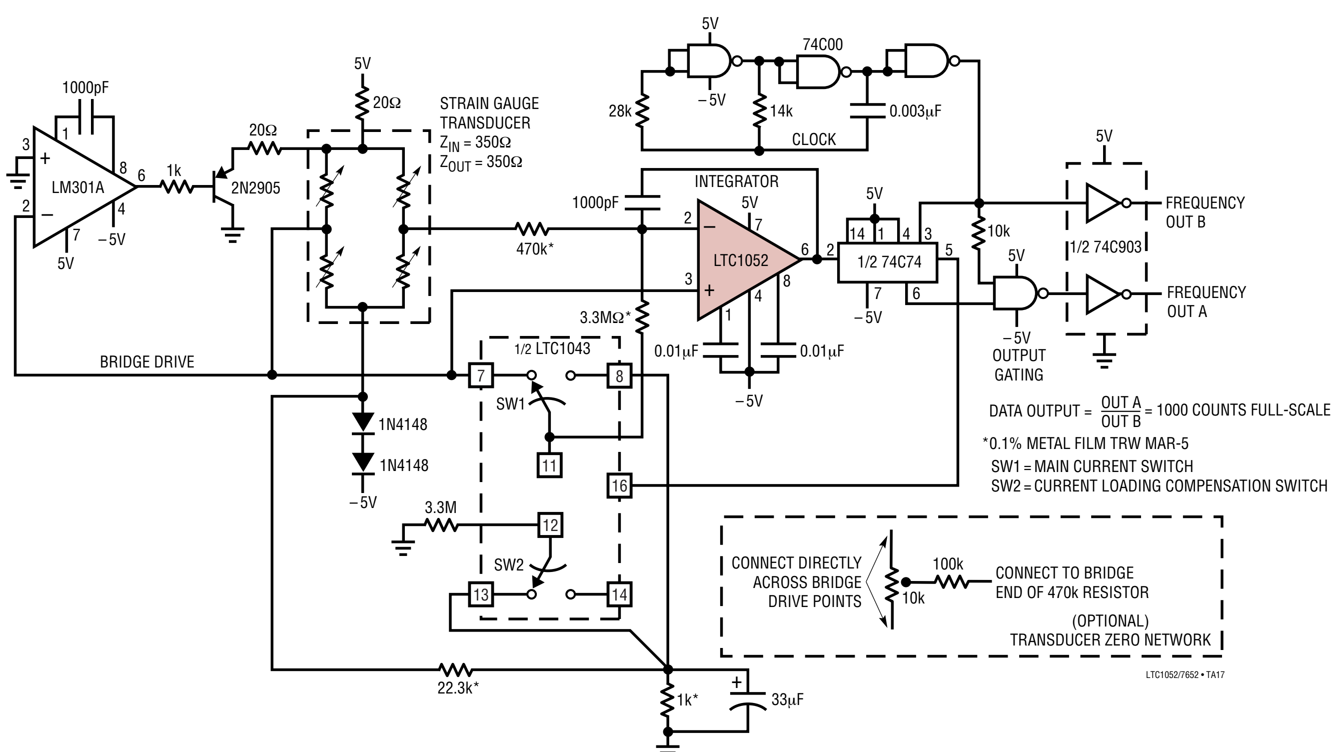
LTC1052/7652 • TA15

TYPICAL APPLICATIONS

Direct Thermocouple-to-Frequency Converter

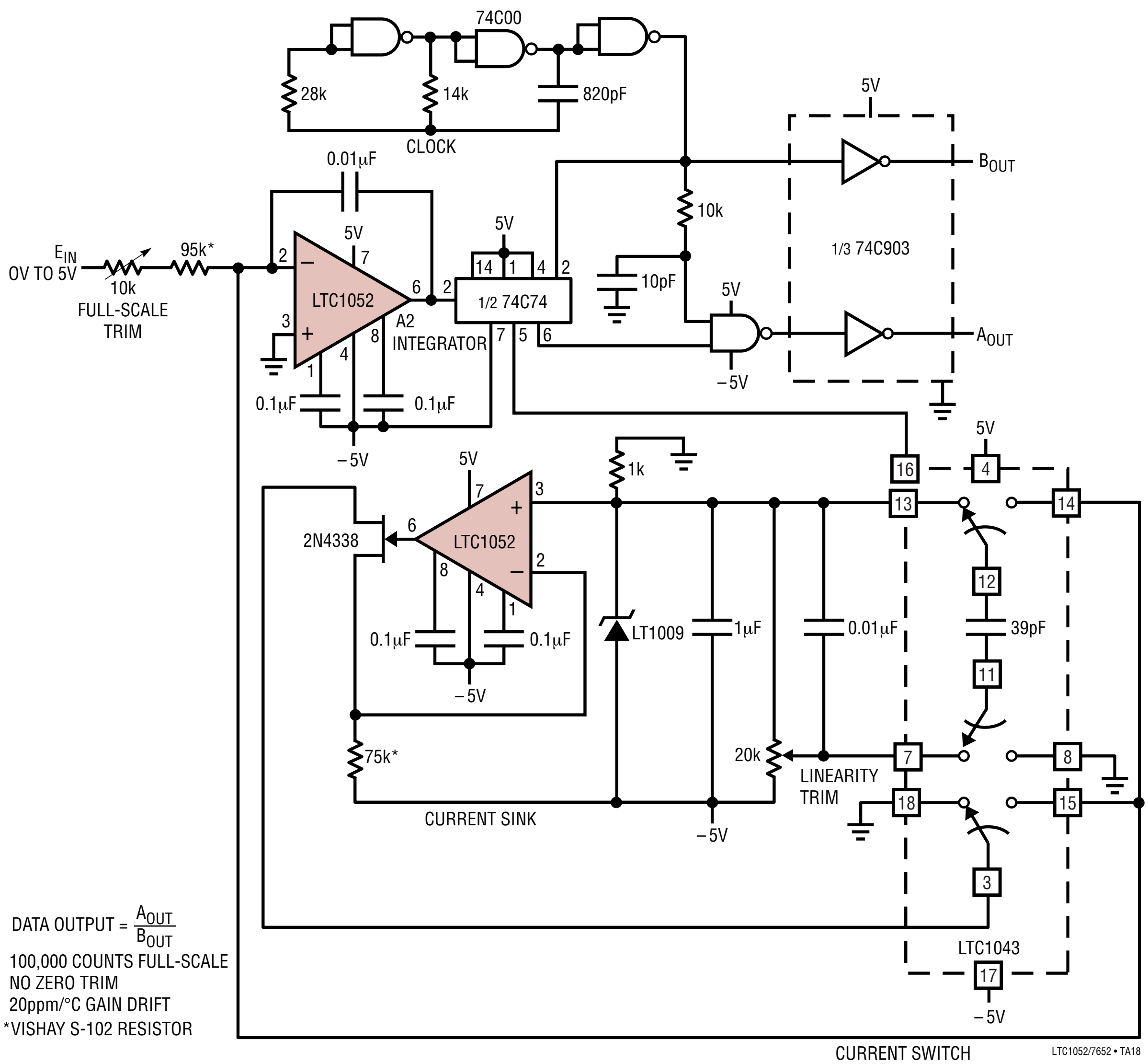


Direct 10-Bit Strain Gauge Digitizer



TYPICAL APPLICATIONS

16-Bit A/D Converter

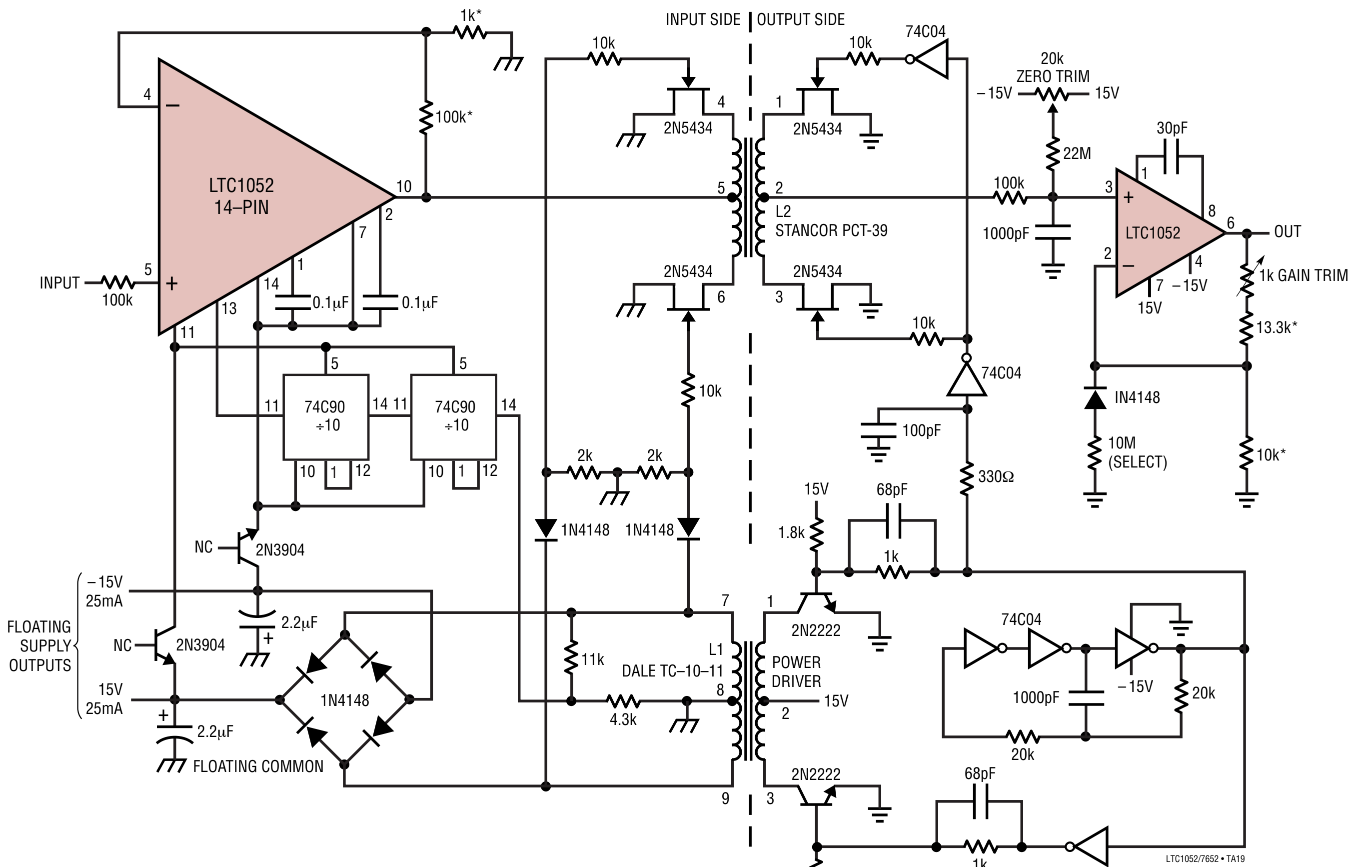


DATA OUTPUT = $\frac{A_{OUT}}{B_{OUT}}$

100,000 COUNTS FULL-SCALE
NO ZERO TRIM
20ppm/°C GAIN DRIFT
*VISHAY S-102 RESISTOR

TYPICAL APPLICATIONS

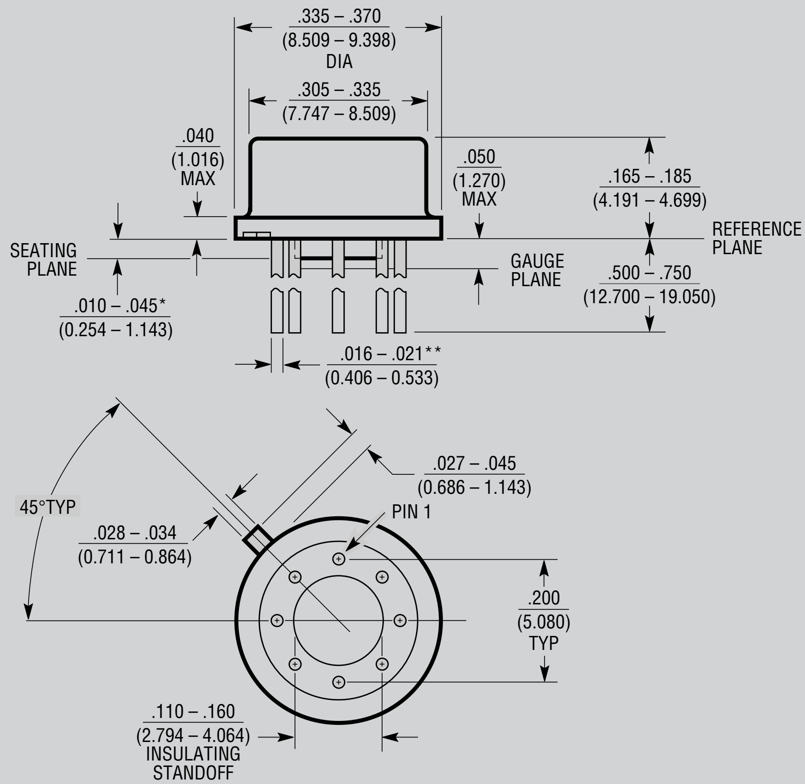
Precision Isolation Amplifier



250V ISOLATION
0.03% ACCURACY
*1% FILM RESISTOR

PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.200 Inch PCD)
(Reference LTC DWG # 05-08-1320)



*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

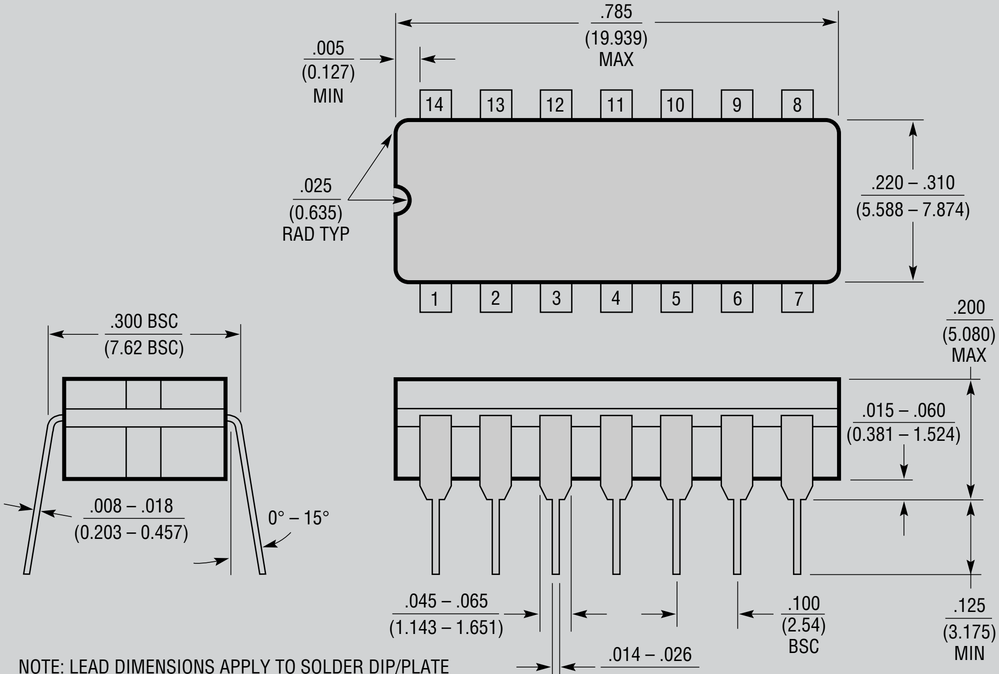
**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS .016 – .024 (0.406 – 0.610)

H8(TO-5) 0.200 PCD 0801

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

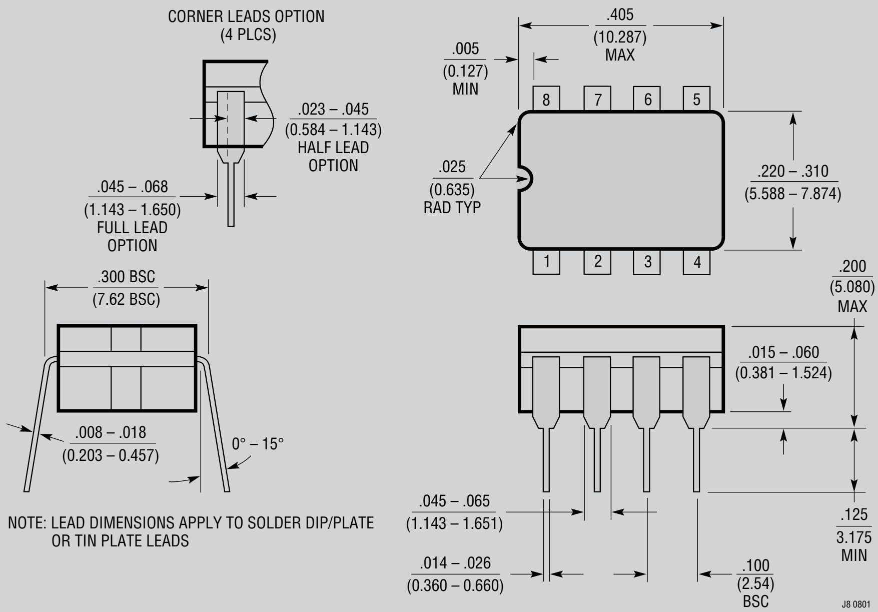


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE
OR TIN PLATE LEADS

OBSOLETE PACKAGE

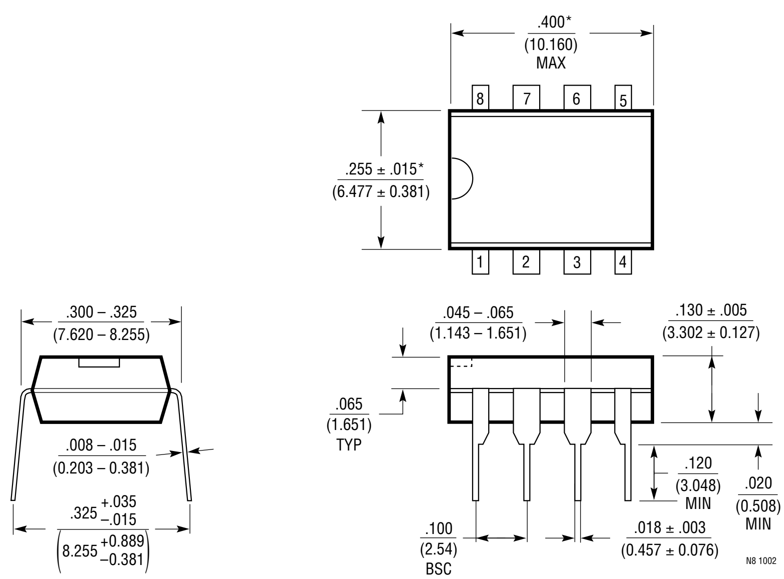
PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

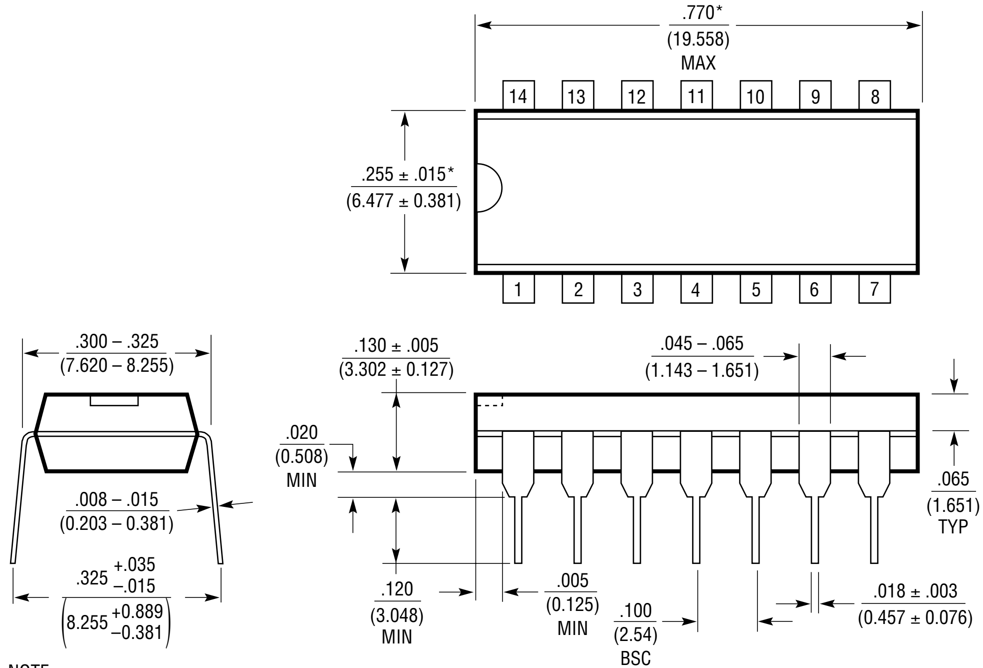
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

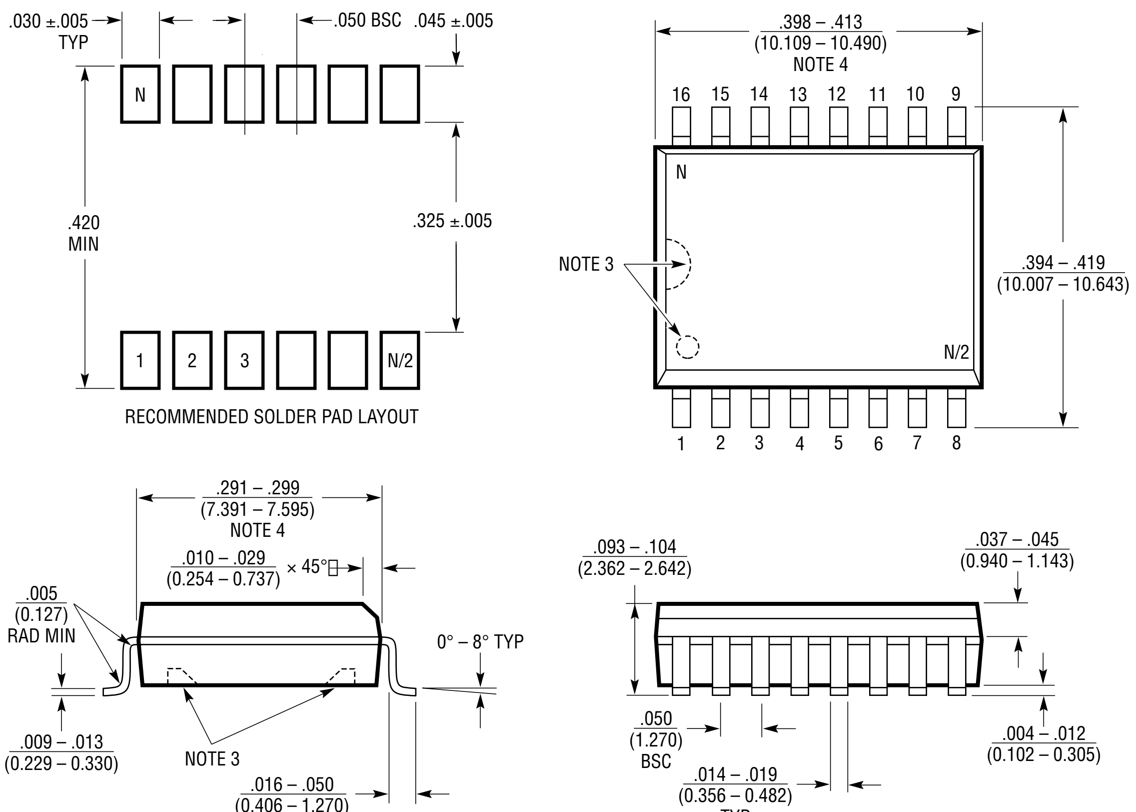
N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S16 (WIDE) 0502

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