74HC173; 74HCT173

Quad D-type flip-flop; positive-edge trigger; 3-state

Rev. 3 — 8 November 2016 Product data sheet

1. General description

The 74HC173; 74HCT173 is a quad positive-edge triggered D-type flip-flop. The device features clock (CP), master reset (MR), two input enable ($\overline{E}1$, $\overline{E}2$) and two output enable ($\overline{OE}1$, $\overline{OE}2$) inputs. When the input enables are LOW, the outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on either input enable will cause the device to go into a hold mode, outputs hold their previous state independently of clock and data inputs. A HIGH on MR forces the outputs LOW independently of clock and data inputs. A HIGH on either output enable pin causes the outputs to assume a high-impedance OFF-state. Operation of the output enable inputs does not affect the state of the flip-flops. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC173: CMOS level
  - For 74HCT173: TTL level
- Gated input enable for hold (do nothing) mode
- Gated output enable control mode
- Edge-triggered D-type register
- Asynchronous master reset
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC173D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT173D				
74HC173DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT173DB				
74HC173PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

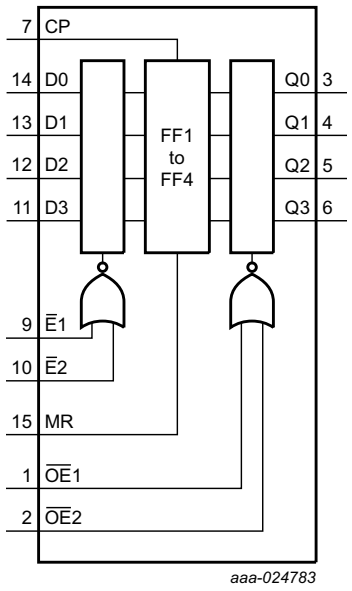


Fig 1. Functional diagram

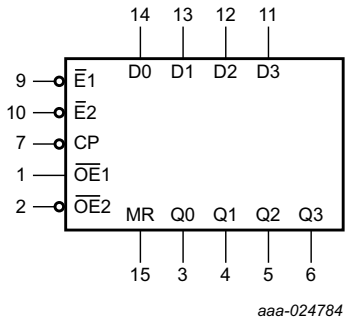


Fig 2. Logic symbol

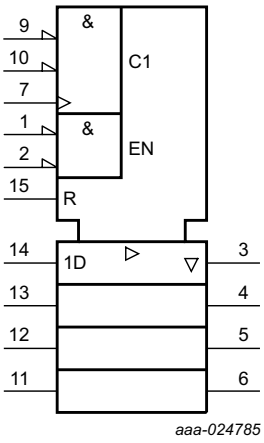


Fig 3. IEC logic symbol

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

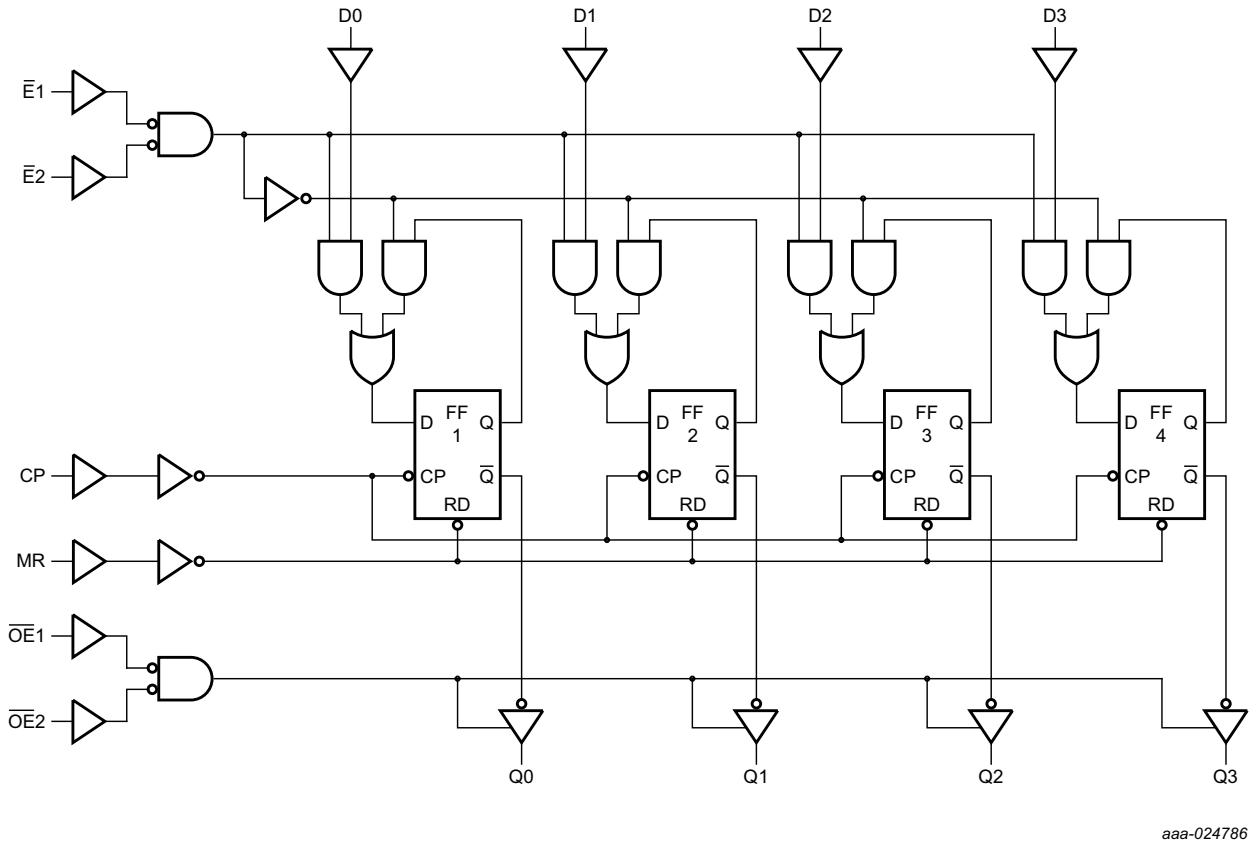


Fig 4. Logic diagram

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

5. Pinning information

5.1 Pinning

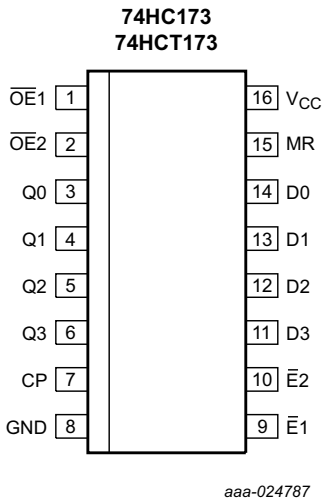


Fig 5. Pin configuration SO16

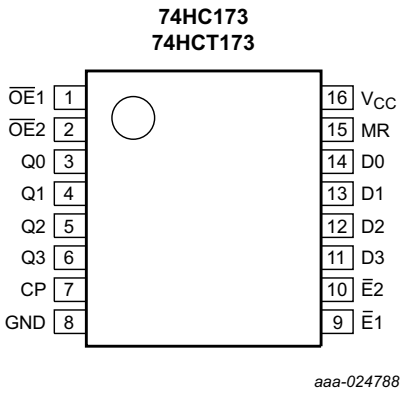


Fig 6. Pin configuration SSOP16 and TSSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1$, $\overline{OE}2$	1, 2	output enable input (active LOW)
Q0, Q1, Q2, Q3	3, 4, 5, 6	3-state flip-flop output
CP	7	clock input (LOW-to-HIGH, edge triggered)
GND	8	ground (0 V)
$\overline{E}1$, $\overline{E}2$	9, 10	data enable input (active LOW)
D0, D1, D2, D3	14, 13, 12, 11	data input
MR	15	asynchronous master reset (active HIGH)
V_{CC}	16	supply voltage

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

6. Functional description

Table 3. Function table[1]

Register operating mode	Inputs					Outputs
	MR	CP	$\overline{E1}$	$\overline{E2}$	Dn	Qn (register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (do nothing)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

Table 4. Function table[1]

3-state buffer operating mode	Inputs			Outputs			
	Qn (register)	$\overline{OE1}$	$\overline{OE2}$	Q0	Q1	Q2	Q3
Read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
Disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q_n = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition;
X = don't care;
Z = high impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±35	mA
I_{CC}	supply current		-	+70	mA
I_{GND}	ground current		−70	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	SO16 and (T)SSOP16 package [1]	-	500	mW

[1] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC173			74HCT173			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC173										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 6.0 V; V_O = V_{CC} or GND	-	-	±0.5	-	±5.0	-	±10	μA

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

Table 7. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT173										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = -20$ μA	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -6.0$ mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = 20$ μA	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0$ mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V; $I_O = 0$ A	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		$\overline{OE}1$, $\overline{OE}2$	-	50	180	-	225	-	245	μA
		MR	-	60	216	-	270	-	294	μA
		$\overline{E}1$, $\overline{E}2$	-	40	144	-	180	-	196	μA
		Dn	-	25	90	-	112.5	-	122.5	μA
		CP	-	100	360	-	450	-	490	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC173										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	16	30	-	37	-	45	ns
t_{PHL}	High to LOW propagation delay	MR to Qn; see Figure 8								
		V_{CC} = 2.0 V	-	44	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	16	30	-	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	13	26	-	33	-	38	ns
t_{en}	enable time	$\overline{OE}$n to Qn; see Figure 9 [2]								
		V_{CC} = 2.0 V	-	52	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	19	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	15	26	-	33	-	38	ns
t_{dis}	disable time	$\overline{OE}$n to Qn; see Figure 9 [3]								
		V_{CC} = 2.0 V	-	52	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	19	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	15	26	-	33	-	38	ns
t_t	transition time	see Figure 7 [4]								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t_W	pulse width	CP HIGH or LOW; see Figure 7								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR HIGH; see Figure 8								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t_{rec}	recovery time	MR to CP; see Figure 8								
		V_{CC} = 2.0 V	60	–8	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	–3	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	–2	-	13	-	15	-	ns

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	$\overline{En}$ to CP; see Figure 10								
		V_{CC} = 2.0 V	100	33	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	12	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	10	-	21	-	26	-	ns
		Dn to CP; see Figure 10								
		V_{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	5	-	13	-	15	-	ns
t_h	hold time	$\overline{En}$ to CP; see Figure 10								
		V_{CC} = 2.0 V	0	–17	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	–6	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	–5	-	0	-	0	-	ns
		Dn to CP; see Figure 10								
		V_{CC} = 2.0 V	1	–11	-	1	-	1	-	ns
		V_{CC} = 4.5 V	1	–4	-	1	-	1	-	ns
		V_{CC} = 6.0 V	1	–3	-	1	-	1	-	ns
f_{max}	maximum frequency	CP; see Figure 7								
		V_{CC} = 2.0 V	6	26	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V	30	80	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	88	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	95	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [5]	-	20	-	-	-	-	-	pF
74HCT173										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		V_{CC} = 4.5 V	-	20	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
t_{PHL}	High to LOW propagation delay	MR to Qn; see Figure 8								
		V_{CC} = 4.5 V	-	20	37	-	46	-	56	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
t_{en}	enable time	$\overline{OE}n$ to Qn; V_{CC} = 4.5 V; see Figure 9 [2]	-	20	35	-	44	-	53	ns
t_{dis}	disable time	$\overline{OE}n$ to Qn; V_{CC} = 4.5 V; see Figure 9 [3]	-	19	30	-	38	-	45	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 7 [4]	-	5	12	-	15	-	19	ns
t_W	pulse width	CP HIGH or LOW; V_{CC} = 4.5 V; see Figure 7	16	7	-	20	-	24	-	ns
		MR HIGH; V_{CC} = 4.5 V; see Figure 8	15	6	-	19	-	22	-	ns

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{rec}	recovery time	MR to CP; V_{CC} = 4.5 V; see Figure 8	12	–2	-	15	-	18	-	ns
t_{su}	set-up time	$\overline{En}$ to CP; V_{CC} = 4.5 V; see Figure 10	22	13	-	28	-	33	-	ns
		Dn to CP; V_{CC} = 4.5 V; see Figure 10	12	7	-	15	-	18	-	ns
t_h	hold time	$\overline{En}$ to CP; V_{CC} = 4.5 V; see Figure 10	0	–6	-	0	-	0	-	ns
		Dn to CP; V_{CC} = 4.5 V; see Figure 10	0	–3	-	0	-	0	-	ns
f_{max}	maximum frequency	CP; see Figure 7								
		V_{CC} = 4.5 V	30	80	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	88	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V; V_{CC} = 5 V; f_i = 1 MHz [5]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_{en} is the same as t_{PZH} and t_{PZL}.

[3] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

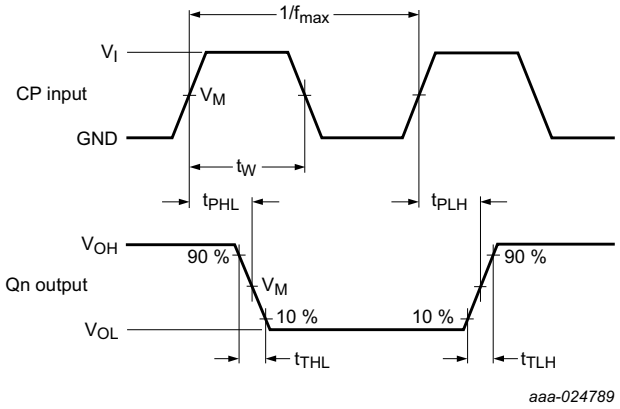
[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

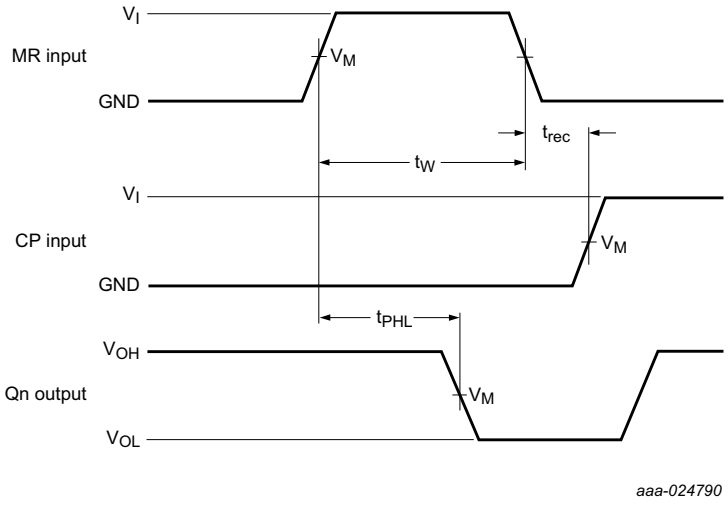
11. Waveforms



Measurement points are given in Table 9.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock (CP) to outputs (Qn) propagation delays, clock pulse width, output transition times and maximum frequency



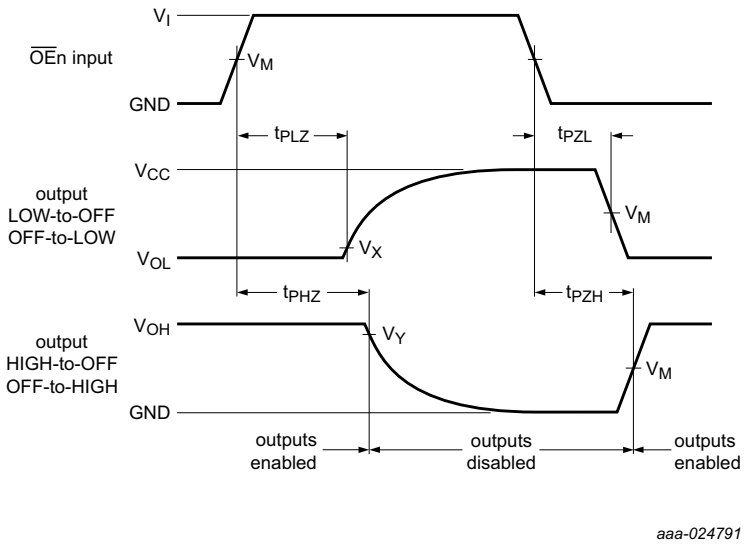
Measurement points are given in Table 9.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The master reset (MR) pulse width, master reset to output (Qn) propagation delays, and the master reset to clock (CP) recovery times

All information provided in this document is subject to legal disclaimers.

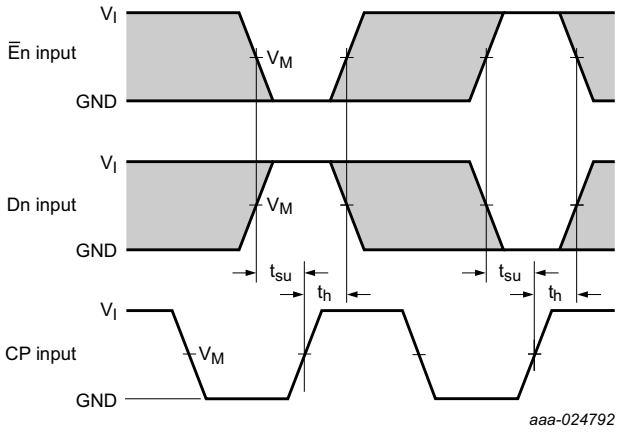
© Nexperia B.V. 2017. All rights reserved



Measurement points are given in Table 9.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. 3-state enable and disable times



The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 9.

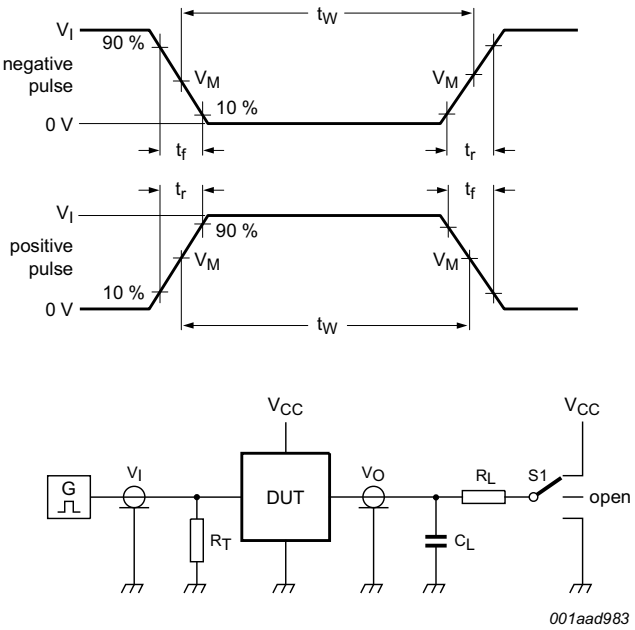
Fig 10. The data set-up and hold times from input ($\overline{E}$n, Dn) to clock (CP)

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC173	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
74HCT173	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved



Test data is given in Table 10.

Test circuit definitions:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance.

S1 = Test selection switch

Fig 11. Test circuit for measuring switching times

Table 10. Test data

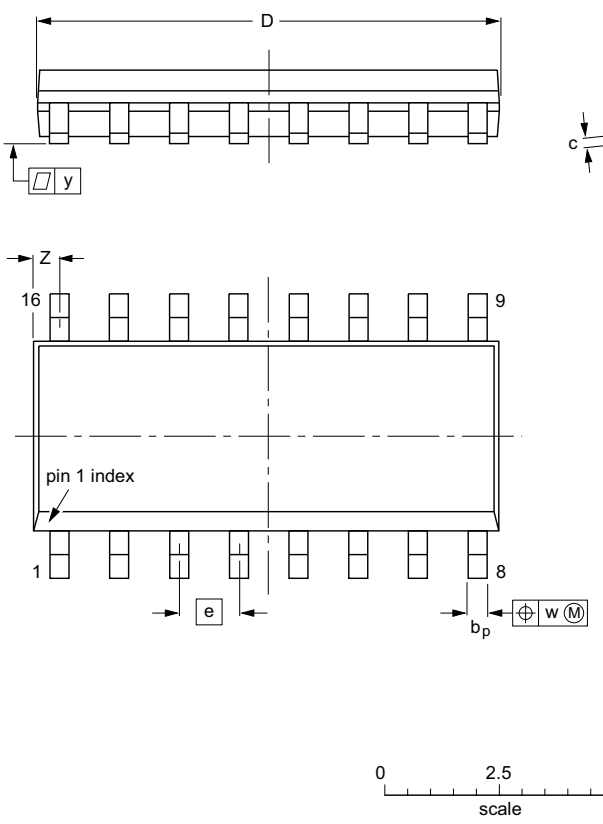
Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC173	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT173	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

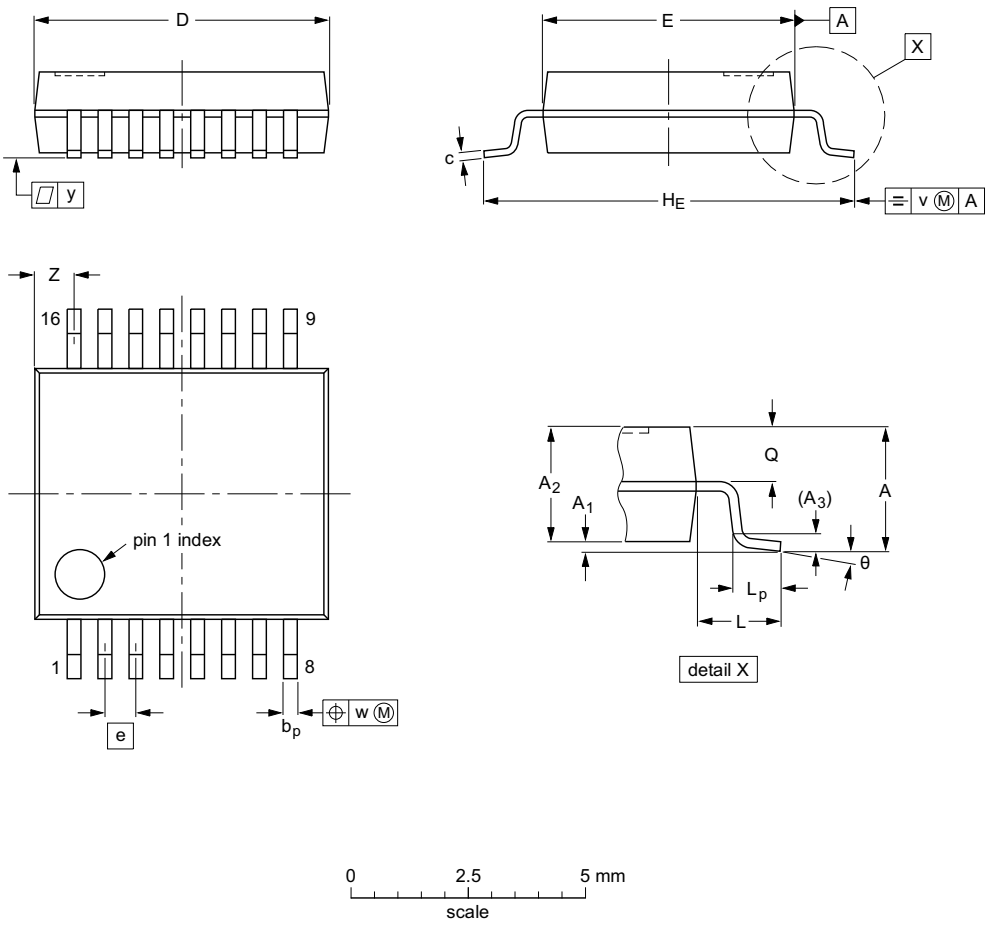
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT109-1 (SO16)

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

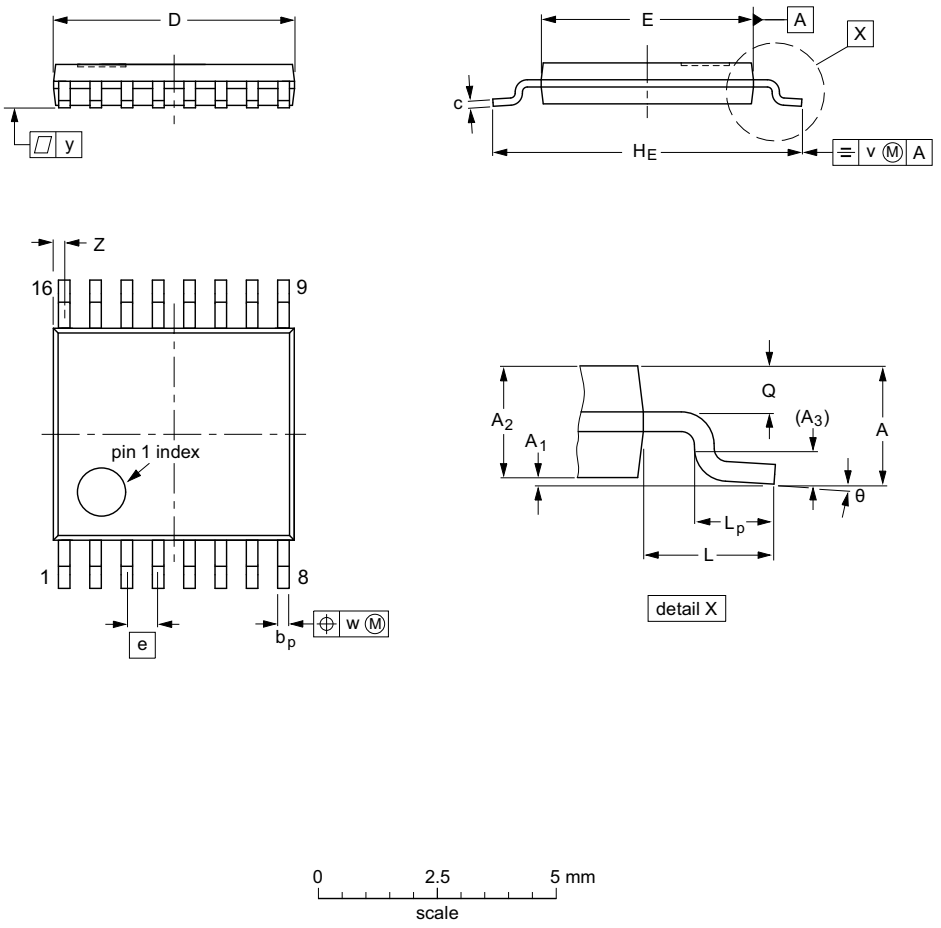
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT338-1 (SSOP16)

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT403-1 (TSSOP16)

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT173 v.3	20161108	Product data sheet	-	74HC_HCT173 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HCT173N and 74HC173N removed.			
74HC_HCT173 v.2	19901201	Product specification	-	-

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2017. All rights reserved

17. Contents

1 General description 1
2 Features and benefits 1
3 Ordering information 2
4 Functional diagram 2
5 Pinning information 4
5.1 Pinning 4
5.2 Pin description 4
6 Functional description 5
7 Limiting values 5
8 Recommended operating conditions 6
9 Static characteristics 6
10 Dynamic characteristics 8
11 Waveforms 11
12 Package outline 14
13 Abbreviations 17
14 Revision history 17
15 Legal information 18
15.1 Data sheet status 18
15.2 Definitions 18
15.3 Disclaimers 18
15.4 Trademarks 19
16 Contact information 19
17 Contents 20

© **Nexperia B.V. 2017. All rights reserved**

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 08 November 2016

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Flip-Flops ***category:***

Click to view products by NXP ***manufacturer:***

Other Similar products are found below :

NLV74HC74ADTR2G NLV74HC11ADR2G NTE74LS76A 74LCX16374MTDX MM74HC74AMX 74LVX74MTCX SN74HC273DWR SN74LVC74ADR SN74HC574PWR SN74HC273NSR 74AHC74D.112 74AUP1G74DC.125 74HC112D.652 74HC574D.652 74HCT173D.652 74HCT174D.652 74HCT374D.652 74AHC574D.118 74HC174D.652 74HC273D.652 74HC374D.652 74HC74D.653 74HC74PW.112 74HC107D.652 74HC574D.653 HEF4013BT.653 HEF4027BT.652 74HC107PW.112 74HC73PW.112 74HCT74PW.112 74LV74PW.112 74HC173PW.112 74HC174PW.112 74HC175PW.112 74HC377DB.118 74HC574PW.112 74HC73D.652 74HCT175D.652 74LVC1G74DP.125 74LVC74APW.112 74VHC174FT(BJ) 74VHC273FT(BJ) 74VHCT574AFT(BJ) 74HCT273DB.118 74HC107DB.112 74HC112PW.112 74HCT74DB.112 74LVC1G80GV.125 74LVC1G175GV.125 74LVC1G79GV.125