74HC21

Dual 4-input AND gate Rev. 7 — 30 November 2015

Product data sheet

1. **General description**

The 74HC21 is a dual 4-input AND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features and benefits 2.

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C.

Ordering information 3.

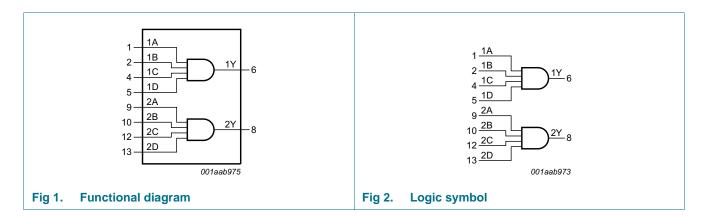
Table 1. **Ordering information**

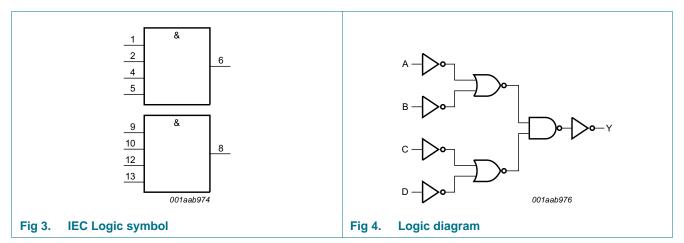
Type number	Package									
	Temperature range	Name	Description	Version						
74HC21D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1						
74HC21DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1						
74HC21PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1						



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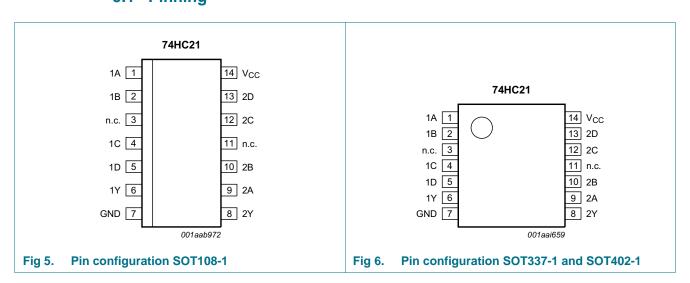
4. Functional diagram





5. Pinning information

5.1 Pinning



74HC2

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 1B, 1C, 1D	1, 2, 4, 5	data input
n.c.	3, 11	not connected
1Y	6	data output
GND	7	ground (0 V)
2Y	8	data output
2A, 2B, 2C, 2D	9, 10, 12, 13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input	nput								
nA	nB	nC	nD	nY					
L	X	Х	Х	L					
Χ	L	Х	Х	L					
Χ	X	L	Х	L					
X	X	X	L	L					
Н	Н	Н	Н	Н					

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±25	mA
I _{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			–65	+150	°C
P _{tot}	total power dissipation	SO14 and (T)SSOP14 packages	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C. For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall	V _{CC} = 2.0 V	-	-	625	ns/V
	rate	V _{CC} = 4.5 V	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	ns/V
T _{amb}	ambient temperature		-40	-	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
lı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μА
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
t _{pd} propagation delay	propagation delay	nA, nB, nC or nD to nY; [1] see Figure 7								
		V _{CC} = 2.0 V	-	33	110	-	140	-	165	ns
		V _{CC} = 4.5 V	-	12	22	-	28	-	33	ns
		V _{CC} = 6.0 V	-	10	19	-	24	-	28	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	10	-	-	-	-	-	ns
t _t	transition time	nY output; see Figure 7 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}$ [3]	-	15	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum \left(C_L \times V_{CC}^2 \times f_o \right)$ where:

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

C_L = output load capacitance in pF;

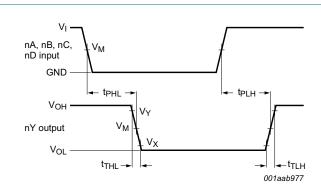
 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

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11. Waveforms



Measurement points are given in Table 8.

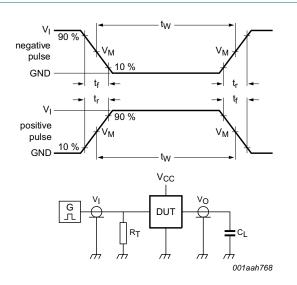
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times

Table 8. Measurement points

Туре	Input	Output					
	V_{M}	V _M	V_X	V_{Y}			
74HC21	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}			

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Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74HC21	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

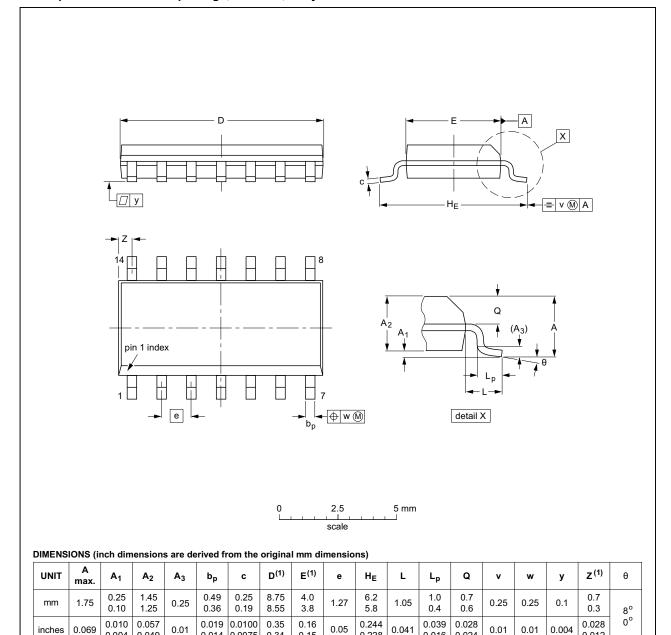
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12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014 0.0075

0.34

0.15

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA	PROJECTION		ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

0.228

0.016

0.024

Fig 9. Package outline SOT108-1 (SO14)

0.004

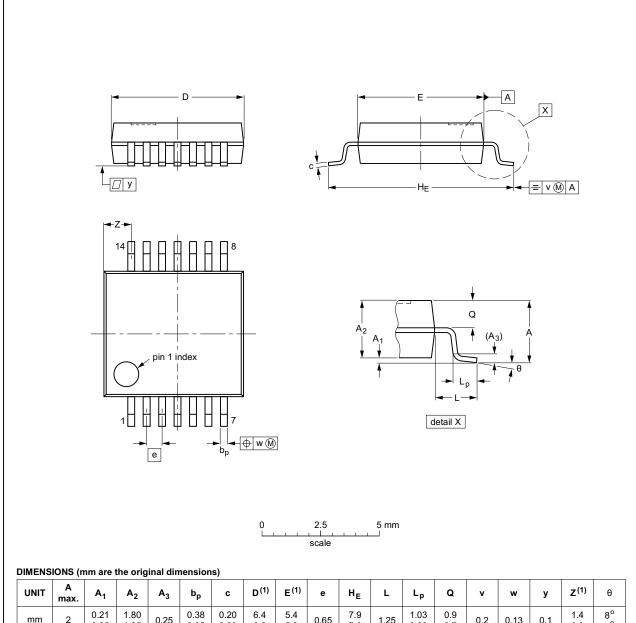
0.049

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	C	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

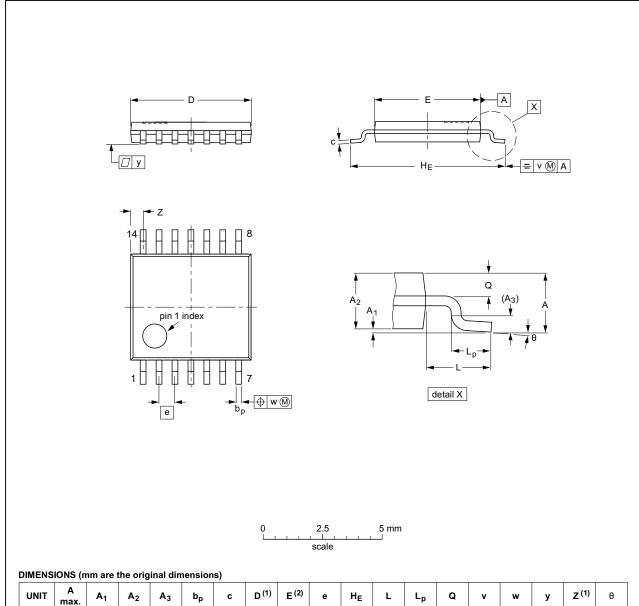
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT337-1		MO-150				99-12-27 03-02-19

Fig 10. Package outline SOT337-1 (SSOP14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNI	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	
501402-1		MO-153				0	

Fig 11. Package outline SOT402-1 (TSSOP14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description			
CMOS	Complementary Metal Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
НВМ	Human Body Model			
MM	Machine Model			
TTL	Transistor-Transistor Logic			

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
74HC21 v.7	20151130	Product data sheet	-	74HC21 v.6			
Modifications:	Type number	ers 74HC21N (SOT27-1) rei	moved.				
74HC21 v.6	20130208	Product data sheet	-	74HC21 v.5			
Modifications:	Section 2: Typo	corrected in the specified te	mperature range.				
74HC21 v.5	20090507	Product data sheet	-	74HC21 v.4			
Modifications:	Table 1: Type number 74HCT21PW changed to 74HC21PW.						
74HC21 v.4	20090407	Product data sheet	-	74HC21 v.3			
Modifications:		of this data sheet has been iniconductors.	redesigned to comply w	ith the new identity guidelines			
	 Legal texts 	have been adapted to the n	ew company name whe	ere appropriate.			
	 Added type 	number 74HC21PW (TSSC	P14 package).				
74HC21 v.3	20041112	Product data sheet	-	74HC_HCT21_CNV v.2			
74HC_HCT21_CNV v.2	19970828	Product specification	-	74HC_HCT21 v.1			
74HC_HCT21 v.1	19901201	Product specification	-	-			

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Document status[1][2]	Product status[3]	Definition				
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.				
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Product [short] data sheet	Production	This document contains the product specification.				

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