74LVC823A

9-bit D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

Rev. 4 — 8 April 2013 Product data sheet

1. General description

The 74LVC823A is a 9-bit D-type flip-flop with common clock (pin CP), clock enable (pin $\overline{CE}$), master reset (pin $\overline{MR}$) and 3-state outputs (pins Qn) for bus-oriented applications. The 9 flip-flops stores the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW to HIGH CP transition, provided pin $\overline{CE}$ is LOW. When pin $\overline{CE}$ is HIGH, the flip-flops hold their data. A LOW on pin $\overline{MR}$ resets all flip-flops. When pin $\overline{OE}$ is LOW, the contents of the 9 flip-flops are available at the outputs. When pin $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pinout architecture
- 9-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	**Name**	**Description**	**Version**
74LVC823AD	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC823ADB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC823APW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74LVC823ABQ	–40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

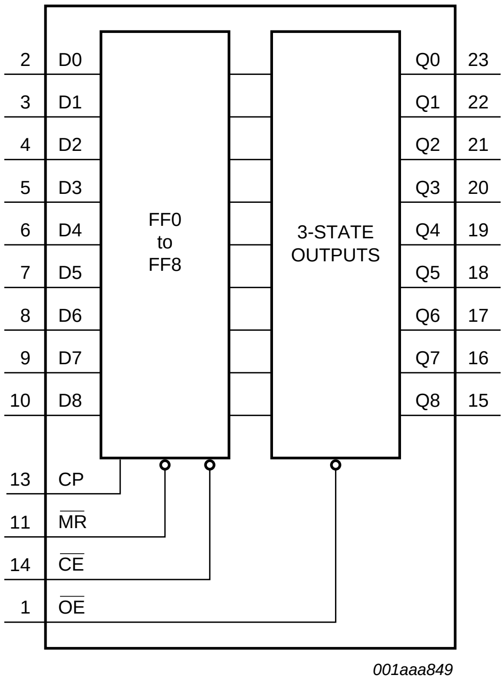

Fig 1. Functional diagram

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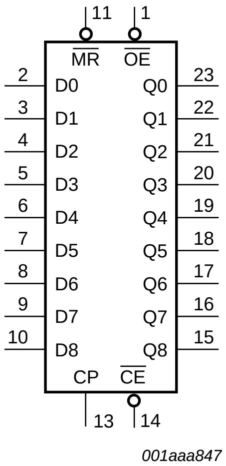

Fig 2. Logic symbol

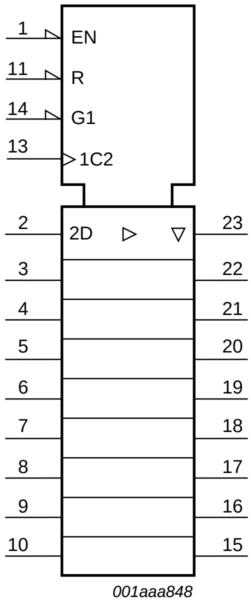

Fig 3. IEC logic symbol

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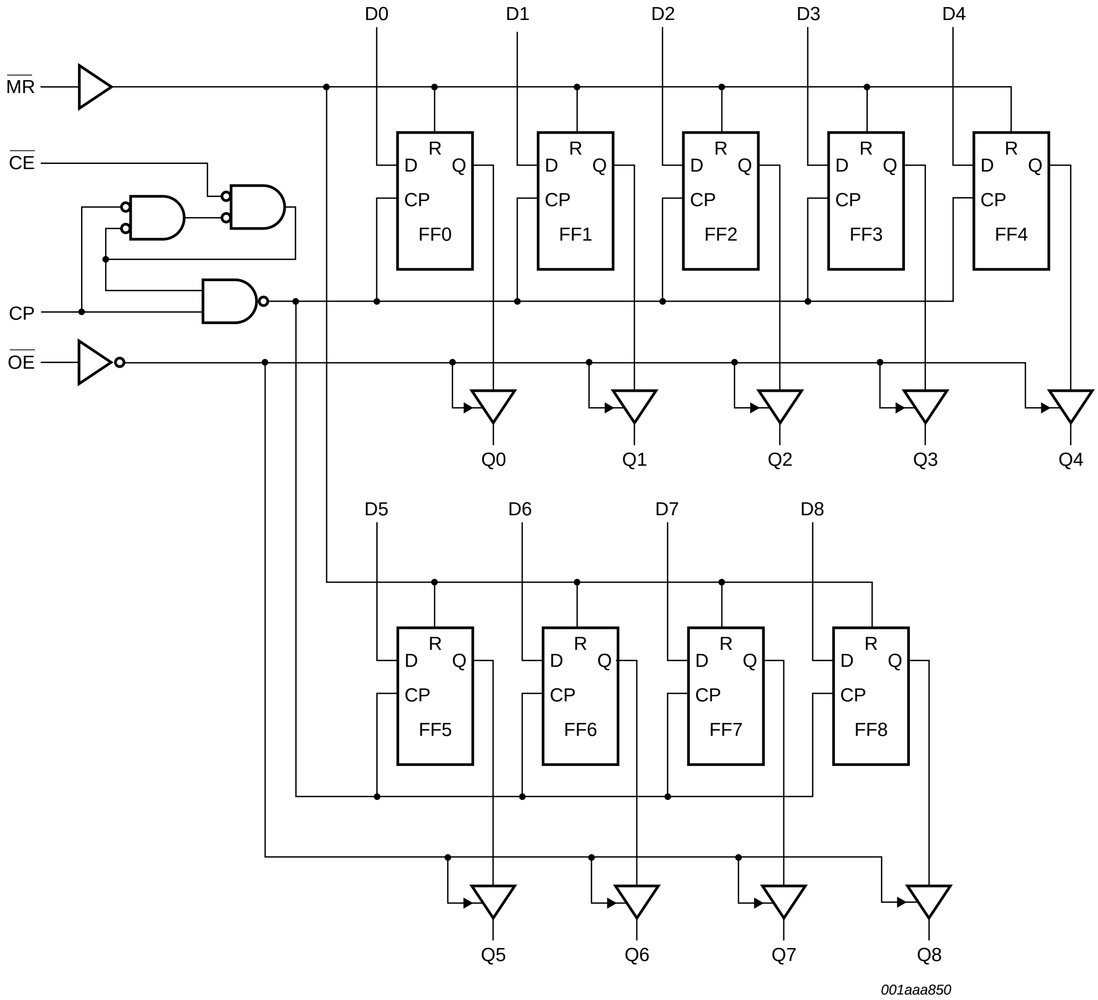

Fig 4. Logic diagram

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5. Pinning information

5.1 Pinning

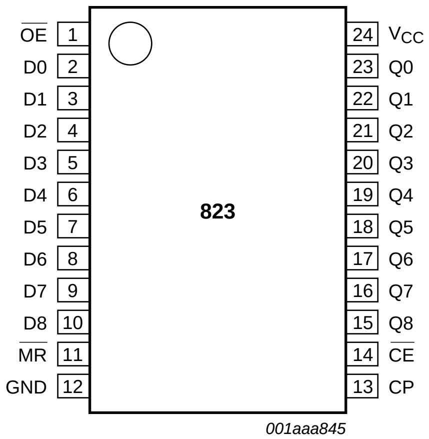
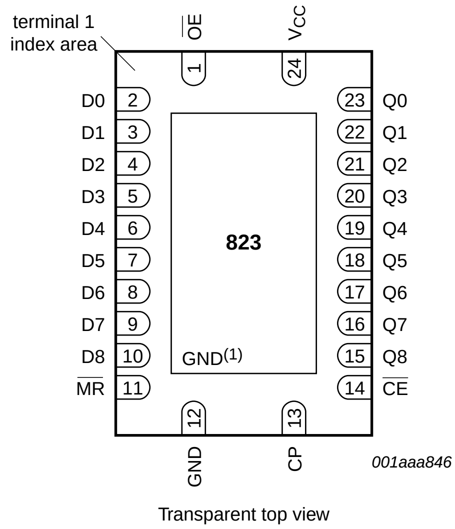


Fig 5. Pin configuration SO24 and (T)SSOP24



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 6. Pin configuration DHVQFN24

5.2 Pin description

Table 2. Pin description

Pin	Name	Description
$\overline{\mathrm{OE}}$	1	output enable input (active LOW)
$\overline{\mathrm{MR}}$	11	master reset input (active LOW)
D[0:8]	2, 3, 4, 5, 6, 7, 8, 9, 10	data input
Q[0:8]	23, 22, 21, 20, 19, 18, 17, 16, 15	3-state flip-flop output
CP	13	clock input (LOW to HIGH; edge-triggered)
$\overline{\mathrm{CE}}$	14	clock enable input (active LOW)
GND	12	ground (0 V)
V_{CC}	24	supply voltage

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6. Functional description

Table 3. Function table [1]

Operating mode	Input					Internal flip-flop	Output
	$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	Dn		Qn
Clear	L	L	X	X	X	L	L
Load and read register	L	H	L	$\uparrow$	l	L	L
	L	H	L	$\uparrow$	h	H	H
Load register and disable outputs	H	H	L	$\uparrow$	l	L	Z
	H	H	L	$\uparrow$	h	H	Z
Hold	L	H	H	NC	X	NC	NC

[1] H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition
Z = high-impedance OFF-state
$\uparrow$ = LOW to HIGH level transition
X = don't care
NC = no change

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	HIGH or LOW state	[2]	–0.5	V_{CC} + 0.5	V
		3-state	[2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO24 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP24 and TSSOP24 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN24 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	HIGH or LOW state	0	-	V_{CC}	V
		3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.2	-	-	V_{CC} – 0.3	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μA

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Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 3.6$ V; $V_O = 5.5$ V or GND;	-	0.1	±5	-	±20	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 5.5$ V	-	0.1	±10	-	±20	μA
I_{CC}	supply current	$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.7$ V to 3.6 V; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0$ V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3$ V (unless stated otherwise) and $T_{amb} = 25$ °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 11.

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Figure 7	[2]						
		$V_{CC} = 1.2$ V		-	20	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V		2.4	8.4	18.7	2.4	21.5	ns
		$V_{CC} = 2.3$ V to 2.7 V		1.7	4.4	9.6	1.7	11.1	ns
		$V_{CC} = 2.7$ V		1.5	4.1	8.9	1.5	11.5	ns
		$V_{CC} = 3.0$ V to 3.6 V		1.5	3.7	8.0	1.5	10.0	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Figure 9							
		$V_{CC} = 1.2$ V		-	15	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V		2.1	9.5	21.4	2.1	24.7	ns
		$V_{CC} = 2.3$ V to 2.7 V		1.5	4.9	10.5	1.5	12.1	ns
		$V_{CC} = 2.7$ V		1.5	4.7	8.8	1.5	11.0	ns
		$V_{CC} = 3.0$ V to 3.6 V		1.5	4.1	7.9	1.5	10.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 10	[2]						
		$V_{CC} = 1.2$ V		-	18	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V		1.7	7.4	16.5	1.7	19.0	ns
		$V_{CC} = 2.3$ V to 2.7 V		1.5	4.2	9.1	1.5	10.5	ns
		$V_{CC} = 2.7$ V		1.5	4.3	8.3	1.5	10.5	ns
		$V_{CC} = 3.0$ V to 3.6 V		1.5	3.4	7.2	1.5	9.0	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 11.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 10 [2]						
		V_{CC} = 1.2 V	-	8.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.3	4.2	10.0	2.3	11.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.3	5.6	1.0	6.5	ns
		V_{CC} = 2.7 V	1.5	3.2	7.1	1.5	9.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	2.9	6.0	1.5	7.5	ns
t_W	pulse width	clock HIGH or LOW; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V_{CC} = 2.7 V	3.3	-	-	3.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.3	1.7	-	3.3	-	ns
		master reset HIGH or LOW; see Figure 9						
		V_{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V_{CC} = 2.7 V	3.3	-	-	3.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.3	1.7	-	3.3	-	ns
t_{su}	set-up time	Dn to CP; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns
		V_{CC} = 2.7 V	1.0	-	-	1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	+1.8	–0.8	-	+1.8	-	ns
		$\overline{CE}$ to CP; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns
		V_{CC} = 2.7 V	1.8	-	-	1.8	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	0.0	-	1.3	-	ns
t_{rec}	recovery time	$\overline{MR}$; see Figure 9						
		V_{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V_{CC} = 2.7 V	2.0	-	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	+1.0	–0.5	-	+1.0	-	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 11.

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_h	hold time	Dn to CP; see Figure 8							
		V_{CC} = 1.65 V to 1.95 V		3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.5	-	-	2.5	-	ns
		V_{CC} = 2.7 V		2.0	-	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.0	0.8	-	2.0	-	ns
		$\overline{CE}$ to CP; see Figure 8							
		V_{CC} = 1.65 V to 1.95 V		3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.0	-	-	2.0	-	ns
		V_{CC} = 2.7 V		1.3	-	-	1.3	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	0.0	-	1.3	-	ns
f_{max}	maximum frequency	see Figure 7							
		V_{CC} = 1.65 V to 1.95 V		100	-	-	80	-	MHz
		V_{CC} = 2.3 V to 2.7 V		125	-	-	100	-	MHz
		V_{CC} = 2.7 V		150	-	-	120	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	200	-	120	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	12.4	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	14.5	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	16.4	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

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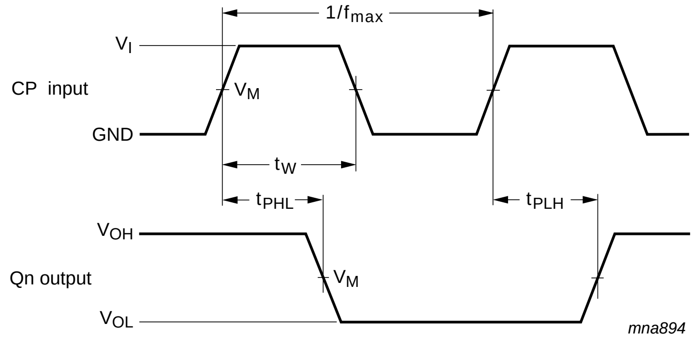
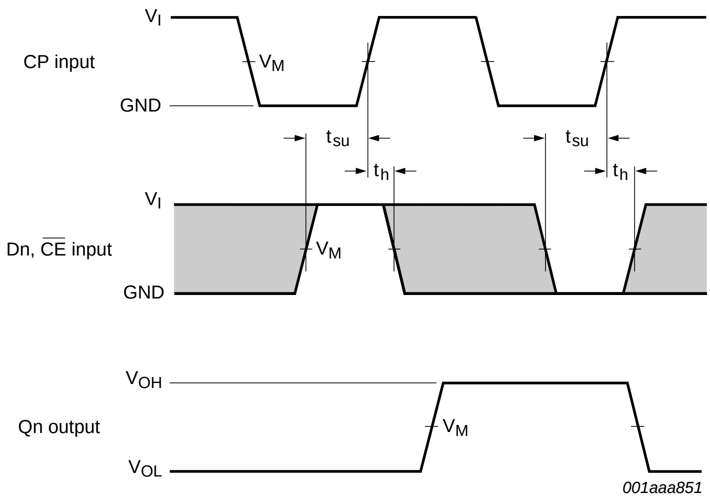
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 7. Clock to output propagation delays, clock pulse width, and maximum frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig 8. Data set-up and hold times for data and clock enable inputs to clock input

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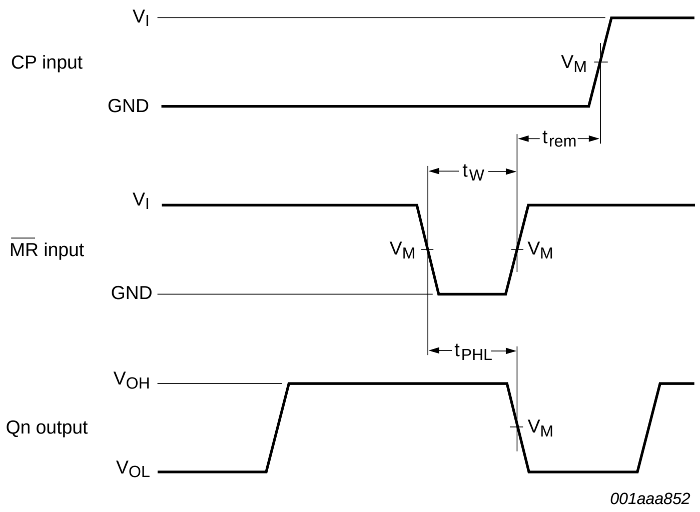
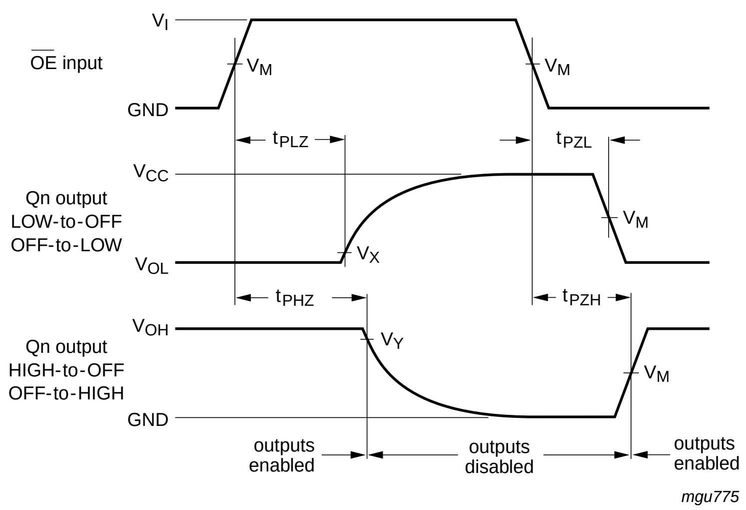


Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 9. Master reset pulse width, master reset to clock removal time and master reset to output propagation delay



Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.

Fig 10. 3-state outputs enable and disable times

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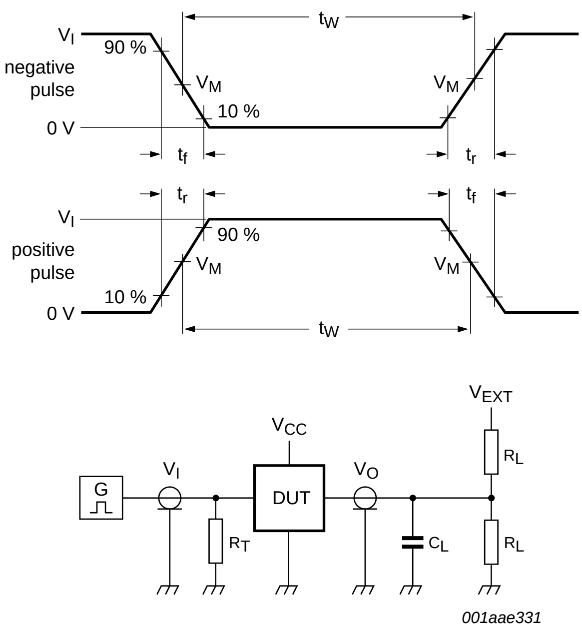
Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 11. Load circuitry for switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

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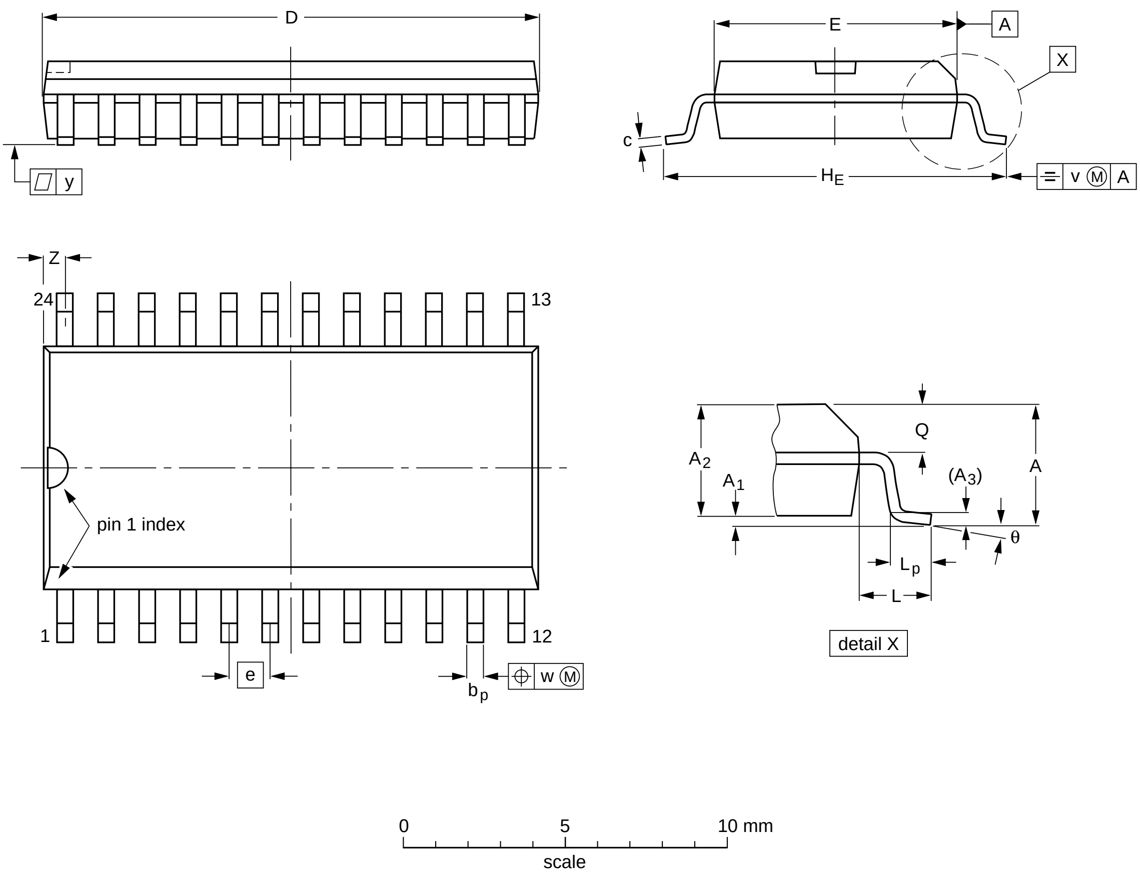
12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT137-1 (SO24)

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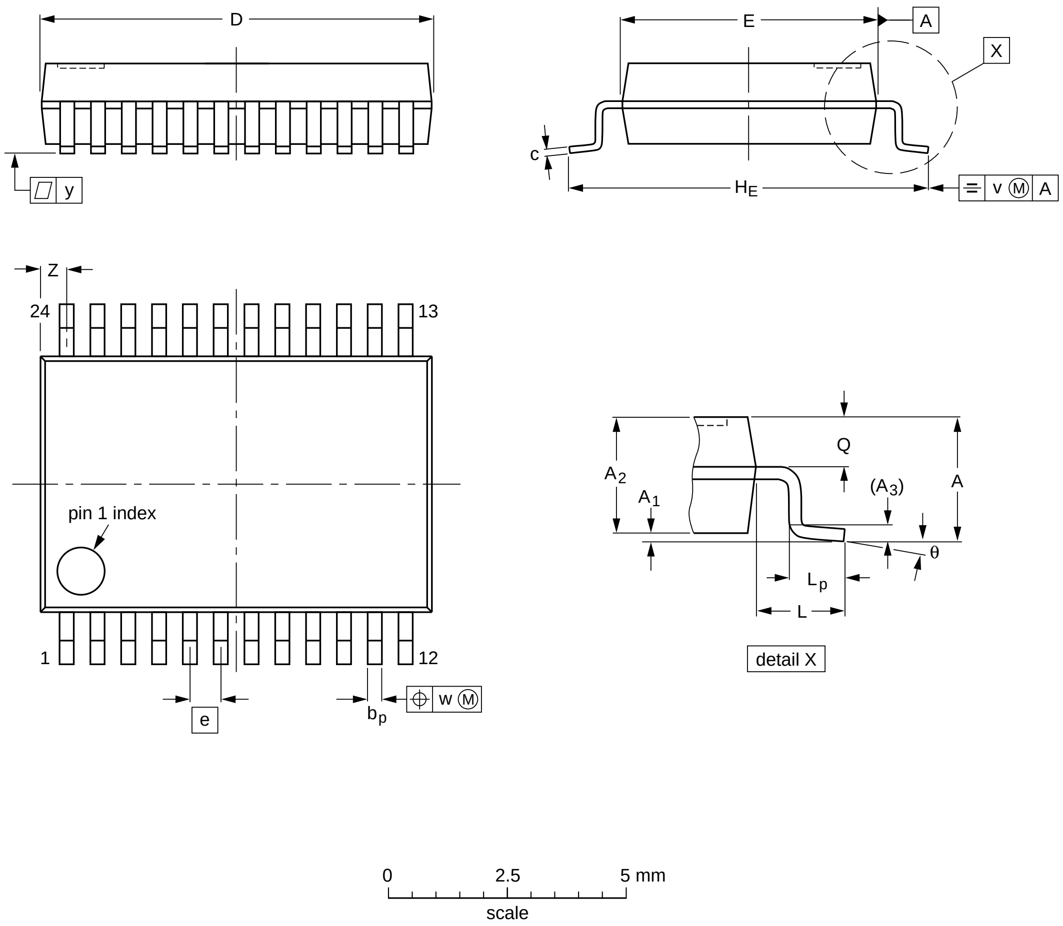
SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT340-1 (SSOP24)

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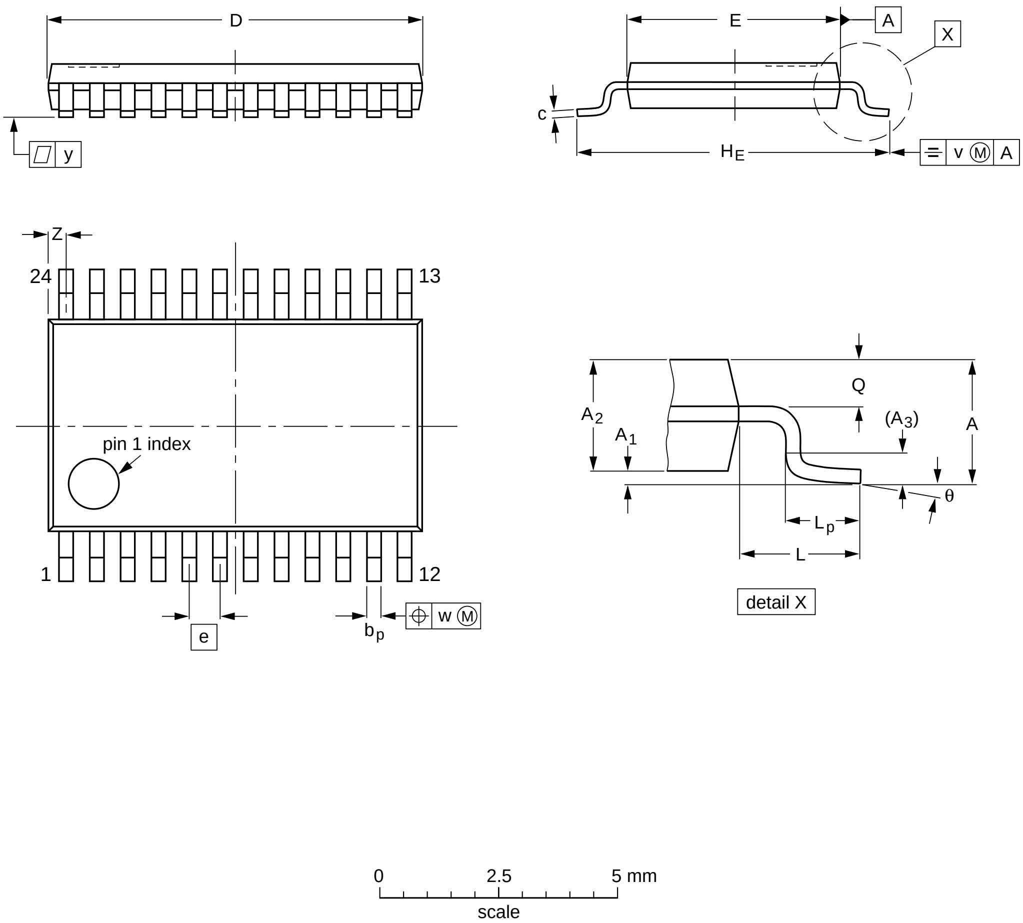
TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT355-1 (TSSOP24)

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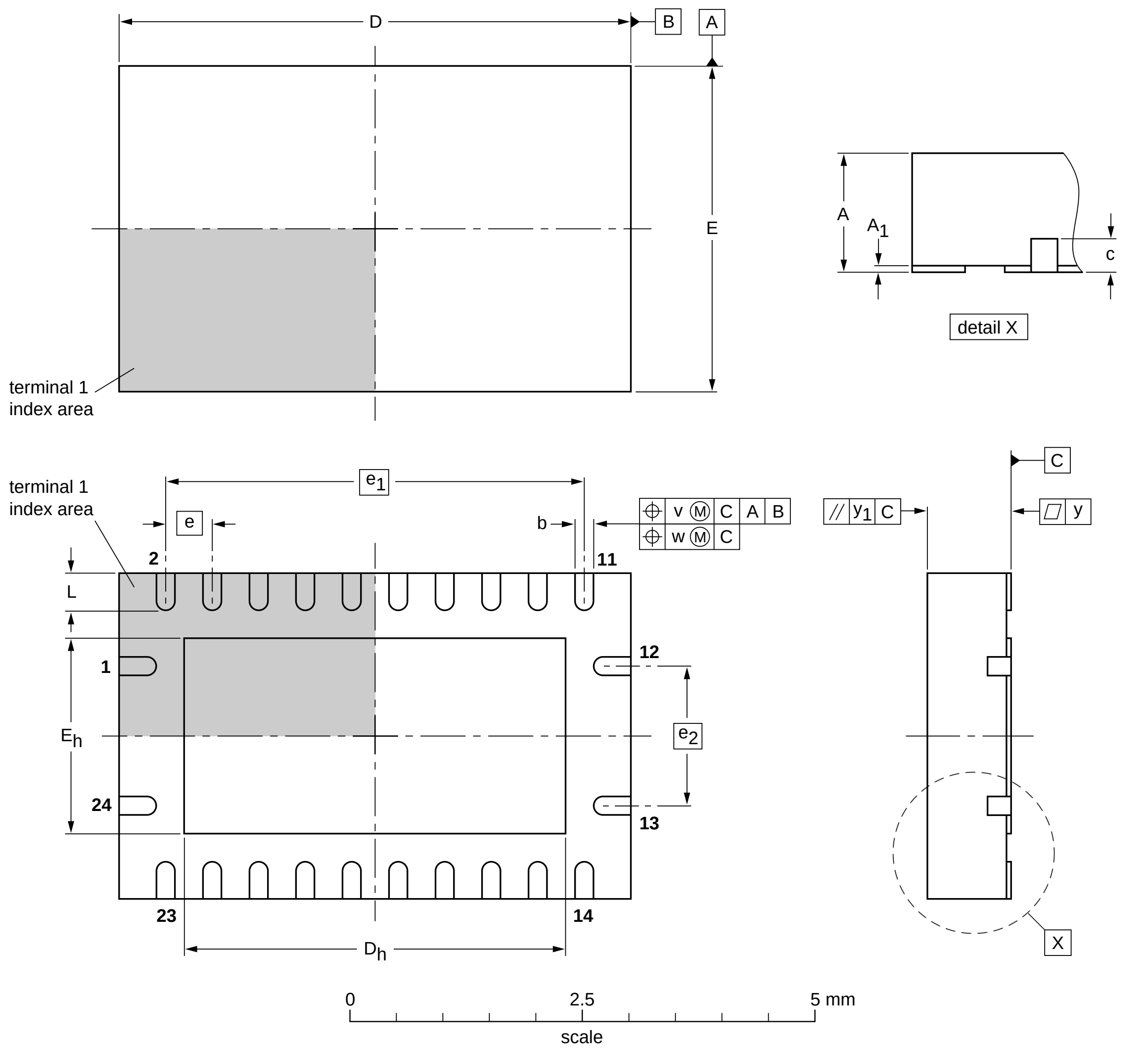
DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig 15. Package outline SOT815-1 (DHVQFN24)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC823A v.4	20130408	Product data sheet	-	74LVC823A v.3
Modifications:	• Features corrected (errata).			
74LVC823A v.3	20130327	Product data sheet	-	74LVC823A v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges.			
74LVC823A v.2	20040510	Product specification	-	74LVC823A v.1
74LVC823A v.1	19980924	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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