74LVCH16541A

16-bit buffer/line driver; 3-state

Rev. 3 — 15 February 2012 Product data sheet

1. General description

The 74LVCH16541A is a 16-bit buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs (1$\overline{OE}$n and 2$\overline{OE}$n). A HIGH on n$\overline{OE}$n causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 Volt tolerant inputs and outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance outputs when V_{CC} = 0 V
- All data inputs have bus hold
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVCH16541ADGG	–40 to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16541ADL	–40 to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

4. Functional diagram

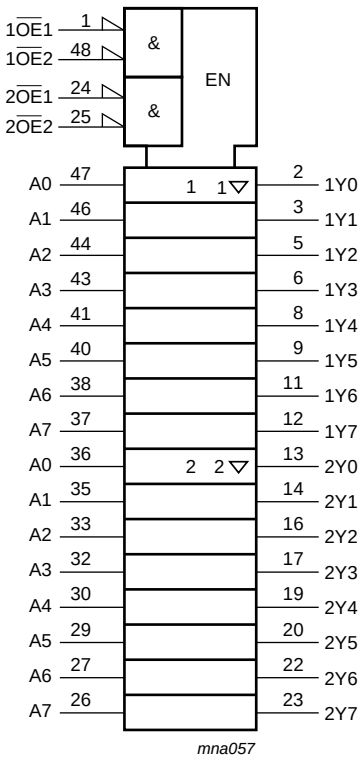


Fig 1. IEC logic symbol

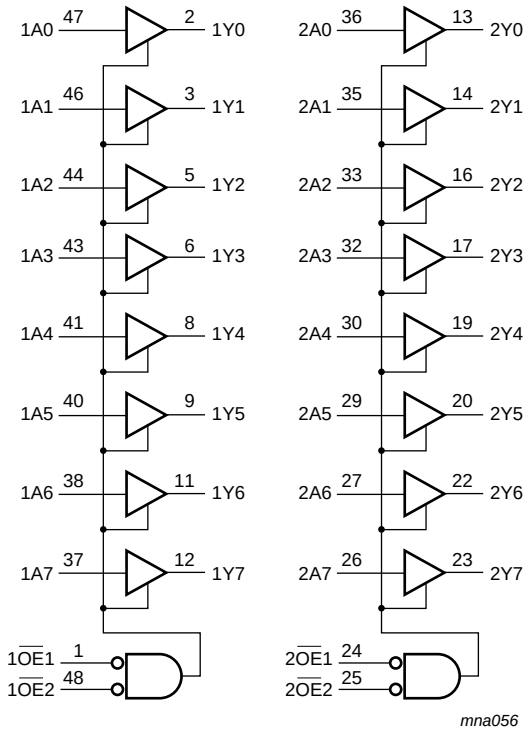


Fig 2. Logic diagram

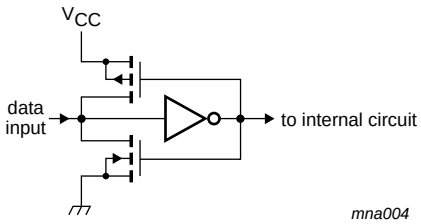


Fig 3. Bus hold circuit

5. Pinning information

5.1 Pinning

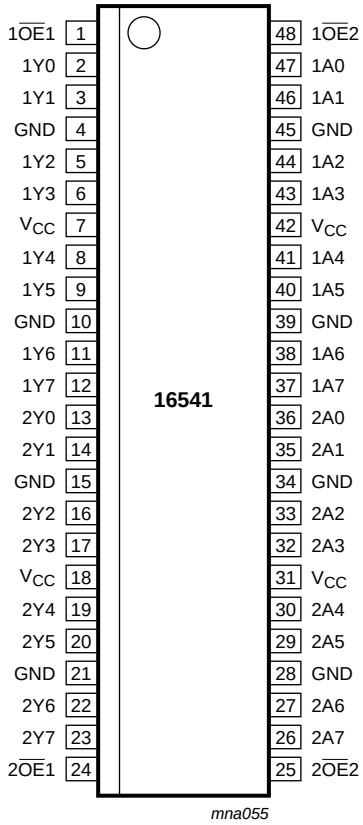


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Name	Pin	Description
1$\overline{OE}$1	1	output enable input (active LOW)
1$\overline{OE}$2	48	output enable input (active LOW)
2$\overline{OE}$1	24	output enable input (active LOW)
2$\overline{OE}$2	25	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	positive supply voltage
1Y[0:7]	2, 3, 5, 6, 8, 9, 11, 12	data output
2Y[0:7]	13, 14, 16, 17, 19, 20, 22, 23	data output
1A[0:7]	47, 46, 44, 43, 41, 40, 38, 37	data input
2A[0:7]	36, 35, 33, 32, 30, 29, 27, 26	data input

6. Functional description

Table 3. Function table[1]

Input			Output
$n\overline{OE}1$	$n\overline{OE}2$	nAn	nYn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
V_I	input voltage		[1]	–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$		–50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2]	–0.5	V_{CC} + 0.5	V
		output 3-state	[2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating operations

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
		functional	1.2	-	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state or V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature	in free air	–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.2	V_{CC}	-	V_{CC} – 0.3	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND[2]	-	±0.1	±5	-	±20	μA

Table 6. Static characteristics *…continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current[2]	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 3.6 V; V_O = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I_{OFF}	power-off leakage supply	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±10	-	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	20	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 1.65 V to 3.6 V; $V_I = V_{CC} - 0.6$ V; I_O = 0 A	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF
I_{BHL}	bus hold LOW current [3][4]	V_{CC} = 1.65; V_I = 0.58 V	10	-	-	10	-	µA
		V_{CC} = 2.3; V_I = 0.7 V	30	-	-	25	-	µA
		V_{CC} = 3.0; V_I = 0.8 V	75	-	-	60	-	µA
I_{BHH}	bus hold HIGH current [3][4]	V_{CC} = 1.65; V_I = 1.07 V	–10	-	-	–10	-	µA
		V_{CC} = 2.3; V_I = 1.7 V	–30	-	-	–25	-	µA
		V_{CC} = 3.0; V_I = 2.0 V	–75	-	-	–60	-	µA
I_{BHLO}	bus hold LOW overdrive current [3][5]	V_{CC} = 1.95 V	200	-	-	200	-	µA
		V_{CC} = 2.7 V	300	-	-	300	-	µA
		V_{CC} = 3.6 V	500	-	-	500	-	µA
I_{BHHO}	bus hold HIGH overdrive current [3][5]	V_{CC} = 1.95 V	–200	-	-	–200	-	µA
		V_{CC} = 2.7 V	–300	-	-	–300	-	µA
		V_{CC} = 3.6 V	–500	-	-	–500	-	µA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input pin.

[3] For data inputs only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nAn to nYn; see Figure 5	[2]						
		V_{CC} = 1.2 V		-	10	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.8	4.7	10.4	1.8	12.0	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	2.6	5.2	1.5	6.0	ns
		V_{CC} = 2.7 V		1.0	2.5	5.0	1.0	6.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.2	4.2	1.0	5.5	ns
t_{en}	enable time	$n\overline{OE}n$ to nYn; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	17	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.5	5.5	14.6	1.5	16.8	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	3.2	7.7	1.0	8.9	ns
		V_{CC} = 2.7 V		1.5	3.4	6.9	1.5	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.6	5.6	1.0	7.0	ns
t_{dis}	disable time	$n\overline{OE}n$ to nYn; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	9.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		2.6	7.3	9.2	2.6	10.6	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	4.1	5.2	1.0	6.0	ns
		V_{CC} = 2.7 V		1.5	4.6	6.5	1.5	8.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	4.5	5.5	1.5	7.0	ns
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	8.5	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	12.1	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	15.3	-	-	-	pF

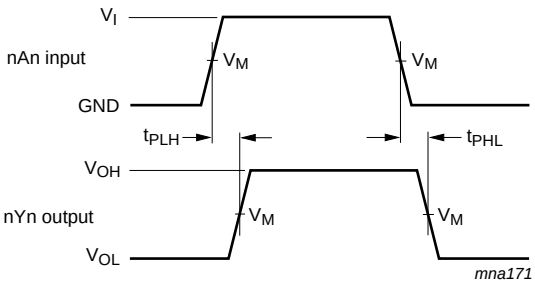
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

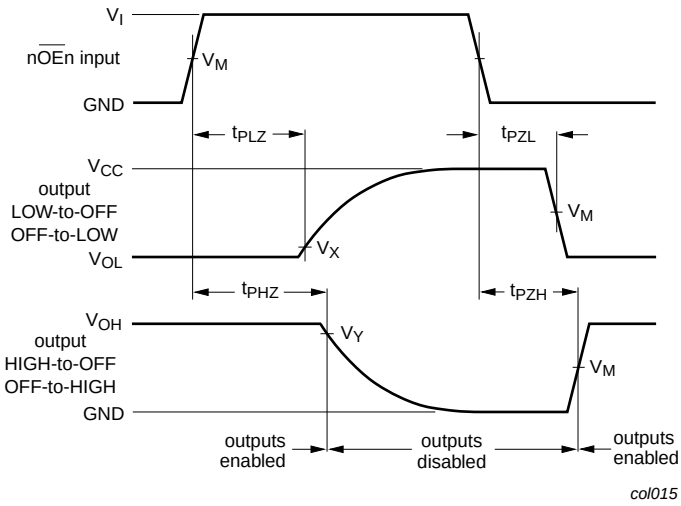
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Input nAn to output nYn propagation delays



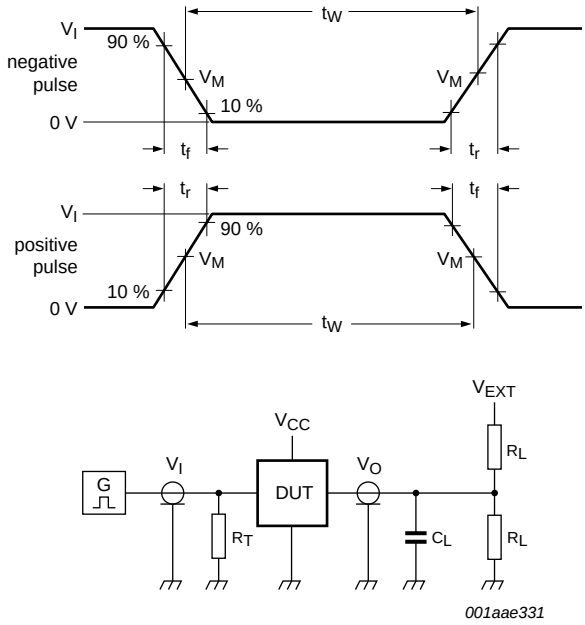
Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	V_M	Input		
V_{CC}		V_I	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	1.5 V	2.7 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	1.5 V	2.7 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

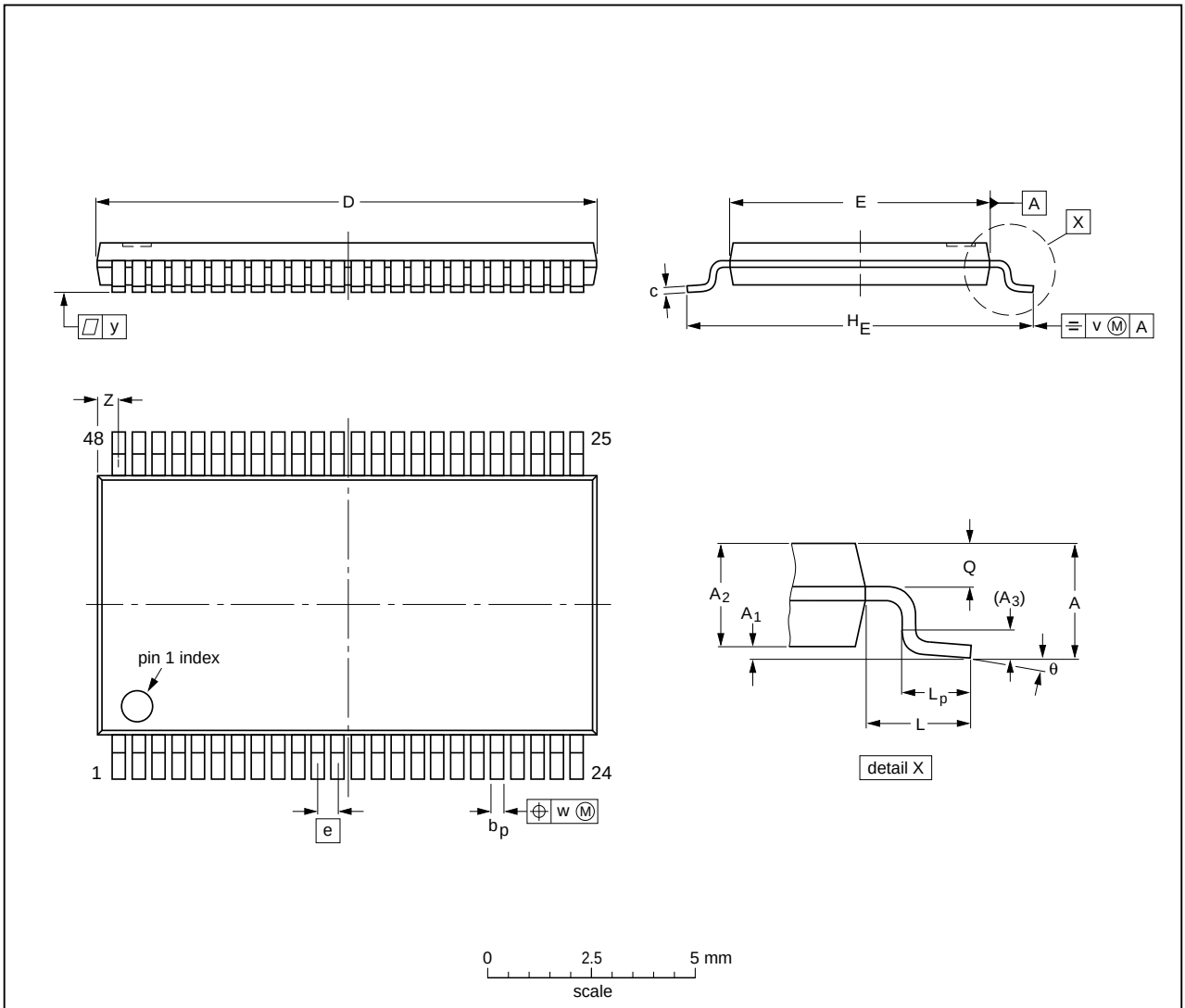
Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

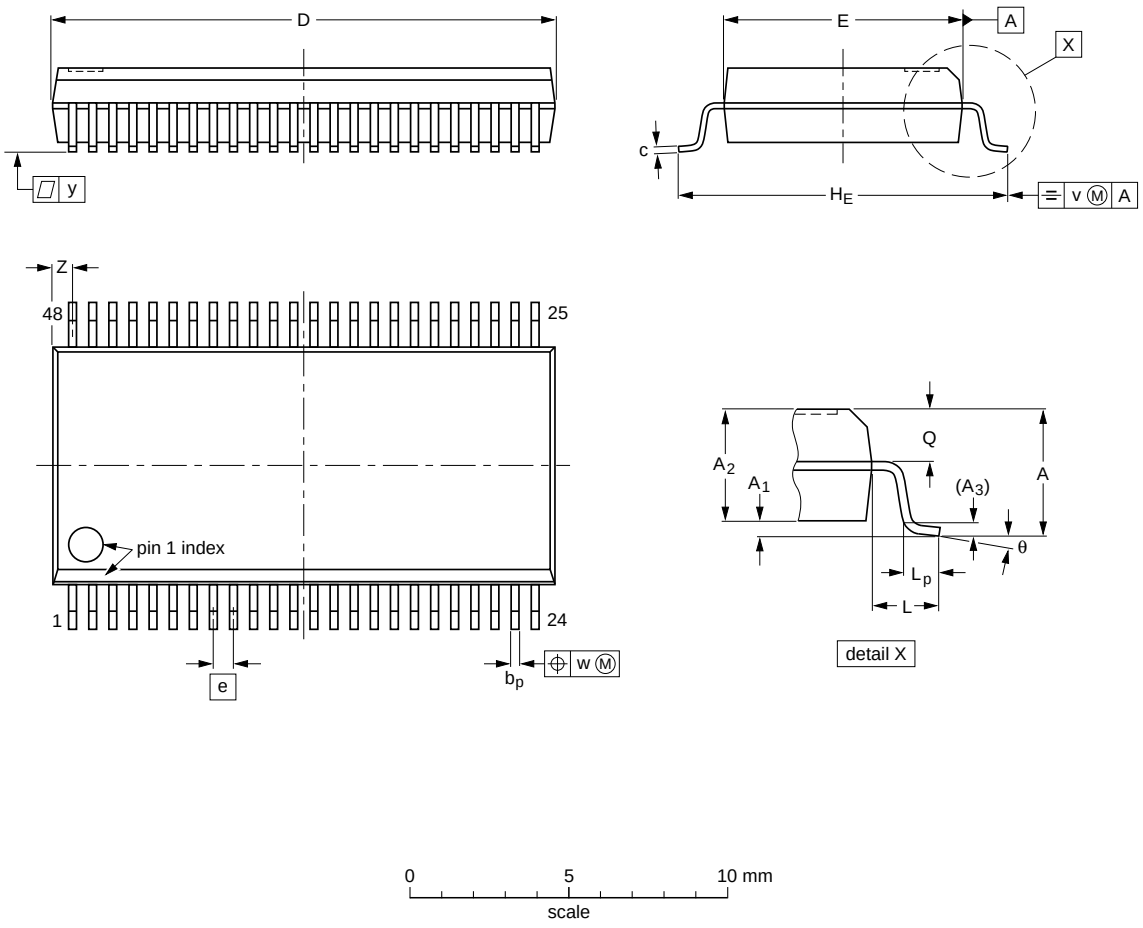
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT362-1 (TSSOP48)

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT370-1 (SSOP48)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCH16541A v.3	20120215	Product data sheet	-	74LVCH16541A v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges.			
74LVCH16541A v.2	20040218	Product specification	-	74LVCH16541A v.1
74LVCH16541A v.1	19980519	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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