



FEATURES

- Access time :55ns
- Low power consumption: Operating current: 10 mA (TYP.) Standby current: 1 μA (TYP)
- Single $2.7V \sim 5.5V$ power supply
- Fully Compatible with all Competitors 5V product
- Fully Compatible with all Competitors 3.3V product
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- All products are ROHS Compliant
- Package: 32-pin 450 mil SOP 32-pin 600 mil P-DIP 32-pin 8mm x 20mm TSOP-I 32-pin 8mm x 13.4mm sTSOP 36-ball 6mm x 8mm TFBGA

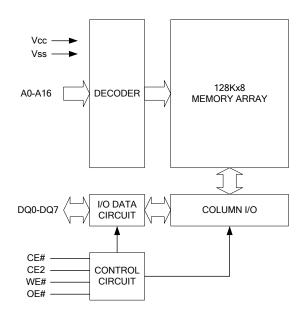
GENERAL DESCRIPTION

The AS6C1008 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C1008 is well designed for very low power system applications, and particularly well suited for battery back-up non-volatile memory application.

The AS6C1008 operates from a single power supply of 2.7V $\sim 5.5V.$

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

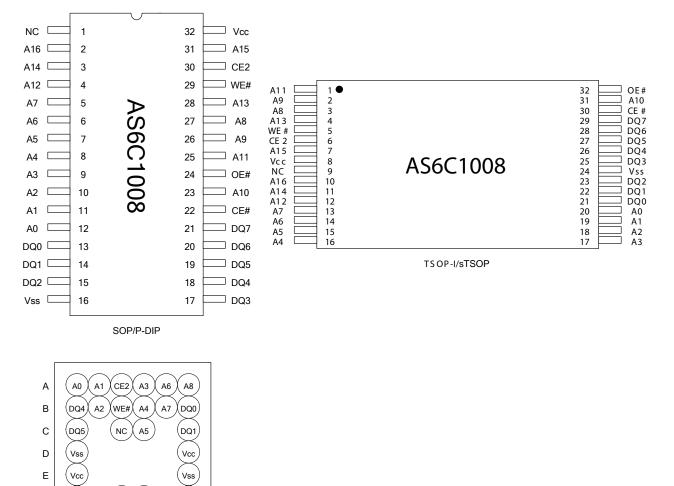


R

128K X 8 BIT LOW POWER CMOS SRAM

PIN CONFIGURATION

February 2007



(NC) NC]

(DQ7)(OE#)(CE#)(A16)(A15)(DQ3)

TFBGA

A10 (A11

F

G

Н

(DQ6)

A9

1 2 3 4 5 6

(DQ2)

∬A12∬A13∬A14



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	VTERM	-0.5 to 7.0	V
		0 to 70(C grade)	
Operating Temperature	TA		°C
		-40 to 85(I grade)	
Storage Temperature	Тѕтс	-65 to 150	°C
Power Dissipation	PD	1	W
DC Output Current	Ιουτ	50	mA
Soldering Temperature (under 10 sec)	TSOLDER	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	Н	Х	Х	Х	High-Z	ISB1
Standby	Х	L	Х	Х	High-Z	ISB1
Output Disable	L	Н	н	Н	High-Z	Icc,Icc1
Read	L	Н	L	Н	Dout	Icc,Icc1
Write	L	Н	Х	L	Din	Icc,Icc1

Note: H = VIH, L = VIL, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDIT	ION	MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	Vcc			2.7	3.0	5.5	V
Input High Voltage	Vih ^{*1}			0.7*Vcc	-	Vcc+0.3	V
Input Low Voltage	VIL ^{*2}			- 0.2	-	0.6	V
Input Leakage Current	ILI	$Vcc \geqq Vin \geqq Vss$		- 1	-	1	μA
Output Leakage Current	Ilo	$V_{CC} \ge V_{OUT} \ge V_{SS},$ Output Disabled		- 1	-	1	μA
Output High Voltage	Vон	Iон = -1mA		2.2	2.7	-	V
Output Low Voltage	Vol	lo∟= 2mA		-	-	0.4	V
Average Operating	lcc	Cycle time = Min. CE# = V _{IL} and CE2 = $I_{I/O}$ = 0mA	Vін, <u>- 55</u>	-	10	60	mA
Power supply Current	ICC1	Cycle time = 1μ s CE# \leq 0.2V and CE2 \geq V _{CC} -0.2V, I _{VO} = 0mA other pins at 0.2V or V _{CC} -0.2V		/, _	1	10	mA
Standby Power	I _{SB1}	$CE# \ge V_{CC}-0.2V$	C*	-	1	20	μA
Supply Current	1281	or CE2≦0.2V	*	-	1	50	μA

*C=Commercial temperature/I= Industrial temperature



Notes:

- 1. $V_{IH}(max) = V_{CC} + 3.0V$ for pulse width less than 10ns.
- 2. VIL(min) = Vss 3.0V for pulse width less than 10ns.
- 3. Over/Undershoot specifications are characterized, not 100% tested.
- 4. Typical values are included for reference only and are not guaranteed or tested.
- Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	CIN	-	6	pF
Input/Output Capacitance	Cı/o	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to Vcc - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	CL =30pF + 1TTL, Iон/IоL = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.		AS6C1008-55			UNIT
			MIN.	MAX.	İ	
Read Cycle Time	trc		55	-		ns
Address Access Time	taa		-	55		ns
Chip Enable Access Time	t ACE		-	55		ns
Output Enable Access Time	toe		-	30		ns
Chip Enable to Output in Low-Z	tcLz*		10	-		ns
Output Enable to Output in Low-Z	to∟z*		5	-		ns
Chip Disable to Output in High-Z	tснz*		-	20		ns
Output Disable to Output in High-Z	tонz*		-	20		ns
Output Hold from Address Change	toн	İ	10	-	İ	ns

(2) WRITE CYCLE

PARAMETER	SYM.	AS6C1008-55			UNIT		
				MIN.	MAX.		
Write Cycle Time	twc			55	-		ns
Address Valid to End of Write	taw			50	-		ns
Chip Enable to End of Write	tcw			50	-		ns
Address Set-up Time	tas			0	-		ns
Write Pulse Width	twp			45	-		ns
Write Recovery Time	twr			0	-		ns
Data to Write Time Overlap	tow			25	-		ns
Data Hold from End of Write Time	tон			0	-		ns
Output Active from End of Write	tow*			5	-		ns
Write to Output in High-Z	twнz*			-	20		ns

*These parameters are guaranteed by device characterization, but not production tested.

February 2007

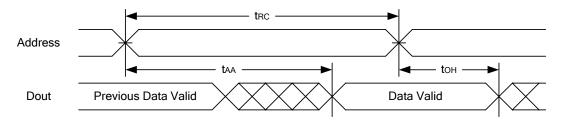


AS6C1008

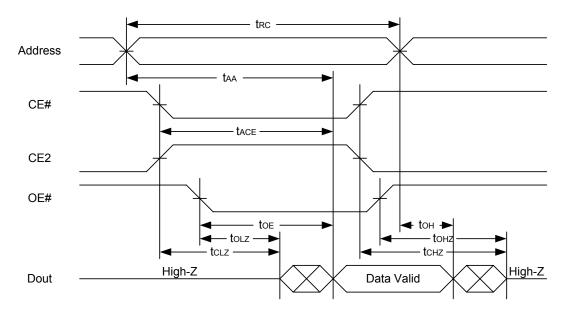
128K X 8 BIT LOW POWER CMOS SRAM

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

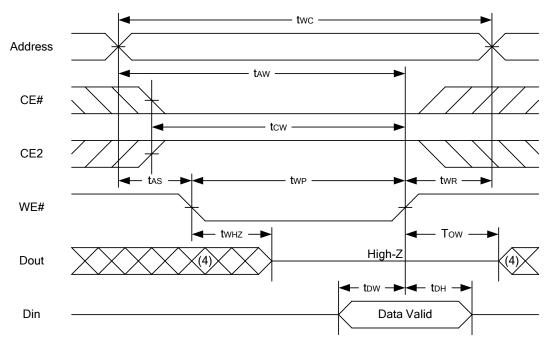
1.WE# is high for read cycle.

2.Device is continuously selected OE# = low, CE# = low., CE2 = high.

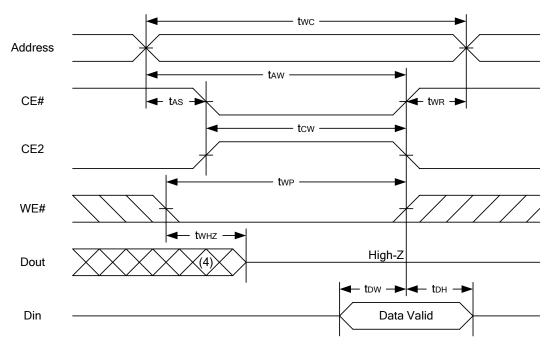
3.Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter. 4.tcLz, tcLz, tcLz and toHz are specified with CL = 5pF. Transition is measured \pm 500mV from steady state.

5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



Notes :

2.A write occurs during the overlap of a low CE#, high CE2, low WE#.

3.During a WE#controlled write cycle with OE# low, twp must be greater than twHz + tpw to allow the drivers to turn off and data to be placed on the bus.

4. During this period, I/O pins are in the output state, and input signals must not be applied.

5.If the CE#low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.

6.tow and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

Alliance Memory Inc.

^{1.}WE#, CE# must be high or CE2 must be low during all address transitions.



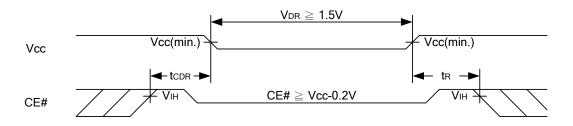
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention		$\begin{array}{l} \text{CE\#} \geqq V_{\text{CC}} \text{-} 0.2 \text{V} \\ \text{or CE2} \leqq 0.2 \text{V} \end{array}$		1.5	-	5.5	V
Data Retention Current		Vcc = 1.5V CE# ≧ Vcc - 0.2V	C**	-	0.5	12	μA
		or CE2 $\leq 0.2V$	**		0	30	μA
Chip Disable to Data Retention Time	tCDR	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	tR			tRC∗	-	-	ns

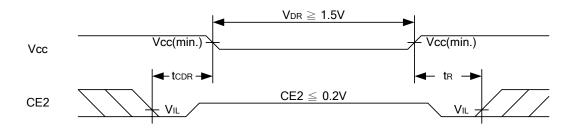
tRC* = Read Cycle Time C=Commercial temp/I = Industrial temp**

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)



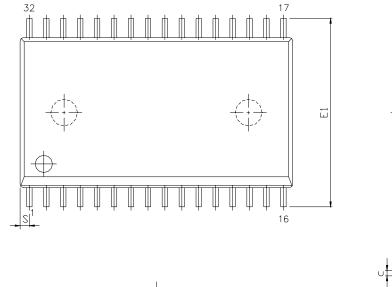
Low Vcc Data Retention Waveform (2) (CE2 controlled)

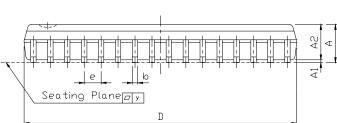


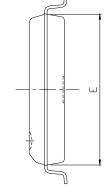


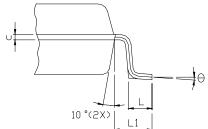
PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension





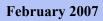




AS6C1008

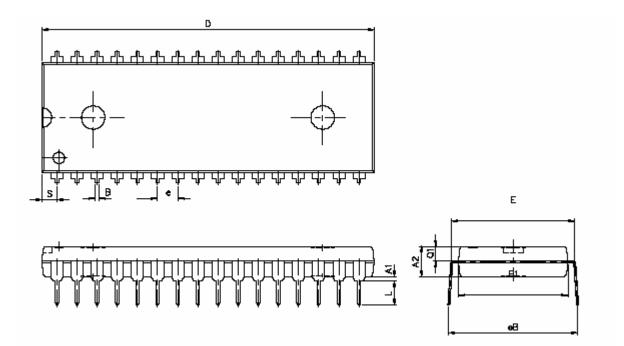
UNIT SYM.	INCH.(BASE)	MM(REF)
A	0.118 (MAX)	2.997 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.111(MAX)	2.82(MAX)
b	0.016(TYP)	0.406(TYP)
С	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
Е	0.445 ±0.005	11.303 ±0.127
E1	0.555 ±0.012	14.097 ±0.305
е	0.050(TYP)	1.270(TYP)
L	0.0347 ±0.008	0.881 ±0.203
L1	0.055 ±0.008	1.397 ±0.203
S	0.026(MAX)	0.660 (MAX)
у	0.004(MAX)	0.101(MAX)
Θ	0° -10°	0° -10°

02/February/07, v 1.0





32 pin 600 mil P-DIP Package Outline Dimension



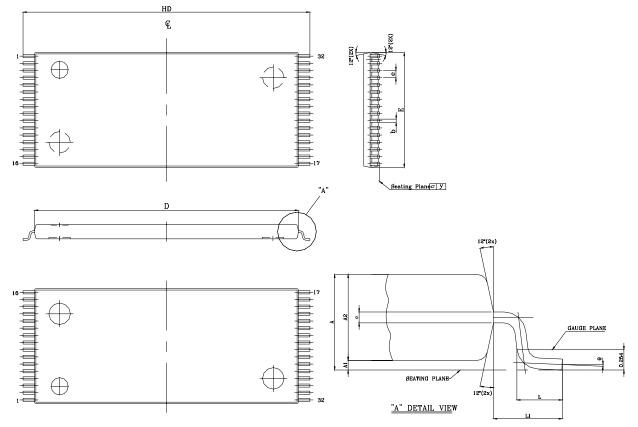
UNIT SYM.	INCH(BASE)	MM(REF)
A1	0.001 (MIN)	0.254 (MIN)
A2	0.150 ± 0.005	3.810 ± 0.127
В	0.018 ± 0.005	0.457 ± 0.127
D	1.650 ± 0.005	41.910 ± 0.127
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.544 ± 0.004	13.818 ± 0.102
е	0.100 (TYP)	2.540 (TYP)
eB	0.640 ± 0.020	16.256 ± 0.508.
L	0.130 ± 0.010	3.302 ± 0.254
S	0.075 ± 0.010	1.905 ± 0.254
Q1	0.070 ± 0.005	1.778 ± 0.127

Note : D/E1/S dimension do not include mold flash.

AS6C1008



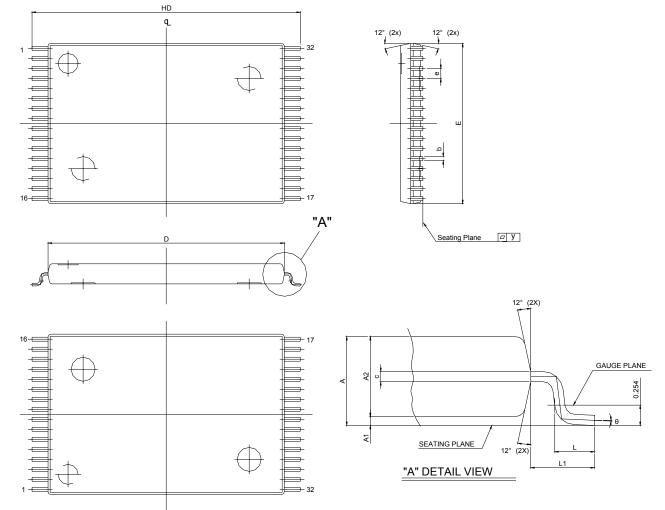
32 pin 8mm x 20mm TSOP-I Package Outline Dimension



UNIT SYM.	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
С	0.005 (TYP)	0.127 (TYP)
D	0.724 ±0.004	18.40 ±0.10
E	0.315 ±0.004	8.00 ±0.10
е	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
у	0.003 (MAX)	0.076 (MAX)
Θ	0°~5°	0°~5°



32 pin 8mm x 13.4mm sTSOP Package Outline Dimension



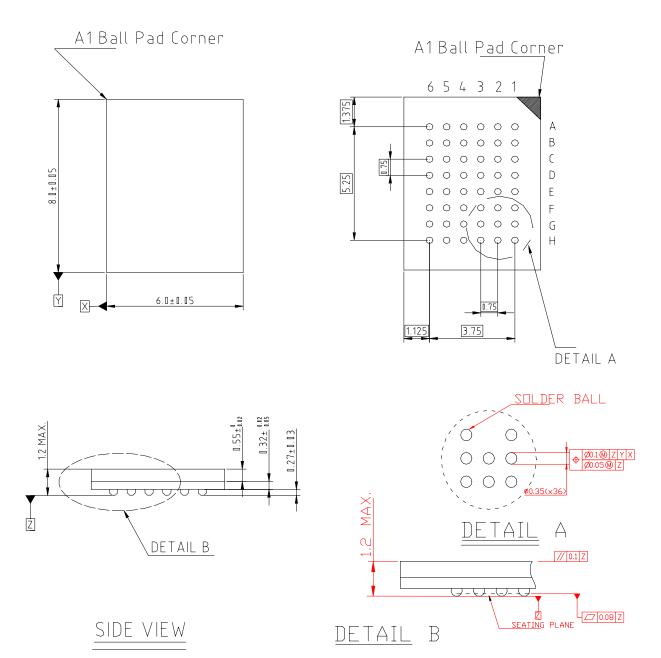
UNIT SYM.	INCH(BASE)	MM(REF)	
A	0.049 (MAX)	1.25 (MAX)	
A1	0.005 ±0.002	0.130 ±0.05	
A2	0.039 ±0.002	1.00 ±0.05	
b	0.008 ±0.01	0.20±0.025	
С	0.005 (TYP)	0.127 (TYP)	
D	0.465 ±0.004	11.80 ±0.10	
E	0.315 ±0.004	8.00 ±0.10	
е	0.020 (TYP)	0.50 (TYP)	
HD	0.528±0.008	13.40 ±0.20.	
L	0.0197 ±0.004	0.50 ±0.10	
L1	0.0315 ±0.004	0.8 ±0.10	
у	0.003 (MAX)	0.076 (MAX)	
Θ	0°~5°	0°~5°	

Alliance Memory Inc.

February 2007



36 ball 6mm × 8mm TFBGA Package Outline Dimension



February 2007

AS6C1008



ORDERING INFORMATION

Ordering Codes

Alliance	Organization	VCC range	Package	Operating Temp	Speed ns
AS6C1008-55PCN	128K X 8	2.7-5.5V	32pin 600mil PDIP	Commercial ~ 0° C to 70° C	55
AS6C1008-55PIN	128K X 8	2.7-5.5V	32pin 600mil PDIP	Industrial ~ -40°C to 85° C	55
AS6C1008-55SIN	128K X 8	2.7-5.5V	32pin 450mil SOP	Industrial ~ -40°C to 85° C	55
AS6C1008-55TIN	128K X 8	2.7-5.5V	32pin TSOP-I (8 x 20 mm)	Industrial ~ -40°C to 85° C	55
AS6C1008-55STIN	128K X 8	2.7-5.5V	32pin sTSOP (8 x 13.4 mm)	Industrial ~ -40°C to 85° C	55
AS6C1008-55BIN	128K X 8	2.7-5.5V	36pin TFBGA (6mm x 8mm)	Industrial ~ -40°C to 85° C	55

Part numbering system

AS6C	1008	- 55	Х	Х	N
low	Device		Package Options: P = 32 pin 600 mil P-DIP S = 32 pin 450 mil SOP	Temperature Range: C = Commercial	N = Lead
	Number		T = 32 pin 430 min 30P T = 32 pin TSOP-I (8mm x 20 mm)		Free ROHS
		Access	ST = 32 pin sTSOP (8 x 13.4 mm)	I = Industrial	Compliant
prefix	08 = by 8	Time	B = 36 ball 6 x 8mm TFBGA	(-40° to +85° C)	Part





Alliance Memory, Inc. 1116 South Amphlett, #2, San Mateo, CA 94402 Tel: 650-525-3737 Fax: 650-525-0449

www.alliancememory.com

Copyright © Alliance Memory All Rights Reserved Part Number: AS6C1008 Document Version: v. 1.0

© Copyright 2003 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.

Alliance Memory Inc.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for SRAM category:

Click to view products by Alliance Memory manufacturer:

Other Similar products are found below :

5962-8855206XA CY6116A-35DMB CY7C128A-45DMB CY7C1461KV33-133AXI CY7C199-45LMB GS8161Z36DD-200I GS88237CB-200I R1QDA7236ABB-20IB0 RMLV0408EGSB-4S2#AA0 IS64WV3216BLL-15CTLA3 IS66WVE4M16ECLL-70BLI PCF8570P K6T4008C1B-GB70 CY7C1353S-100AXC AS6C8016-55BIN AS7C164A-15PCN 515712X IS62WV51216EBLL-45BLI IS63WV1288DBLL-10HLI IS66WVE2M16ECLL-70BLI 47L16-E/SN IS66WVE4M16EALL-70BLI IS62WV6416DBLL-45BLI IS61WV102416DBLL-10TLI CY7C1381KV33-100AXC CY7C1381KV33-100BZXI CY7C1373KV33-100AXC CY7C1381KVE33-133AXI CY7C4042KV13-933FCXC 8602501XA 5962-3829425MUA 5962-8855206YA 5962-8866201XA 5962-8866201YA 5962-8866204TA 5962-8866206MA 5962-8866207NA 5962-8866208UA 5962-8872502XA 5962-8959836MZA 5962-8959841MZA 5962-9062007MXA 5962-9161705MXA N08L63W2AB7I 7130LA100PDG M38510/28902BVA 5962-8971203XA 5962-8971202ZA 5962-8872501LA 5962-8866207UA