



8K X 8 BIT LOW POWER CMOS SRAM

**FEATURES**

- 8192 x 8 bit static CMOS RAM
- 70 ns Access Times
- Common data inputs and outputs
- Three-state outputs
- Typ. operating supply current
  - 70 ns: 10 mA
- Standby current:
  - < 2  $\mu$  A at  $T_a \leq 70^\circ\text{C}$
- Data retention current at 2 V:
  - < 1  $\mu$  A at  $T_a \leq 70^\circ\text{C}$
- TTL/CMOS-compatible
- Automatic reduction of power dissipation in long Read or Write cycles
- Power supply voltage 5 V
- Operating temperature ranges:
  - 0 to 70  $^\circ\text{C}$
  - -40 to 85  $^\circ\text{C}$
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity > 100 mA
- Packages: PDIP28 (600 mil)  
SOP28 (330 mil)

**DESCRIPTION**

The AS6C6264A is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read - Standby
- Write - Data Retention

The memory array is based on a 6-transistor cell.

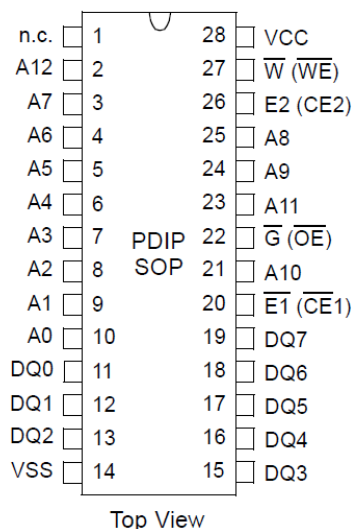
The circuit is activated by the rising edge of E2 (at E1 = L), or the falling edge of E1 (at E2 = H). The address and control inputs open simultaneously. According to the information of W and G, the data inputs, or outputs, are active. In a Read cycle, the data outputs are activated by the falling edge of G, afterwards the data word read will be available at the outputs DQ0 - DQ7. After the address change, the data outputs go High-Z until the new read information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address,

data input and control signals W or G, the operating current (at IO = 0 mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of E2 or W, or by the rising edge of E1, respectively.

Data retention is guaranteed down to 2 V. With the exception of E2, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required. This gate circuit allows to achieve low power standby requirements by activation with TTL-levels too.

If the circuit is inactivated by E2 = L, the standby current

**PIN CONFIGURATION**



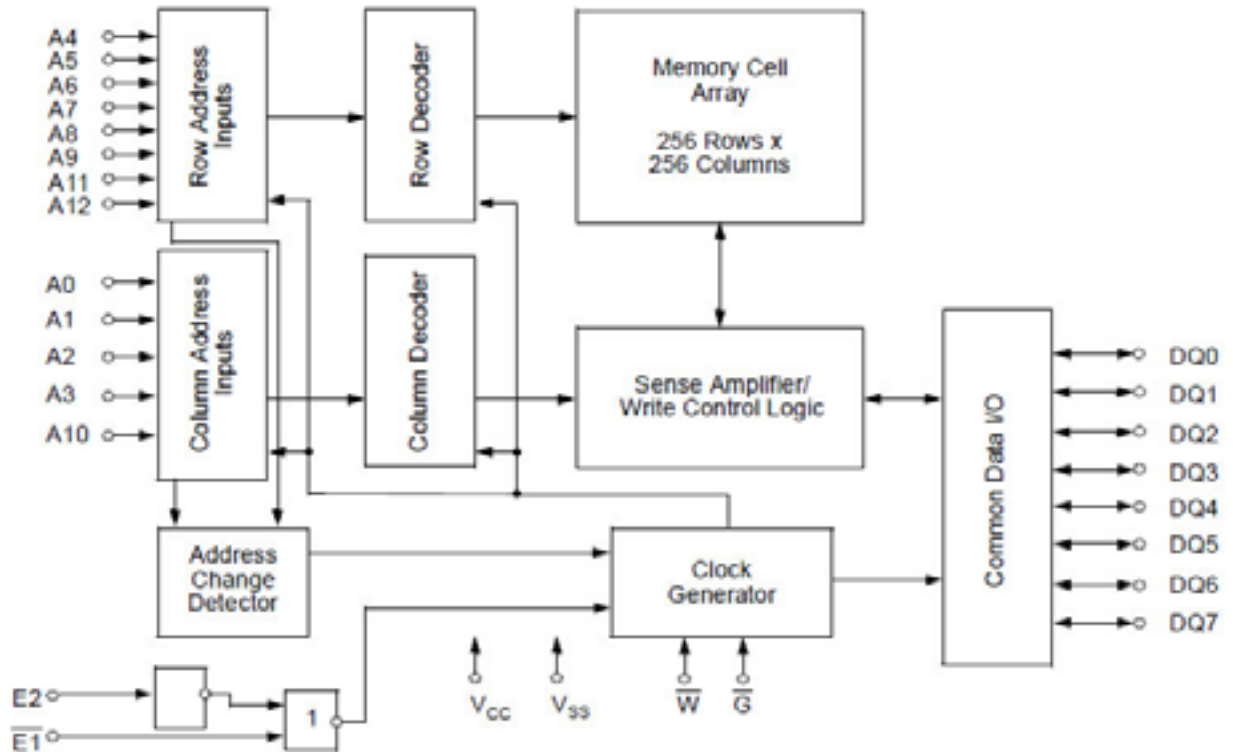
**PIN DESCRIPTION**

Signal Name	Signal Description
A0 - A12	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{\text{E1}}$	Chip Enable 1
E2	Chip Enable 2
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground
n.c.	not connected



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**BLOCK DIAGRAM**



**TRUTH TABLE**

Operating Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	*	L	*	*	High-Z
	H	*	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs Low-Z
Write	L	H	L	*	Data Inputs High-Z

\* H or L



## 8K X 8 BIT LOW POWER CMOS SRAM

**CHARACTERISTICS**

All voltages are referenced to VSS = 0 V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of  $\leq 5$  ns, measured between 10 % and 90 % of VI, as well as input levels of VIL = 0 V and VIH = 3 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the tdis-times, in which cases transition is measured } 200 mV from steady-state voltage.

Absolute Maximum Ratings <sup>a</sup>		Symbol	Min.	Max.	Unit
Power Supply Voltage		V <sub>CC</sub>	-0.3	7	V
Input Voltage		V <sub>I</sub>	-0.3	V <sub>CC</sub> + 0.5 <sup>b</sup>	V
Output Voltage		V <sub>O</sub>	-0.3	V <sub>CC</sub> + 0.5 <sup>b</sup>	V
Power Dissipation		P <sub>D</sub>	-	1	W
Operating Temperature	C-Type	T <sub>a</sub>	0	70	°C
	I-Type		-40	85	°C
Storage Temperature	C/I-Type	T <sub>stg</sub>	-55	125	°C
Output Short-Circuit Current at V <sub>CC</sub> = 5 V and V <sub>O</sub> = 0 V <sup>c</sup>		I <sub>OS</sub>		100	mA

- Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Maximum voltage is 7 V
- Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>		4.5	5.5	V
Data Retention Voltage	V <sub>CC(DR)</sub>		2.0		V
Input Low Voltage <sup>d</sup>	V <sub>IL</sub>		-0.3	0.8	V
Input High Voltage	V <sub>IH</sub>		2.2	V <sub>CC</sub> + 0.3	V

<sup>d</sup> -2 V at Pulse Width 10 ns



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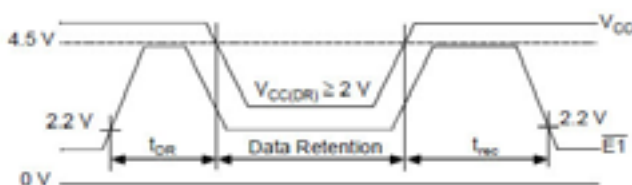
Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	$V_{CC} = 5.5 \text{ V}$ $V_{IL} = 0.8 \text{ V}$ $V_{IH} = 2.2 \text{ V}$ $t_{cW} = 70 \text{ ns}$		55	mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	$V_{CC} = 5.5 \text{ V}$ $V_{ET} = V_{E2} = V_{CC} - 0.2 \text{ V}$ or $V_{E2} = 0.2 \text{ V}$ C-Type I-Type		2 5	$\mu\text{A}$ $\mu\text{A}$
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)T}$	$V_{CC} = 5.5 \text{ V}$ $V_{ET} = V_{E2} = 2.2 \text{ V}$ or $V_{E2} = 0.8 \text{ V}$		3	mA
Supply Current - Data Retention Mode	$I_{CC(DR)}$	$V_{CC(DR)} = 2 \text{ V}$ $V_{ET} = V_{E2} = V_{CC(DR)} - 0.2 \text{ V}$ or $V_{E2} = 0.2 \text{ V}$ C-Type I-Type		1 3	$\mu\text{A}$ $\mu\text{A}$
Output High Voltage	$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -1.0 \text{ mA}$	2.4		V
Output Low Voltage	$V_{OL}$	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 3.2 \text{ mA}$		0.4	V
Output High Current	$I_{OH}$	$V_{CC} = 4.5 \text{ V}$ $V_{OH} = 2.4 \text{ V}$		-1	mA
Output Low Current	$I_{OL}$	$V_{CC} = 4.5 \text{ V}$ $V_{OL} = 0.4 \text{ V}$	3.2		mA
Input Leakage Current					
High	$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ $V_{IH} = 5.5 \text{ V}$ C/I-Type	-	1	$\mu\text{A}$
Low	$I_{IL}$	$V_{CC} = 5.5 \text{ V}$ $V_{IL} = 0 \text{ V}$ C/I-Type	-1	-	$\mu\text{A}$
Output Leakage Current					
High at Three-State Outputs	$I_{OHZ}$	$V_{CC} = 5.5 \text{ V}$ $V_{OH} = 5.5 \text{ V}$ C/I-Type	-	1	$\mu\text{A}$
Low at Three-State Outputs	$I_{OLZ}$	$V_{CC} = 5.5 \text{ V}$ $V_{OL} = 0 \text{ V}$ C/I-Type	-1	-	$\mu\text{A}$



8K X 8 BIT LOW POWER CMOS SRAM

Switching Characteristics	Symbol		Min.	Max.	Unit
	Alt.	IEC			
Time to Output in Low-Z	$t_{LZ}$	$t_{L(QX)}$	5	10	ns
Cycle Time					
Write Cycle Time	$t_{WC}$	$t_{CW}$	70		ns
Read Cycle Time	$t_{RC}$	$t_{cR}$	70		ns
Access Time					
$\overline{E1}$ LOW or E2 HIGH to Data Valid	$t_{ACE}$	$t_{a(E)}$	-	70	ns
$\overline{G}$ LOW to Data Valid	$t_{OE}$	$t_{a(G)}$	-	40	ns
Address to Data Valid	$t_{AA}$	$t_{a(A)}$	-	70	ns
Pulse Widths					
Write Pulse Width	$t_{WP}$	$t_{w(W)}$	50		ns
Chip Enable to End of Write	$t_{CW}$	$t_{w(E)}$	65		ns
Setup Times					
Address Setup Time	$t_{AS}$	$t_{su(A)}$	0		ns
Chip Enable to End of Write	$t_{CW}$	$t_{su(E)}$	65		ns
Write Pulse Width	$t_{WP}$	$t_{su(W)}$	50		ns
Data Setup Time	$t_{DS}$	$t_{su(D)}$	35		ns
Data Hold Time	$t_{DH}$	$t_{h(D)}$	0		ns
Address Hold from End of Write	$t_{AH}$	$t_{h(A)}$	0		ns
Output Hold Time from Address Change	$t_{OH}$	$t_{h(A)}$	5		ns
$\overline{E1}$ HIGH or E2 LOW to Output in High-Z	$t_{HZCE}$	$t_{dis(E)}$	0	25	ns
$\overline{W}$ LOW to Output in High-Z	$t_{HZWE}$	$t_{dis(W)}$	0	30	ns
$\overline{G}$ HIGH to Output in High-Z	$t_{HZOE}$	$t_{dis(G)}$	0	25	ns

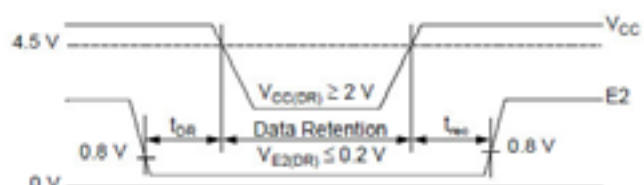
Data Retention Mode  $\overline{E1}$ -Controlled



$$V_{E2(DR)} \geq V_{CC(DR)} - 0.2 \text{ V or } V_{E2(DR)} \leq 0.2 \text{ V}$$

$$V_{CC(DR)} - 0.2 \text{ V} \leq V_{E1(DR)} \leq V_{CC(DR)} + 0.3 \text{ V}$$

Data Retention Mode E2-Controlled

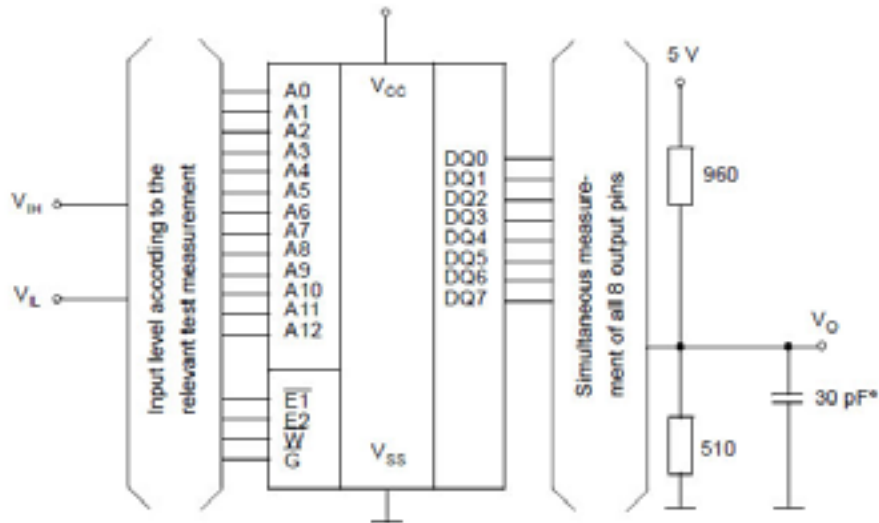


Chip Deselect to Data Retention Time  $t_{DR}$ : min 0 ns  
 Operating Recovery Time  $t_{rec}$ : min  $t_{cR}$



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TEST CONFIGURATION FOR FUNCTIONAL CHECK



\* In measurement of  $t_{dis(E)}$ ,  $t_{dis(W)}$ ,  $t_{dis(G)}$  the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 5.0\text{ V}$ $V_I = V_{SS}$	$C_I$		8	pF
Output Capacitance	$f = 1\text{ MHz}$ $T_a = 25\text{ }^\circ\text{C}$	$C_O$		10	pF

All pins not under test must be connected with ground by capacitors.

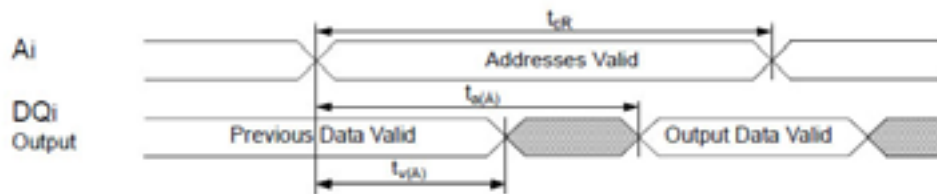
Device Marking (example)



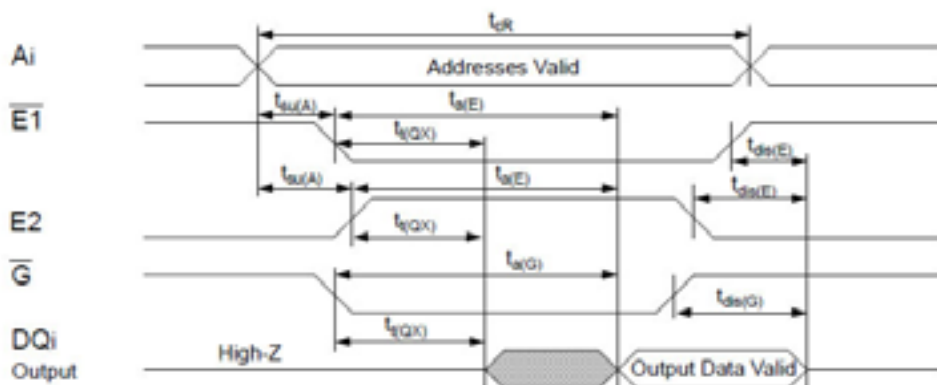


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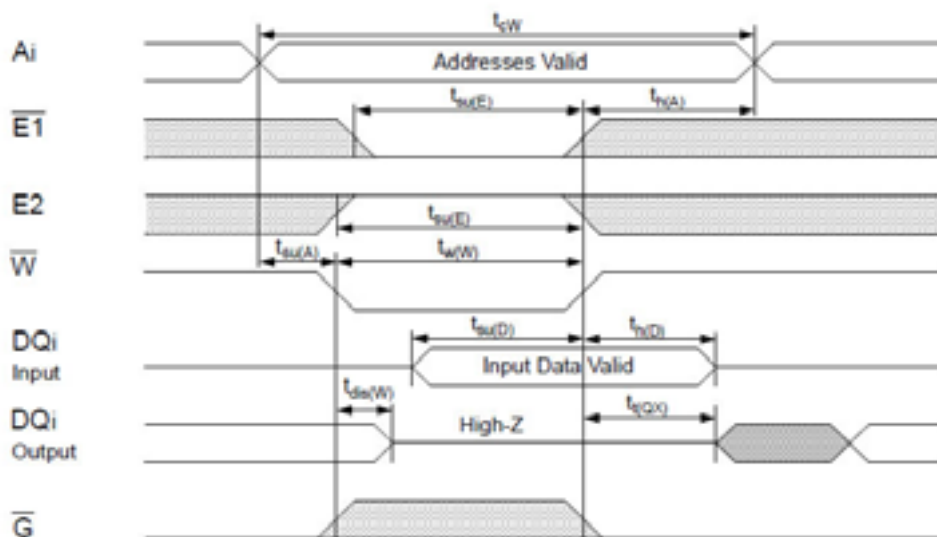
Read Cycle 1 (during Read cycle:  $\overline{E1} = \overline{G} = V_{IL}$ ,  $E2 = \overline{W} = V_{IH}$ )



Read Cycle 2 (during Read cycle:  $\overline{W} = V_{IH}$ )



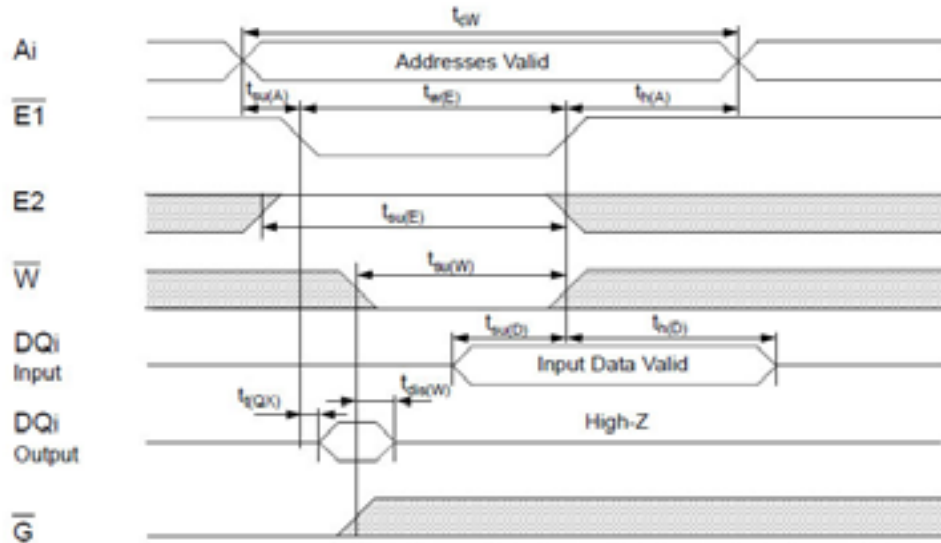
Write Cycle 1 ( $\overline{W}$ -controlled)



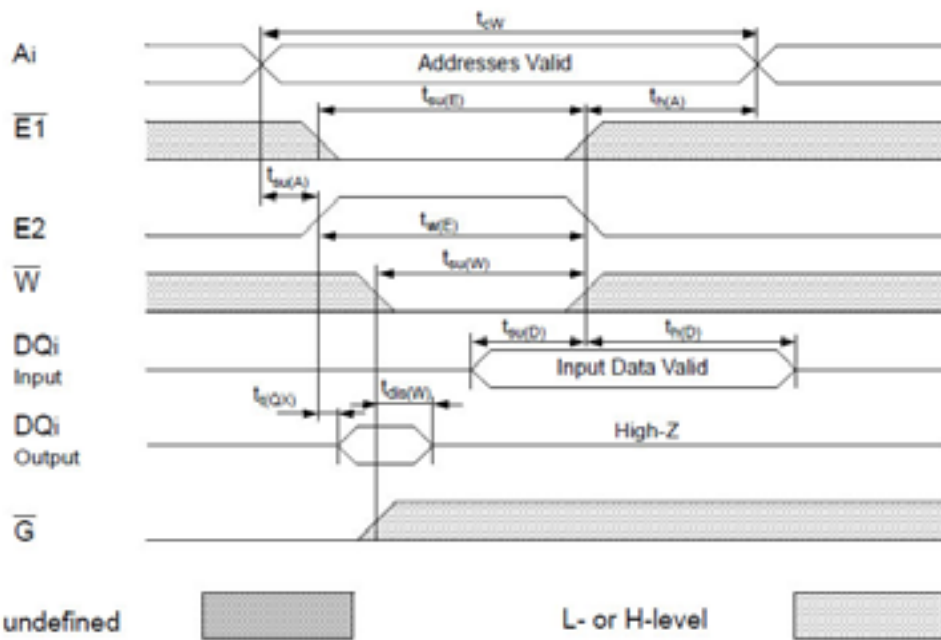


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Write Cycle 2 ( $\overline{E1}$ -controlled)



Write Cycle 3 ( $E2$ -controlled)



The information describes the type of component and shall not be considered as assured characteristic. Terms of delivery and rights to change design reserved.





## 8K X 8 BIT LOW POWER CMOS SRAM

**ORDERING INFORMATION**

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C6264A-70SCN	8K x 8	4.5 - 5.5V	28pin 330 mil SOP	Commercial- 0 C – 70 C	70
AS6C6264A-70SIN	8K x 8	4.5 - 5.5V	28pin 330 mil SOP	Industrial ~ -40 C - 85 C	70
AS6C6264A-70PCN	8K x 8	4.5 - 5.5V	28pin 600 mil P-DIP	Commercial- 0 C – 70 C	70
AS6C6264A-70PIN	8K x 8	4.5 - 5.5V	28pin 600 mil P-DIP	Industrial ~ -40 C - 85 C	70

**PART NUMBERING SYSTEM**

AS6C	6264	A	-70	X	X	N
SRAM prefix	Device Number: Low Power (64K)	Die Rev	Access Time	Package Option: P=28pin 600mil PDIP S=28pin 330mil SOP	Temperature Range: C = Commercial (0 to 70 C) I = Industrial (-40 to + 85 C)	N = Lead Free RoHS compliant part



## 8K X 8 BIT LOW POWER CMOS SRAM



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