

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™ Power-MOSFET, 25 V
BSB008NE2LX

Data Sheet

Rev. 2.0
Final

1 Description

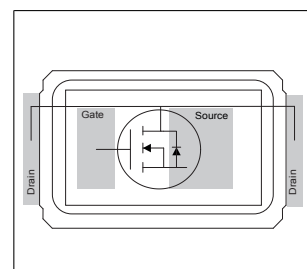
Features

- Optimized for e-fuse and OR-ing application
- Ultra low $R_{DS(on)}$ in CanPAK-MX footprint
- Low profile (<0.7 mm)
- 100% avalanche tested
- 100% R_g Tested
- Double-sided cooling
- Compatible with DirectFET® package MX footprint and outline ¹⁾
- Qualified according to JEDEC²⁾ for target applications



Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$	0.8	$m\Omega$
I_D	180	A
Q_{oss}	74	nC
$Q_g(0V..10V)$	258	nC



Type / Ordering Code	Package	Marking	Related Links
BSB008NE2LX	MG-WDSON-2	04E2	-

¹⁾ CanPAK™ uses DirectFET® technology licensed from International Rectifier Corporation. DirectFET® is a registered trademark of International Rectifier Corporation.

²⁾ J-STD20 and JESD22

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	180 165 46	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=45\text{ K/W}$
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Avalanche current, single pulse ²⁾	I_{AS}	-	-	40	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	600	mJ	$I_D=40\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	89 2.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=45\text{ K/W}$
Operating and storage temperature	T_j , T_{stg}	-40	-	150	°C	IEC climatic category; DIN IEC 68-1: 40/150/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	-	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	1.4	K/W	-
Device on PCB, 6 cm ² cooling area ³⁾	R_{thJA}	-	-	45	K/W	-

¹⁾ See figure 3 for more detailed information

²⁾ See figure 13 for more detailed information

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	10 100	μA	$V_{DS}=25\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=25\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.75 0.6	1.0 0.8	m Ω	$V_{GS}=4.5\text{ V}$, $I_D=25\text{ A}$ $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$
Gate resistance	R_G	0.3	0.5	1.0	Ω	-
Transconductance	g_{fs}	120	240	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=30\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	12000	16000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=12\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	3800	5100	pF	$V_{GS}=0\text{ V}$, $V_{DS}=12\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	3300	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=12\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	12.6	-	ns	$V_{DD}=12\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	47.2	-	ns	$V_{DD}=12\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	75	-	ns	$V_{DD}=12\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	32.4	-	ns	$V_{DD}=12\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	27	36	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	19	-	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	73	110	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	81	-	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	Q_g	-	146	194	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.2	-	V	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	Q_g	-	258	343	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	88	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge	Q_{oss}	-	74	98	nC	$V_{DD}=12\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	89	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.78	-	V	$V_{GS}=0\text{ V}, I_F=30\text{ A}, T_J=25\text{ °C}$
Reverse recovery charge	Q_{rr}	-	20	-	nC	$V_R=15\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$

5 Electrical characteristics diagrams

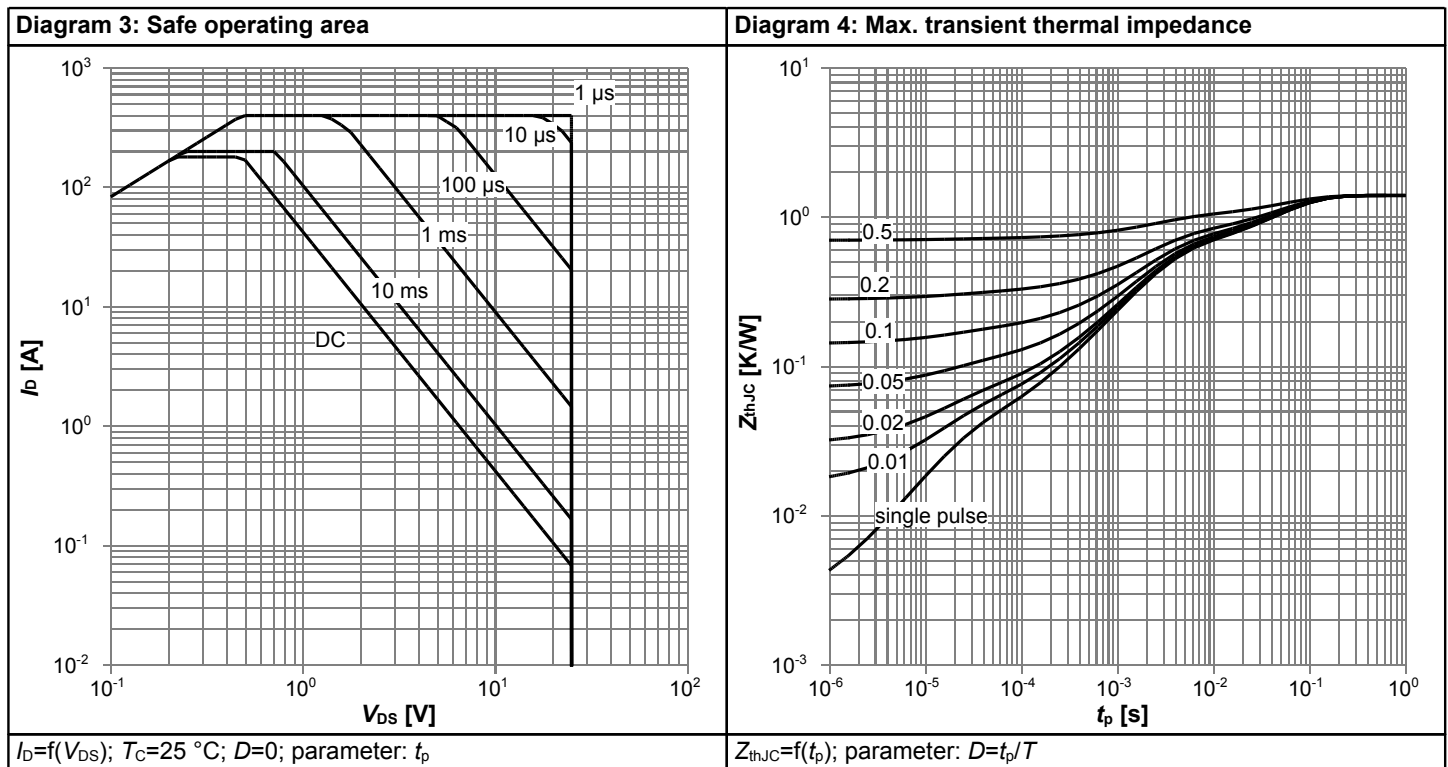
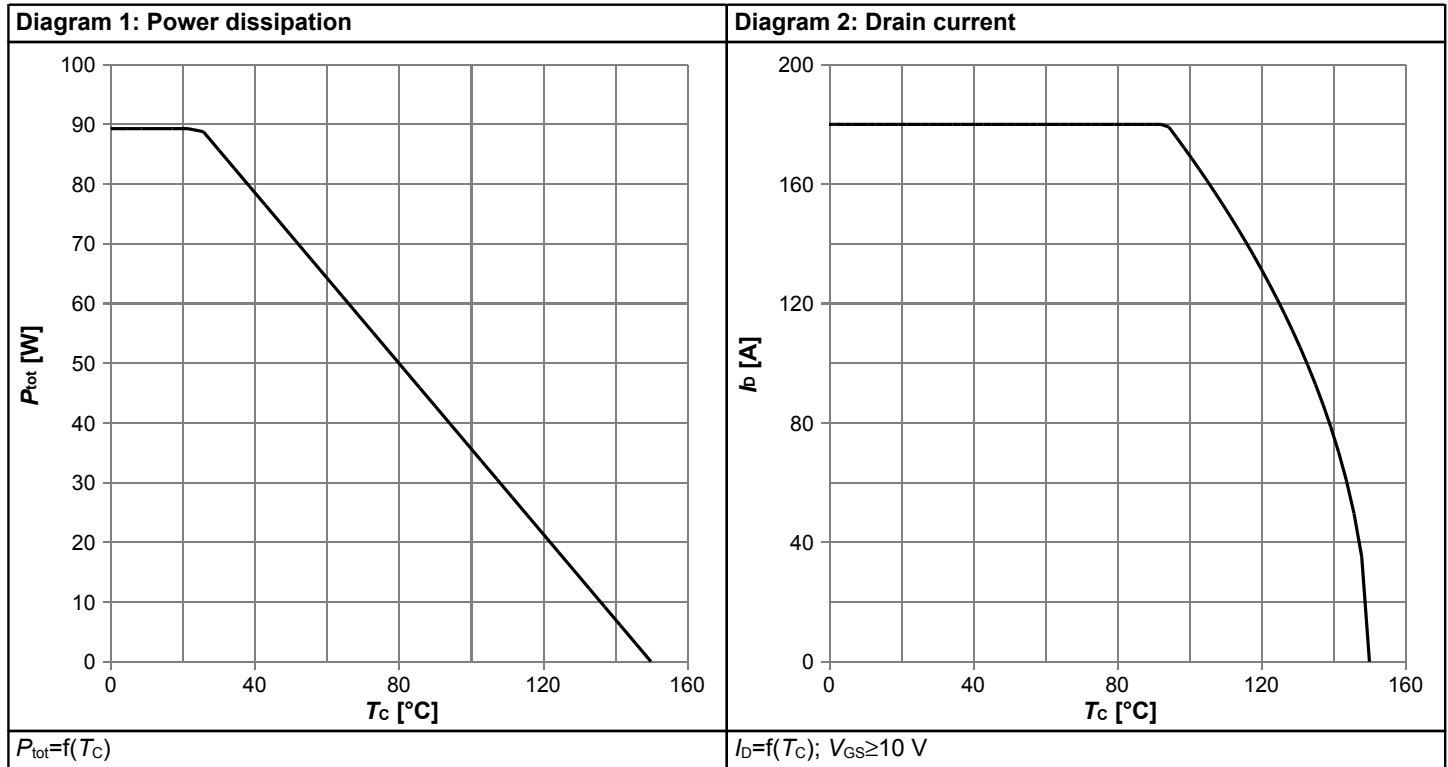
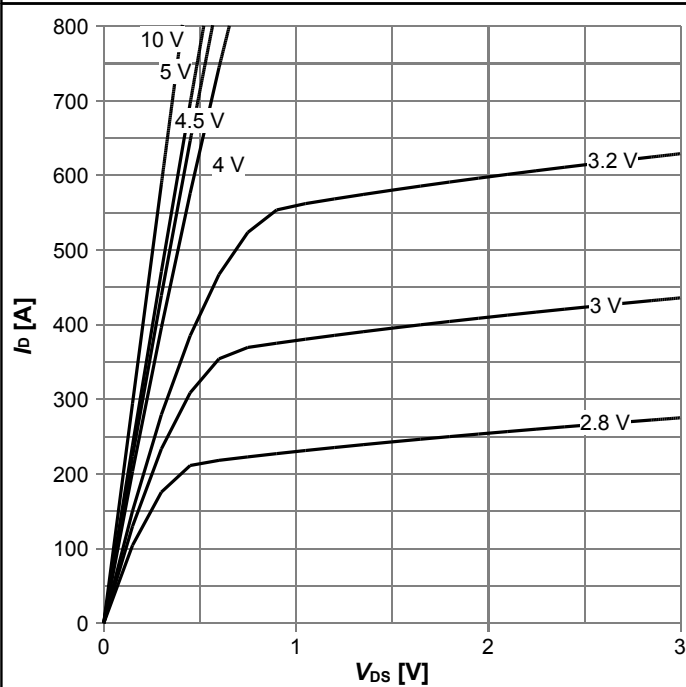
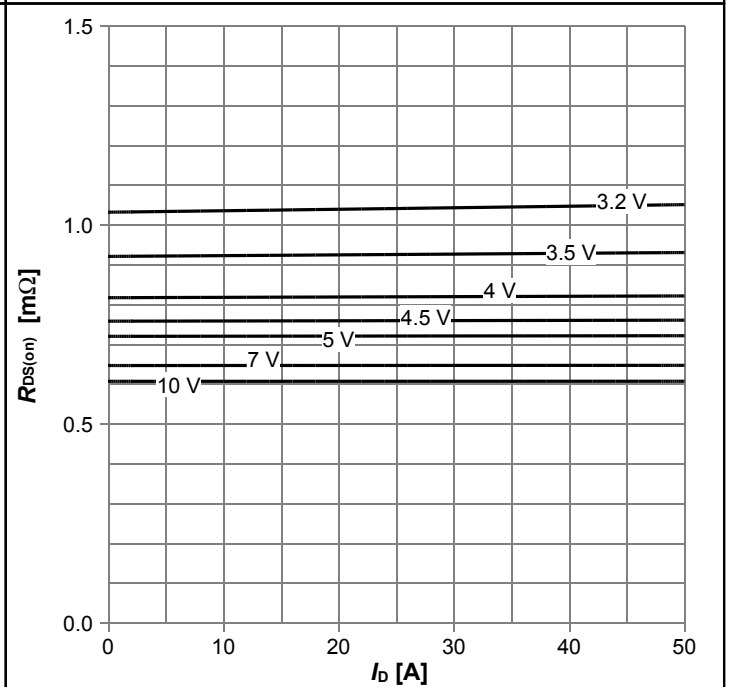


Diagram 5: Typ. output characteristics



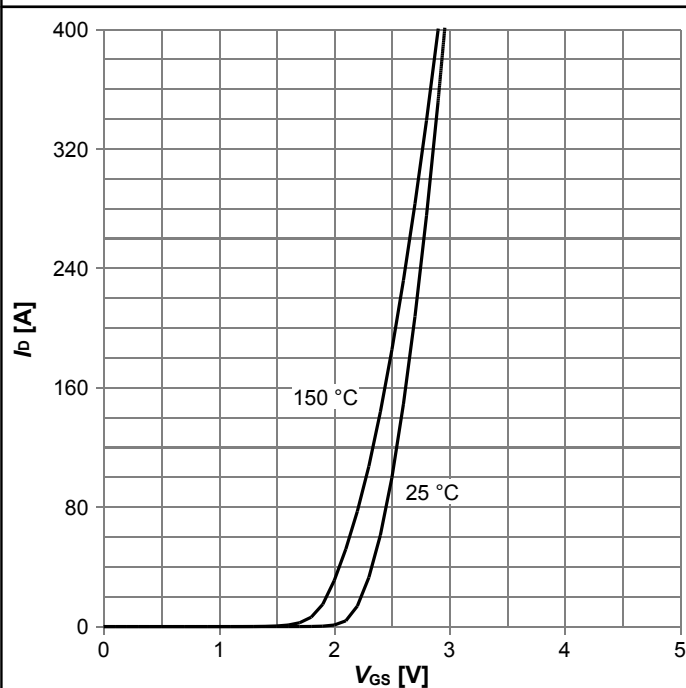
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



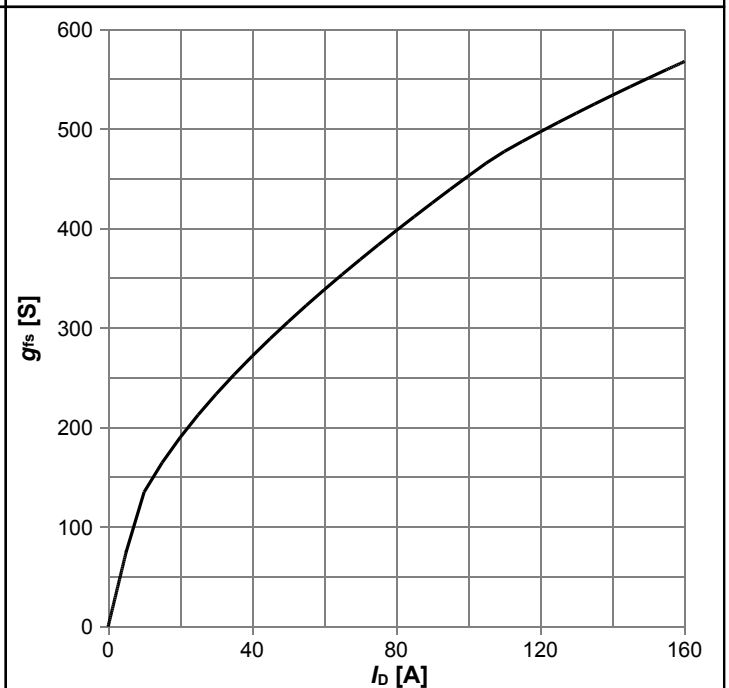
$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



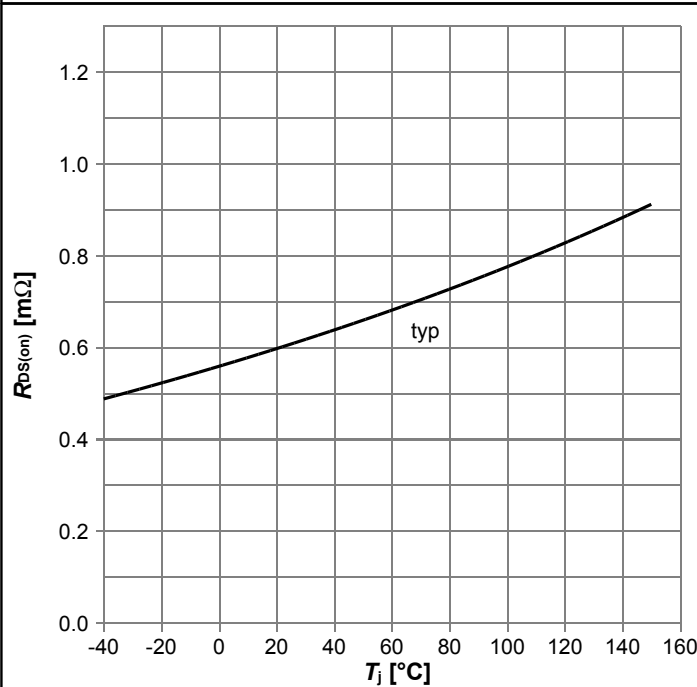
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. forward transconductance



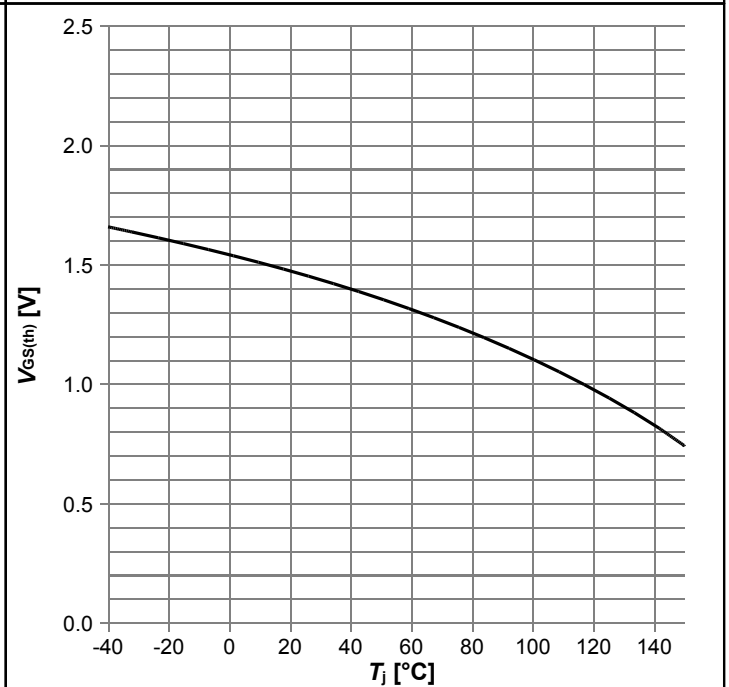
$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



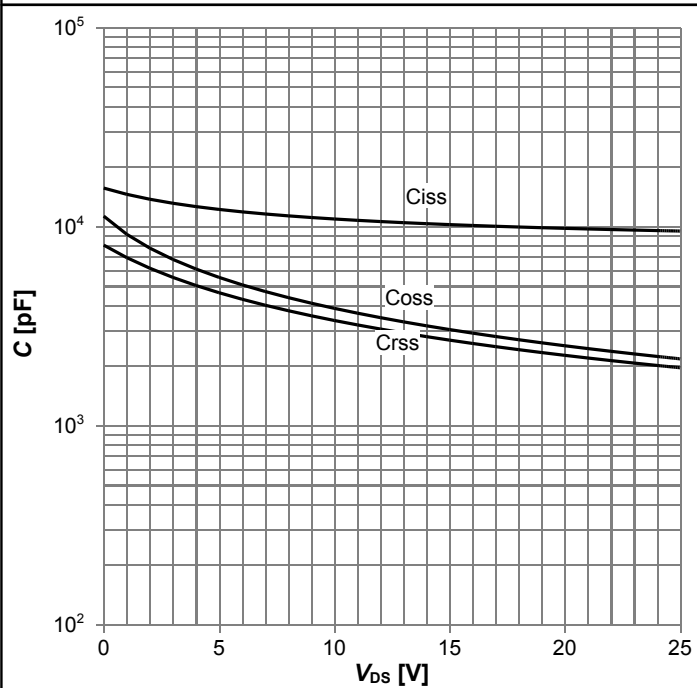
$R_{DS(on)}=f(T_j)$; $I_D=30\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



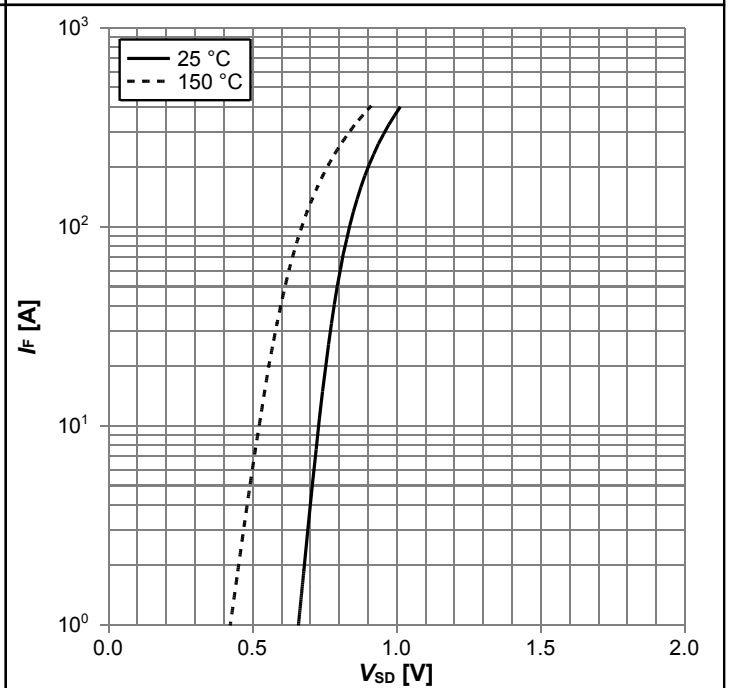
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=250\ \mu\text{A}$

Diagram 11: Typ. capacitances



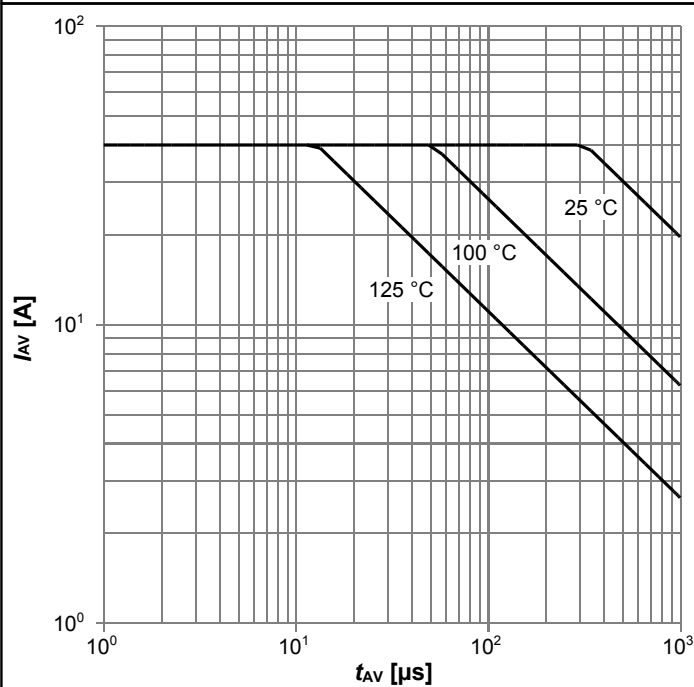
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



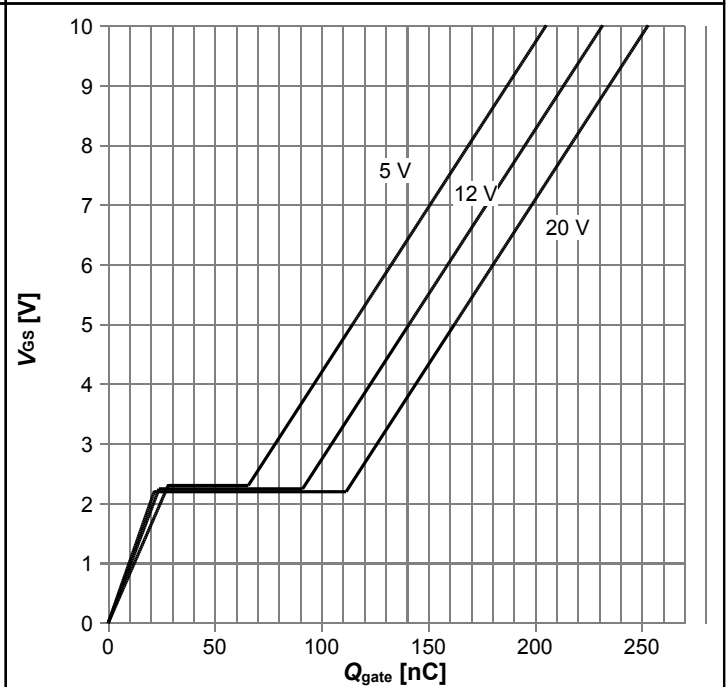
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



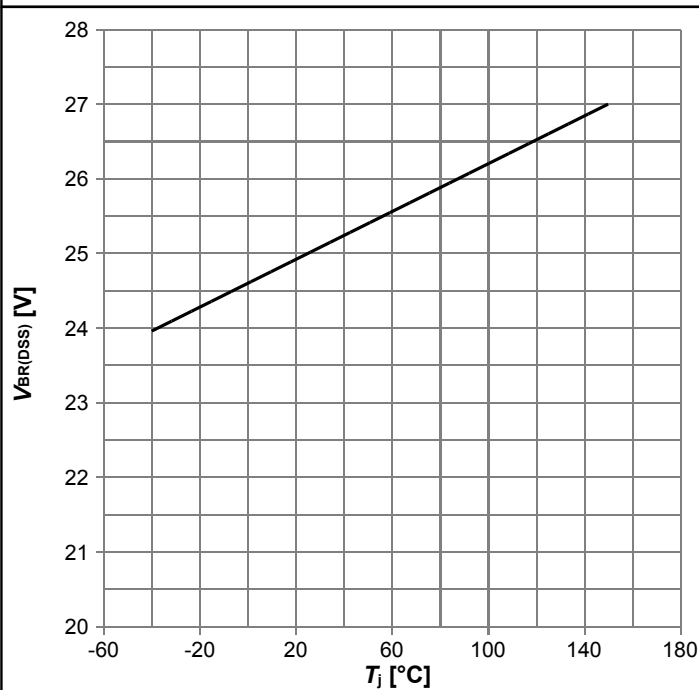
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



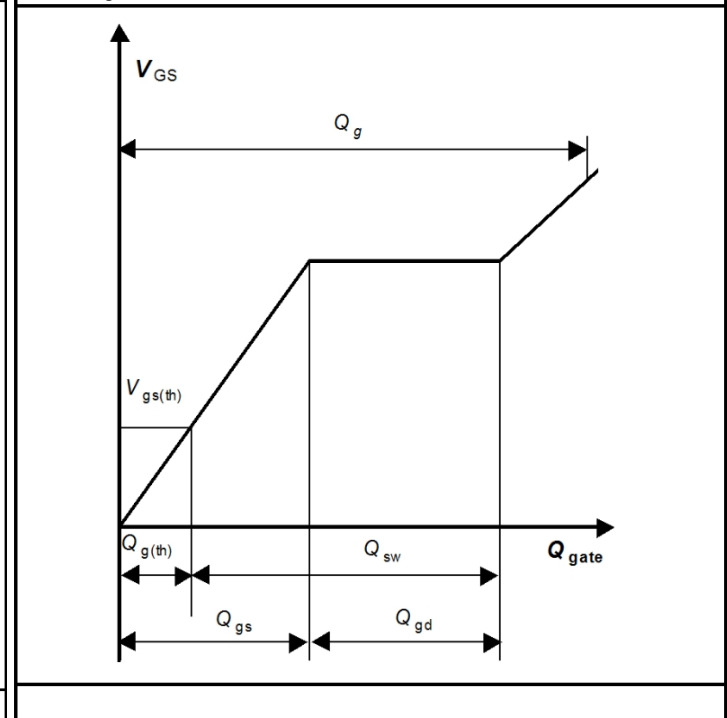
$V_{GS}=f(Q_{gate}); I_D=30 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



6 Package Outlines

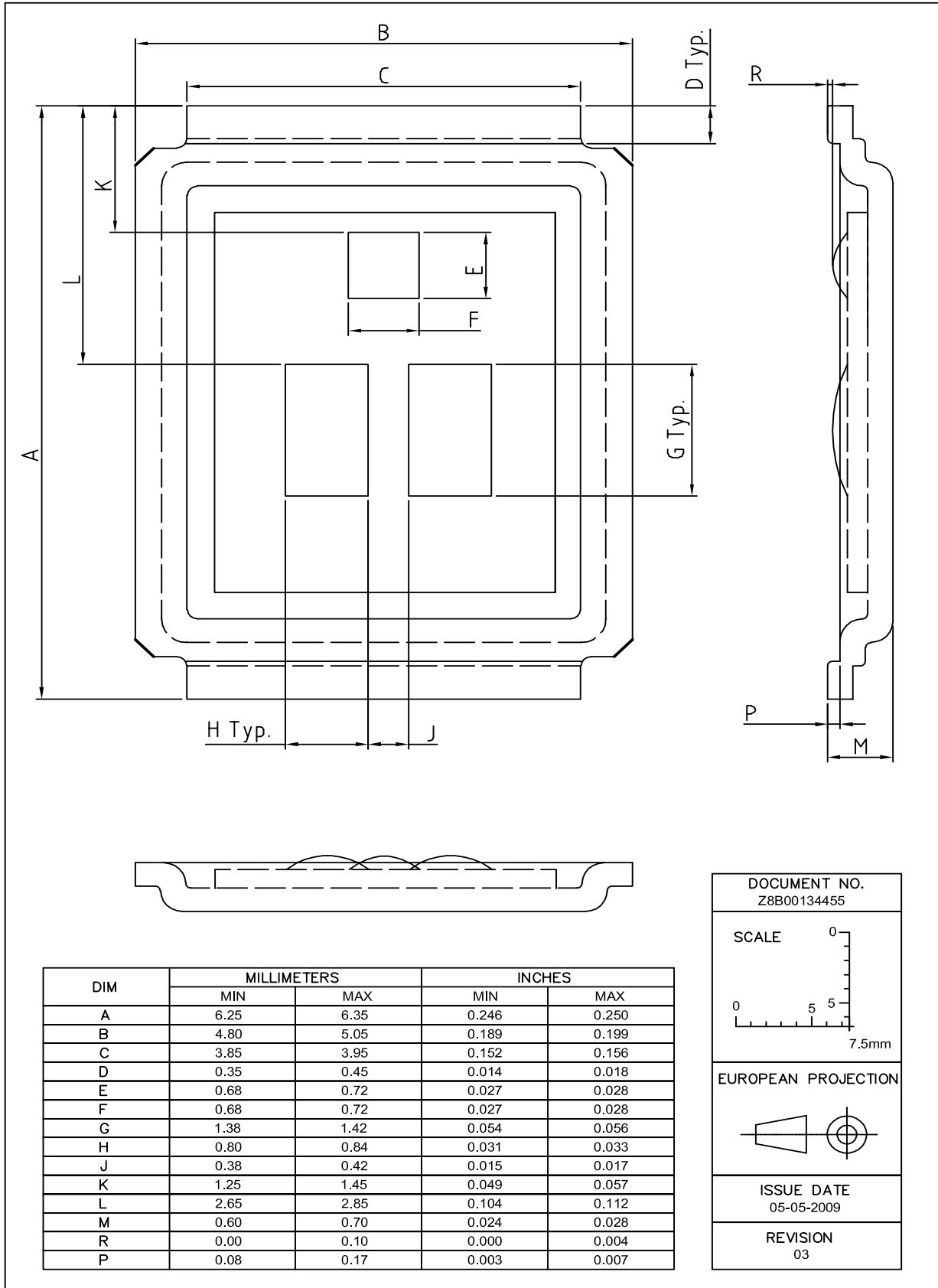


Figure 1 Outline MG-WDSO-2, dimensions in mm/inches

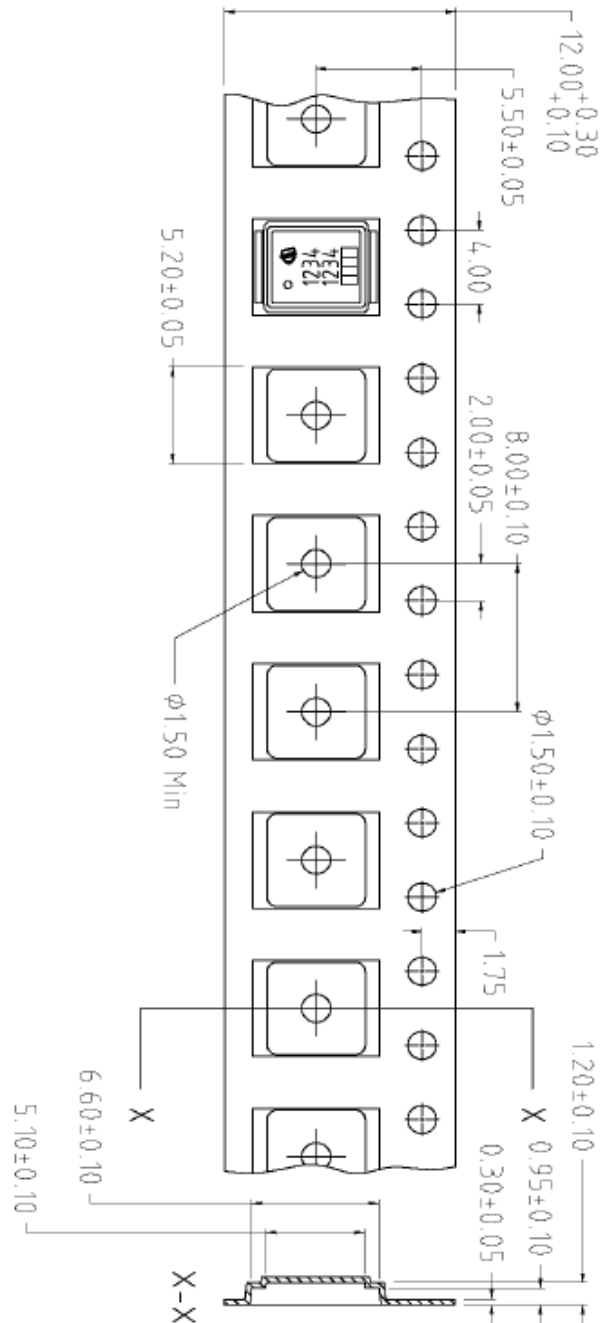
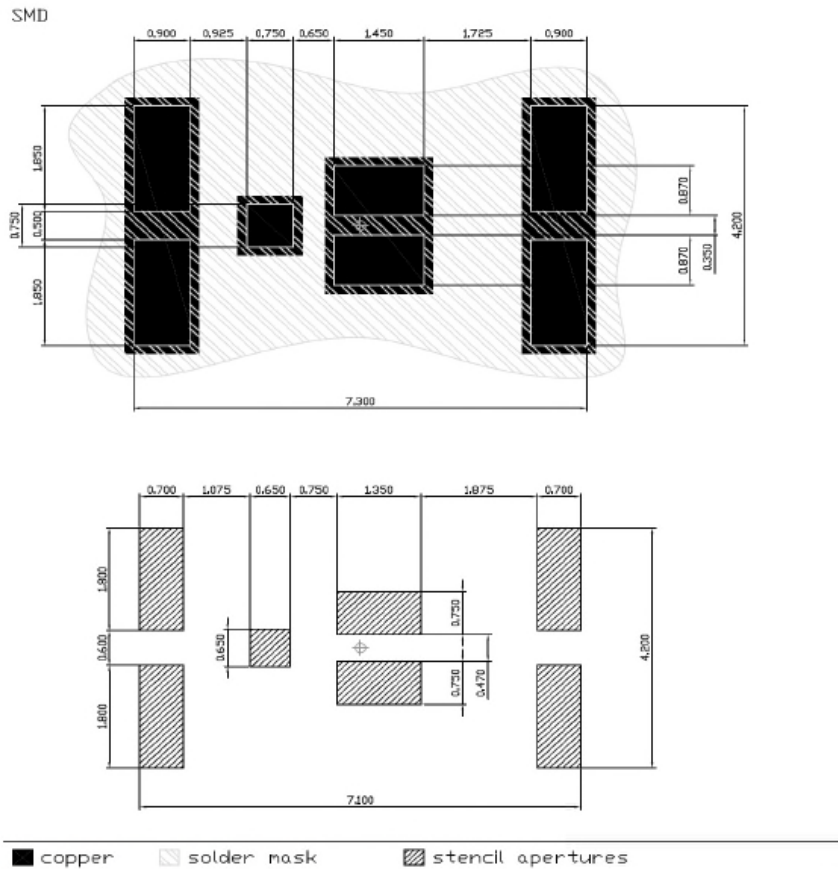


Figure 2 Outline Tape CanPAK MX, dimensions in mm



Dimensions in mm
Recommended stencil thickness 150 µm

Marking Layout

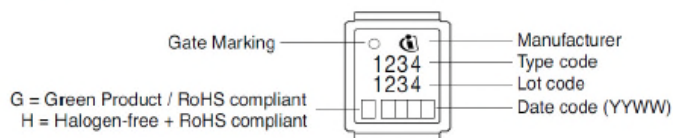


Figure 3 Outline Boardpads and apertures CanPAK MX, dimensions in mm

Revision History

BSB008NE2LX

Revision: 2015-01-20, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-01-20	Release of final version

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