SIEMENS

Microcomputer Components

16-Bit CMOS Single-Chip Microcontroller

C164CI

Data Sheet 02.98 Preliminary

http://www.siemens.de/Semiconductor/

C164CI **Revision History:**	**1998-02 Preliminary**
Previous Releases:	04.97 (Advance Information)
Page	**Subjects**
3, 4	Alternate functions for P5 added.
25...30	Register Table updated.
32, 33	I_{P6H} and I_{P6L} removed.
33, 34	Supply current specification improved.
33, 34	Idle supply current specification I_{IDO} improved. (Referring to Revision 11.97)
39, 40	ADC specification improved.
49, 50	Description for $\overline{\text{READY}}$ removed.
–	“AC Characteristics Demultiplexed Bus” removed.
–	“AC Characteristics External Bus Arbitration” removed.

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SIEMENS

C16x-Family of
High-Performance CMOS 16-Bit Microcontrollers

C164CI

Preliminary
C164CI 16-Bit Microcontroller

- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- 500 ns Multiplication (16 × 16 bit), 1 µs Division (32/16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Clock Generation via On-Chip PLL or via Direct or Prescaled Clock Input
- Up to 4 MBytes Linear Address Space for Code and Data
- 2 KByte On-Chip Internal RAM (IRAM)
- 64 KByte On-Chip OTP (C164CI-8EM) or ROM (C164CI-8RM)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-Bit or 16-Bit External Data Bus
- Multiplexed External Address/Data Bus
- Four optional Chip Select Signals $\overline{CS0}$ - $\overline{CS3}$
- 1024 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes with Flexible Power Management
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 32 Interrupt sources
- 8-Channel 10-bit A/D Converter with 9.7 µs Conversion Time (8.2 µs min.)
- 8-Channel 16-bit General Purpose Capture/Compare Unit (CAPCOM2)
- Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
- Two Serial Channels (Synchronous/Asynchronous and High-Speed Synchronous)
- Multi-Functional General Purpose Timer Unit with three 16-bit Timers
- On-Chip Full-CAN Interface (V2.0B active) with 15 Message Objects and Basic CAN Feature
- Up to 59 General Purpose I/O Lines
- Programmable Watchdog Timer and Oscillator Watchdog
- On-Chip Real Time Clock
- Ambient temperature range -40 to 125 °C
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 80-Pin MQFP Package, 0.65 mm pitch

This document describes the **SAF-C164CI-8EM** and the **SAK-C164CI-8EM**.
For simplicity all versions are referred to by the term **C164CI** throughout this document.

Introduction

The C164CI is a new low cost derivative of the Siemens C166 Family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 8 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. It also provides on-chip ROM or OTP and clock generation via PLL. The C164CI derivative is especially suited for cost sensitive applications.

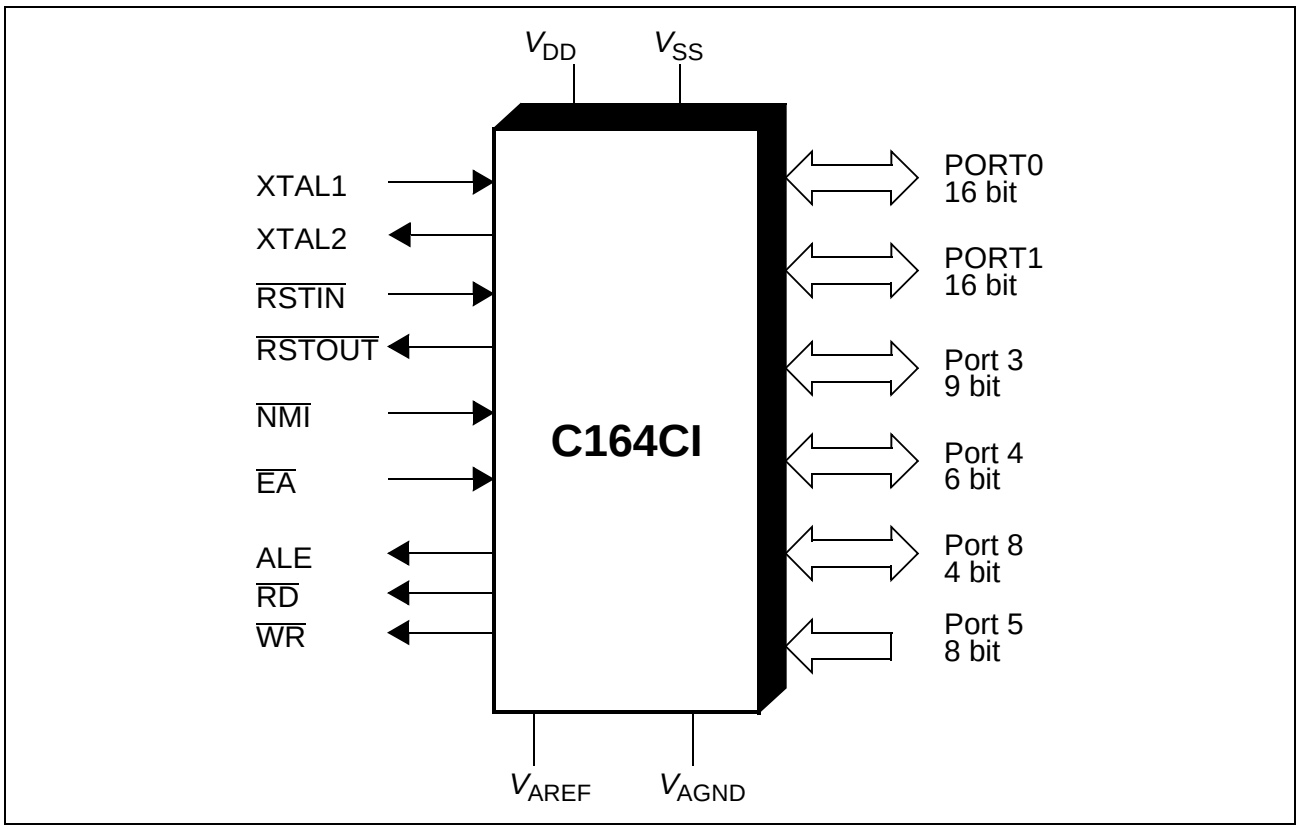


Figure 1
Logic Symbol

Ordering Information

The ordering code for Siemens microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, ie. its function set
- the specified temperature range
- the package
- the type of delivery.

For the available ordering codes for the C164CI please refer to the
„**Product Information Microcontrollers**“, which summarizes all available microcontroller variants.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

Pin Configuration
(top view)

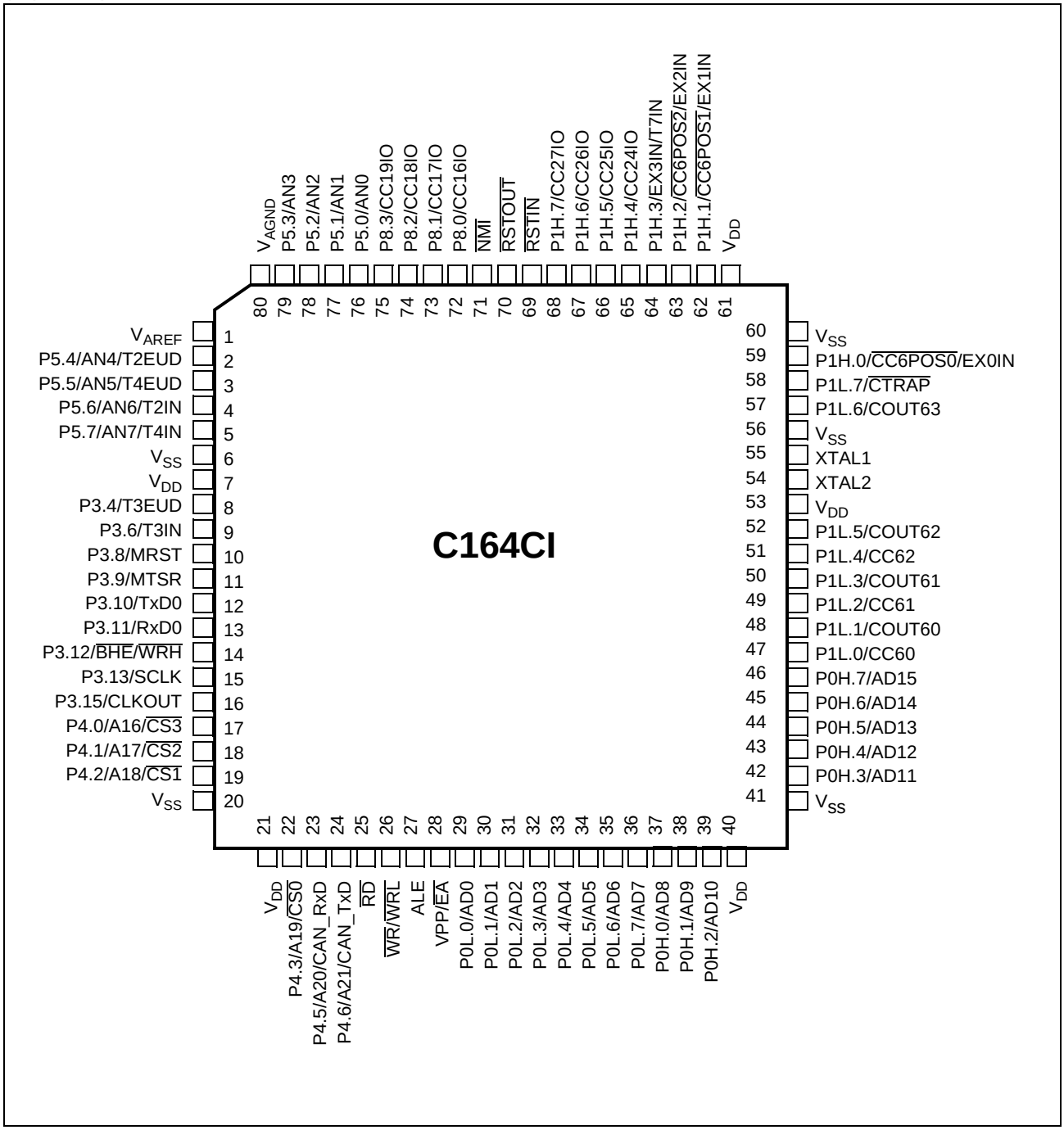


Figure 2

Pin Definitions and Functions

Symbol	Pin Number	Input (I) Output (O)	Function
P5.0 – P5.7	76 - 79, 2 - 5	I I I	Port 5 is a 8-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as the (up to 8) analog input channels for the A/D converter, where P5.x equals ANx (Analog input channel x). The following pins of Port 5 also serve as timer inputs: P5.4 T2EUD GPT1 Timer T2 Ext.Up/Down Ctrl.Input P5.5 T4EUD GPT1 Timer T4 Ext.Up/Down Ctrl.Input P5.6 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture P5.7 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture
P3.4, P3.6, P3.8 – P3.13, P3.15	8, 9, 10 – 15, 16	I/O I/O I/O I/O I/O	Port 3 is a 9-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 3 pins also serve for alternate functions: P3.4 T3EUD GPT1 Timer T3 Ext.Up/Down Ctrl.Input P3.6 T3IN GPT1 Timer T3 Count/Gate Input P3.8 MRST SSC Master-Rec./Slave-Transmit I/O P3.9 MTSR SSC Master-Transmit/Slave-Rec. O/I P3.10 TXD0 ASC0 Clock/Data Output (Asyn./Syn.) P3.11 RXD0 ASC0 Data Input (Asyn.) or I/O (Syn.) P3.12 $\overline{BHE}$ Ext. Memory High Byte Enable Signal, $\overline{WRH}$ Ext. Memory High Byte Write Strobe P3.13 SCLK SSC Master Clock Outp./Slave Cl. Inp. P3.15 CLKOUT System Clock Output (=CPU Clock)
P4.0 – P4.3 P4.5 – P4.6	17 - 19, 22, 23 - 24	I/O I/O I/O I/O	Port 4 is a 6-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 can be used to output the segment address lines: P4.0 A16 Least Significant Segment Addr. Line $\overline{CS3}$ Chip Select 3 Output ... ... P4.3 A19 Segment Address Line $\overline{CS0}$ Chip Select 0 Output P4.5 A20 Segment Address Line, CAN_RxD CAN Receive Data Input P4.6 A21 Most Significant Segment Addr. Line, CAN_TxD CAN Transmit Data Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
$\overline{RD}$	25	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$ / $\overline{WRL}$	26	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
ALE	27	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	28	I	External Access Enable pin. A low level at this pin during and after Reset forces the C164CI to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. **Note:** This pin also accepts the programming voltage for OTP versions of the C164CI.
PORT0: P0L.0 – P0L.7, P0H.0 - P0H.7	29 - 36 37 - 39, 42 - 46	I/O	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address and data (AD) bus. Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 - A15 AD8 - AD15

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function		
PORT1: P1L.0 – P1L.7, P1H.0 - P1H.7		I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 1 pins also serve for alternate functions:		
	47	I/O	P1L.0	CC60	CAPCOM6: Input / Output of Ch. 0
	48	O	P1L.1	COUT60	CAPCOM6: Output of Channel 0
	49	I/O	P1L.2	CC61	CAPCOM6: Input / Output of Ch. 1
	50	O	P1L.3	COUT61	CAPCOM6: Output of Channel 1
	51	I/O	P1L.4	CC62	CAPCOM6: Input / Output of Ch. 2
	52	O	P1L.5	COUT62	CAPCOM6: Output of Channel 2
	57	O	P1L.6	COUT63	Output of 10-bit Compare Channel
	58	I	P1L.7	$\overline{\text{CTRAP}}$	CAPCOM6: Trap Input
			$\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. A low level on this pin switches the compare outputs of the CAPCOM6 unit to the logic level defined by software.		
	59	I	P1H.0	$\overline{\text{CC6POS0}}$	CAPCOM6: Position 0 Input
		I		EX0IN	Fast External Interrupt 0 Input
	62	I	P1H.1	$\overline{\text{CC6POS1}}$	CAPCOM6: Position 1 Input
		I		EX1IN	Fast External Interrupt 1 Input
	63	I	P1H.2	$\overline{\text{CC6POS2}}$	CAPCOM6: Position 2 Input
		I		EX2IN	Fast External Interrupt 2 Input
	64	I	P1H.3	EX3IN	Fast External Interrupt 3 Input
		I		T7IN	CAPCOM2: Timer T7 Count Input
	65	I	P1H.4	CC24IO	CAPCOM2: CC24 Capture Input
	...	...	...	...	...
	68	I	P1H.7	CC27IO	CAPCOM2: CC27 Capture Input
XTAL1	55	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator		
XTAL2	54	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.		
$\overline{\text{RSTIN}}$	69	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the C164CI. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is pulled low for the duration of the internal reset sequence upon a software or WDT reset. [1]		

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
$\overline{\text{RSTOUT}}$	70	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	71	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C164CI to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
P8.0 – P8.3	72 - 75	I/O I/O	Port 8 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 8 pins also serve for alternate functions: P8.0 CC16IO CAPCOM2: CC16 Cap.-In/Comp.Out ... ... P8.3 CC19IO CAPCOM2: CC19 Cap.-In/Comp.Out
	72 ... 75	I/O ... I/O	
V_{AREF}	1	-	Reference voltage for the A/D converter.
V_{AGND}	80	-	Reference ground for the A/D converter.
V_{DD}	7, 21, 40, 53, 61	-	Digital Supply Voltage: + 3 V / + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode
V_{SS}	6, 20, 41, 56, 60	-	Digital Ground.

[1] The following behaviour differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT.
- After a reset bit BDRSTEN is cleared.
- Bit WDTR will always be '0', even after a watchdog timer reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.

Functional Description

The C164CI is a low cost downgrade of the high performance microcontroller C167CR with OTP or internal ROM, reduced peripheral functionality and a high performance Capture Compare Unit with an additional functionality.

The architecture of the C164CI combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C164CI.

Note: All time specifications refer to a CPU clock of 20 MHz
(see definition in the AC Characteristics section).

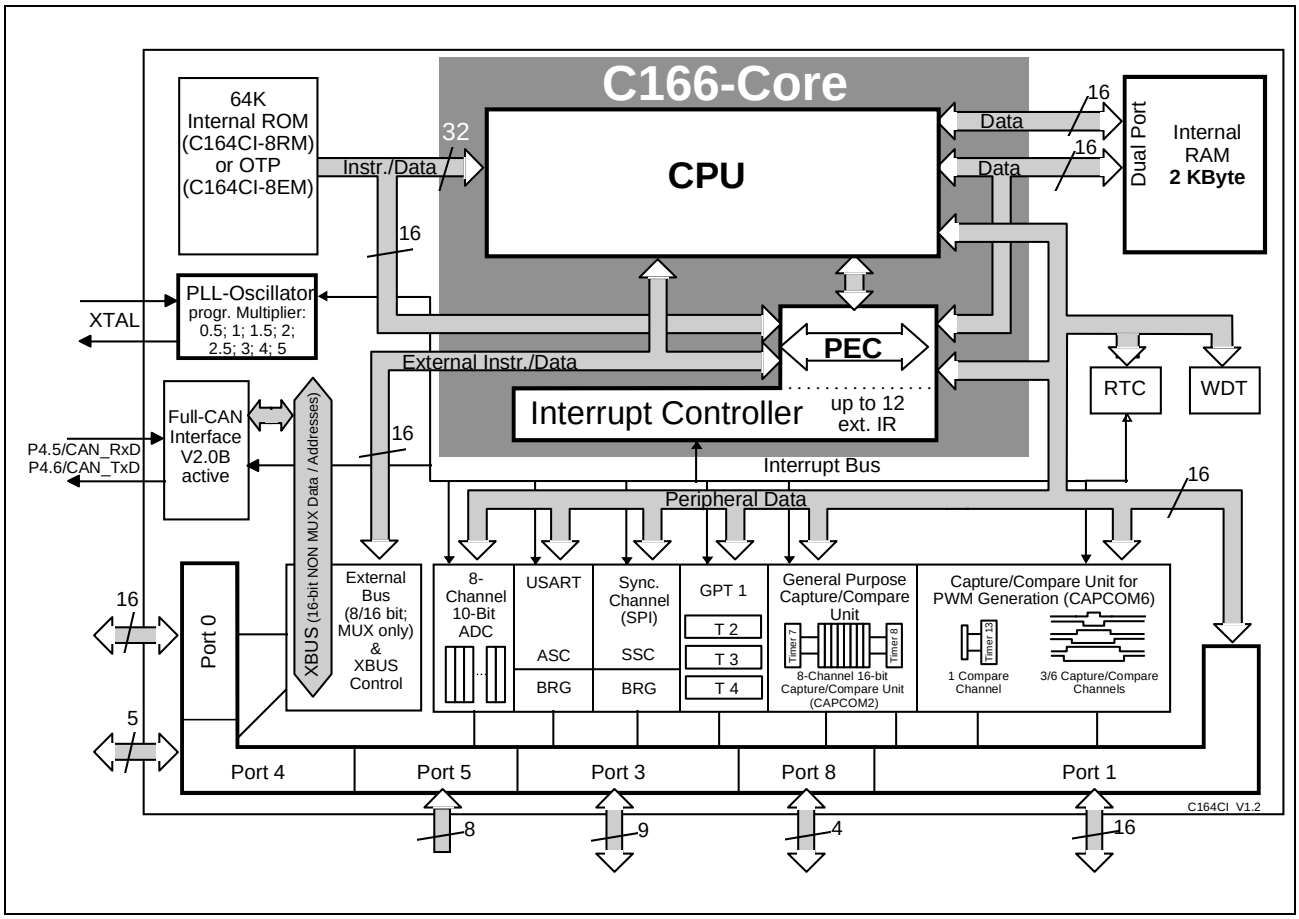


Figure 3
Block Diagram

Memory Organization

The memory space of the C164CI is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 4 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C164CI incorporates 64 KByte of on-chip ROM or OTP memory for code or constant data. The OTP memory can be programmed by the CPU itself (in system, eg. during booting) or directly via an external interface (eg. before assembly). The programming time is approx. 100 µsec per word. An external programming voltage V_{PP} = 11.5 V must be supplied for this purpose (via pin $\overline{EA}$).

2 KBytes of on-chip Internal RAM are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2 * 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C16x family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 4 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of two different external memory access modes, which are as follows:

– 16-/18-/20-/22-bit Addresses, 16-bit Data, Multiplexed

– 16-/18-/20-/22-bit Addresses, 8-bit Data, Multiplexed

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which allow to access different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

For applications which require less than 4 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. It outputs all 6 address lines, if an address space of 4 MBytes is used.

Note: When the on-chip CAN Module is to be used the segment address output on Port 4 must be limited to 4 bits (ie. A19...A16) in order to enable the alternate function of the CAN interface pins.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C164CI's instructions can be executed in just one machine cycle which requires 100 ns at 20-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

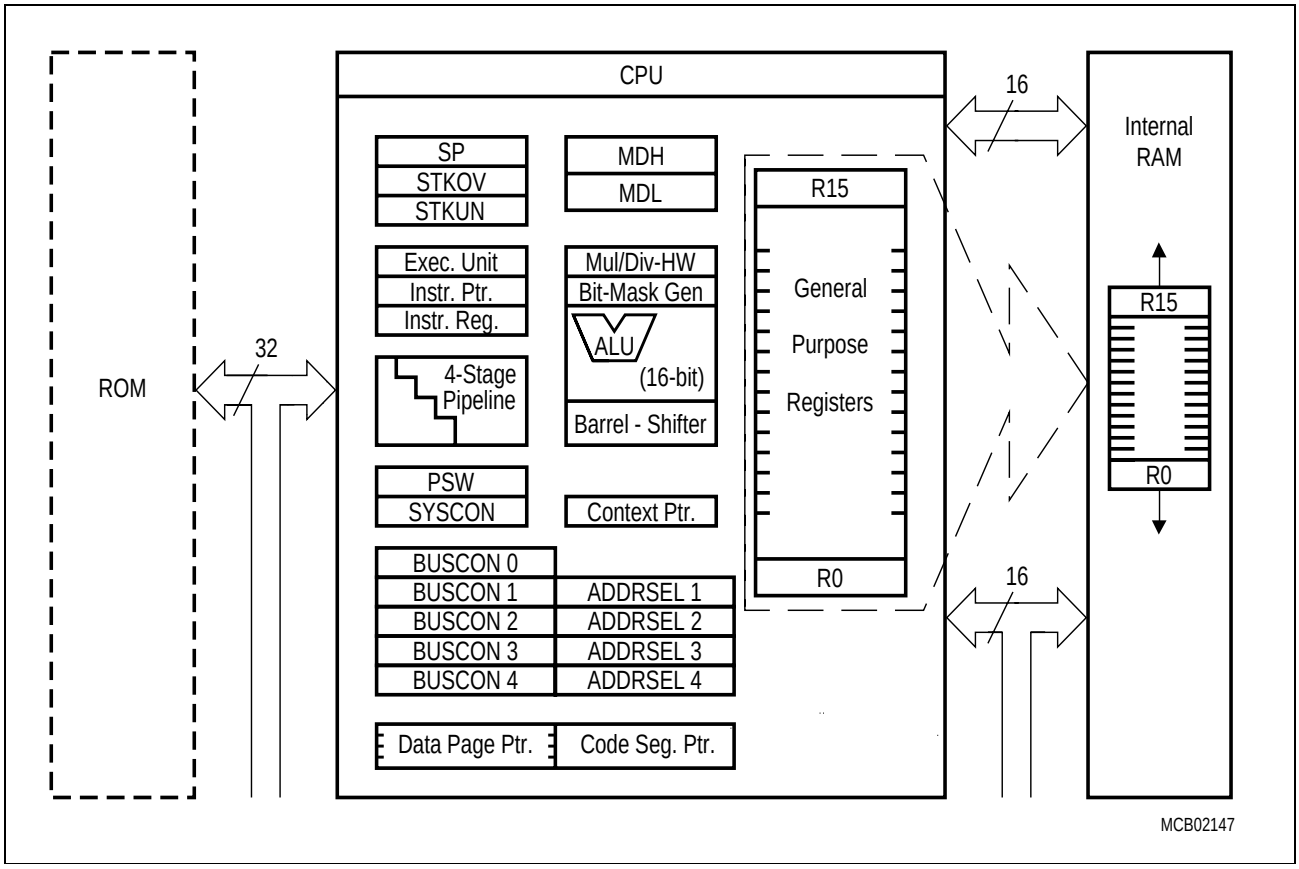


Figure 4
CPU Block Diagram

The CPU disposes of an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at a time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 2048 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C164CI instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 250 ns to 600 ns (in case of internal program execution), the C164CI is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C164CI supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C164CI has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible C164CI interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
Fast External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
Fast External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
Fast External Interrupt 2	CC10IE	CC10IE	CC10INT	$00'0068_H$	$1A_H$
Fast External Interrupt 3	CC11IE	CC11IE	CC11INT	$00'006C_H$	$1B_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0	28_H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4	29_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC426NT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Timer 7	T7IR	T7IE	T7INT	$00'00F4_H$	$3D_H$
CAPCOM Timer 8	T8IR	T8IE	T8INT	$00'00F8_H$	$3E_H$
CAPCOM 6 Interrupt	CC6IR	CC6IE	CC6INT	$00'00FC_H$	$3F_H$
XPER Node 0 Int / CAN	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
XPER Node 3 Int / PLL / T14	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
CAPCOM 6 Timer 12	T12IR	T12IE	T12INT	$00'0134_H$	$4D_H$
CAPCOM 6 Timer 13	T13IR	T13IE	T13INT	$00'0138_H$	$4E_H$
CAPCOM 6 Emergency	CC6EIR	CC6EIE	CC6EINT	$00'013C_H$	$4F_H$

The C164CI also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Exception Condition	**Trap Flag**	**Trap Vector**	**Vector Location**	**Trap Number**	**Trap Priority**
Reset Functions:					
Hardware Reset		RESET	$00'0000_H$	00_H	III
Software Reset		RESET	$00'0000_H$	00_H	III
Watchdog Timer Overflow		RESET	$00'0000_H$	00_H	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	$00'0008_H$	02_H	II
Stack Overflow	STKOF	STOTRAP	$00'0010_H$	04_H	II
Stack Underflow	STKUF	STUTRAP	$00'0018_H$	06_H	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	$00'0028_H$	$0A_H$	I
Protected Instruction Fault	PRTFLT	BTRAP	$00'0028_H$	$0A_H$	I
Illegal Word Operand Access	ILLOPA	BTRAP	$00'0028_H$	$0A_H$	I
Illegal Instruction Access	ILLINA	BTRAP	$00'0028_H$	$0A_H$	I
Illegal External Bus Access	ILLBUS	BTRAP	$00'0028_H$	$0A_H$	I
Reserved			$[2C_H – 3C_H]$	$[0B_H – 0F_H]$	
Software Traps TRAP Instruction			Any $[00'0000_H –$ $00'01FC_H]$ in steps of 4_H	Any $[00_H – 7F_H]$	Current CPU Priority

The Capture/Compare Unit CAPCOM2

The general purpose CAPCOM2 unit supports generation and control of timing sequences on up to 8 channels with a maximum resolution of 400 ns (at 20 MHz system clock). The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.
Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/ compare register array.
Each dual purpose capture/compare register, which may be individually allocated to either CAPCOM timer and programmed for capture or compare function, has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘capture’d) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Compare Modes	**Function**
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible. Registers CC16 & CC24 → pin CC16IO Registers CC17 & CC25 → pin CC17IO Registers CC18 & CC26 → pin CC18IO Registers CC19 & CC27 → pin CC19IO

The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one 10-bit compare channel.
In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions. The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.
In capture mode the contents of compare timer 12 is stored in the capture registers upon a signal transition at pins CCx.
For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer 12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).
Compare timers 12 (16-bit) and 13 (10-bit) are free running timers which are clocked by the prescaled CPU clock.

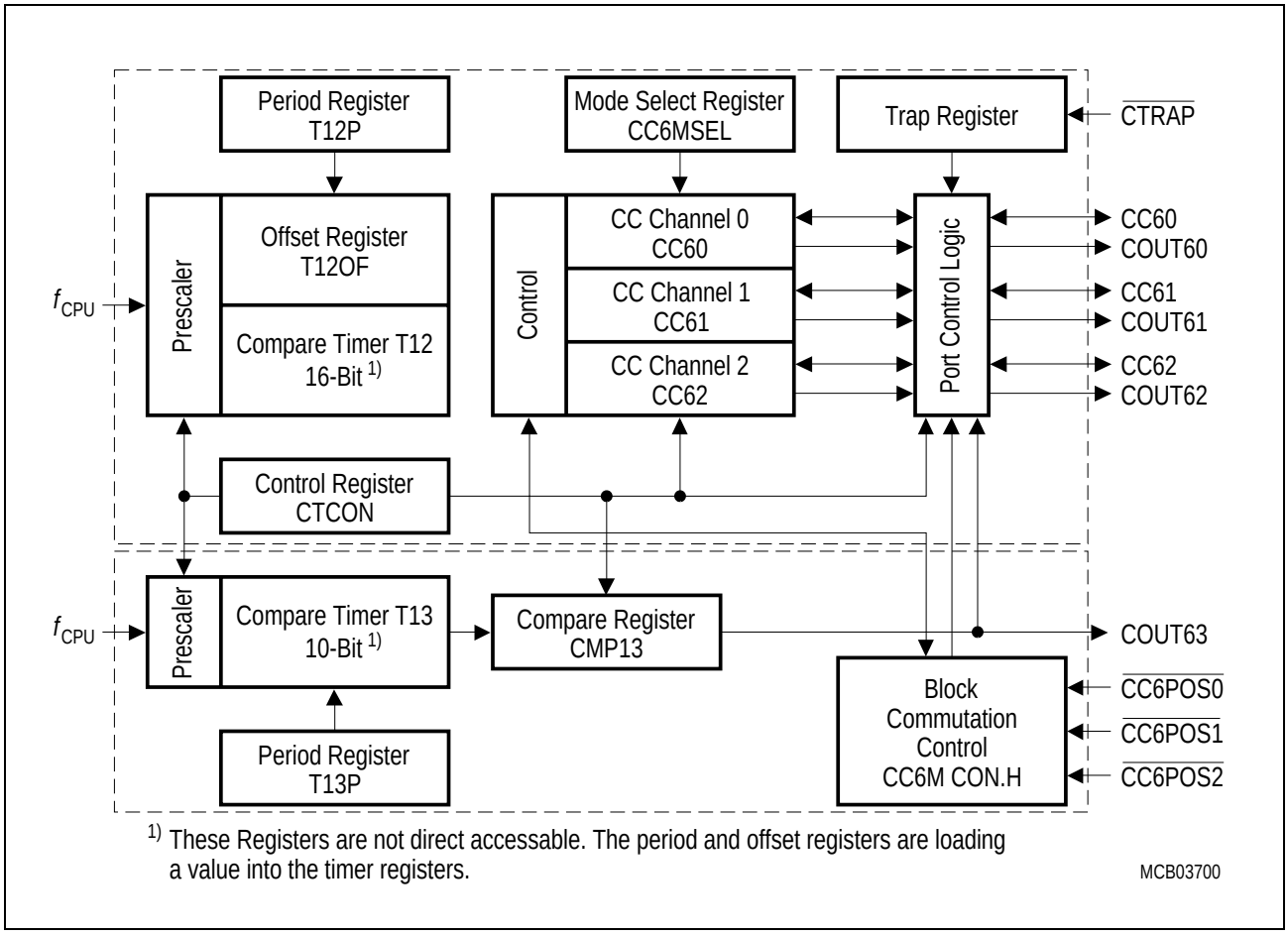


Figure 5
CAPCOM6 Block Diagram

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates three 16-bit timers. Each timer may operate independently in a number of different modes, or may be concatenated with another timer.

Timer T3 can be configured for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. Timers T2 and T4 can only be operated in timer mode.

In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes the associated port pin (T3IN) serves as gate or clock input. The maximum resolution of the timers is 400 ns (@ 20 MHz CPU clock).

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on pin T3EUD for T3 to facilitate eg. position tracking.

In Incremental Interface Mode timer T3 can be directly connected to the incremental position sensor signals A and B via the respective inputs T3IN and T3EUD. Direction and count signals are internally derived from these two input signals, so the contents of timer T3 corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/ underflow. The state of this latch may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload registers for timer T3. When used as reload registers, timers T2 and T4 are stopped. Timer T3 is reloaded with the contents of T2 or T4 triggered by a selectable state transition of its toggle latch T3OTL.

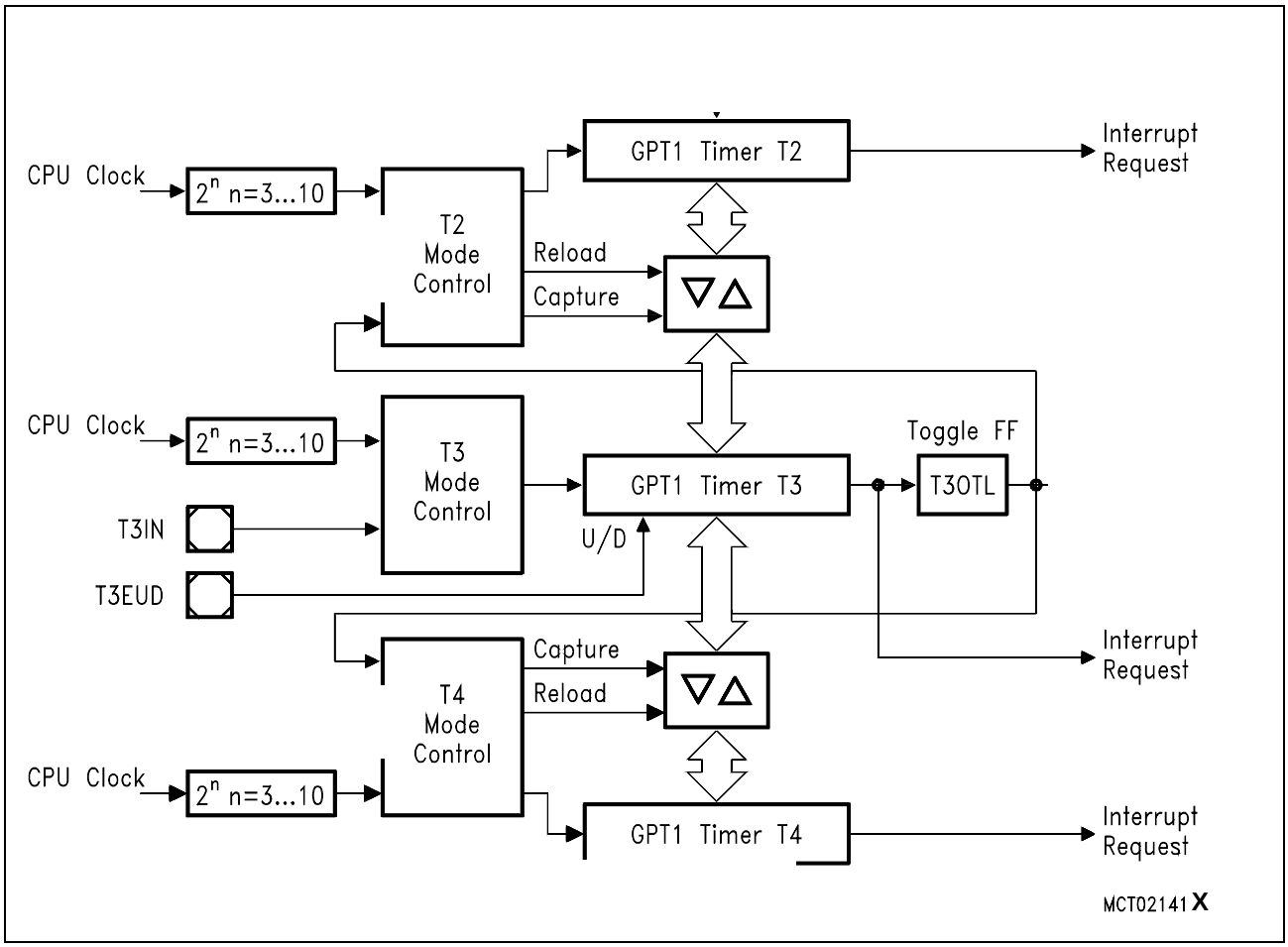


Figure 6
GPT Block Diagram

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 µs and 420 ms can be monitored (@ 20 MHz). The default Watchdog Timer interval after reset is 6.55 ms (@ 20 MHz).

Real Time Clock

The Real Time Clock (RTC) module of the C164CI consists of a chain of 3 divider blocks, a fixed 8-bit divider, the reloadable 16-bit timer T14 and the 32-bit RTC timer (accessible via registers RTCH and RTCL). The RTC module is directly clocked with the on-chip oscillator frequency divided by 32 via a separate clock driver and is therefore independent from the selected clock generation mode of the C164CI. All timers count up.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt
- 48-bit timer for long term measurements

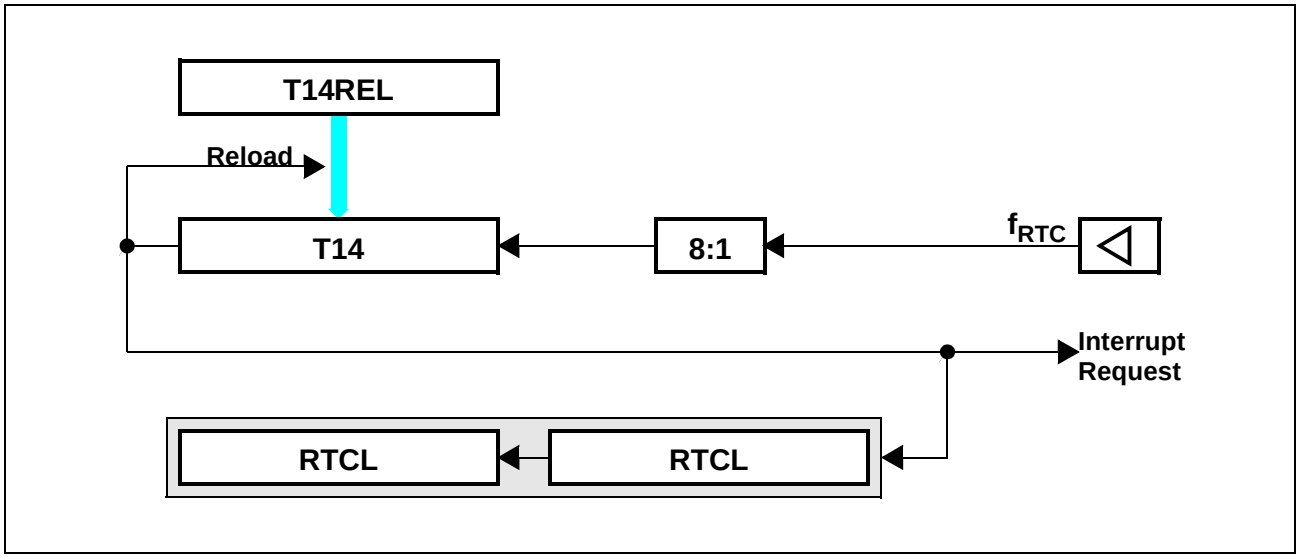


Figure 6-1
RTC Block Diagram

Note: The register associated with the RTC are not effected by a reset in order to maintain the correct system time even when intermediate resets are executed.

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 8 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 8 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C164CI supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (eg. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/ Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Siemens 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 625 KBaud and half-duplex synchronous communication at up to 2.5 MBaud @ 20 MHz CPU clock.
A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).
In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 5 Mbaud @ 20 MHz CPU clock. It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 3 separate interrupt vectors are provided.
The SSC transmits or receives characters of 2...16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

CAN-Module

The integrated CAN-Module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), ie. the on-chip CAN-Module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

The module provides Full CAN functionality on up to 15 message objects. Message object 15 may be configured for Basic CAN functionality. Both modes provide separate masks for acceptance filtering which allows to accept a number of identifiers in Full CAN mode and also allows to disregard a number of identifiers in Basic CAN mode. All message objects can be updated independent from the other objects and are equipped for the maximum message length of 8 bytes.

The bit timing is derived from the XCLK and is programmable up to a data rate of 1 MBaud. The CAN-Module uses two pins of Port 4 to interface to a bus transceiver.

Note: When the CAN interface is to be used the segment address output on Port 4 must be limited to 4 bits, ie. A19...A16. This is necessary to enable the alternate function of the CAN interface pins.

Parallel Ports

The C164CI provides up to 59 IO lines which are organized into five input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of two IO ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them.
PORT0 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A21/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.

Ports P1L, P1H and P8 are associated with the capture inputs or compare outputs of the CAPCOM units and/or serve as external interrupt inputs.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$ and the system clock output (CLKOUT).
Port 5 is used for the analog input channels to the A/D converter.

All port lines that are not used for these alternate functions may be used as general purpose IO lines.

Instruction Set Summary

The table below lists the instructions of the C164CI in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“C16x Family Instruction Set Manual”**.

This document also provides a detailled description of each instruction.

Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack und update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Special Function Registers Overview

The following table lists all SFRs which are implemented in the C164CI in alphabetical order. **Bit-addressable** SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Name	Physical Address	8-Bit Address	Description	Reset Value
ADCIC b	$FF98_H$	CC_H	A/D Converter End of Conversion Interrupt Control Register	0000_H
ADCON b	$FFA0_H$	$D0_H$	A/D Converter Control Register	0000_H
ADEIC b	$FF9A_H$	CD_H	A/D Converter Overrun Error Interrupt Control Register	0000_H
ADDAT	$FEA0_H$	50_H	A/D Converter Result Register	0000_H
ADDAT2	$F0A0_H$ **E**	50_H	A/D Converter 2 Result Register	0000_H
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	0000_H
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
C1BTR	$EF04_H$ **X**	---	CAN Bit Timing Register	$UUUU_H$
C1CSR	$EF00_H$ **X**	---	CAN Control / Status Register	$XX01_H$
C1GMS	$EF06_H$ **X**	---	CAN Global Mask Short	$UFUU_H$
C1IR	$EF02_H$ **X**	---	CAN Interrupt Register	XX_H
C1LGML	$EF0A_H$ **X**	---	CAN Lower Global Mask Long	$UUUU_H$
C1LMLM	$EF0E_H$ **X**	---	CAN Lower Mask of Last Message	$UUUU_H$
C1UGML	$EF08_H$ **X**	---	CAN Upper Global Mask Long	$UUUU_H$
C1UMLM	$EF0C_H$ **X**	---	CAN Upper Mask of Last Message	$UUUU_H$
CC10IC b	$FF8C_H$	$C6_H$	CAPCOM Register 10 Interrupt Control Register	0000_H
CC11IC b	$FF8E_H$	$C7_H$	CAPCOM Register 11 Interrupt Control Register	0000_H

Name	Physical Address	8-Bit Address	Description	Reset Value
CC16	$FE60_H$	30_H	CAPCOM Register 16	0000_H
CC16IC b	$F160_H$ **E**	$B0_H$	CAPCOM Register 16 Interrupt Control Register	0000_H
CC17	$FE62_H$	31_H	CAPCOM Register 17	0000_H
CC17IC b	$F162_H$ **E**	$B1_H$	CAPCOM Register 17 Interrupt Control Register	0000_H
CC18	$FE64_H$	32_H	CAPCOM Register 18	0000_H
CC18IC b	$F164_H$ **E**	$B2_H$	CAPCOM Register 18 Interrupt Control Register	0000_H
CC19	$FE66_H$	33_H	CAPCOM Register 19	0000_H
CC19IC b	$F166_H$ **E**	$B3_H$	CAPCOM Register 19 Interrupt Control Register	0000_H
CC24	$FE70_H$	38_H	CAPCOM Register 24	0000_H
CC24IC b	$F170_H$ **E**	$B8_H$	CAPCOM Register 24 Interrupt Control Register	0000_H
CC25	$FE72_H$	39_H	CAPCOM Register 25	0000_H
CC25IC b	$F172_H$ **E**	$B9_H$	CAPCOM Register 25 Interrupt Control Register	0000_H
CC26	$FE74_H$	$3A_H$	CAPCOM Register 26	0000_H
CC26IC b	$F174_H$ **E**	BA_H	CAPCOM Register 26 Interrupt Control Register	0000_H
CC27	$FE76_H$	$3B_H$	CAPCOM Register 27	0000_H
CC27IC b	$F176_H$ **E**	BB_H	CAPCOM Register 27 Interrupt Control Register	0000_H
CC60	$FE30_H$	18_H	CAPCOM 6 Register 0	0000_H
CC61	$FE32_H$	19_H	CAPCOM 6 Register 1	0000_H
CC62	$FE34_H$	$1A_H$	CAPCOM 6 Register 2	0000_H
CC6EIC b	$F188_H$ **E**	$C4_H$	CAPCOM 6 Emergency Interrupt Control Reg.	0000_H
CC6IC b	$F17E_H$ E	BF_H	CAPCOM 6 Interrupt Control Register	0000_H
CC6MCON b	$FF32_H$	99_H	CAPCOM 6 Mode Control Register	$00FF_H$
CC6MIC b	$FF36_H$	$9B_H$	CAPCOM 6 Mode Interrupt Control Register	0000_H
CC6MSEL	$F036_H$ **E**	$1B_H$	CAPCOM 6 Mode Select Register	0000_H
CC8IC b	$FF88_H$	$C4_H$	CAPCOM Register 8 Interrupt Control Register	0000_H
CC9IC b	$FF8A_H$	$C5_H$	CAPCOM Register 9 Interrupt Control Register	0000_H
CCM4 b	$FF22_H$	91_H	CAPCOM Mode Control Register 4	0000_H
CCM6 b	$FF26_H$	93_H	CAPCOM Mode Control Register 6	0000_H
CMP13	$FE36_H$	$1B_H$	CAPCOM 6 Timer 13 Compare Register	0000_H
CP	$FE10_H$	08_H	CPU Context Pointer Register	$FC00_H$
CSP	$FE08_H$	04_H	CPU Code Segment Pointer Register (8 bits, not directly writeable)	0000_H
CTCON b	$FF30_H$	98_H	CAPCOM 6 Compare Timer Control Register	1010_H

Name	Physical Address	8-Bit Address	Description	Reset Value
DP0H **b**	$F102_H$ **E**	81_H	P0H Direction Control Register	00_H
DP0L **b**	$F100_H$ **E**	80_H	P0L Direction Control Register	00_H
DP1H **b**	$F106_H$ **E**	83_H	P1H Direction Control Register	00_H
DP1L **b**	$F104_H$ **E**	82_H	P1L Direction Control Register	00_H
DP3 **b**	$FFC6_H$	$E3_H$	Port 3 Direction Control Register	0000_H
DP4 **b**	$FFCA_H$	$E5_H$	Port 4 Direction Control Register	00_H
DP8 **b**	$FFD6_H$	EB_H	Port 8 Direction Control Register	00_H
DPP0	$FE00_H$	00_H	CPU Data Page Pointer 0 Register (10 bits)	0000_H
DPP1	$FE02_H$	01_H	CPU Data Page Pointer 1 Register (10 bits)	0001_H
DPP2	$FE04_H$	02_H	CPU Data Page Pointer 2 Register (10 bits)	0002_H
DPP3	$FE06_H$	03_H	CPU Data Page Pointer 3 Register (10 bits)	0003_H
EXICON **b**	$F1C0_H$ **E**	$E0_H$	External Interrupt Control Register	0000_H
EXISEL **b**	$F1DA_H$ **E**	ED_H	External Interrupt Source Select Register	0000_H
IDCHIP	$F07C_H$ **E**	$3E_H$	Identifier	$0A01_H$
IDMANUF	$F07E_H$ **E**	$3F_H$	Identifier	1820_H
IDMEM	$F07A_H$ **E**	$3D_H$	Identifier	$X010_H$
IDPROG	$F078_H$ **E**	$3C_H$	Identifier	$XXXX_H$
ISNC **b**	$F1DE_H$ **E**	EF_H	Interrupt Subnode Control Register	0000_H
LAR	$EFn4_H$ **X**	---	CAN Lower Arbitration Register (msg. **n**)	$UUUU_H$
MCFG	$EFn6_H$ **X**	---	CAN Message Configuration Register (msg. **n**)	UU_H
MCR	$EFn0_H$ **X**	---	CAN Message Control Register (msg. **n**)	$UUUU_H$
MDC **b**	$FF0E_H$	87_H	CPU Multiply Divide Control Register	0000_H
MDH	$FE0C_H$	06_H	CPU Multiply Divide Register – High Word	0000_H
MDL	$FE0E_H$	07_H	CPU Multiply Divide Register – Low Word	0000_H
ODP3 **b**	$F1C6_H$ **E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP8 **b**	$F1D6_H$ **E**	EB_H	Port 8 Open Drain Control Register	00_H
ONES **b**	$FF1E_H$	$8F_H$	Constant Value 1’s Register (read only)	$FFFF_H$
OPAD	$EDC2_H$ **X**	---	OTP Programming Interface Address Register	0000_H
OPCTRL	$EDC0_H$ **X**	---	OTP Programming Interface Control Register	0007_H
OPDAT	$EDC4_H$ **X**	---	OTP Programming Interface Data Register	0000_H
P0H **b**	$FF02_H$	81_H	Port 0 High Register (Upper half of PORT0)	00_H
P0L **b**	$FF00_H$	80_H	Port 0 Low Register (Lower half of PORT0)	00_H
P1H **b**	$FF06_H$	83_H	Port 1 High Register (Upper half of PORT1)	00_H

Name		Physical Address		8-Bit Address	Description	Reset Value
P1L	**b**	$FF04_H$		82_H	Port 1 Low Register (Lower half of PORT1)	00_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (8 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$
P5DIDIS	**b**	$FFA4_H$		$D2_H$	Port 5 Digital Input Disable Register	0000_H
P8	**b**	$FFD4_H$		EA_H	Port 8 Register (8 bits)	00_H
PECC0		$FEC0_H$		60_H	PEC Channel 0 Control Register	0000_H
PECC1		$FEC2_H$		61_H	PEC Channel 1 Control Register	0000_H
PECC2		$FEC4_H$		62_H	PEC Channel 2 Control Register	0000_H
PECC3		$FEC6_H$		63_H	PEC Channel 3 Control Register	0000_H
PECC4		$FEC8_H$		64_H	PEC Channel 4 Control Register	0000_H
PECC5		$FECA_H$		65_H	PEC Channel 5 Control Register	0000_H
PECC6		$FECC_H$		66_H	PEC Channel 6 Control Register	0000_H
PECC7		$FECE_H$		67_H	PEC Channel 7 Control Register	0000_H
PICON	**b**	$F1C4_H$	**E**	$E2_H$	Port Input Threshold Control Register	0000_H
PSW	**b**	$FF10_H$		88_H	CPU Program Status Word	0000_H
RP0H	**b**	$F108_H$	**E**	84_H	System Startup Configuration Register (Rd. only)	XX_H
RTCH		$F0D6_H$	**E**	$6B_H$	RTC High Register	$XXXX_H$
RTCL		$F0D4_H$	**E**	$6A_H$	RTC Low Register	$XXXX_H$
S0BG		$FEB4_H$		$5A_H$	Serial Channel 0 Baud Rate Generator Reload Register	0000_H
S0CON	**b**	$FFB0_H$		$D8_H$	Serial Channel 0 Control Register	0000_H
S0EIC	**b**	$FF70_H$		$B8_H$	Serial Channel 0 Error Interrupt Control Register	0000_H
S0RBUF		$FEB2_H$		59_H	Serial Channel 0 Receive Buffer Register (read only)	$XXXX_H$
S0RIC	**b**	$FF6E_H$		$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC	**b**	$F19C_H$	**E**	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF		$FEB0_H$		58_H	Serial Channel 0 Transmit Buffer Register	0000_H
S0TIC	**b**	$FF6C_H$		$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H
SP		$FE12_H$		09_H	CPU System Stack Pointer Register	$FC00_H$
SSCBR		$F0B4_H$	**E**	$5A_H$	SSC Baudrate Register	0000_H

Name	Physical Address	8-Bit Address	Description	Reset Value
SSCCON b	$FFB2_H$	$D9_H$	SSC Control Register	0000_H
SSCEIC b	$FF76_H$	BB_H	SSC Error Interrupt Control Register	0000_H
SSCRB	$F0B2_H$ **E**	59_H	SSC Receive Buffer (read only)	$XXXX_H$
SSCRIC b	$FF74_H$	BA_H	SSC Receive Interrupt Control Register	0000_H
SSCTB	$F0B0_H$ **E**	58_H	SSC Transmit Buffer (write only)	0000_H
SSCTIC b	$FF72_H$	$B9_H$	SSC Transmit Interrupt Control Register	0000_H
STKOV	$FE14_H$	$0A_H$	CPU Stack Overflow Pointer Register	$FA00_H$
STKUN	$FE16_H$	$0B_H$	CPU Stack Underflow Pointer Register	$FC00_H$
SYSCON b	$FF12_H$	89_H	CPU System Configuration Register	$0XX0_H$ [1)]
SYSCON2 b	$F1D0_H$ **E**	$E8_H$	CPU System Configuration Register 2	0000_H
SYSCON3 b	$F1D4_H$ **E**	EA_H	CPU System Configuration Register 3	0000_H
T12IC b	$F190_H$ **E**	$C8_H$	CAPCOM 6 Timer 12 Interrupt Control Register	0000_H
T12OF	$F034_H$ **E**	$1A_H$	CAPCOM 6 Timer 12 Offset Register	0000_H
T12P	$F030_H$ **E**	18_H	CAPCOM 6 Timer 12 Period Register	0000_H
T13IC b	$F198_H$ **E**	CC_H	CAPCOM 6 Timer 13 Interrupt Control Register	0000_H
T13P	$F032_H$ **E**	19_H	CAPCOM 6 Timer 13 Period Register	0000_H
T14	$F0D2_H$ **E**	69_H	RTC Timer 14 Register	$XXXX_H$
T14REL	$F0D0_H$ **E**	68_H	RTC Timer 14 Reload Register	$XXXX_H$
T2	$FE40_H$	20_H	GPT1 Timer 2 Register	0000_H
T2CON b	$FF40_H$	$A0_H$	GPT1 Timer 2 Control Register	0000_H
T2IC b	$FF60_H$	$B0_H$	GPT1 Timer 2 Interrupt Control Register	0000_H
T3	$FE42_H$	21_H	GPT1 Timer 3 Register	0000_H
T3CON b	$FF42_H$	$A1_H$	GPT1 Timer 3 Control Register	0000_H
T3IC b	$FF62_H$	$B1_H$	GPT1 Timer 3 Interrupt Control Register	0000_H
T4	$FE44_H$	22_H	GPT1 Timer 4 Register	0000_H
T4CON b	$FF44_H$	$A2_H$	GPT1 Timer 4 Control Register	0000_H
T4IC b	$FF64_H$	$B2_H$	GPT1 Timer 4 Interrupt Control Register	0000_H
T7	$F050_H$ **E**	28_H	CAPCOM Timer 7 Register	0000_H
T78CON b	$FF20_H$	90_H	CAPCOM Timer 7 and 8 Control Register	0000_H
T7IC b	$F17A_H$ **E**	BD_H	CAPCOM Timer 7 Interrupt Control Register	0000_H
T7REL	$F054_H$ **E**	$2A_H$	CAPCOM Timer 7 Reload Register	0000_H
T8	$F052_H$ **E**	29_H	CAPCOM Timer 8 Register	0000_H
T8IC b	$F17C_H$ **E**	BE_H	CAPCOM Timer 8 Interrupt Control Register	0000_H

Name	Physical Address	8-Bit Address	Description	Reset Value
T8REL	$F056_H$ **E**	$2B_H$	CAPCOM Timer 8 Reload Register	0000_H
TFR **b**	$FFAC_H$	$D6_H$	Trap Flag Register	0000_H
TRCON **b**	$FF34_H$	$9A_H$	CAPCOM 6 Trap Enable Control Register	$00XX_H$
UAR	$EFn2_H$ **X**	---	CAN Upper Arbitration Register (msg. **n**)	$UUUU_H$
WDT	$FEAE_H$	57_H	Watchdog Timer Register (read only)	0000_H
WDTCON **b**	$FFAE_H$	$D7_H$	Watchdog Timer Control Register	$00XX_H$ [2]
XP0IC **b**	$F186_H$ **E**	$C3_H$	X-Peripheral 0 Interrupt Control Register	0000_H
XP3IC **b**	$F19E_H$ **E**	CF_H	X-Peripheral 3 Interrupt Control Register	0000_H
ZEROS **b**	$FF1C_H$	$8E_H$	Constant Value 0's Register (read only)	0000_H

[1] The system configuration is selected during reset.

[2] The reset value depends on the indicated reset source.

Absolute Maximum Ratings

Ambient temperature under bias (T_A):
SAF-C164CI ..... –40 to +85 °C
SAK-C164CI ..... –40 to +125 °C
Storage temperature (T_{ST}) ..... – 65 to +150 °C
Voltage on V_{DD} pins with respect to ground (V_{SS}) ..... –0.5 to +6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... –0.5 to V_{DD} +0.5 V
Input current on any pin during overload condition ..... –10 to +10 mA
Absolute sum of all input currents during overload condition ..... |100 mA|
Power dissipation ..... 1.5 W

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C164CI and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C164CI will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C164CI.

DC Characteristics

V_{DD} = 4.25 - 5.5 V; V_{SS} = 0 V; f_{CPU} = 20 MHz
T_A = -40 to +85 °C for SAF-C164CI
T_A = -40 to +125 °C for SAK-C164CI

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage (TTL)	V_{IL}	SR	– 0.5	0.2 V_{DD} – 0.1	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	– 0.5	2.0	V	–
Input high voltage, all except $\overline{RSTIN}$ and XTAL1 (TTL)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage $\overline{RSTIN}$	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS		400	-	mV	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL1} = 1.6 mA
Output high voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH}	CC	0.9 V_{DD} 2.4	–	V	I_{OH} = – 500 µA I_{OH} = – 2.4 mA
Output high voltage [1] (all other outputs)	V_{OH1}	CC	0.9 V_{DD} 2.4	–	V V	I_{OH} = – 250 µA I_{OH} = – 1.6 mA
Input leakage current (Port 5)	I_{OZ1}	CC	–	±200	nA	0.45V< V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2}	CC	–	±500	nA	0.45V< V_{IN} < V_{DD}
Overload current	I_{OV}	SR	–	±5	mA	[5] [8]
$\overline{RSTIN}$ pullup resistor	R_{RST}	CC	50	250	kΩ	–
Read/Write inactive current [4]	I_{RWH}	[2]	–	-40	µA	V_{OUT} = 2.4 V
Read/Write active current [4]	I_{RWL}	[3]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [4]	I_{ALEL}	[2]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current [4]	I_{ALEH}	[3]	500	–	µA	V_{OUT} = 2.4 V
PORT0 configuration current [4]	I_{P0H}	[2]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L}	[3]	-100	–	µA	V_{IN} = V_{ILmax}

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
XTAL1 input current	I_{IL} CC	–	± 20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [5] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current (active) with all peripherals active	I_{DD}	–	10 + 3.5 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL2} f_{CPU} in [MHz] [6]
Idle mode supply current with all peripherals active	I_{IDX}	–	5 + 1.25 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [6]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}	–	500 + 50 × f_{OSC} [9]	µA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [6]
Power-down mode supply current with RTC running	I_{PDR}	–	100 + 25 × f_{OSC} [9]	µA	V_{DD} = 5.5 V f_{OSC} in [MHz] [7]
Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = 5.5 V [7]

Notes

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2) The maximum current may be drawn while the respective signal line remains inactive.

3) The minimum current must be drawn in order to drive the respective signal line active.

4) This specification is only valid during Reset, or during Adapt-mode.

5) Not 100% tested, guaranteed by design characterization.

6) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and 20 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.
The oscillator also contributes to the total supply current. The given values refer to the worst case, i.e. I_{PDRmax}. For lower oscillator frequencies the respective supply current can be reduced accordingly.

7) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

8) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. V_{OV} > V_{DD} + 0.5 V or V_{OV} < V_{SS} – 0.5 V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage (V_{DD} and V_{SS}) must remain within the specified limits.

9) This parameter is determined mainly by the current consumed by the oscillator. This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.
A typical value for I_{PDR} at room temperature and f_{OSC} = 16 MHz is 300 µA.

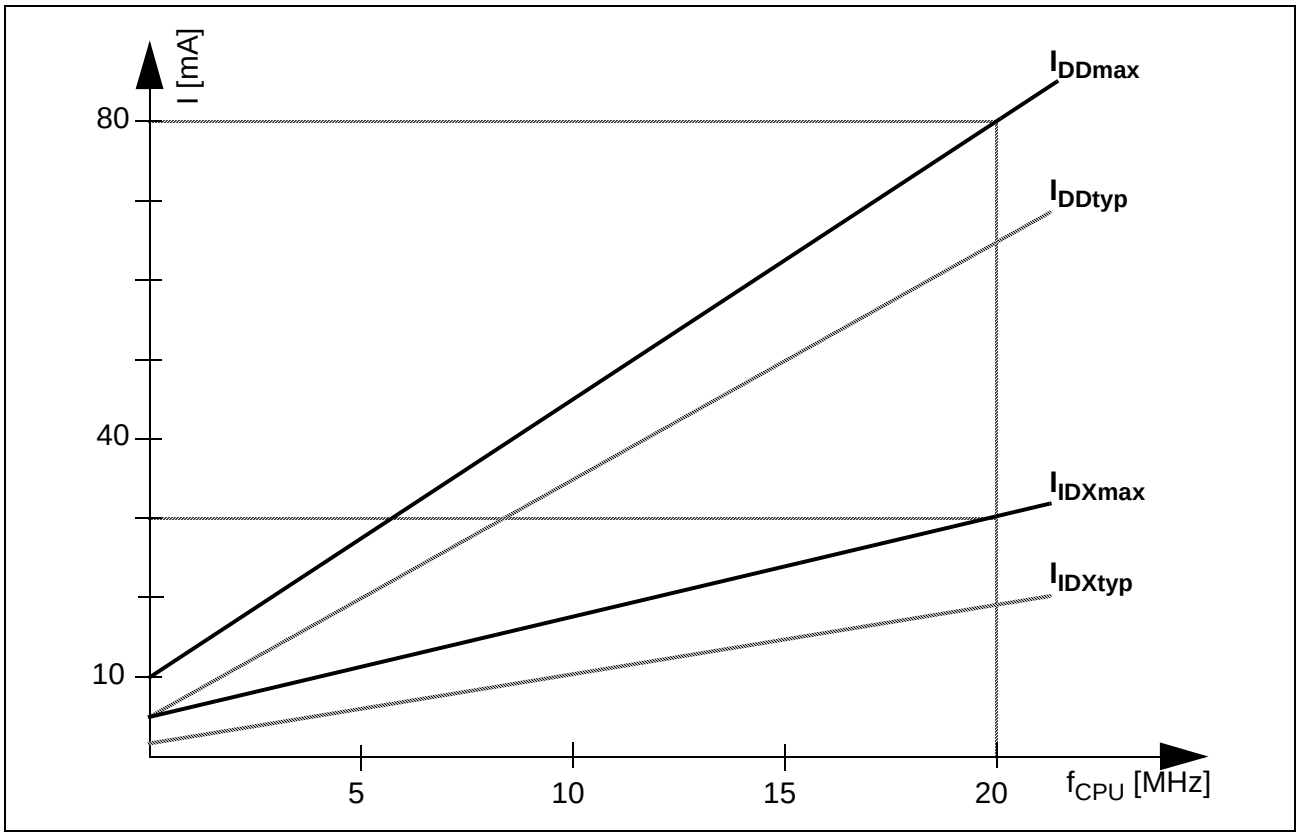


Figure 7
Active and Idle Supply Current as a Function of Operating Frequency

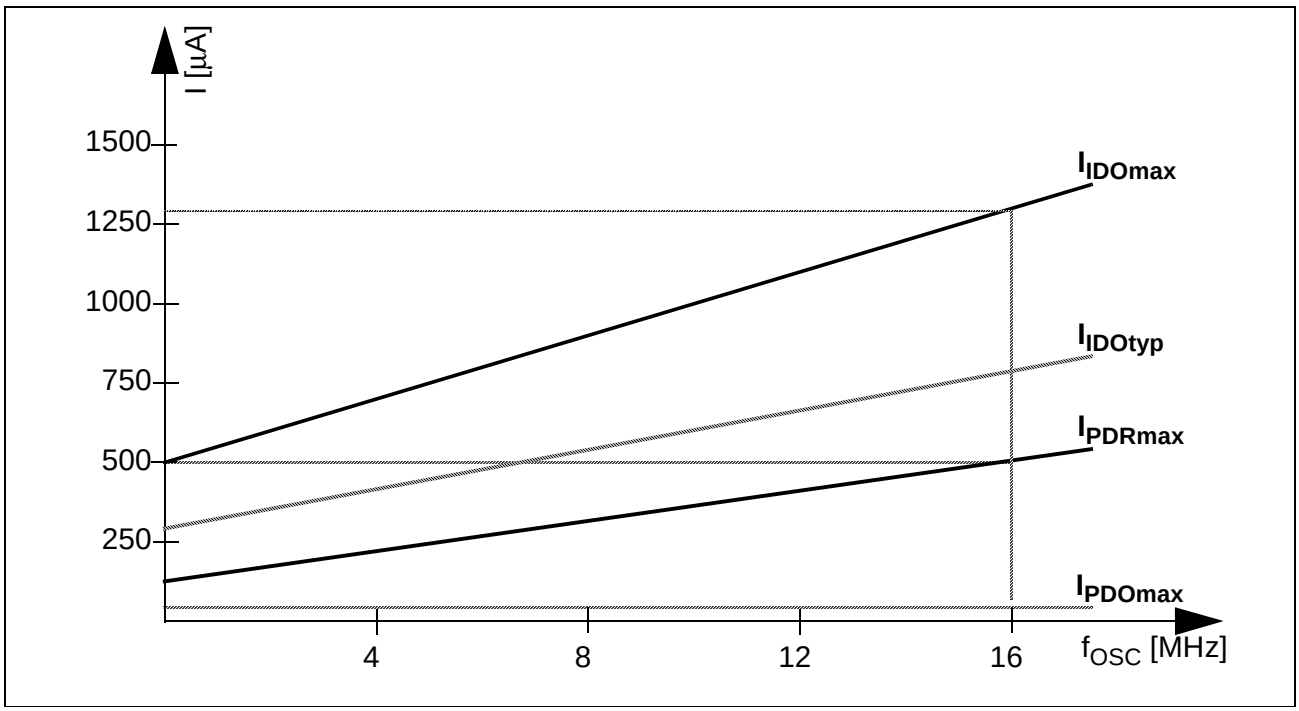


Figure 8
Idle and Power Down Supply Current as a Function of Oscillator Frequency

AC Characteristics
Definition of Internal Timing

The internal operation of the C164CI is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (eg. pipeline) or external (eg. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see figure below).

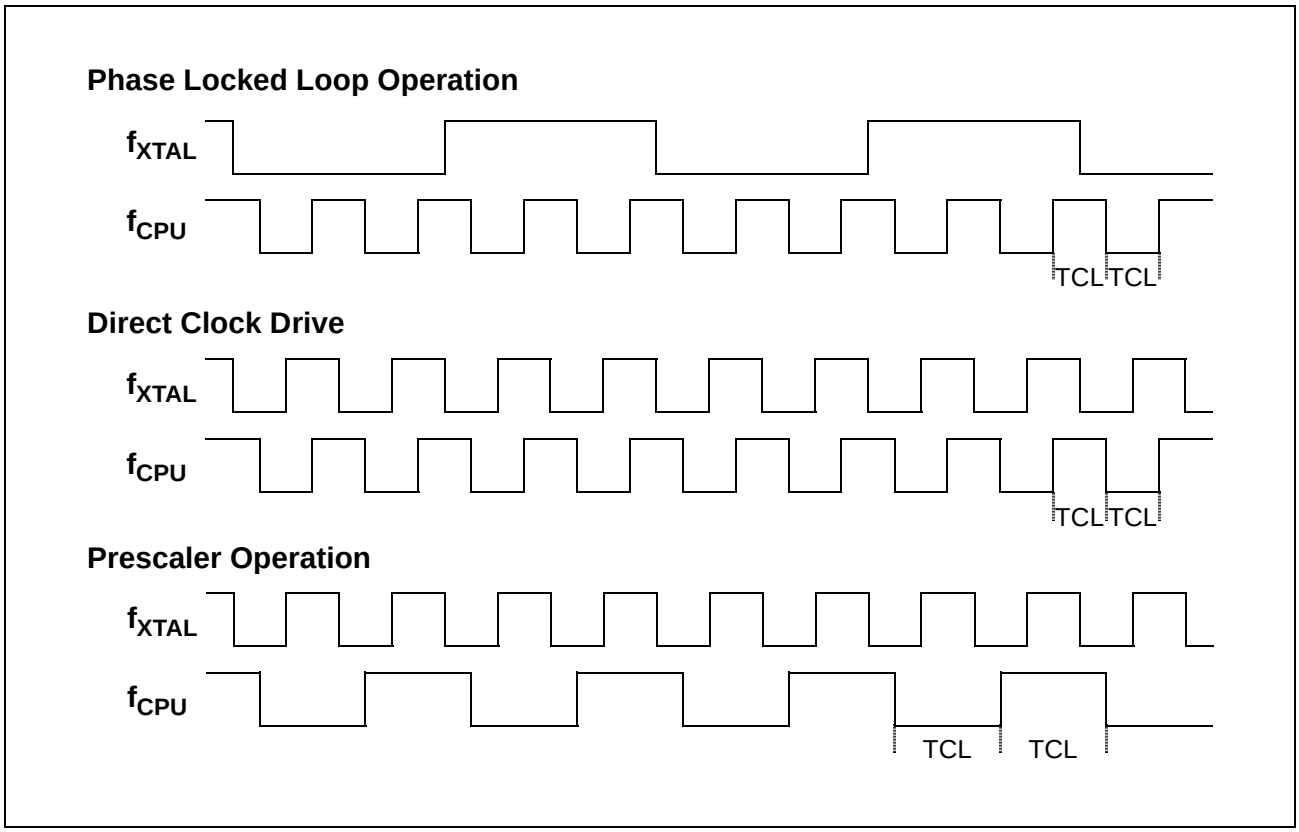


Figure 9
Generation Mechanisms for the CPU Clock

The CPU clock signal can be generated via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU}. This influence must be regarded when calculating the timings for the C164CI.

Note: The example for PLL operation shown in the figure above refers to a PLL factor of 4.

The used mechanism to generate the CPU clock is selected during reset via the logic levels on pins P0.15-13 (P0H.7-5).

The table below associates the combinations of these three bits with the respective clock generation mode.

C164CI Clock Generation Modes

P0.15-13 (P0H.7-5)			CPU Frequency $f_{CPU} = f_{XTAL} * F$	External Clock Input Range [1]	Notes
1	1	1	$f_{XTAL} * 4$	2.5 to 5 MHz	Default configuration
1	1	0	$f_{XTAL} * 3$	3.33 to 6.66 MHz	
1	0	1	$f_{XTAL} * 2$	5 to 10 MHz	
1	0	0	$f_{XTAL} * 5$	2 to 4 MHz	
0	1	1	$f_{XTAL} * 1$	1 to 20 MHz	Direct drive [2]
0	1	0	$f_{XTAL} * 1.5$	6.66 to 13.3 MHz	
0	0	1	$f_{XTAL} / 2$	2 to 40 MHz	CPU clock via prescaler
0	0	0	$f_{XTAL} * 2.5$	4 to 8 MHz	

[1] The external clock input range refers to a CPU clock range of 10...20 MHz.
[2] The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal ’001’ during reset the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (ie. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{XTAL} for any TCL.

Direct Drive

When pins P0.15-13 (P0H.7-5) equal ’011’ during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (ie. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{XTAL} * DC_{min} \qquad \text{(DC = duty cycle)}$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{XTAL} is compensated so the duration of 2TCL is always $1/f_{XTAL}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula $2TCL = 1/f_{XTAL}$.

Note: The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} * DC_{max}$) instead of TCL_{min}.

Phase Locked Loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (ie. $f_{CPU} = f_{XTAL} * \mathbf{F}$). With every **F**'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothely, ie. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and figure below).
For a period of $\boldsymbol{N}$ * TCL the minimum value is computed using the corresponding deviation $D_{\boldsymbol{N}}$:

$$TCL_{min} = TCL_{NOM} * (1 - D_{\boldsymbol{N}} / 100)$$

$D_{\boldsymbol{N}} = \pm(4 - \boldsymbol{N}/15)$ [%],
where $\boldsymbol{N}$ = number of consecutive TCLs
and $1 \le \boldsymbol{N} \le 40$.

So for a period of 3 TCLs (ie. $\boldsymbol{N} = 3$): $D_{\boldsymbol{3}} = 4 - \boldsymbol{3}/15 = 3.8\%$,
and $(3TCL)_{min} = 3TCL_{NOM} * (1 - 3.8 / 100) = 3TCL_{NOM} * 0.962$ (57.72 nsec @ f_{CPU} = 25 MHz).

This is especially important for bus cycles using waitstates and eg. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (eg. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

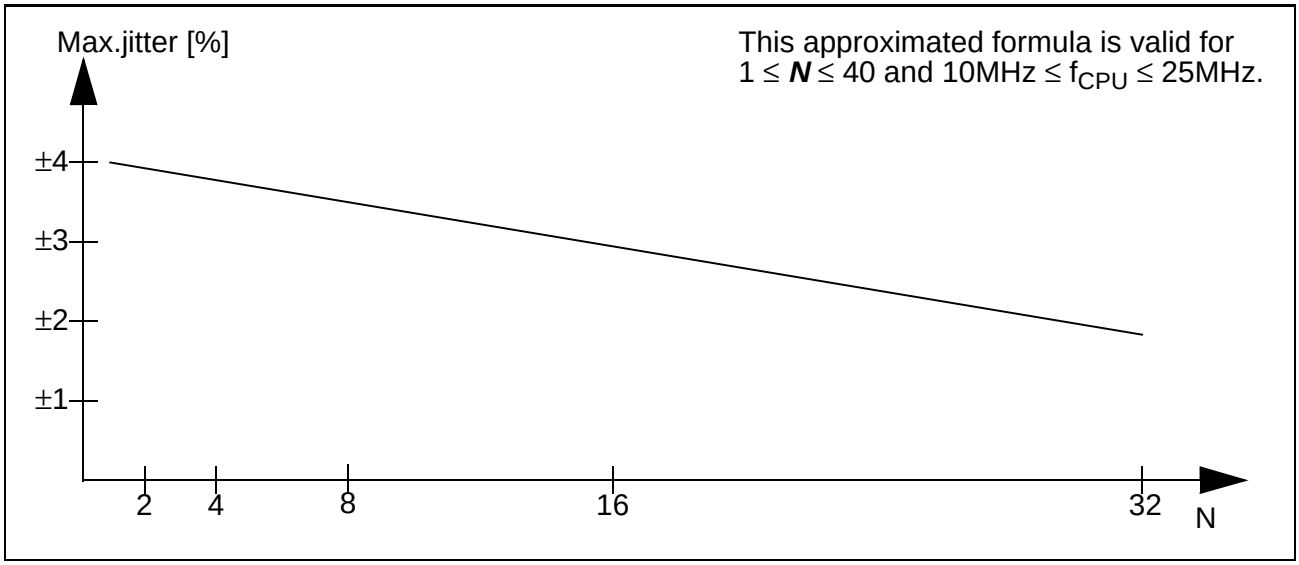


Figure 10
Approximated Maximum PLL Jitter

AC Characteristics
External Clock Drive XTAL1

V_{DD} = 4.25 - 5.5 V; V_{SS} = 0 V
T_A = -40 to +85 °C for SAF-C164CI
T_A = -40 to +125 °C for SAK-C164CI

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	50	8000	25	4000	75 [1]	500 [1]	ns
High time	t_1	SR	18 [2]	–	6	–	10	–	ns
Low time	t_2	SR	18 [2]	–	6	–	10	–	ns
Rise time	t_3	SR	–	10 [2]	–	6 [2]	–	10 [2]	ns
Fall time	t_4	SR	–	10 [2]	–	6 [2]	–	10 [2]	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.
2) The clock input signal must reach the defined levels V_{IL} and V_{IH2}.

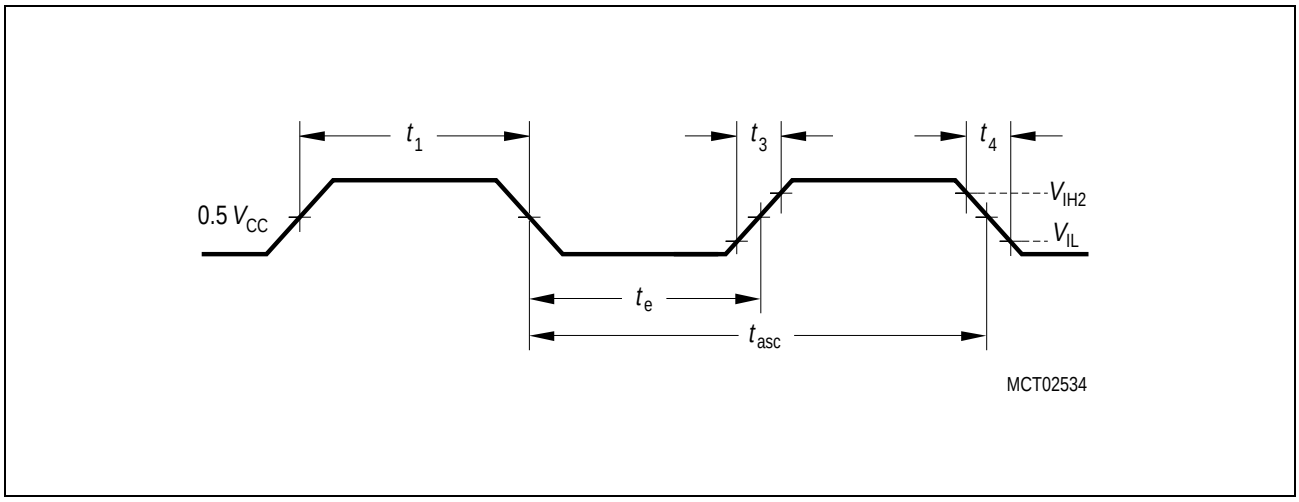


Figure 11
External Clock Drive XTAL1

A/D Converter Characteristics

V_{DD} = 4.25 - 5.5 V; V_{SS} = 0 V
T_A = -40 to +85 °C for SAF-C164CI
T_A = -40 to +125 °C for SAK-C164CI
4.0 V ≤ V_{AREF} ≤ V_{DD}+0.1 V ; V_{SS}-0.1 V ≤ V_{AGND} ≤ V_{SS}+0.2 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	1)
Basic clock frequency	f_{BC}	0.5	6	MHz	2)
Conversion time	t_C CC	–	40 t_{BC} + t_S + 2 t_{CPU}		3) t_{CPU} = 1 / f_{CPU}
Total unadjusted error	TUE CC	–	± 2	LSB	4)
Internal resistance of reference voltage source	R_{AREF} SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC} SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns] 6) 7)
ADC input capacitance	C_{AIN} CC	–	33	pF	6)

Sample time and conversion time of the C164CI's A/D Converter are programmable. The table below should be used to calculate the above timings.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

ADCON.15|14 (ADCTC)	A/D Converter Basic clock f_{BC} 2)	ADCON.13|12 (ADSTC)	Sample time t_S 7)
00	f_{CPU} / 4	00	t_{BC} * 8
01	f_{CPU} / 2	01	t_{BC} * 16
10	f_{CPU} / 16	10	t_{BC} * 32
11	f_{CPU} / 8	11	t_{BC} * 64

Converter Timing Example:

Assumptions: f_{CPU} = 20 MHz (ie. t_{CPU} = 50 ns), ADCTC = '00', ADSTC = '00'.

Basic clock f_{BC} = f_{CPU} / 4 = 5 MHz, ie. t_{BC} = 200 ns.
Sample time t_S = t_{BC} * 8 = 1600 ns.
Conversion time t_C = t_S + 40 t_{BC} + 2 t_{CPU} = (1600 + 8000 + 100) ns = 9.7 µs.

Notes

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from the table above.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

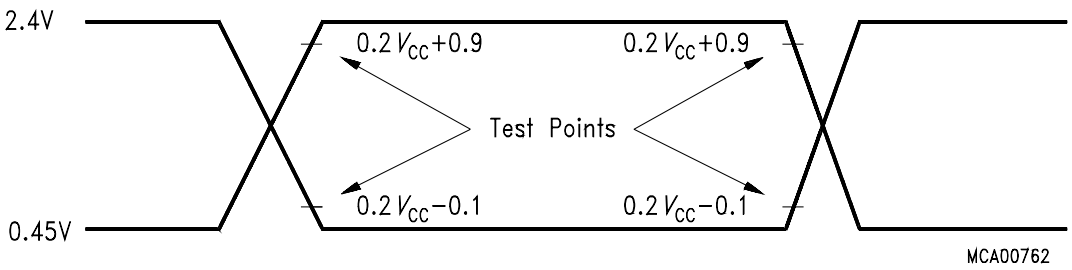
4) TUE is tested at V_{AREF}=5.0V, V_{AGND}=0V, V_{DD}=4.9V. It is guaranteed by design for all other voltages within the defined voltage range.
The specified TUE is guaranteed only if an overload condition (see I_{OV} specification) occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, guaranteed by design.

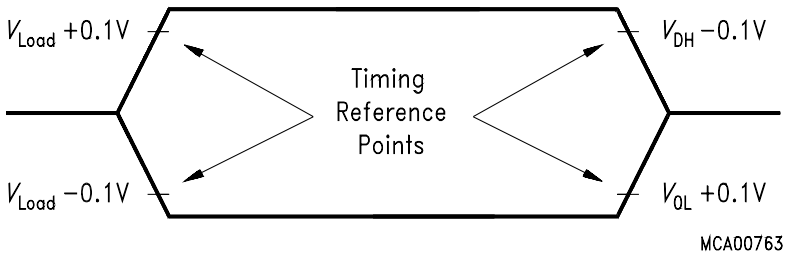
7) During the sample time the input capacitance C_I can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample time t_S depend on programming and can be taken from the table above.

Testing Waveforms



AC inputs during testing are driven at 2.4 V for a logic ‘1’ and 0.45 V for a logic ‘0’. Timing measurements are made at V_{IH} min for a logic ‘1’ and V_{IL} max for a logic ‘0’.

Figure 12
Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

Figure 13
Float Waveforms

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

AC Characteristics
Multiplexed Bus

V_{DD} = 4.25 - 5.5 V; V_{SS} = 0 V
T_A = -40 to +85 °C for SAF-C164CI
T_A = -40 to +125 °C for SAK-C164CI
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	9 + t_A	–	TCL - 16 + t_A	–	ns
Address hold after ALE	t_7	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	31	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	40 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	65 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	30 + t_C	–	2TCL - 20 + t_C	ns

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	55 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	55 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	70 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	36 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	30 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In	t_{39}	SR	–	55 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40}	CC	61 + t_F	–	3TCL - 14 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	21 + t_A	–	TCL - 4 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	25	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	26 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	51 + t_C	–	3TCL - 24 + t_C	ns

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (with RW delay)	t_{48}	CC	40 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (no RW delay)	t_{49}	CC	65 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	36 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	30 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns

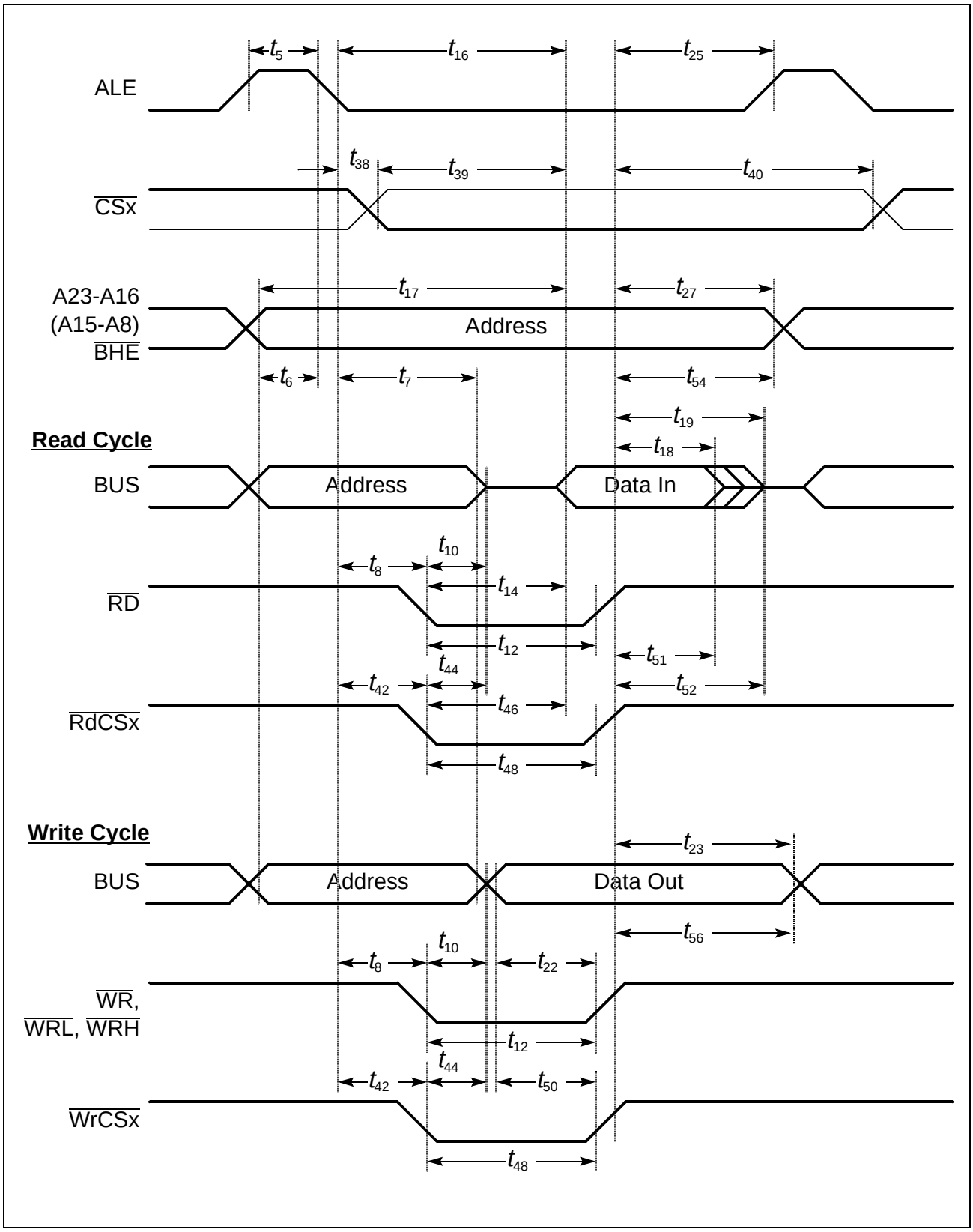


Figure 14-1
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

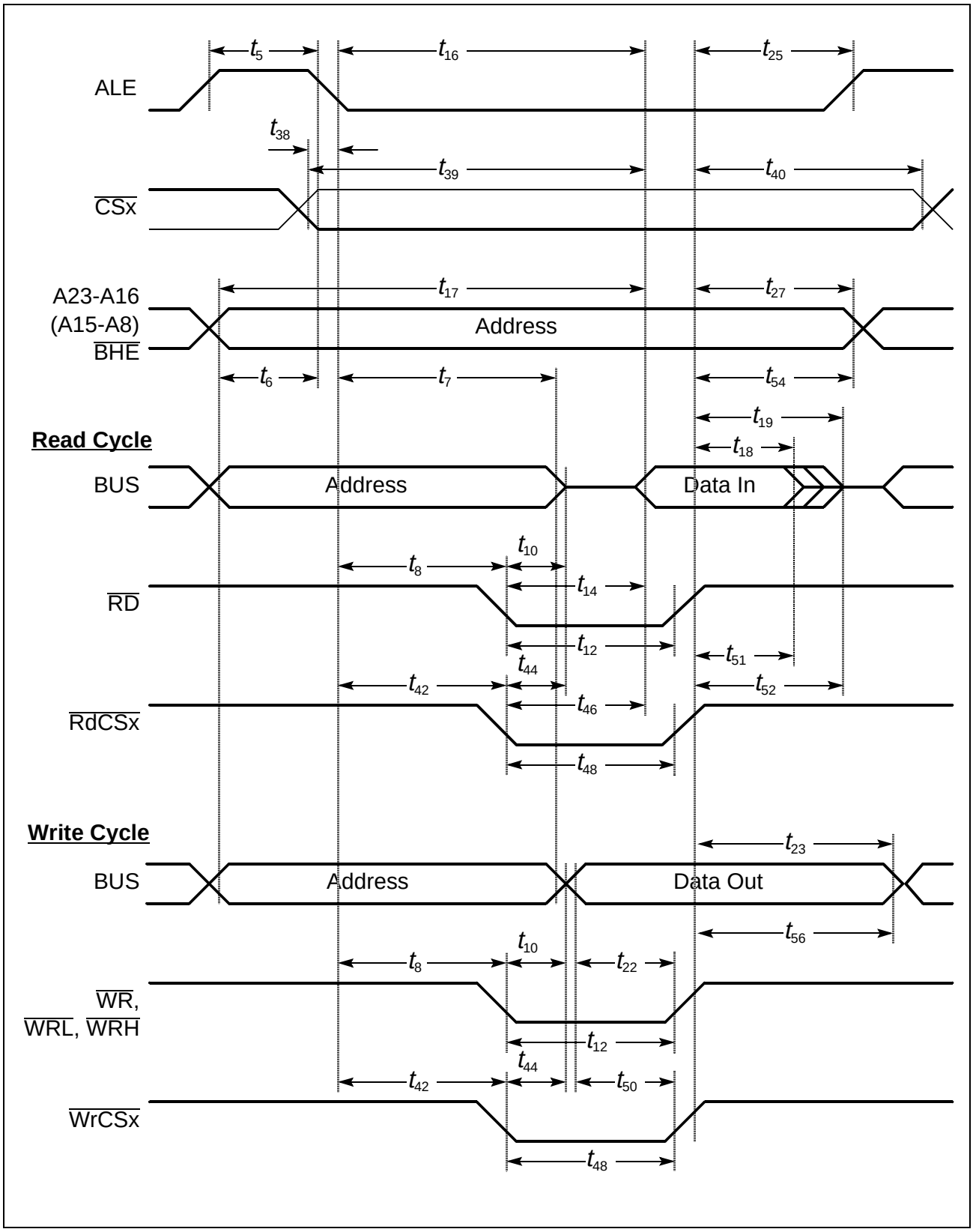


Figure 14-2
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

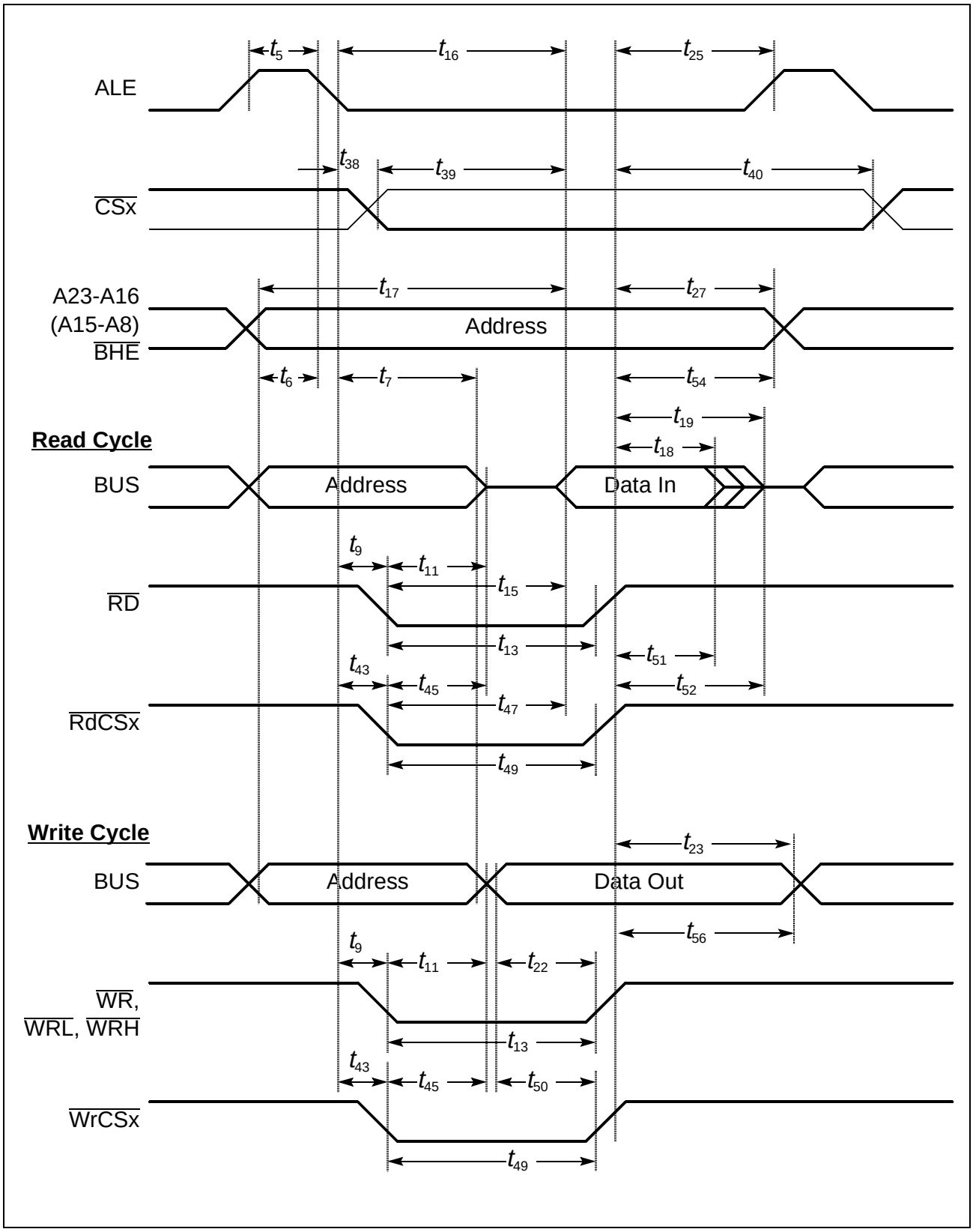


Figure 14-3
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

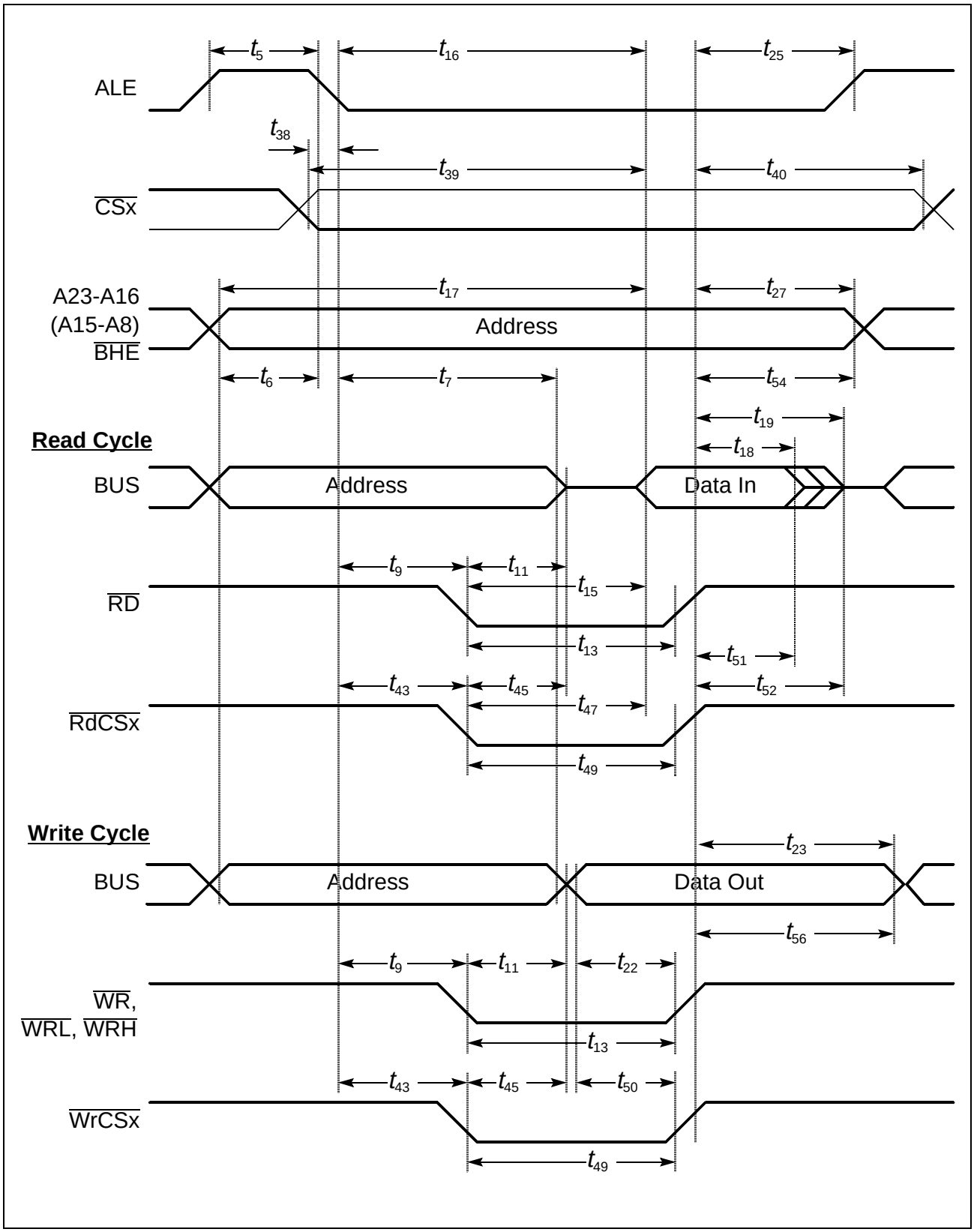


Figure 14-4
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics
CLKOUT

V_{DD} = 4.25 - 5.5 V; V_{SS} = 0 V
T_A = -40 to +85 °C for SAF-C164CI
T_A = -40 to +125 °C for SAK-C164CI
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	50	50	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	19	–	TCL – 6	–	ns
CLKOUT low time	t_{31}	CC	15	–	TCL – 10	–	ns
CLKOUT rise time	t_{32}	CC	–	4	–	4	ns
CLKOUT fall time	t_{33}	CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	0 + t_A	10 + t_A	0 + t_A	10 + t_A	ns

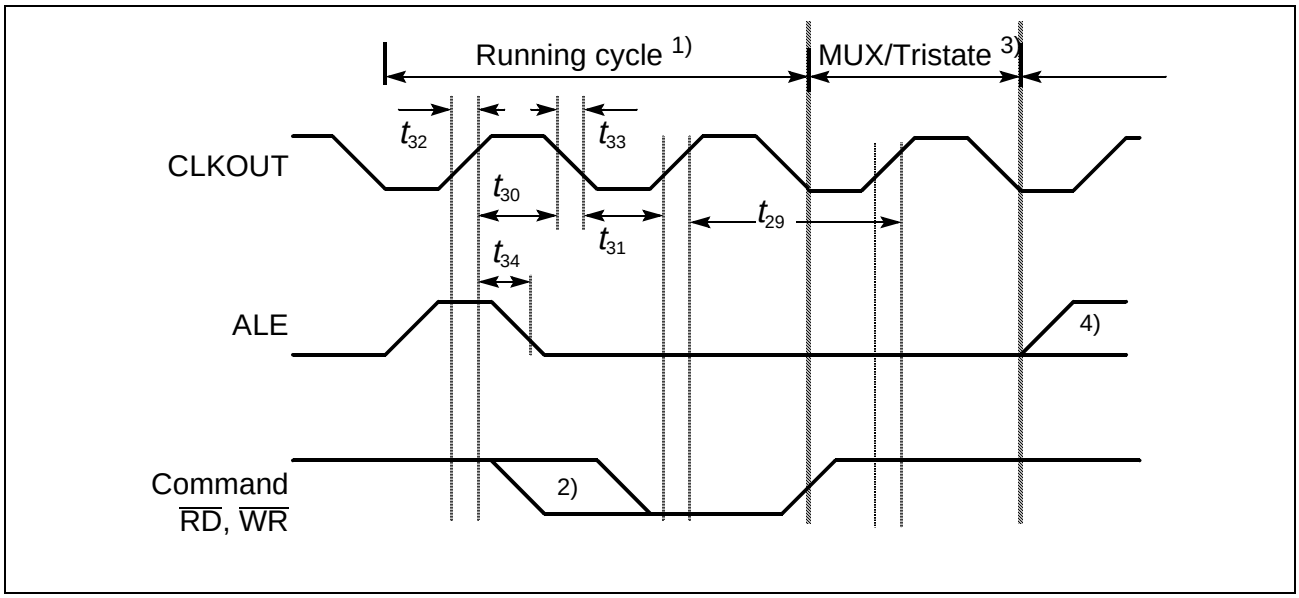


Figure 15
CLKOUT Timing

Notes

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

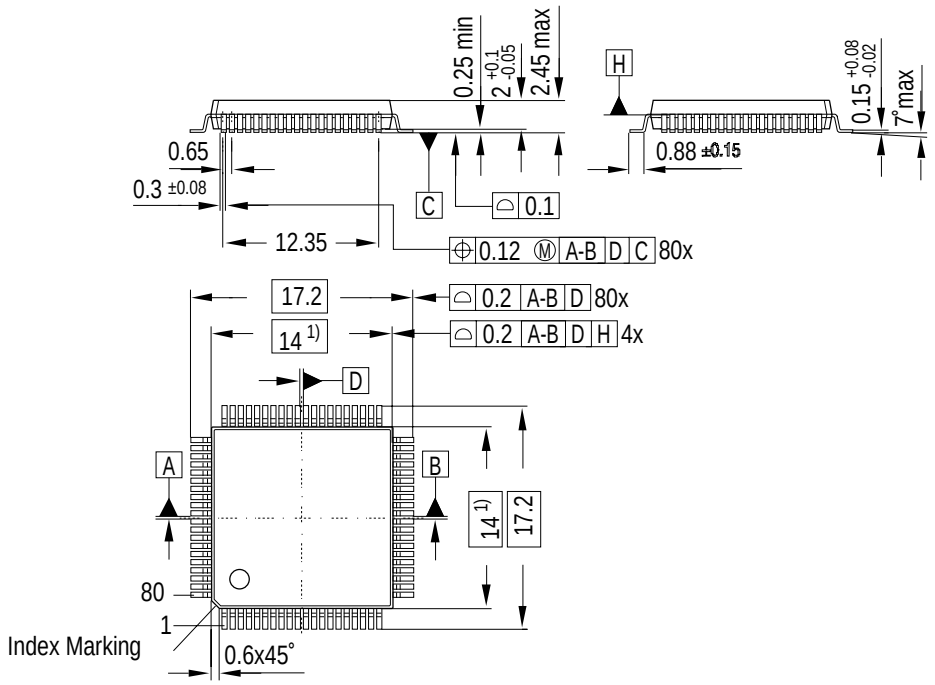
2) The leading edge of the respective command depends on RW-delay.

3) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles.

4) The next external bus cycle may start here.

Package Outline

Plastic Package, P-MQFP-80-1 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Figure 16

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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