

Display Elektronik GmbH

DATA SHEET

e-Paper MODULE

DEE 152152A – W

1,5“
e-PAPER DISPLAY

Product Specification

Ver.: 0

22.03.2018

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Specification for 1,5" e-Paper Module

Model NO. : DEE 152152A-W

Prepared by	Checked by	Approved by
QY	YL	MH

Customer approval

Customer	Approved by	Date of Approval

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Version	Content	Date	Producer
0	New Release	22.03.2018	QY

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1 General Description

This e-Paper is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 1.54" active area contains 152x152 pixels, and has 2-bit full display capabilities. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- ◆ 152 x 152 Pixels Display
- ◆ White Reflectance above 30%
- ◆ Contrast Ratio above 8:1
- ◆ Ultra Wide Viewing Angle
- ◆ Ultra Low Power Consumption
- ◆ Pure Reflective Mode
- ◆ Bi-Stable Display
- ◆ Landscape, Portrait Modes
- ◆ Hard-Coat Antiglare Display Surface
- ◆ Ultra Low Current Deep Sleep Mode
- ◆ On Chip Display RAM
- ◆ Waveform stored in On-Chip OTP
- ◆ Serial Peripheral Interface available
- ◆ On-Chip Oscillator
- ◆ On-Chip Booster and Regulator Control for generating VCOM, Gate and Source Driving Voltage
- ◆ I²C Signal Master Interface to read External Temperature Sensor

3 Application

Electronic Shelf Label System

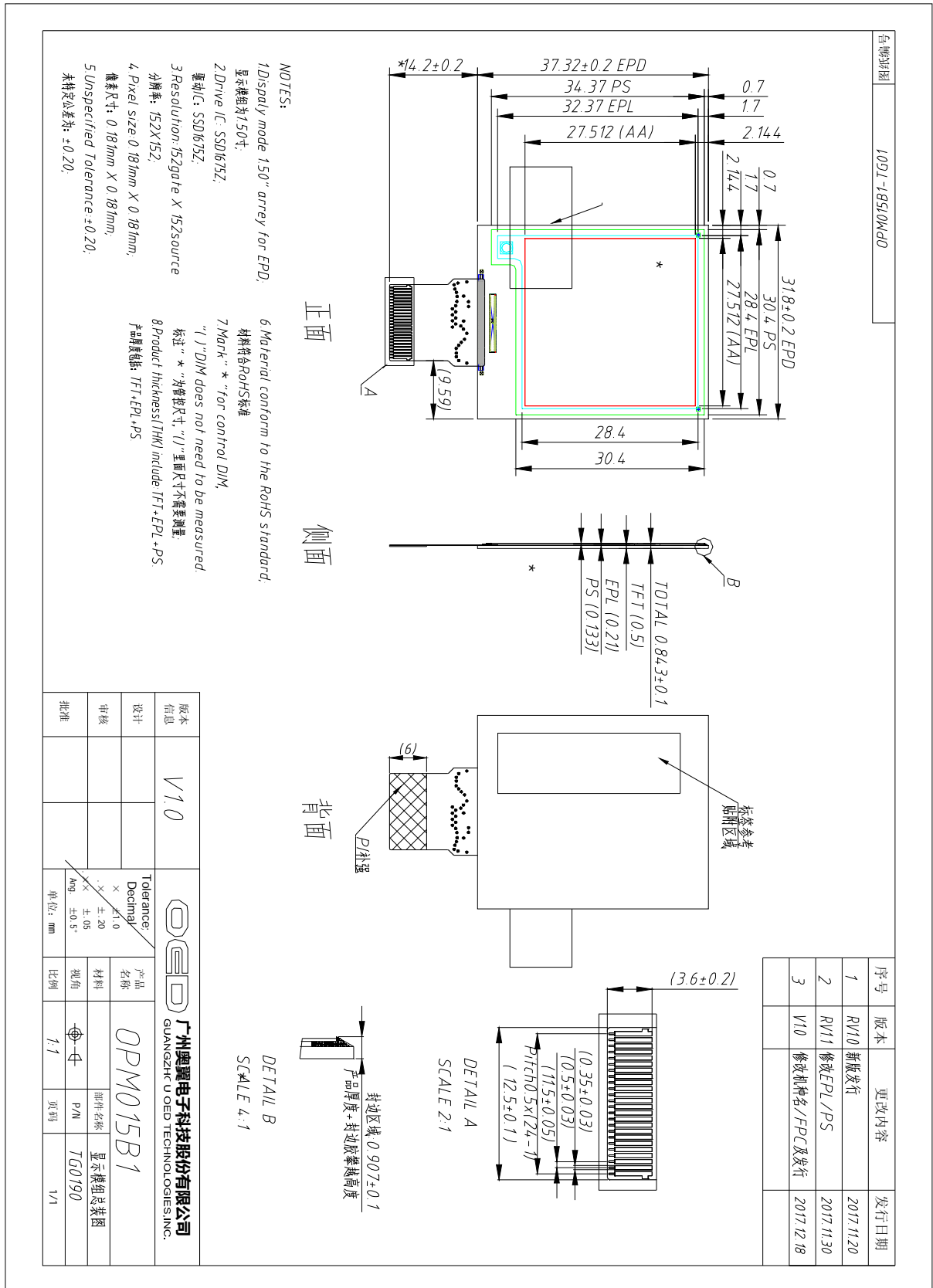
4 Mechanical Specification

4.1 Dimension

Parameter	Specifications	Unit
Screen Size	1.54	Inch
Display Resolution	152 x 152	Pixel
Active Area	27.512 x 27.512	mm
Pixel Pitch	0.181 x 0.181	mm
Pixel Configuration	Rectangle	
Outline Dimension	31.80 x 37.32 x 0.843	mm
Weight	2.1	g

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4.2 Mechanical Drawing of EPD Module



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5 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSYN	O	Busy state output pin	Note 5-3
10	RSTN	I	Reset signal input. Active Low.	
11	D/C	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDD	P	Power Supply for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage 2	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

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Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to $V_{dd} + 0.5$	V
Logic Output voltage	V_{OUT}	-0.5 to $V_{dd} + 0.5$	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: $V_{SS}=0V$, $V_{DD}=3.0V$, $T_{OPR}=25^{\circ}C$.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{dd}	-	VDD	2.2	3.0	3.7	V
High level input voltage	V_{IH}	-	-	$0.8 V_{dd}$	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	$0.2 V_{dd}$	V
High level output voltage	V_{OH}	$I_{OH} = -100\mu A$	-	$0.9 V_{dd}$	-	-	V
Low level output voltage	V_{OL}	$I_{OL} = 100\mu A$	-	-	-	$0.1 V_{dd}$	V
OTP Program voltage	V_{PP}	-	VPP	-	7.5	-	V
Typical power panel	P_{TYP}	-	-	-	12	30	mW
Deep sleep mode	P_{STPY}	-	-	-	3	-	uW
Typical operating current	I_{opr_VDD}	$V_{dd}=3.0V-$	-	-	4.0	10	mA

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Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	20	--	uA
Deep sleep mode current	IdslpVDD	VDD=3.0V DC/DC OFF No clock No output load Ram data not retain	VDD	-	1	--	uA
Operation temperature range	T _{OPR}	-	-	0	-	50	°C
Operation relative humidity	RHop	-	-	-	-	70	%RH
Operation illuminance intensity	E	indoor only	-	-	-	2000	lux
Storage temperature range	T _{STG}	-	-	0	-	50	°C
Storage relative humidity	RHst	-	-	30	-	60	%RH

Notes: 1. The typical power is measured with following transition:from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

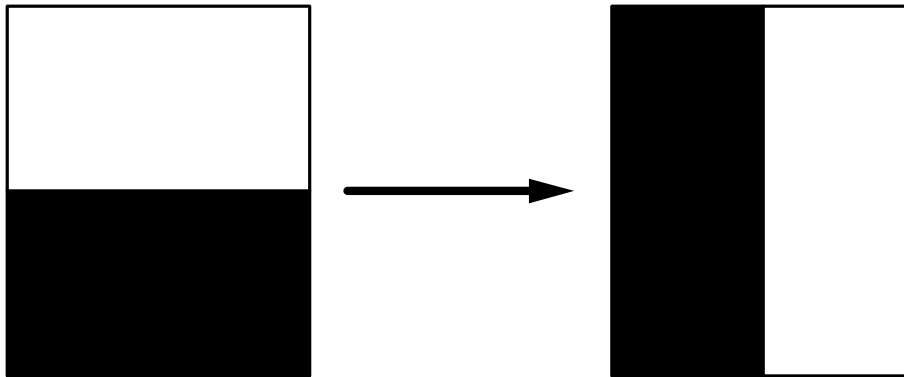


Figure 10-2 The typical power consumption measure pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-3.0	-	-0.2	V
Positive Source output voltage	V _{SH}	-	S0-103	+14.5	+15	+15.5	V
Negative Source output voltage	V _{SL}	-	S0-103	-15.5	-15	-14.5	V
Positive gate output voltage	V _{gh}	-	g0-g211	+21	+22	+23	V
Negative gate output voltage	V _{gl}	-	g0-g211	-21	-20	-19	V

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6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Connand Interface		Control Signal		
	SDA	SCL	CSB	D/C	RSTN
4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
3-wire SPI	SDIN	SCLK	CSB	L	RSTN

Table 10-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

Function	CSB	D/C	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

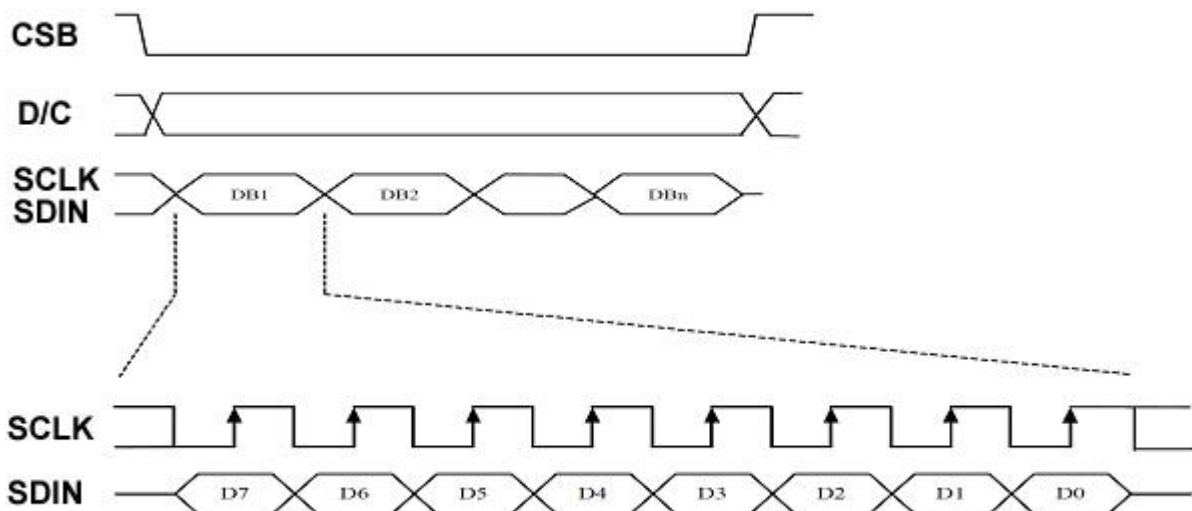


Figure 10-4-2: Write procedure in 4-wire SPI mode

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6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

Table 10-4-3: Control pins of 3-wire Serial interface

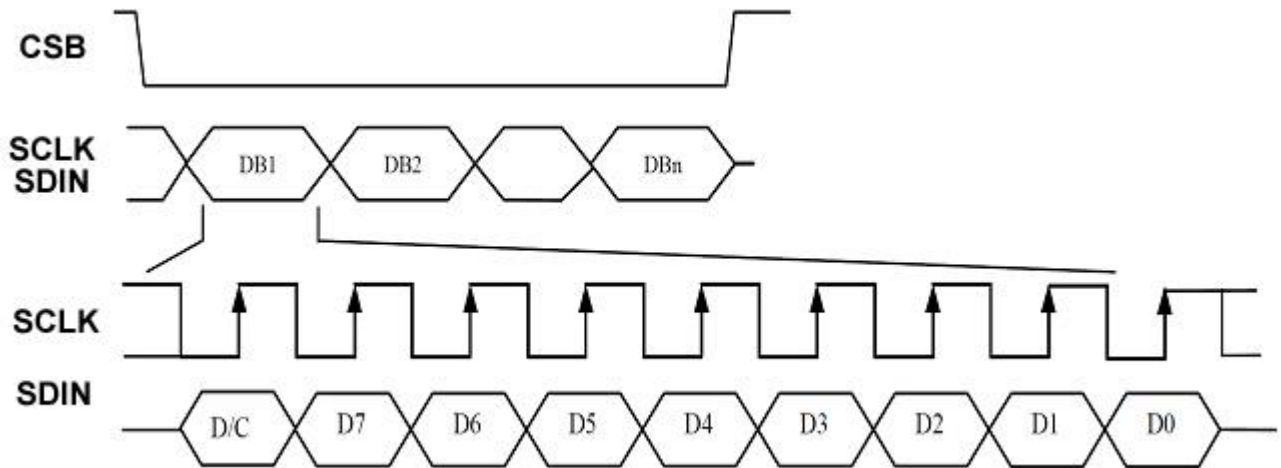


Figure 10-4-3: Write procedure in 3-wire SPI mode

6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25°C.

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VDD =2.4 to 3.3V	CL	0.95	1	1.05	MHz

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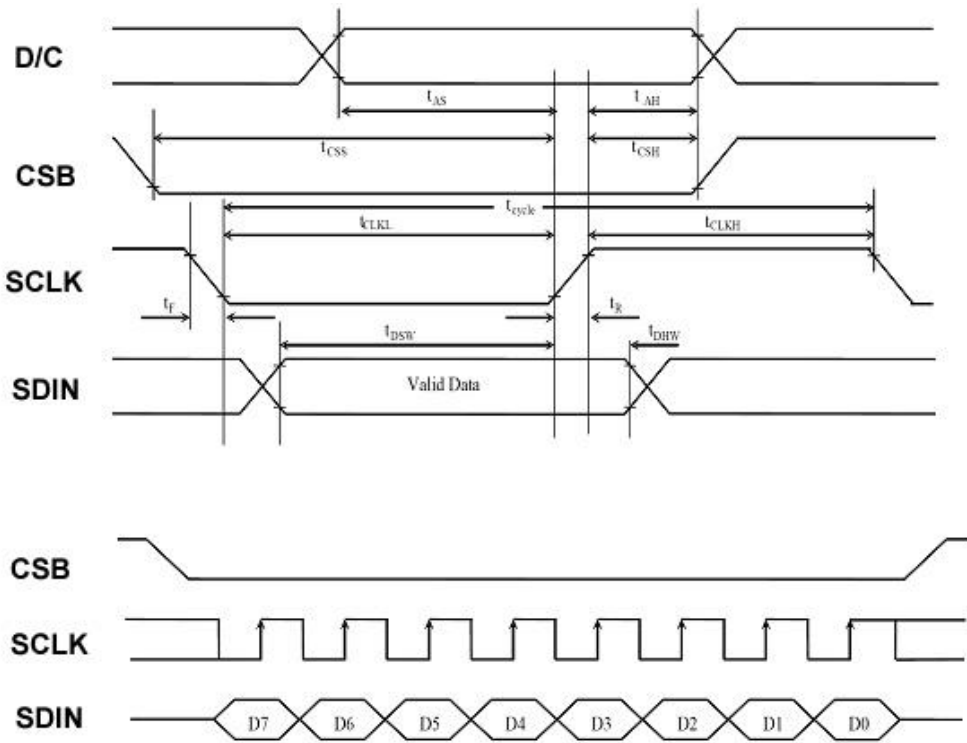


Figure 10-4-4: Serial interface characteristics

($V_{dd} - V_{SS} = 2.4V$ to $3.3V$, $T_{OPR} = 25^{\circ}C$, $CL=20pF$)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_{R}	Rise Time [20% ~ 80%]	-	-	15	ns
t_{F}	Fall Time [20% ~ 80%]	-	-	15	ns

Table 10-4-4: Serial Interface Timing Characteristics

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6.4.5 Command Table

R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description		
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[8:0] = 127h Set B[2:0] = 0h		
0	1		A7	A6	A5	A4	A3	A2	A1	A0				
0	1		0	0	0	0	0	0	0	A8				
0	1		0	0	0	0	0	B2	B1	B0				
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Set A[7:0] = 8Bh Set B[7:0] = 9Ch Set C[7:0] = 96h Set D[7:0] = 0Fh		
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀				
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀				
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control		
0	1		0	0	0	0	0	0	0	A ₀				
													A[0] :	Description
													0	Normal Mode [POR]
											1	Enter Deep Sleep Mode		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.		
0	1		0	0	0	0	0	A ₂	A ₁	A ₀				
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.		

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R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description					
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh[POR]					
0	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄							
0	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0							
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.					
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[3:0] BW RAM option					
0	1		A ₇	0	0	A ₄	A ₃	A ₂	A ₁	A ₀			<table border="1"> <tr> <td>0000</td> <td>Normal</td> </tr> <tr> <td>0100</td> <td>Bypass RAM content as 0</td> </tr> <tr> <td>1000</td> <td>Inverse RAM content</td> </tr> </table>	0000	Normal	0100	Bypass RAM content as 0
0000	Normal																
0100	Bypass RAM content as 0																
1000	Inverse RAM content																

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R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																																
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation																																																																
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			Parameter (in Hex)																																																															
												Enable Clock Signal, Then Enable Analog Then Load Temperature Sensor Then Load LUT Then INITIAL DISPLAY Then PATTERN DISPLAY Then Disable CP Then Disable OSC	FF [POR]																																																															
												Setting for LUT from OTP according to external Temperature Sensor operation 2 Enable Clock Signal, Then Enable Analog Then Load LUT Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	D7																																																															
												Setting for LUT from MCU Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	C7																																																															
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM= 1 For Black pixel: Content of Write RAM = 0																																																																
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]																																																																
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			<table border="1"> <thead> <tr> <th>A[7:0]</th> <th>vcom</th> <th>A[7:0]</th> <th>vcom</th> </tr> </thead> <tbody> <tr><td>08h</td><td>-0.2</td><td>44h</td><td>-1.7</td></tr> <tr><td>0Bh</td><td>-0.3</td><td>48h</td><td>-1.8</td></tr> <tr><td>10h</td><td>-0.4</td><td>4Bh</td><td>-1.9</td></tr> <tr><td>14h</td><td>-0.5</td><td>50h</td><td>-2</td></tr> <tr><td>17h</td><td>-0.6</td><td>54h</td><td>-2.1</td></tr> <tr><td>1Bh</td><td>-0.7</td><td>58h</td><td>-2.2</td></tr> <tr><td>20h</td><td>-0.8</td><td>5Bh</td><td>-2.3</td></tr> <tr><td>24h</td><td>-0.9</td><td>5Fh</td><td>-2.4</td></tr> <tr><td>28h</td><td>-1</td><td>64h</td><td>-2.5</td></tr> <tr><td>2Ch</td><td>-1.1</td><td>68h</td><td>-2.6</td></tr> <tr><td>2Fh</td><td>-1.2</td><td>6Ch</td><td>-2.7</td></tr> <tr><td>34h</td><td>-1.3</td><td>6Fh</td><td>-2.8</td></tr> <tr><td>37h</td><td>-1.4</td><td>73h</td><td>-1.54</td></tr> <tr><td>3Ch</td><td>-1.5</td><td>78h</td><td>-3</td></tr> <tr><td>40h</td><td>-1.6</td><td>Other</td><td>NA</td></tr> </tbody> </table>	A[7:0]	vcom	A[7:0]	vcom	08h	-0.2	44h	-1.7	0Bh	-0.3	48h	-1.8	10h	-0.4	4Bh	-1.9	14h	-0.5	50h	-2	17h	-0.6	54h	-2.1	1Bh	-0.7	58h	-2.2	20h	-0.8	5Bh	-2.3	24h	-0.9	5Fh	-2.4	28h	-1	64h	-2.5	2Ch	-1.1	68h	-2.6	2Fh	-1.2	6Ch	-2.7	34h	-1.3	6Fh	-2.8	37h	-1.4	73h	-1.54	3Ch	-1.5	78h	-3	40h	-1.6	Other
A[7:0]	vcom	A[7:0]	vcom																																																																									
08h	-0.2	44h	-1.7																																																																									
0Bh	-0.3	48h	-1.8																																																																									
10h	-0.4	4Bh	-1.9																																																																									
14h	-0.5	50h	-2																																																																									
17h	-0.6	54h	-2.1																																																																									
1Bh	-0.7	58h	-2.2																																																																									
20h	-0.8	5Bh	-2.3																																																																									
24h	-0.9	5Fh	-2.4																																																																									
28h	-1	64h	-2.5																																																																									
2Ch	-1.1	68h	-2.6																																																																									
2Fh	-1.2	6Ch	-2.7																																																																									
34h	-1.3	6Fh	-2.8																																																																									
37h	-1.4	73h	-1.54																																																																									
3Ch	-1.5	78h	-3																																																																									
40h	-1.6	Other	NA																																																																									

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R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description										
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [70 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n]. Refer to Session 6.7 Waveform Setting										
0	1		LUT [70 bytes]																			
0	1																					
0	1																					
...	...																					
0	1																					
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set A[6:0] = 00h										
0	1		0	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀												
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set A[3:0] = 09h										
0	1		0	0	0	0	A ₃	A ₂	A ₁	A ₀												
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD										
0	1		A ₇	A ₆	A ₅	A ₄	0	0	A ₁	A ₀		A[7:0] = C0h [POR], set VBD as HiZ.										
												A [7:6] :Select VBD option <table border="1" style="margin-left: 20px;"> <tr> <td>A[7:6]</td> <td>Select VBD as</td> </tr> <tr> <td>00</td> <td>GS Transition Defined in A[1:0]</td> </tr> <tr> <td>01</td> <td>Fix Level Defined in A[5:4]</td> </tr> <tr> <td>10</td> <td>VCOM</td> </tr> <tr> <td>11[POR]</td> <td>HiZ</td> </tr> </table>	A[7:6]	Select VBD as	00	GS Transition Defined in A[1:0]	01	Fix Level Defined in A[5:4]	10	VCOM	11[POR]	HiZ
A[7:6]	Select VBD as																					
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01	Fix Level Defined in A[5:4]																					
10	VCOM																					
11[POR]	HiZ																					
												A [5:4] Fix Level Setting for VBD <table border="1" style="margin-left: 20px;"> <tr> <td>A[5:4]</td> <td>VBD level</td> </tr> <tr> <td>00[POR]</td> <td>VSS</td> </tr> <tr> <td>01</td> <td>VSH1</td> </tr> <tr> <td>10</td> <td>VSL</td> </tr> <tr> <td>11</td> <td>VSH2</td> </tr> </table>	A[5:4]	VBD level	00[POR]	VSS	01	VSH1	10	VSL	11	VSH2
A[5:4]	VBD level																					
00[POR]	VSS																					
01	VSH1																					
10	VSL																					
11	VSH2																					
												A [1:0] GS Transition setting for VBD <table border="1" style="margin-left: 20px;"> <tr> <td>A[1:0]</td> <td>VBD Transition</td> </tr> <tr> <td>00[POR]</td> <td>LUT0</td> </tr> <tr> <td>01</td> <td>LUT1</td> </tr> <tr> <td>10</td> <td>LUT2</td> </tr> <tr> <td>11</td> <td>LUT3</td> </tr> </table>	A[1:0]	VBD Transition	00[POR]	LUT0	01	LUT1	10	LUT2	11	LUT3
A[1:0]	VBD Transition																					
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10	LUT2																					
11	LUT3																					

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R/W#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], XStart, POR = 00h B[4:0]: XEA[4:0], XEnd, POR = 13h
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	B ₄	B ₃	B ₂	B ₁	B ₀		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		0	0	0	0	0	0	0	B ₈		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD8:0], POR is 000h
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		

7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		8:1	10:1	-	-	11-2
White Δ L 24h	Reduce		-	≤ 4	-	-	-
T _{update}	Image update time	at 25 °C	-	2100	-	ms	-

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

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8 Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

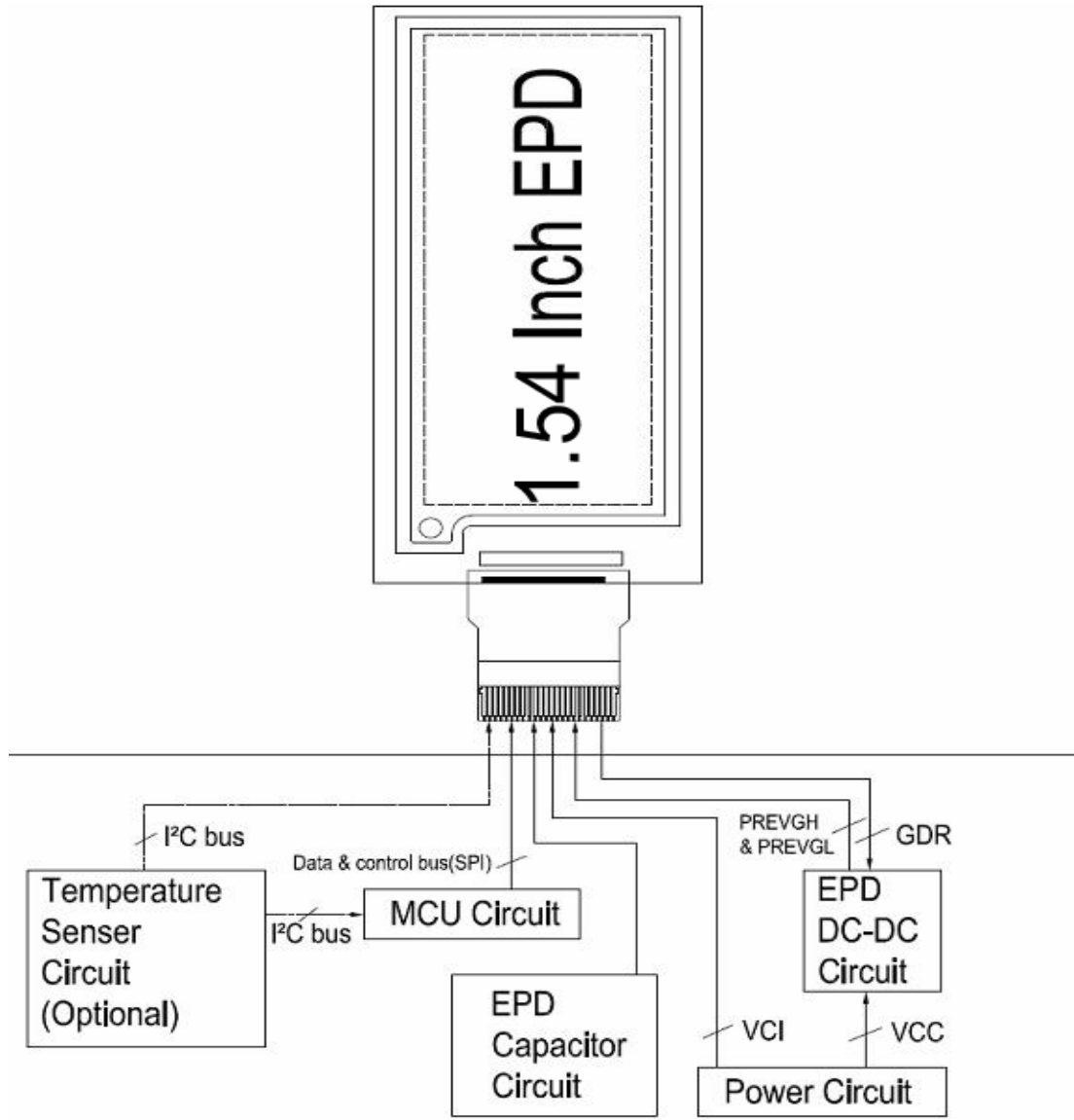
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9 Reliability Test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 168 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 168 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 168hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

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10 Block Diagram



Driver PCBA

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