1 AS-interface Features

- Actuator-Sensor Interface (AS-i) is the simplest automation networking solution.
- AS-Interface is the ideal choice for networking sensors and actuators in factory automation and process control environments.
- It is especially suitable for lower levels of plant automation where simple field devices, such as switches, need to communicate in a stand-alone local area automation network controlled by PLC or PC.
- AS-Interface is an open worldwide industry standard, IEC 62026-2 and EN 50295 (EU).

2 ASI4U

ASI4U is a monolithic CMOS integrated circuit certified for AS-i (Actuator Sensor Interface) networks.

ASI4U is a pin compatible successor of the A²SI integrated circuit.

Complete Specification V3.0 compliant

3 ASI4U Evaluation Board Features

The ASI4U Evaluation Board demonstrates the integration of the ASI4U IC in an application specific design case. This evaluation board helps to reduce development effort and development time for ASI4U application projects. It demonstrates an IC reference design, illustrates simple application circuits and deals with recommendations concerning necessary external components and PCB design issues.

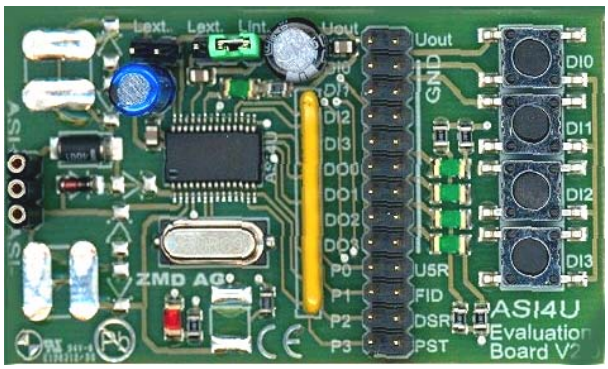

Figure 1: ASI4U Evaluation Board Hardware

Ordering name: ASI4U Evaluation Board V2.0
Ordering code: 3600100143

Application support is available through the e-mail hotline asi@zmd.de

ASI4U Evaluation Board

Application Note

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List of Tables:

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4 References

[1] Actuator Sensor Interface (AS-interface®) Complete Specification Version 3.0, Sep.16.2004

[2] ASI4U Data Sheet

[3] ZMD AS-interface Programmer Manual

[4] ASI4U Safety Advice

5 Scope

Application hints, mentioned in this document should be understood as guidelines for designing applications using the ASI4U. No guarantee can be given for completeness or fully conformity to certain standards. The ASI4U has been designed to comply with IEC 62026-2 and EN 50295, but since the ASI4U is a component and not a complete system, other components in a system may influence or even jeopardize the performance of the whole system. Therefore, system conformity with standards is not the responsibility of ZMD but remains at the customer.

Recommendations are based on experience with various ASI4U applications at this point in time and may be updated as more information becomes available. However, there is no guarantee that these recommendations will lead to a successful application in all cases.

It is recommended also to consult the ASI4U Data Sheet for complete and detailed information about full features and properties of the ASI4U.

6 ASI4U Evaluation Board Application Modes

The ASI4U Evaluation Board allows to evaluate different application modes by modifying the board hardware:

- Standard application mode with internal electronic inductor
- Standard application mode with external inductor
- Isolated transmitter mode for high symmetrical applications

The assembled and delivered form is the Standard application mode with internal electronic inductor. By change/add some electronic parts and by cutting some electrical connections the ASI4U Evaluation board can be modified for usage in different application modes.

6.1 Standard Application with Internal Electronic Inductor

The ZMD ASI4U Evaluation Board contains the following application as default assembly option.

This application mode is recommended for simple AS-interface applications with an maximal load of 55mA. The load capability of the internal electronic inductor is specified with 55mA. This current includes the ASI4U supply current of approximately 6mA as well.

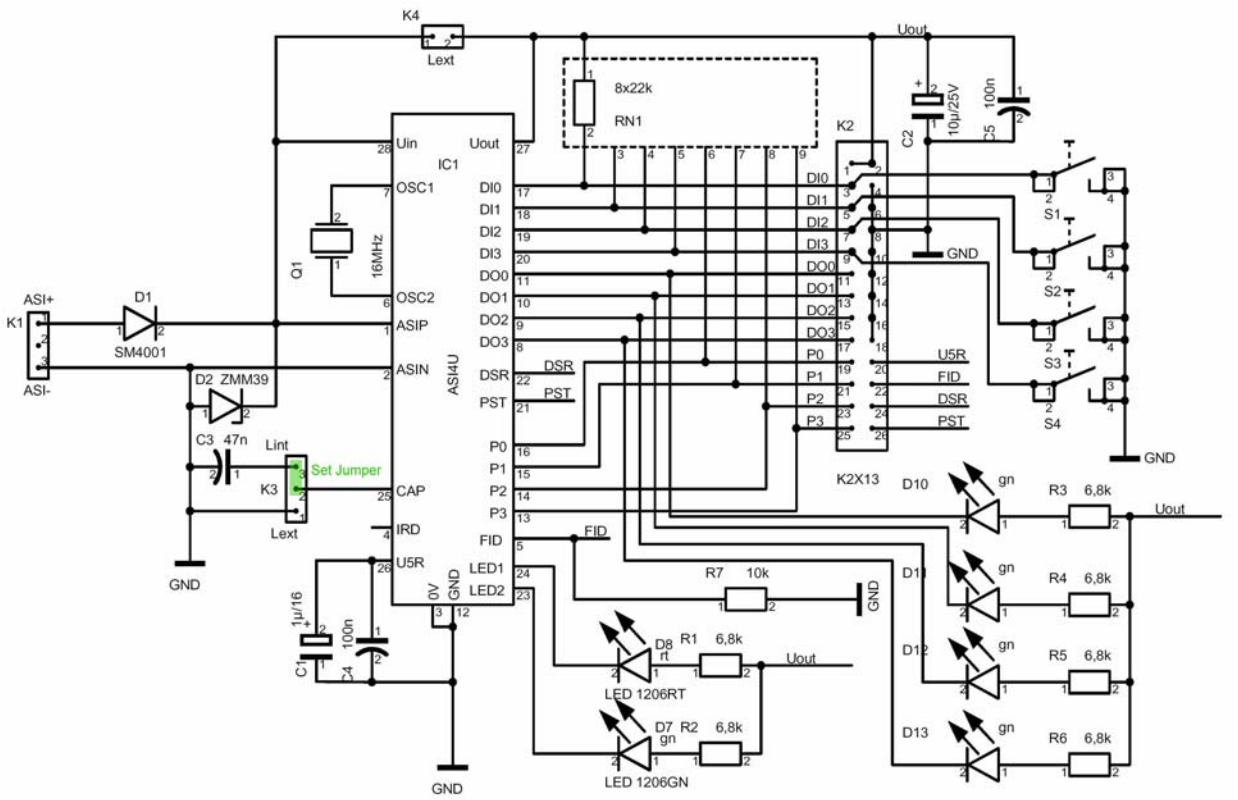

Figure 2: ASI4U Evaluation Board standard application using the internal inductor

The ASI4U provides a sensor supply, which is inductively decoupled from the AS-i bus voltage, at pin UOUT. The decoupling is realized by an IC internal electronic inductor circuit. The impedance (inductivity) can be adjusted by an external capacitor at pin CAP. For standard application a value of 47nF is recommended between pin CAP and GND.
The electronic inductor will be turned off if pin CAP is connected to 0V. This option requires an external connection between UIN and UOUT for proper IC operation, realized by bridge K4. The possibility to turn off the IC internal electronic inductor is helpful to realize high symmetrical extended power applications (see following chapter).
Overloading the electronic inductor for more than 2 seconds by drawing too much current shuts down the entire IC in order to avoid a shift of the input impedance, which may have negative influence to the communication of the remaining AS-i network clients. The fail-safe shutdown mode can only be left by power cycling the AS-i supply voltage.

In case of connection with external ground based hardware (sensor elements, actuators) or different supply voltage of connected components a galvanic isolation (e.g. optocouplers) at the input and output stages will be necessary. With respect to module symmetry and EMC insensitivity it is recommended to use the “Isolated Transmitter Mode Application” in case of GND loaded applications.

6.1 Standard Application with External Inductor

This application mode is a circuit proposal for simple AS-interface applications with an maximal load of more than 55mA. Further it is recommended to avoid IC internal power dissipation provoked by the internal electronic inductor (high temperature environment). The load capability of the internal electronic inductor is limited 55mA. To disable the internal electronic inductor it is necessary to connect the ASI4U CAP pin (PIN25) to GND. Thereby the internal circuit will be switched into a high impedance state. To provide the sensor voltage at Uout a connection between Uin (PIN27) and Uout (PIN28) becomes necessary (close Jumper K4).

Note that this application may also influence module symmetry and EMC behavior if high currents are decoupled in an unsymmetrical way (only one inductor in the positive path) and module GND is connected to equipment GND (Earth).

In case of separate external sensor/actuator supply voltage or a different supply voltage for the connected components a galvanic isolation (e.g. optocouplers) at the input and output stages is necessary.

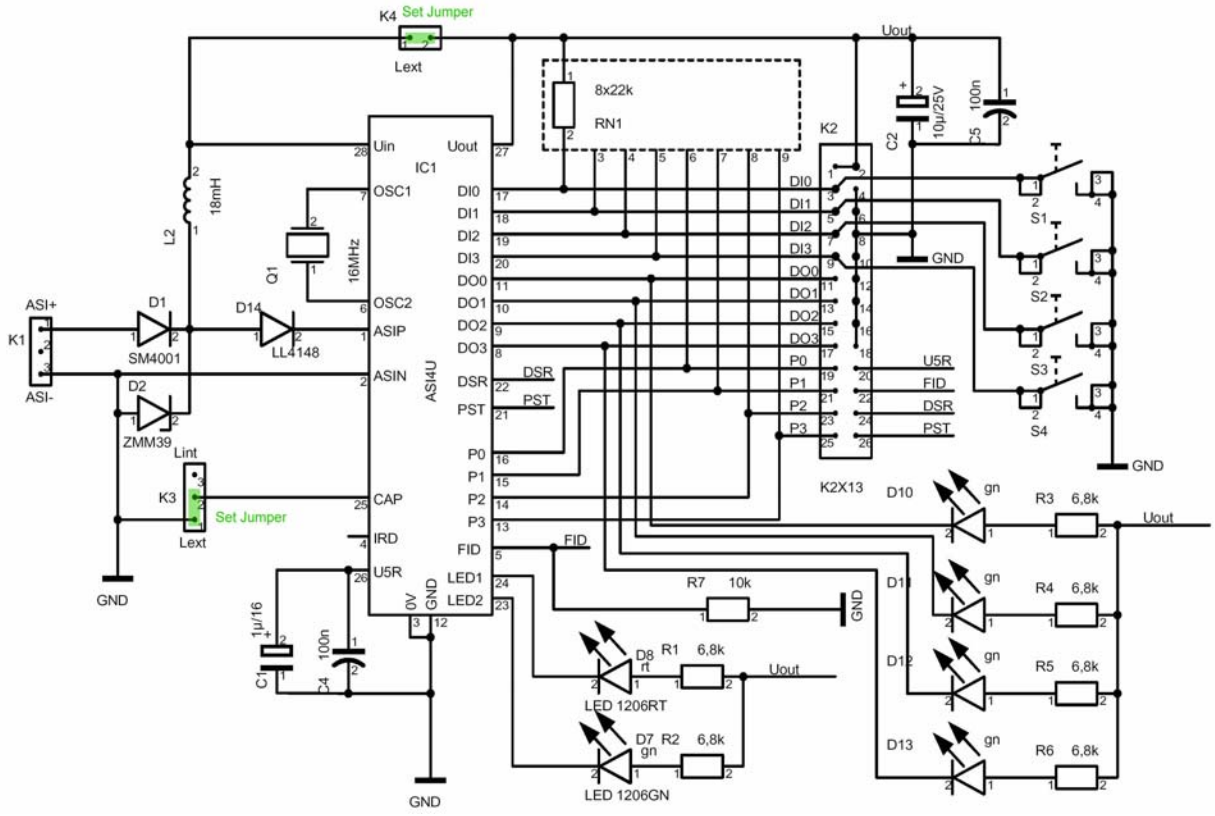

Figure 3: ASI4U Evaluation Board standard application with external inductor

The inductor L2 in the positive path works as decoupling unit to separate the ASi pulses from the bus voltage. During fast power switching events at Uout or during module switch off phase a negative voltage pulse will be provoked at L2. To keep this voltage spikes away from the sensitive ASIP pin at the ASI4U a additional diode (D2) is recommended.

The Diode D14 protect the ASIP input from negative voltage spikes generated by switching events at the inductor L2.

Following changes are necessary to use the ASI4U Evaluation Board in this application mode:

	Refer to Mark in Figure 4
• set jumper K4 (connect ASI4U pin Uin and pin Uout)	1
• set jumper at K3 to GND (switch pin Cap to GND)	2
• cut wire at footprint of L2	3
• add inductor L2, value 18mH	3
• cut wire at footprint of D14	4
• add diode D14 (1N4148) to protect ASIP from negative voltage spikes	4

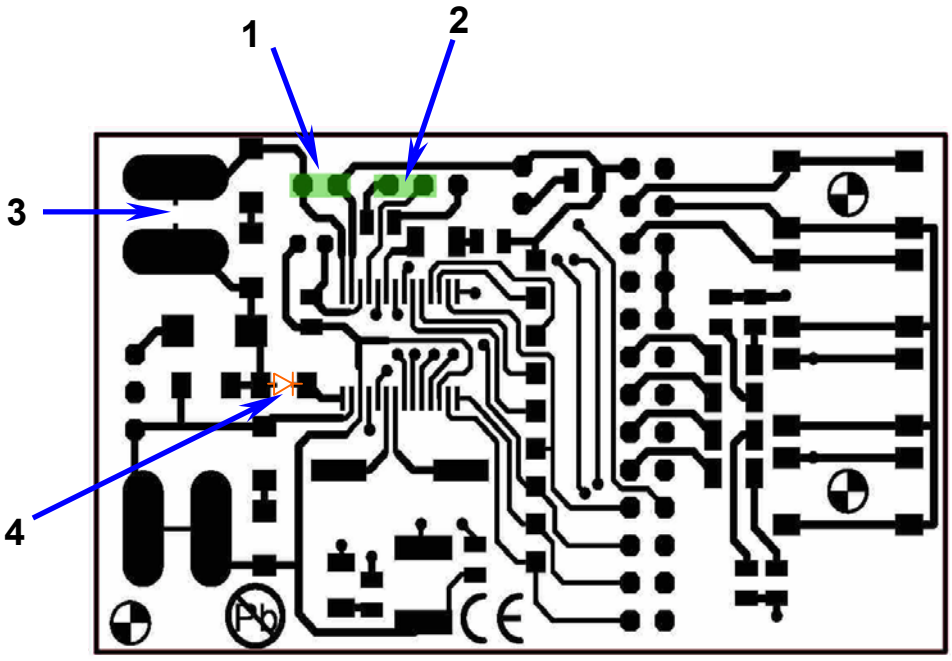

Figure 4: ASI4U Evaluation Board Top Layer and changes for standard application with external inductor

6.2 Isolated Transmitter Mode for High Symmetrical Applications

The ASI4U is the first AS-interface IC that supports floating operation of the AS-i receiver and transmitter (within certain limits) in relation to IC ground. So far, the ASIN pin always had to be connected to the same potential like IC ground, preventing full symmetrical input circuits with external coils. The figures illustrate the new functionality. If one compares the relation Z1 / Z2, which is a measure for symmetry of the AS-i module input towards machine ground, it becomes obvious that the new circuit is more symmetrical since Z1 and Z2 are more equal than in the conventional solution.

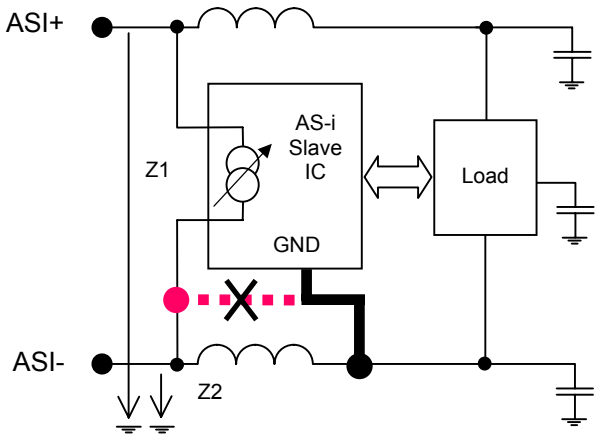

Figure 5: Newly supported application of AS-i IC with two external coils

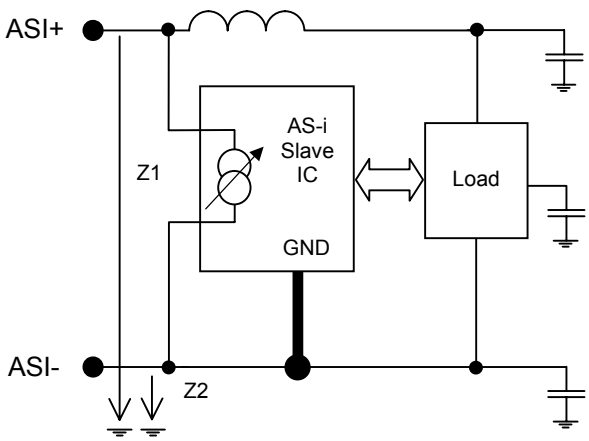

Figure 6: Conventional application of AS-i IC with one external coil

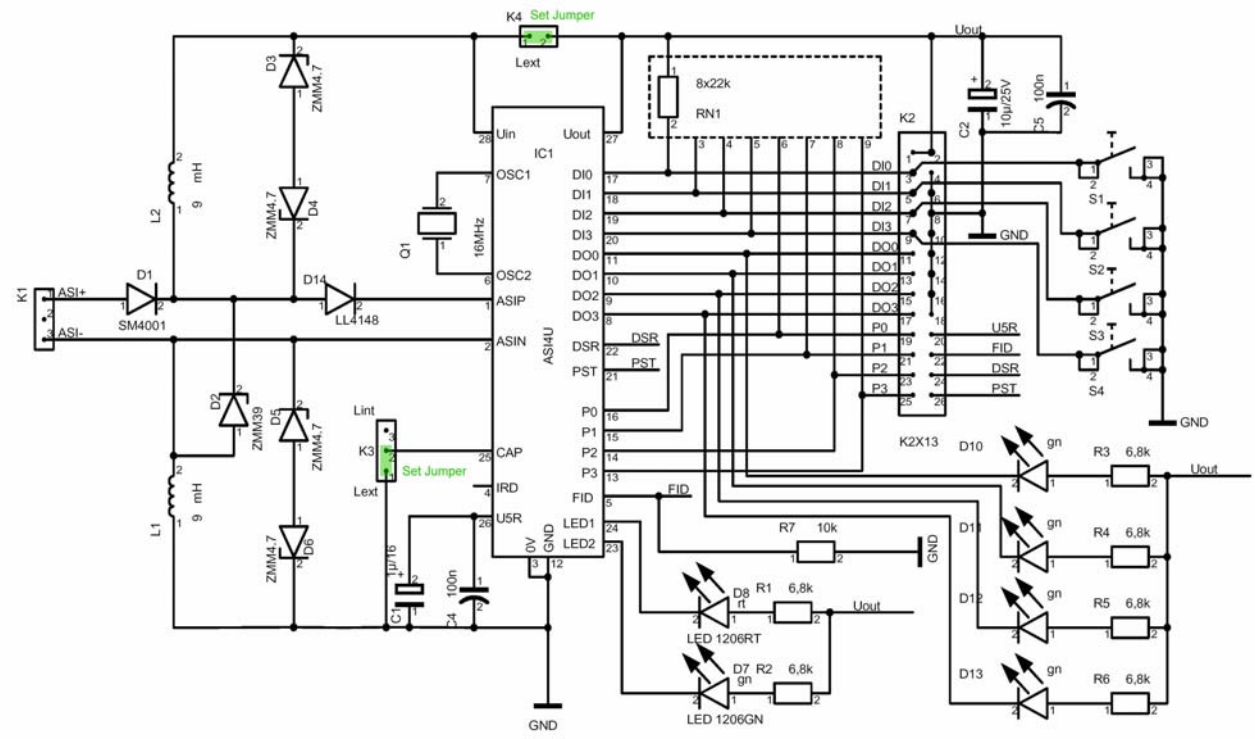

Figure 7: ASI4U Evaluation Board with Isolated Transmitter Mode for High Symmetrical Applications

The isolated transmitter mode is recommended for high symmetrical, high power applications. This application makes the external galvanic isolation with optocouplers unnecessary.
D5 and D6 are important to protect the ASIN pin from negative voltage compared to 0V/GND pin. This negative voltage, which is provoked by module switch on/off events at inductor L1, should not exceed 6V. Diodes D3 and D4 are necessary for module symmetry. A fast operating fuse is recommended in the final application to avoid clamping of the AS-I bus voltage by an module internal short circuit between GND and Uout. This clamping will be provoked by a created path trough D3,D4,D5 and D6. To avoid clamping the ASi Bus in case of a short circuit diode D3 can be replaced by an capacitive equivalent capacitor. For the ZMD ASI4U application board in combination with ZMM4,7V diodes a capacitor of 68pF is recommended instead of D3. See also following picture. The replacement of this diode by a capacitor should be evaluated by measuring the impedance and symmetry characteristic over the specified frequency range.

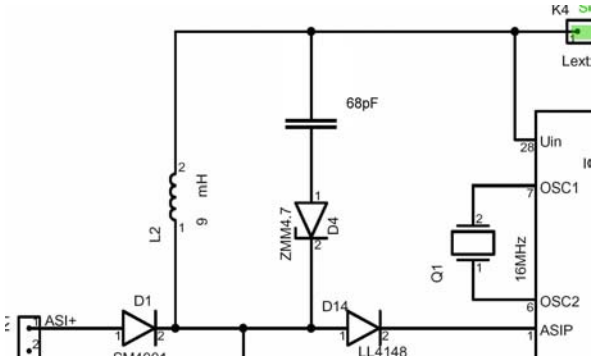

Figure 8: Replacement of D3 by a Capacitor

Following changes are necessary to use the ASI4U Evaluation Board in this application mode:

	Refer to Mark in Figure 9
• set jumper K4 (connect ASI4U pin Uin and pin Uout)	1
• set jumper at K3 to GND (switch pin Cap to GND)	2
• cut wire at footprint of L2	3
• add inductor L2, value 9mH	3
• cut wire at footprint of L1	4
• add inductor L1, value 9mH	4
• cut wire at footprint of D14	5
• add diode D14 (1N4148) to protect ASIP from negative voltage spikes	5
• add diode D3 (ZMM4,7) for symmetry to ASIN	6
• add diode D4 (ZMM4,7) for symmetry to ASIN	7
• add diode D5 (ZMM4,7) to protect ASIN from negative potential	8
• add diode D6 (ZMM4,7) to protect ASIN from negative potential	9

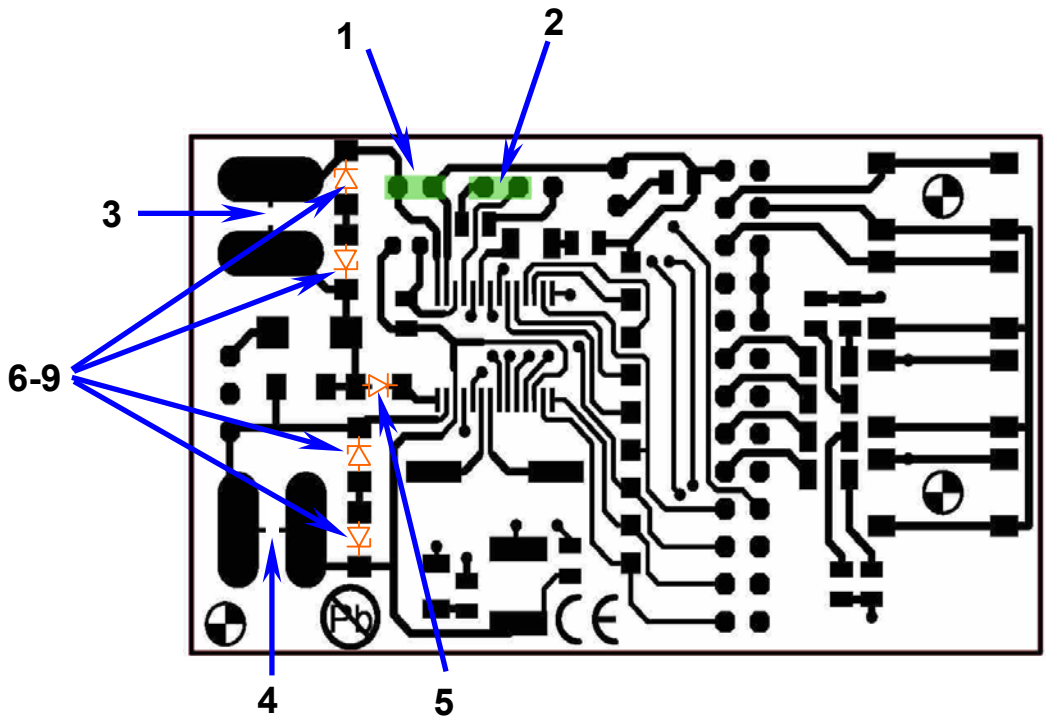

Figure 9: ASI4U Evaluation Board Top Layer and changes for standard application with external inductor

6.3 Complete Schematic Diagram

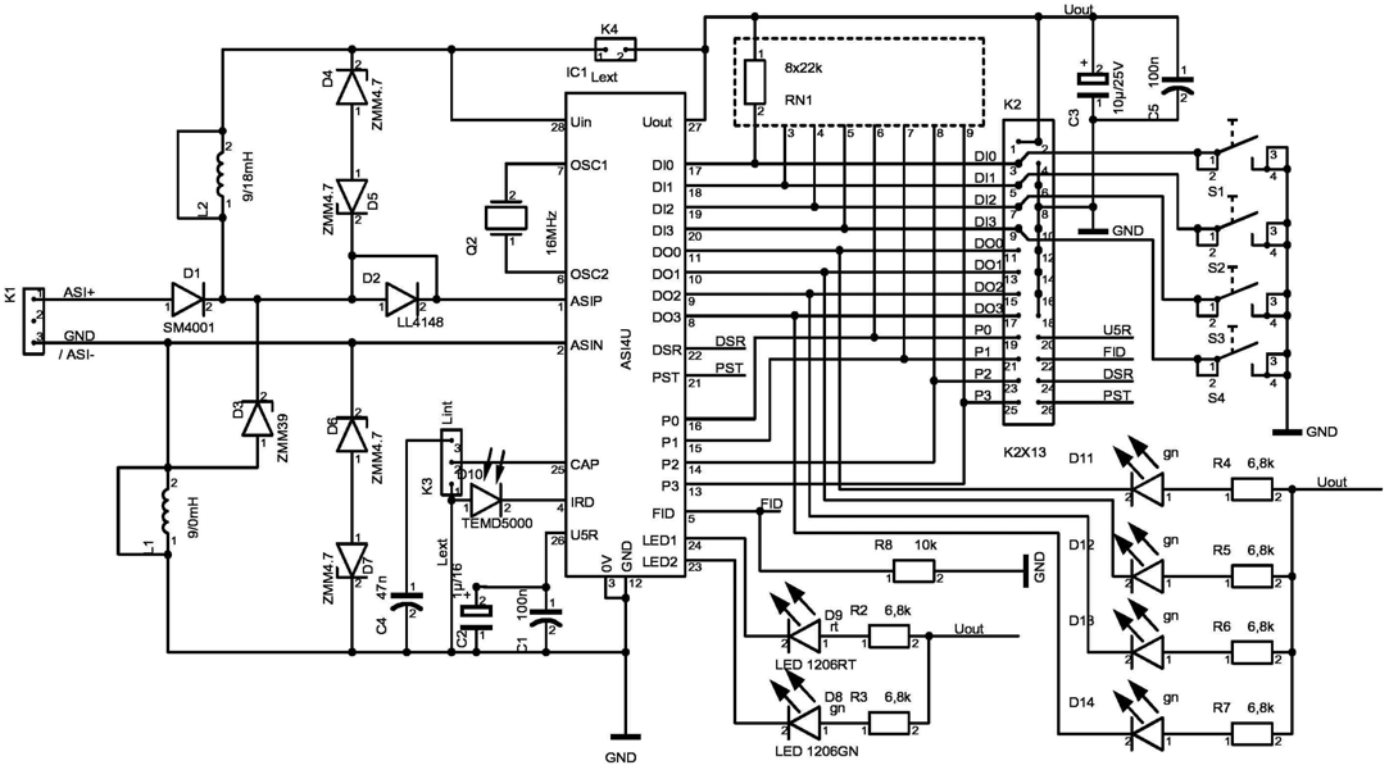

Figure 10: ASI4U Evaluation Board full Schematic

6.4 Complete Component Placement Specification

The complement placement specification contains all assembly options with all electronic parts. The detailed application specific assembly form has to fit to the operation mode of the module. Standard delivery form is the normal slave operation mode with internal electronic inductor.

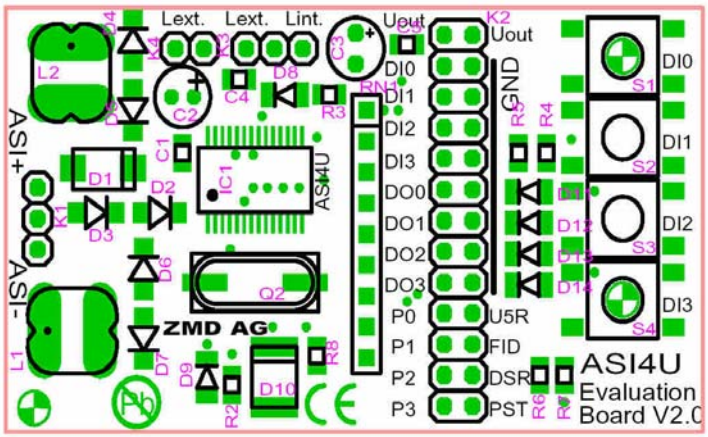

Figure 11: ASI4U Evaluation Board complete placement option

The following table shows a complete part list for all assembly options. All part names correspond with part names in figure 10 and 11.

Table 1: Part list

No	Name	Value	Package	Comment
1	C1	100n	0805	
2	C2	1µ/16V	4x4mm	
3	C3	10µ/35V	5x5mm	
4	C4	47n	0805	
5	C5	100n	0805	
6	D1	SM4001	DO214	
7	D10	TEMD5000	TEMD5000	Manufacturer: Temic
8	D11	LED GN	1206	
9	D12	LED GN	1206	
10	D13	LED GN	1206	
11	D14	LED GN	1206	
12	D2	LL4148	MINI-MELF	
13	D3	ZMM39	MINI-MELF	
14	D4	ZMM4,7	MINI-MELF	
15	D5	ZMM4,7	MINI-MELF	
16	D6	ZMM4,7	MINI-MELF	
17	D7	ZMM4,7	MINI-MELF	
18	D8	LED GN	1206	
19	D9	LED RT	1206	
20	IC1	ASI4U	SSOP28	AS-interface IC (ZMD)
21	K1	strip connector 3 pin	1X03	
22	K2	strip connector 2x13 pin	grid 2,54mm	
23	K3	strip connector 3 pin	grid 2,54mm	
24	K4	strip connector 2 polig	grid 2,54mm	
25	L1	9mH/18mH	ASI-Coil WE-ASI	WUERTH Electronic
26	L2	9mH	ASI-Coil WE-ASI	WUERTH Electronic
27	Q2	16MHz/8MHz	HC49/4H	
28	R2	6,8k	0805	
29	R3	6,8k	0805	
30	R4	6,8k	0805	
31	R5	6,8k	0805	
32	R6	6,8k	0805	
33	R7	6,8k	0805	
34	R8	10k	0805	
35	RN1	8x22k	9-SIL-1	
36	S1	SMD-push button	6x6mm	
37	S2	SMD-push button	6x6mm	
38	S3	SMD-push button	6x6mm	
39	S4	SMD-push button	6x6mm	

7 ASI4U Configuration

7.1 Internal EEPROM

7.1.1 General Information

The ASI4U provides an on-chip E²PROM with typical write cycle times of 12.5 ms and read cycle times of 110ns. The non-volatile memory is divided into an user area and a firmware area. The user area stores the address of a circuit configured as a slave, along with an ID_Code (ID code extension 1) assigned by the user. If the IC is operating in extended address mode, then the most significant bit of this 4-bit data word is used to determine whether it is a so-called A-slave or B-slave.

The firmware area is used to select the operating mode (master, repeater, slave) and for storage of component-specific slave identification codes. Also, flags in this section enable or disable special IC features. By setting the Program_Mode_Disable flag in the EEPROM, the manufacturer of AS-i devices can protect the whole firmware area against accidental overwriting.

AS-i Complete Specification compliance note:

In order to ensure full compliance with the AS-i Complete Specification, the *Program_Mode_Disable* flag must be set in the final manufacturing and configuration process before an AS-i slave device is being delivered to field application users.

7.1.2 EEPROM Content

Table 2: EEPROM Content

ASI4U internal E²PROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
0	0 … 3	*A0 … A3*	Slave address low nibble
1	0	*A4*	Slave address high nibble
2	0 … 2	*ID1_Bit0 … ID1_Bit2*	*ID_Code_Extension_1*
2	3	*ID1_Bit3*	*ID_Code_Extension_1*, A/B slave selection in extended address mode
3 … 7			Not implemented
8	0 … 3	*ID_Bit0 … ID_Bit3*	*ID_Code*
9	0 … 3	*ID2_Bit0 … ID2_Bit3*	*ID_Code_Extension_2*
A	0 … 3	*IO_Bit0 … IO_Bit3*	*IO_Code*
B	0	*Multiplex_Data*	Multiplexed bi-directional Data Port mode
	1	*Multiplex_Paramter*	Multiplexed bi-directional Parameter Port mode
	2	*P0_Watchdog_Activation*	Watchdog can be activated/deactivated by the logic value at parameter pin P0. Watchdog_Active must **not** be set.
	3	*Watchdog_Active*	Communication watchdog is continuously activated.

ASI4U internal E²PROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
C	0	*Master_Mode*	If set, Firmware Area cannot be accessed.
	1	*Program_Mode_Disable*	If set, Firmware Area is protected against overriding.
	2	*Repeater_Mode*	If set, Firmware Area cannot be accessed.
	3	*Invert_Data_In*	All Data Port inputs are inverted.
D	0 … 3	*DI_Invert_Configuration*	Enables separate input data inverting for selected DI pins. *Invert_Data_In* must **not** be set.
E	0 … 3	*DI_Filter_Configuration*	Enables unitary anti-bouncing filters for selected DI pins
F	0 … 2	*DI_Filter_Time_Constant*	Defines a time constant for the input filter. For coding rules see chapter **Fehler! Verweisquelle konnte nicht gefunden werden.**.
	3	*P1_Filter_Activation*	If flag is set, the logic value at the parameter pin P1 determines whether the filter function is active or inactive If flag is not set, *DI_Filter_Configuration* activates the filter function.
10	0 … 3	*Data_Out_Configuration*	Defines whether the corresponding Data Port output pin is driven by the Data Output Register (sensitive to the *Data_Exchange* command) or the *Data_Out_Value* Register (E²PROM configured).
11	0 … 3	*Data_Out_Value*	Stores *static Data Port output* value if selected by *Data_Out_Configuration*
12	0	*Enhanced_Status_Indication*	If set, Enhanced Status Indication Mode according to AS-i Complete Specification is activated. **Activates LED2 output! For compatibility to A²SI board layouts this flag must not be set (=‘0’).**
	1	*Dual_LED_Mode*	If set, LED1 and LED2 output signals are controlled to comply with Dual LED indication schemes of AS-i. Generated signals depend also on value of *Enhanced_Sta-tus_Indication* flag. Direct connection of a Dual LED is supported. **Activates LED2 output! For compatibility to A²SI board layouts this flag must not be set (= ‘0’).**
	2	*FID_Invert*	The FID input value is inverted before further processing
	3	*Safety_Mode*	If set, the ASI4U Safety Mode is enabled and a special data input routing is activated.

User Area *Firmware Area*

7.1.3 EEPROM User Area Write Access

It is possible to program the content of the address field (EEPROM address 0) and the ID_Code_Extention_1. Therefore particular master calls (*Address_Assignment* (ADRA) or *Write_Extended_ID_Code1* (WID1)) will be provided. For a functional description of the AS-i master calls, please refer to the AS-i Complete Specification [1]. Both calls are only available at slave address 0x0. By the definition of the master calls it is clear which EEPROM locations must be addressed even if no specific selection is made. The Address_Assignment will effect EEPROM address 0x0 and 0x1. The Write_Extended_ID_Code1 accesses EEPROM address 0x2.

7.1.4 EEPROM Firmware Area Write Access

A write access to the internal EEPROM is only possible if the following restrictions are observed:

- ASI4U IC is configured to Slave-Mode
- ASI4U IC is programmed to slave address 0
- Only the ASI4U IC to program is connected to the system

The *program mode* is intended to be used during production set-up of an AS-i slave component at the manufacturer's site. It can be entered by sending the *Enter_Program_Mode* call (refer to AS-i Complete Specification). The reception of the *Enter_Program_Mode* (PRGM) call sets the *Program_Mode* Flag within the ASI4U. It should be noted that no response is generated to the *Enter_Program_Mode* call.

If the *Program_Mode* flag is set, Write_Parameter (WPAR) and Data_Exchange (DEXG) calls have other meanings. The address bits A3...A0 of the master telegrams are then used to address one of the nineteen memory locations of the EEPROM. Address bit A4 is don't care. The information bits I3...I0 (normally used for output data) carry the data which shall be stored or is read from the EEPROM. The Write Parameter initiates a write access. The Data_Exchange is used to read out a specific EEPROM word.

Important: In *Program_Mode* the ASI4U will generally accept master calls of any slave address regardless of the value of its own address register.

Any *Write_Parameter* (WPAR) call initializes an autonomous write process within the IC. The status of the write process can be monitored by evaluating the status register of the IC. If bit S0 is set (logical '1') the write process is not finished yet and the programming data is still volatile. If bit S3 is set, the write procedure did not successfully complete either because the write cycle was interrupted or due to an internal error. In order to program the data correctly the write request should be repeated. The status register can be read using the AS-i Master call Read_Status.

7.1.5 Recommended EEPROM Access Procedures in Program Mode

As outlined above, the content of the EEPROM can be set-up in *program mode* using master call *Write_Parameter* (WPAR) for write access and *Data_Exchange* (DEXG) for read access for

verifying programmed data. As read and write access can not be performed within a single AS-i cycle (master call + slave response), read and write procedures must apply to several rules:

Write Access:

In general, the slave status shall be checked after the master has issued a call that writes data into the EEPROM. As long as the slave status indicates that the write process is still going on (S0 = 1, S3 = 0), no further EEPROM accesses should be requested (refer to 7.1.2.1 for AS-i Complete Specification compliance).

An EEPROM programming procedure should be created in consideration of the following steps:

1. Set slave address to zero (if not yet done) by using *Delete_Address* (DELA) call.

2. Enter the ASI4U program mode by transmitting *Enter_Program_Mode* (PRGM) call.

3. Check the IC's status by using the *Read_Status* (RDST) call (this is recommended prior to attempting any write access to the EERPOM). If status bit S0 = 1, wait at least 25 ms and repeat this step.

4. Perform the write access by transmitting a *Write_Parameter* (WPAR) call. As already mentioned – compared with normal operation mode, WPAR works differently in *Program_Mode.*

5. Check the IC's status again (*Read_Status* (RDST) call). If S0 was reset to '0', write cycle finished successfully and next EEPROM location may be accessed.

6. Leave the program mode by transmitting a *Reset* (RST) call.

7.1.6 EEPROM Configuration Tool

For module evaluation and configuration ZMD provides a special evaluation tool. The ZMD AS-interface Programmer makes it easy to configure the IC internal EEPROM. A graphical user interface allows to configure the EEPROM content in an easy way.

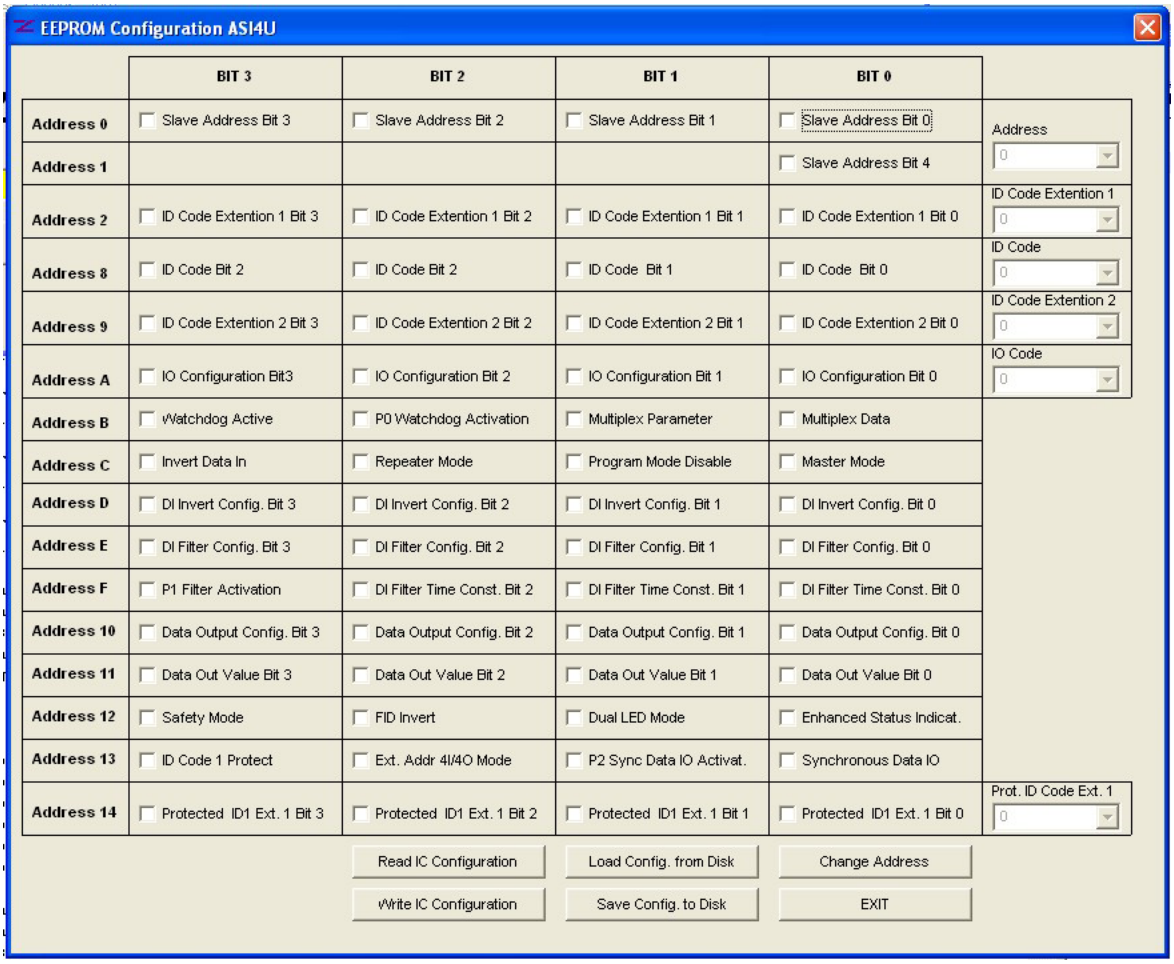

Figure 12: ZMD AS-interface Programmer - ASI4U EEPROM programming

For detailed information refer to the ZMD AS-interface Programmer Manual [3].

7.2 Operation Modes

7.2.1 Overview

Basically, ASI4U can operate in four modes. These are ***slave mode, slave mode with safety feature***, ***master mode***, and ***repeater mode***. After a reset, the circuit enters one of these modes depending on the non-volatile EEPROM flags.

Table 3: ASI4U Operation Modes

Mode	Master_Mode_Bit	Repeater_Mode_Bit	Safety_Mode_Bit	Remarks
Slave Mode	0	0	0	Program mode possible
Slave Mode with Safety Feature	0	0	1	Program mode possible
Master Mode	1	0	0	Program mode impossible
Repeater Mode	1	1	0	Program mode impossible
Monitor Mode	0	1	0	Program mode impossible

ZMD delivers ASI4U pre-programmed devices in two configurations:

- *Slave Mode:* By default ASI4U ICs are delivered in slave mode. In this case, the entire EEPROM is cleared (all bits set to zero). Slave address is equal to zero and ASI4U is operating in standard address mode. By entering program mode, initial settings can be changed. An IC in slave mode can be configured to any other operational mode by using the program mode.

- *Master Mode:* Bit 0 (*Master_Mode_Bit*) at EEPROM address 0xC set to '1' selects master operation mode of the IC. The remaining memory space is cleared (all bits set to zero). In Master Mode, it is impossible to enter the program mode of the ASI4U. Once the IC is set to Master Mode, the configuration cannot be changed again.

Check the ASI4U Data Sheet or contact ZMD for detailed ordering information.

6.1.2 Regular Slave Operation

The AS-i Complete Specification **[1]** defines a extended address mode which permits a maximum of 62 slaves to be operated on a single network. Since the basic format of a telegram was not changed, slaves using old and new addressing standard can still work together in one system. However, it should be noted that *Standard Slaves* (slaves which use the old addressing standard) will consume two addresses of the address space which otherwise could be assigned to two slave addresses in extended mode.

To accommodate this enhancement, additional addresses were not simply counted up from 32 to 61, but two types of slaves (A-type, B-type) were defined (**Figure 13).** A standard slave will be abbreviated with S-slave. A- and B-type slaves share the same 5-bit standard address but can be separated through *Information Bit* I3 of the Master telegram which acts as the select bit (see also AS-i Complete Specification **[1]**). **Figure 13** demonstrates the meaning of I3 changes in extended address mode. I3 cannot be used to transfer data from the master to the slave, thus the data word can only be 3 bits wide in this direction. However, data transfers from a slave to the master remain 4 bit wide.

Configuration information that defines whether a slave is in extended address mode or not depends on the value of the non-volatile ID-Code register. The AS-i Complete Specification [1] reserves the value 0xA as the ID-Code for slaves in extended address mode. Any other value of the ID-Code register sets the ASI4U to standard address mode operation.

Configuration of an A- or B-Slave is done by bit 3 of *ID_Code_Extension_1* register. If a slave is in extended address mode, the value of this bit is compared to the SEL bit (I3 bit) of the master call. The call is accepted if they match and address register of the slave equals the 5 address bits in the master telegram. It should be noted that bit I3 of a master telegram may represent the bit (SEL) or the inverted select bit (~SEL) depending on type of call.

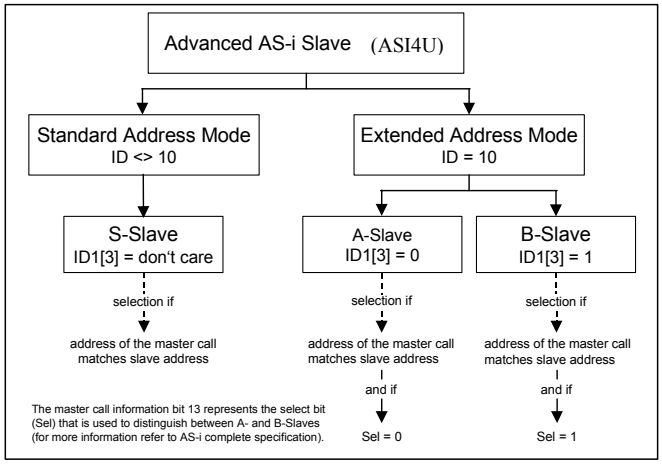

Figure 13: Slave Addressing Modes

7.2.2 Master-, Repeater-, Monitor Mode

The ASI4U in master or repeater mode operates as a physical layer transceiver. No logical telegram or algorithm generation is supported. An incoming Manchester-II coded data stream will be converted into an AS-interface telegram and vice versa. In master and repeater mode different UART functions are activated to signal strobe and error states. A connected microcontroller communicates with the ASI4U via this Manchester bit stream ant recognized the provided strobe and error signals. The AS-interface protocol machine must be integrated into this microcontroller.

For detailed description see ASI4U Datasheet.

7.2.3 Safety Mode

However, the ASI4U provides additional data preprocessing functions at the data input channel. These are mainly the anti bouncing filters and the new Synchronous Data I/O Mode, defined in the Complete Specification 3.0. The fault reaction time of an AS-i Safety module could increase by 40ms if some of the new features became activated by intention, by accident or hardware fault.

For Detailed Information refer to the ASI4U Datasheet[1] and to the ASI4U Safety Advice[4].

For Safety applications it is strongly recommended to use the special ASI4U safety mode, which provides a self controlled data routing of the input data in the internal hardware flow.

The ASI4U is designed to allow replacement of A²SI ICs in existing board layouts and applications. It is also strongly recommended to use the new ASI4U Safety-Mode, if the ASI4U shall replace the A²SI in existing ASI-Safety designs. Only then, the same fault reaction times as with the A²SI are guaranteed.
For compatibility with the modified data input routing in Safety Mode, the user has to adapt the safety code table stored in the external micro controller. Only Safety Code Sequences containing the value 1110 are permitted.

If the IC is operated in Safety Mode, the user must pay special attention to the fact that the *Synchronous Data I/O Mode* as well as the *Data Input Filters* remain disabled by appropriate E²PROM configuration.
Application of the ASI4U in Standard Mode (no Safety Mode enabled) for AS-i Safety products is basically possible if an additional Fault Reaction Time of 40ms is taken into account.

Further detailed informations are available in the ASI4U Datasheet.

7.2.4 A²SI Compatibility Mode

The ASi4U was also designed to replace the A²SI in existing designs. Both ICs are pin and drop in compatible. In standard delivery form the ASI4U operates compatible to the A²SI. All new and optional features must be enabled by setting the responsible EEPROM bit.

Note: Due to complex analog designs the system behavior of a module which replaces the A²SI by an ASI4U must be verified to guarantee the specification conform operation.

In order to provide a LED2 output signal, according to the AS-intercace Complete Specification, a further pin becomes necessary. The U5RD Pin of the A²SI was replaced by the LED2 Pin of the ASI4U. In A²SI compatibility mode this pin is switched to high impedance state in order to avoid leakage current trough this pin. New options to drive this LED2 pin must be enabled by setting the responsible EEPROM bit (see ASI4U Datasheet).

7.3 AS-i Channel Selection

An ASI4U circuit operating in slave mode has three different options for AS-i input channels. The first one is the normal channel which can be connected to a standard AS-i cable. The second channel, the so-called Infrared Addressing Channel, is dedicated for simplified configuration of AS-i slaves in the final field application. Third option is the CMOS mode of the IRD channel.

7.3.1 AS-i channel

Via the ASIP pin and ASIN pin the IC is able to communicate in standard AS-i communication modus at the AS-interface bus. At the AS-i bus power and data will be transferred at a 2-wired cable. The AS-i channel has the possibility to separates this combination of power and data. The data information from the bus will be blocked to the Voltage output Via the internal electronic inductor. The voltage output (Uout) can provide up to 55mA output current at a voltage level of 24V

(not stabilized). Modulated data information will be handled separate in the AS-I receiver unit. The receiver unit provides digital output information for the internal state machine.

7.3.2 Infrared channel

The infrared channel was designed for programming-, configuration- and maintenance purposes in the target field application. The automatic detection and channel selection in case of a received telegram is a new innovation. To lock this channel to the current telegram input channel a so called “Magic sequence” has to be applied to the infrared input. This sequence contains 5 syntax correct AS-i calls(e.g. read status). After sending this commands within a timeslot of 8ms the IC locks the active communication channel to this port. The regular AS-i channel becomes inactive. This channel switching principle allows to communicate with a AS-i salve module during running AS-i communication.

The receiving path of the IR-channel is supported by a special photo-diode input (IRD) while the output transmitter utilizes the status indicator LED to send response telegrams. Both, the input and the output process use MAN-II-coded signals. In both cases, emitted light corresponds to logic high in the MAN-II-coded signal. The IR-input automatically adapts to the amplitude of the photo current signal supplied by a photo-diode.

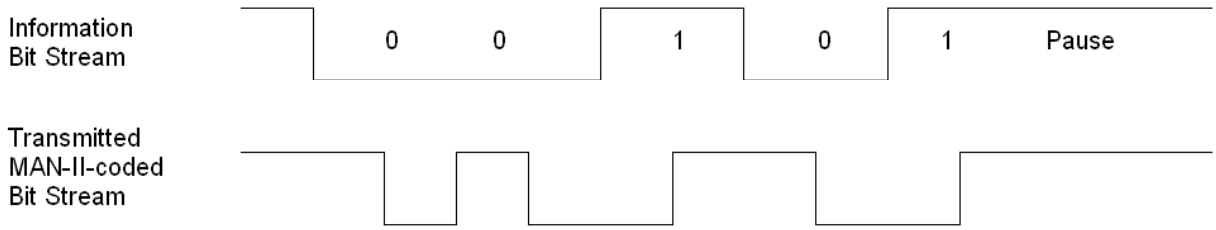

Figure 14: Manchester-II coded data stream

After reset, the ASI4U returns to the normal operation mode at the standard AS-i channel. This reset may be a power on reset, a reset at DSR input pin or a reset telegram as well.

Further detailed information is available in the ASI4U Datasheet.

7.3.3 CMOS Channel

In addition to the AC current input mode, the IRD input can also operate in CMOS input mode. Mode switching is only possible as long as the IC has not locked to the addressing channel by reception of a Magic Sequence already. On principle, that input mode that lead to the activation of the addressing channel will remain locked until the addressing channel is deactivated (by IC reset).

The CMOS mode is entered if the IRD input voltage is above 2.5V (logic high) for more than 7.680 ms (-6.66%). It is left, if the IRD input voltage is below 1.0V (logic low) for more than 7.680 ms (-6.66%). The initial input mode after IC initialization is determined at the end of the initialization phase and depends on the value of the IRD input signal at that time.

8 Application Info

8.1. Pin Description

Table 4: Pin List

28-Pin SSOP Pin Number	Name	Type	Description	Remarks
1	ASIP	INOUT	to be connected to the AS-i-line ASI+ via reverse polarity protection diode	
2	ASIN	INOUT	to be connected to the AS-i-line ASI-	ASIN should be interconnected with the 0V-pin. Route from ASI- to ASIN and then to 0V.
3	0V	SUPPLY	Common 0V for all IC-ports except ASIP/ASIN	Must to be interconnected with GND. This interconnection should be as short as possible to avoid voltage drops between the pins.
4	IRD	IN	Addressing channel input	In slave mode connected to a photo-diode or as CMOS input, in master/repeater mode regular CMOS-input. Note: In slave mode this is a very sensitive input.
5	FID	IN	Input peripheral fault indication	Refer to DI0
6	OSC2	INOUT	Crystal oscillator (8 or 16MHz x-tal)	The x-tal oscillator does not require additional electronic components.
7	OSC1	IN	Crystal oscillator / external clock input	
8	DO3	OUT	Output of data D3	Open-drain output
9	DO2	OUT	Output of data D2	Open-drain output
10	DO1	OUT	Output of data D1	Open-drain output
11	DO0	OUT	Output of data D0	Open-drain output
12	GND	SUPPLY	Digital IO ground	NOTE: GND and 0V must be connected externally by low resistance and low inductance wiring.
13	P3	I/O	Input/output of parameter P3	Open-drain output, input refer to DI0
14	P2	I/O	Input/output of parameter P2 / Receive Strobe in ”Master Mode”	Open-drain output, input refer to DI0
15	P1	I/O	Input/output of parameter P1 / Power Fail in ”Master Mode”	Open-drain output, input refer to DI0
16	P0	I/O	Input/output of parameter P0 / Data Clock in ”Master Mode”	Open-drain output, input refer to DI0
17	DI0	IN	Input of data D0	Contains an internal pull-up transistor, The input voltage is internally clamped to 5V (consider higher input current if V_{IN} > 5V)
18	DI1	IN	Input of data D1	Refer to DI0

28-Pin SSOP Pin Number	Name	Type	Description	Remarks
19	DI2	IN	Input of data D2	Refer to DI0
20	DI3	IN	Input of date D3	Refer to DI0
21	PST	INOUT	Parameter strobe output	Open-drain output, input refer to DI0 The input is only used for production test
22	DSR	INOUT	Data strobe output/reset input	Open-drain output, input refer to DI0
23	LED2	OUT	Output LED "AS-i-Diagnosis"	Open-drain output in case of new LED functionality is activated
24	LED1	OUT	Output LED "AS-i-Diagnosis" / addressing channel output	Open-drain output, there is an input for test reasons
25	CAP	INOUT	Control capacitor fot internal electronic inductor	Recommended values for C is 47nF to provide a conform impedance
26	U5R	Voltage OUT	Stabilized 5V supply	Can be used to that supply external circuits with up to 4mA
27	U_{OUT}	Voltage OUT	Unstabilized external circuit (e.g. sensor, actuator) supply	approximately V_{UIN} minus 7 volt
28	U_{IN}	SUPPLY	Input of the power supply block	Usually to be connected to the AS-i-line ASI+ via reverse polarity protection diode

8.2. External Components

In order to optimize the input impedance of the IC, the CAP pin needs to be connected to the 0V pin by serial connection of a capacitor C_{CAP}. The capacitor C_{CAP} defines the internal low-pass filter time constant; lower values decrease the impedance but improve (shorten) the turn-on time; higher values do not improve the impedance but do increase turn-on time. Turn-on time also depends on the load capacitor at U_{OUT}. After connecting the slave to the power, the capacitor at UOUT is charged with the maximum current I_{UOUT}.

In order to achieve optimal operation of the circuit, a few external components are required. Table 5 lists all required external components either as a minimum requirement or for more sophisticated solution.

Table 5: ASI4U External Components

Pin 1 to pin 2 or Pin to external node	External components		Remarks
	Minimum requirement	Optimal solution	
CAP to 0V	47nF	47nF	Impedance Control C for internal electronic inductor
CAP to 0V	0Ohm		Connect CAP pin to GND to disable the internal electronic inductor
U5R to 0V	1µF electrolyte capacitor in parallel 10 nF ceramic capacitor	2.2µF electrolyte capacitor in parallel 100 nF ceramic capacitor	
U_{OUT} to 0V	10µF electrolyte capacitor in parallel 100 nF ceramic capacitor		Higher value of the electrolyte capacitor is recommended if there are strong load current changes.
OSC1 to OSC2	8.000 or 16.000MHz standard x-tal, dedicated load capacitance approximately 7 ... 15pF		
LED to U_{OUT}		Pull-up resistor typical 100 kohm	If no LED is being connected and if the PCB is causing a high parasitic capacitance at the LED pin
DSR to U5R or U_{OUT}		Pull-up resistor typical 22 kohm	In order to avoid EMC problems (accidental reset of the IC due to strong EMI).
U_{IN} to reverse polarity protection diode or ASI+		10 µH inductor	Avoids RF oscillations on small PCBs.
ASIP to ASIN, 0V, GND If applicable U_{IN} to ASIN, 0V, GND	Zener diode 39V, 0.5W		To comply with the AS-i Complete Specification **[1]**, a reverse polarity protection diode must be applied. Evaluated types: ZMM39, BZV55C39
IRD to U5R		10kOhm	Reduces the sensitivity of the IRD input.
IRD to U5R		Pull-up resistor typical 10 kOhm	Ensures in master mode that a open IRD input does not cause a continuously “on” sender stage and subsequently a thermal shut down

8.3. Critical Parasitic Loads

The function of the ASI4U circuit is guaranteed within the operating conditions that are specified in ASI4U Data Sheet. These conditions are violated, there might be a risk of malfunctions. The designer of an application circuit, in particular the designer of a PCB layout, provoke violations of specified values if the influence of parasitic loads is underestimated.

Table 6: Critical Parasitic Loads

Parasitic Load	Malfunction	Reason	Recommendation
Parasitic load capacitance at DSR is too high.	IC performs a reset after performing a DEXG call	DSR is tied to low for more than 35 ms	Implement a pull-up resistor or decrease the pull resistor to U5R (or U_{OUT})
Parasitic load capacitance at parameter port is to high	Read back wrong parameter value	Parameter output value “overwrites” parameter input value	Degrease output capacity or increase pull up current by adding a pull up resistor to Uout
Unused (floating) DSR pin	EMC problems due to accidental resets	Internal pull-up resistor does not keep DSR stable on high.	Implement a pull-up resistor to U5R (or U_{OUT})
Overloaded OSC1/OSC2 pins (parasitic caps)	x-tal oscillator does not work	The IC contains a low-power oscillator that is not dedicated to drive external loads	Keep the parasitic cap between OSC1 and OSC2 below 7 pF and keep the parasitic load to ground below 2 pF.

8.4. PCB Design Recommendations

To assure correct operation of the IC, following facts should be considered when designing a PCB for an ASI4U application:

- Interconnection between X-tal and IC should be as short as possible. Large parasitic capacities at the pins should be avoided.
- An IR photo-diode between IRD and 0V should be connected with shortest possible wires to avoid interference from parasitic signals.
- Pin 0V and GND must be directly connected. The de-coupling capacitors between U5R and GND/0V shall be placed as close as possible to the U5R and 0V pin, respectively.
- De-coupling capacitors between U_{OUT} and GND/0V shall be placed as close as possible to U_{OUT} and 0V pins, respectively. This recommendation is the same if a resistor is put in series with the electrolyte capacitor.
- The ground node of the external slave electronic circuitry (that is controlled by the ASI4U) should directly be connected to GND pin (the wire should **not** pass through to pin 0V and then to pin GND). It should have a low-ohmic resistance and a low inductance.

- The connection of the ASIN pin to the 0V pin should not run via the GND pin. This wiring resistance may have some inductance (maximum value not yet defined). The optimal routing is ASI- to ASIN, then to 0V, and then to GND.

- Parasitic capacitors from the pins LED and DSR to Ground (0V/GND) should keep low.

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9.4 AS-International Association

Documentation and promotional materials as well as detailed technical specifications regarding the AS-Interface Bus Standard are available from:

AS-International Association:	Contact - Rolf Becker Zum Taubengarten 52 D-63571 Gelnhausen PO Box 1103 Zip (63551) Phone: +49 6051 47 32 12 Fax: +49 6051 4732 82 E-mail: info@as-interface.net Internet: www.as-interface.net

Refer to www.as-interface.net for contact information on local AS-Interface associations which provide special support within Europe, in the US and in Japan.

ASI4U Evaluation Board

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