EQCO875SC.3/ EQC850SC.3
Single Coax Transceiver for Fast Ethernet

1.1 Features

- Combined transmitter and receiver with an integrated equalizer to form a full-duplex bidirectional connection over a single 75Ω coax cable (EQCO875SC.3) or 50Ω coax cable (EQCO850SC.3)
- Compatible with FX version of Fast Ethernet
- Low Power - 205mW from single 3.3V supply
- Integrated termination resistors for low external discrete count
- Fully supports PoE based Power distribution over the coax, on top of the data signals
- 16-pin, 0.65mm pin pitch, 4mm QFN package
- Pb-free and RoHS compliant

1.2 Applications

This solution is useful and economical for many markets and applications, including the following:

- Camera networks - Home Security, Surveillance, industrial/inspection, medical cameras
- Home Networking over coax infrastructure
  - When Cat5 or Cat6 cabling is not available and existing 75Ω coax is not used for analogue TV signals.
  - TV, STB, PVR connections including inter-room links

1.3 Typical Cable Lengths

Version	EQCO875SC range using	
	RG11	RG6 (∅ 5mm)
EQCO875SC.3	225m	150m

Table 1: Typical Device Performance

2 Functional Description

2.1 Overview

The EQCO875SC.3 single coax transceiver is designed to simultaneously transmit and receive signals on a single 75Ω coax cable for fast ethernet. A sister product, the EQCO850SC.3 can achieve similar performance when used in 50Ω coaxial systems

The EQCO875SC.3 is ideally suited for Fast Ethernet connections over 75Ω coax cable at 125Mbps[1] data rate. The EQCO875SC.3 connects seamlessly to any FX[2]-compliant physical layer controller (PHY). For correct operation the signals are expected to be 4B/5B encoded, DC balanced and to have a bit rate of 125 Mbps.

This EQCO875SC.3 is useful and economical for connecting remote PoE enabled Fast Ethernet IP cameras and other Ethernet over Coax applications.

Figure 1 (below) illustrates a typical Ethernet Coaxial connection:

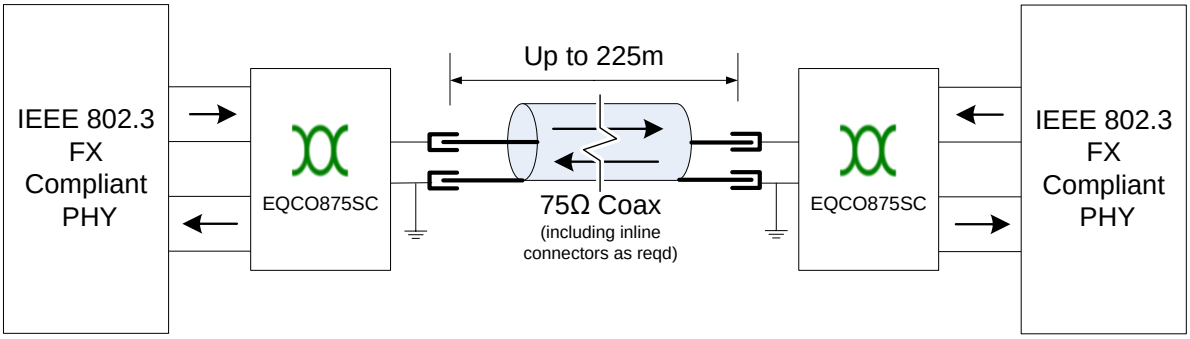

Figure 1: Coaxial Ethernet PMD connection

Figure 2 (below) shows a simplified block diagram of the EQCO875SC.3 when in Fast Ethernet mode:

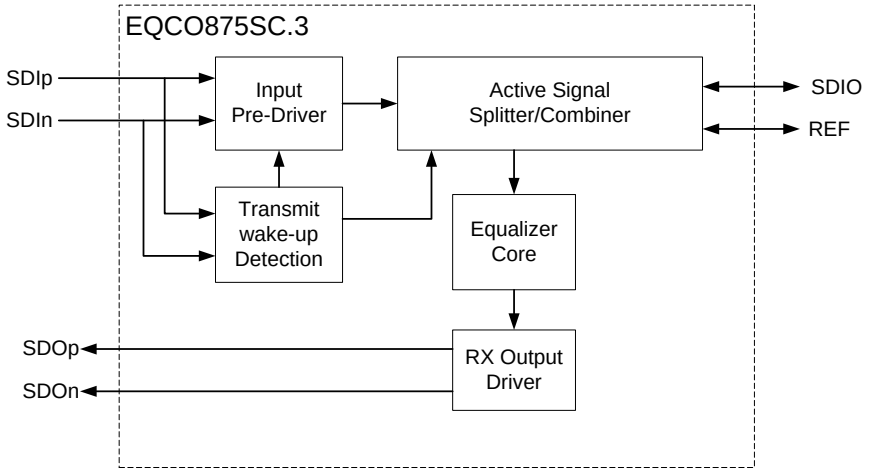

Figure 2: EQCO875SC.3 block diagram showing electrical connections

[1] Wire rate after 4B/5B coding
[2] FX is the terminology used in 802.3 to denote Fibre Optic transmission

2.2 Package and Pinout

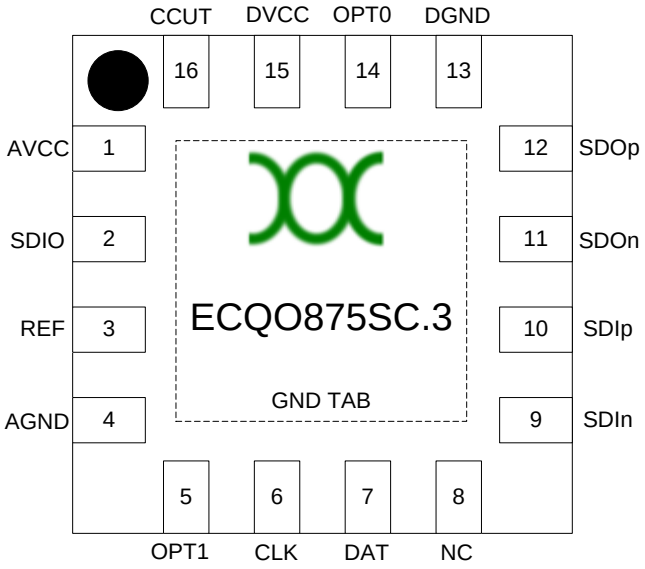

Figure 3: EQCO875SC.3 Pin Layout (viewed from top)

2.3 Pin Descriptions

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Connect to ground of power supply
15	DVCC	Power	Digital VCC Connect to +3.3V power supply
13	DGND	Power	Digital GND Connect to ground of power supply
1	AVCC	Power	Analog VCC Connect to +3.3V power supply via Ferrite Bead (RF Choke) and capacitor to cable outer screen
4	AGND	Power	Analog GND Connect to cable outer screen
2	SDIO	Bidirectional	Serial Input Output Connect to centre conductor of 75Ω coax cable.
3	REF	Bidirectional	Reference Connect through 75Ω resistor (or impedance matched to cable) to cable outer screen
8	NC	Output	Do not connect
10, 9	SDIp/SDIn	Input	Serial Input Positive/Negative Differential serial input. Connect to the Ethernet PHY FX out pins.
12, 11	SDOp/ SDOn	Output	Serial Output Positive/Negative Differential serial output. Connect to the Ethernet PHY FX in pins.
14,5	OPT0, OPT1	Input	Connect Opt0 to DGND and Opt1 to DVCC to enable Fast Ethernet mode
6,7	CLK, DAT	Input	Used for Production test, Connect to DGND.
16	CCUT	Analog	Cable Cut Detection

Table 2: Device Pin List

2.3.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. The serial data received on these pins will be transmitted on SDIO. The Input Pre-Driver automatically corrects for variations in signal levels and different edge slew rates at these inputs before they go into the Active Splitter/Combiner for transmission over the coax.

Both SDIp and SDIn inputs are differentially terminated by 110 Ω on chip. The center of the 110 Ω is connected to DGND with a 10 kΩ resistor for DC biasing. The inputs also have protection diodes to ground for ESD purposes. These inputs **should always be capacitively coupled** to the FX output of the Ethernet PHY. A Transmit Wake-up detection circuit puts both the Input Pre-Driver and the Active Signal Splitter/Combiner into a low power mode when no signal is detected on the SDIp/SDIn signal pair.

2.3.2 SDIO/REF

The signal on the SDIO pin is the sum of the incoming signal (i.e. the signal transmitted by the EQCO875SC on the far end side of the coax) and the outgoing signal (i.e. the signal created based on SDIp/SDIn). The far end signal is extracted by subtraction of the near end signal and it is this voltage that the equalizer analyses and adaptively equalizes for level and frequency response based on the knowledge that the originating signal is 4B/5B encoded before transmission.

The REF signal carries a precise anti-phase current to the transmit current on SDIO. REF must be connected directly to AGND **at the connector** (see Figure 8) via a resistor precisely matched to the impedance of the coaxial cable used.

2.3.3 SDOp/SDOn

SDOp/SDOn together form a differential pair outputting the reconstructed far end transmit signal. The common mode output voltage of these signals is 1.2V and they have an internal differential source matching of 100Ω according to LVDS standards, allowing AC or DC coupling to Ethernet PHYs.

2.3.4 CCUT

Pin 16 of the EQCO875SC is an optional signal for cable cut detection. If used, it can detect when there is a cut in the cable and it shuts down the internal receiver to stop reflections from being interpreted as data. This feature is not compatible with sending power over the cable as this might expose pin 16 to voltages higher than this input can tolerate. To use this feature connect this signal to inner of the coax connector via a 3kΩ resistor. If used, the connection between the 3kΩ resistor and the 75Ω transmission line between SDIO and the inner contact of the coax connector should be kept as short as possible, to avoid stub effects in the transmission line.

2.3.5 OPT0, OPT1

Connect Opt0 to DGND, and Opt1 to DVCC to enable Fast Ethernet mode.

2.3.6 CLK, DAT Pins

These pins are normally used to access an internal register during production test. Connect them to DGND for normal operation. **They must not be left floating**.

2.4 Circuit Operation

2.4.1 Pre-driver

The Pre-driver removes any dependency on Ethernet PHY for the amplitude and rise time of the outgoing signal on SDIO.

2.4.2 Active signal splitter/combiner

The active splitter/combiner [3] controls the amplitude and rise time of the outgoing coax signal and transmits it via a precise 75Ω output termination resistor. The output resistor when balanced with the coax characteristic impedance also forms part of a hybrid splitter circuit which subtracts the TX output from the signal on the SDIO output to give yield the far end TX signal. The return loss of the coax termination is a key factor in the performance of the line Hybrid.

2.4.3 Equalizer Core

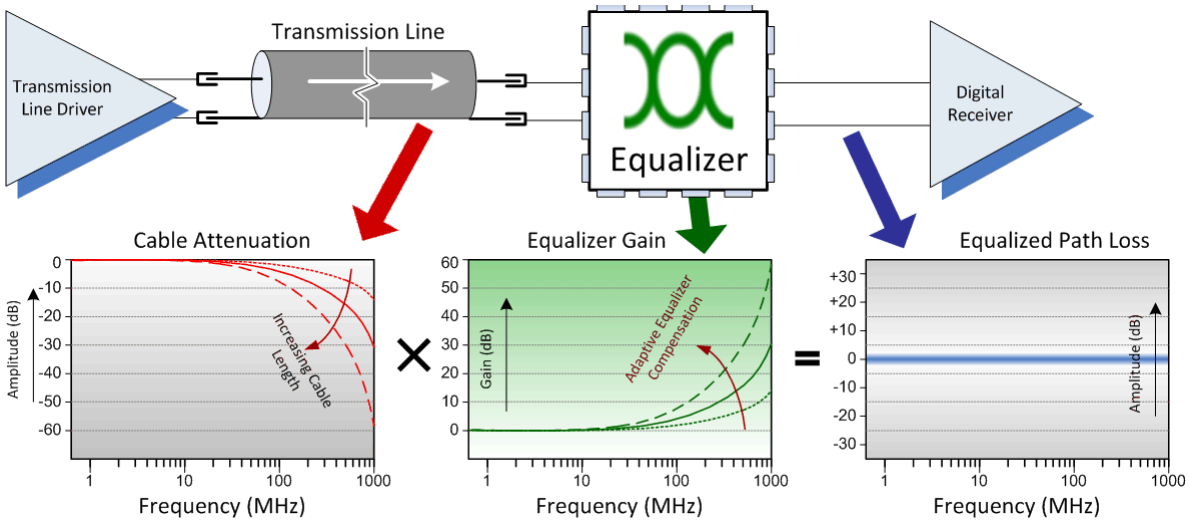

Figure 4: Principle of Equalizer Operation

The EQCO875SC has an embedded equalizer in the receive path with unique characteristics:

- Auto-adaptive

  The equalizer controls a multiple pole analog filter which compensates for attenuation of the cable, as illustrated in Figure 4. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable gain

  EQCO875SCs are used in pairs; one at each end of the coax. The EQCO875SC can be used with any FAST ETHERNET compliant Fibre Optic PHY; any differences in transmit amplitude are removed by the input pre-driver. The receiver equalizer has variable gain to compensate for attenuation through the coax.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Conditions	Min	Typ	Max	Units
Storage Temperature		-65		+150	°C
Ambient Temperature	Power Applied	-55		+125	°C
Operating Temperature	Normal Operation (VCC=3.3V±5%)	-10		+70	°C
Supply Voltage to Ground		-0.5		+4.0	V
DC Input Voltage		-0.5		+4.0	V
DC Voltage to Outputs		-0.5		+4.0	V
Output current into Outputs	Outputs Low			90	mA
Electro Static Discharge (ESD) HBM	JEDEC EIA/JESD-A114A	>3.3			kV
Electro Static Discharge (ESD) contact	IEC 61000-4-2	>8			kV
Latch-Up Current		>200			mA(DC)

Table 3: Absolute Maximum Ratings

3.2 Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
Power supply					
V_{CC}	Supply Voltage	3.135	3.3	3.465	V
I_S	Supply Current, both transmitting and receiving[2]	47.5	62.5	75.5	mA
I_{sr}	Supply Current when not transmitting[2]	25	35	43	mA
SDIp/SDIn Inputs (LVDS like)					
ΔV_i	Input amplitude $V_{SDIp,n}$[2]	250		800	mV
V_{turnon}	Minimal ΔV_i to turn on transmit function	100	140	200	mV
V_{cmin}	Common-mode input voltage (terminated to ground with protection diodes)[3]		0		V
R_{input}	Differential input termination[2]	85	104	115	Ω
SDIO connection to Coax					
Z_{coax}	Required Coax Cable Characteristic Impedance	72 (48)	75 (50)	78 (52)	Ω
R_{SDIO}	Input impedance between SDIO and AGND[2]	65 (46)	75 (51)	86 (55)	Ω
R_{loss}	Coax Return Loss as seen on SDIO pin Frequency range = 10 MHz-62.5 MHz	15			dB
ΔV_{TX}	Transmit Amplitude	250	300	350	mV

Parameter	Description	Min	Typ	Max	Unit
t_{rise_tx}	Rise/fall time 20% to 80% of ΔV_{TX} [3]	350	450	550	ps
Att_{max}	Cable Attenuation Budget @ 62.5MHz (Fast Ethernet) [3]		10		dB
$\Delta V_{RX\ min}$	Minimum input for fully reconstructed output [3]		40		mV
SDOp/SDOn Outputs (LVDS like)					
ΔV_o	Output amplitude $V_{SDOp,n}$ [1]	250	350	450	mV
V_{cmout}	Common-mode output voltage [1]	1.1	1.2	1.3	V
R_{output}	Differential termination between SDOp and SDOn [2]	85	102	115	Ω
t_{rise_o}	Rise /fall time 20% to 80% of $V_{SDOp,n}$ [3]	150	240	350	ps

Table 4: Electrical Characteristics (see notes), EQCO875SC.2 and (EQCO850SC.2).

[1] Over full VCC range
[2] Over full VCC range and full operating temperature range (-10 °C to 70 °C)
[3] Guaranteed by design

3.3 Jitter Performance

Parameter	Conditions	Min	Typ	Max	Units
Jitter peak to peak on SDO	150m RG6 coax; over full Vcc, ΔV_{TX} and Temp range; 125 Mbps ; pattern PRBS7		40%	50%	UI

Table 5: Jitter at SDO

4 Package Drawing

The EQCO875SC is packaged in a 16 pin Micro Lead frame Package (MLP) also known as Quad Flat No Lead (QFN) package. The package outline conforms to JEDEC MO-220.

Dimensions in Figure 5 and Figure 6 are in millimeters.

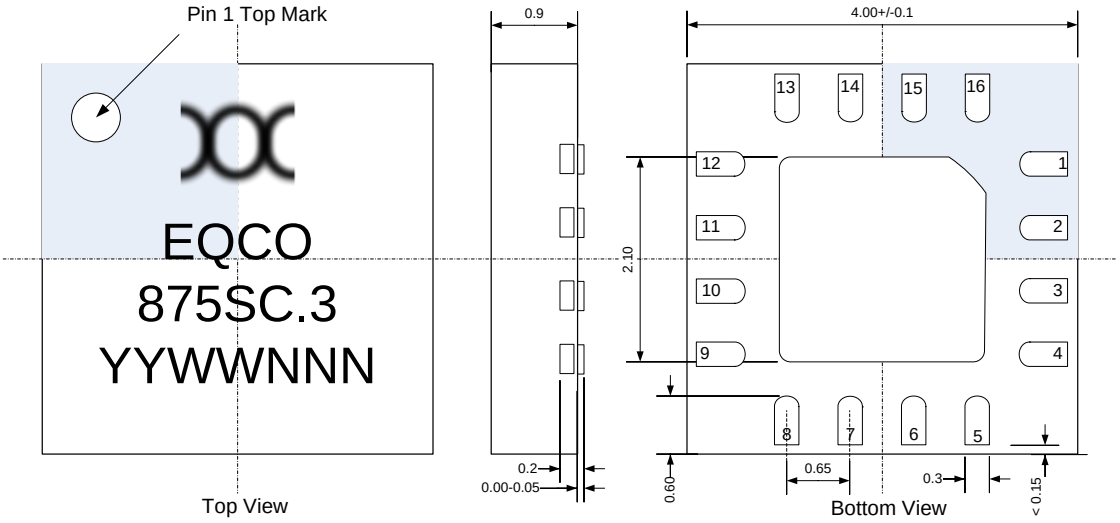

Figure 5: Package Drawing

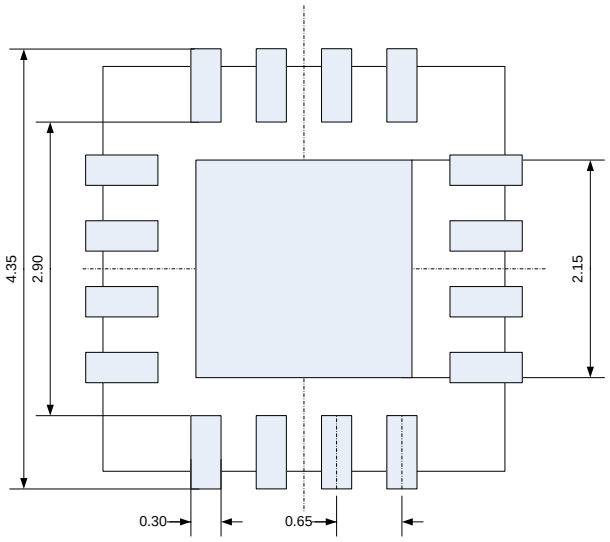

Figure 6: Recommended PCB Footprint

5 Application Information

5.1 Typical Application Circuit

Figure 7 shows a typical application circuit for the EQCO875SC.3 in Ethernet mode:

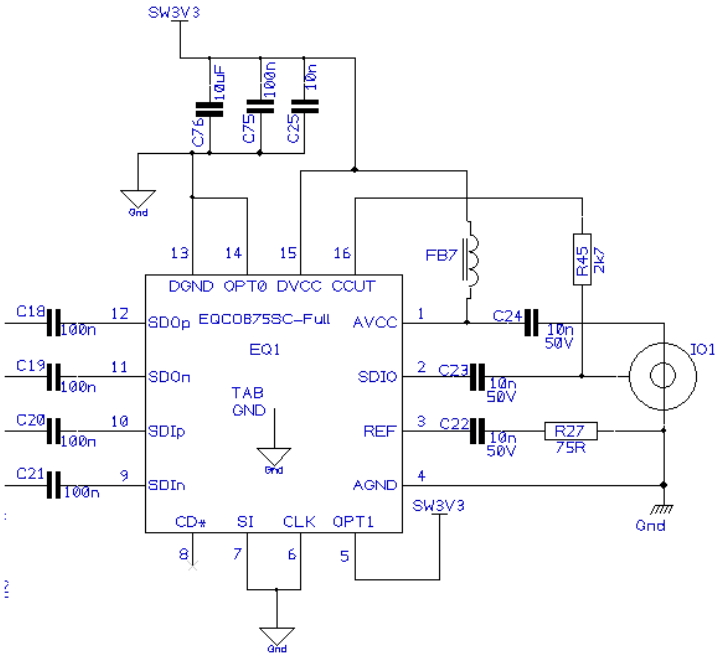

Figure 7: Typical Schematic Implementation

To improve isolation from noise on the board power plane and improve EMC immunity and emissions, it is recommended to power the transmit side of equalizer (AVCC) through a ferrite bead (FB7). C24 is used to reference AVCC to the ground directly at the connector IO1, while AGND is also connected directly to the connector.

A 10nF decoupling capacitor (C25) should be placed as close as possible between the DVCC pin and the DGND pin. Ground vias should be placed as close as possible to the device GND pins to minimize inductance. C75 and C76 in the above circuit remove lower frequency noise and are typically required when deploying DC-DC converter based power supplies.

C18-C21 are the coupling capacitors to the 100BaseFX PHY. The cable cut signal is fed into the connector using R45 and the SDIO signal through C23. The REF signal is terminated with an identical capacitor, C22 and 75Ω resistor R27. In case of an implementation for 50 Ω coax, the EQCO850SC.3 should be used, and R27 should have a value of 50 Ω. In that case the coaxial connector should also be of a 50-Ω type.

5.1.1 PCB layout (4 layer PCB)

The following diagram shows the layout of the critical section of the PCB corresponding to the circuit of Figure 7 from the coax connector to the twin differential pairs:

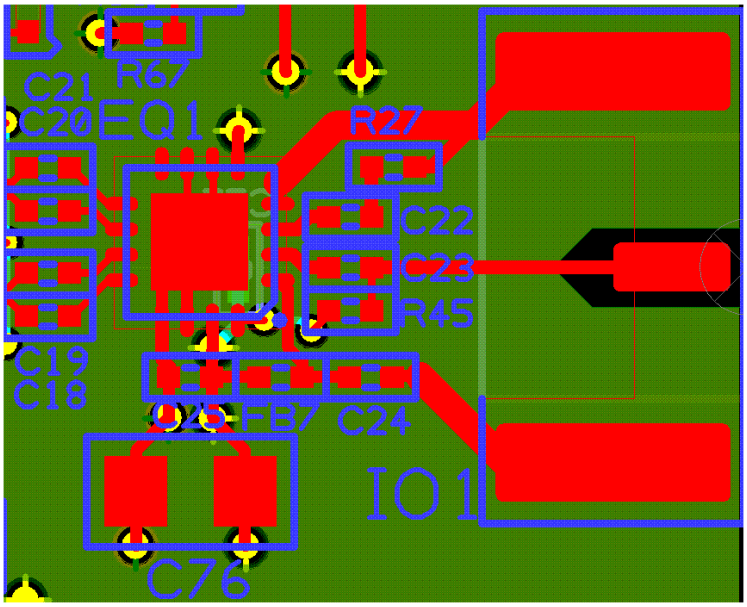

Figure 8: typical PCB Layout

Because signals are strongly attenuated by a long cable, special attention must be paid on the PCB layout between the coaxial connector and the EQCO875SC.1. The EQCO875SC.3 should be as close as is practical to the coaxial connector. The trace between the coaxial connector and the SDIO pin of the EQCO875SC.3 must be a 75Ω trace referenced to GND (shown in green above). To avoid noise pickup other traces carrying digital signals or fast switching signals should be placed as far away as possible from this trace. Note how close R45 Is to C23 so as to minimize the stub caused by this component connection.

The ground layout on the EQCO875SC.3 is crucial to the EMC and EMI performance of the circuit. The AGND connection should be made directly to the body of the connector as shown. Similarly AVCC should be decoupled directly to the connector body (see position of C24). The termination resistor (R27 in Figure 7 and Figure 8) must have its ground connection at the connector body and the C22, R27 trace must be kept as short as possible. The impedance of all the traces must be well controlled, including on the connector itself.

The SDIp/SDIn and SDOp/SDOn differential traces (shown here going through C18-C21) should be matched in length to minimize time of arrival skew. For traces longer than a few mm the impedance of the differential transmit and receive signals should be laid out as 100Ω differential traces and the termination to the PHY should be placed close to the PHY, not to the EQCO875SC.1.

6 Document Control

6.1 Version History

Version	Date	Author	Comments
2v0	28 Jan 2014	M. Kuijk	Merging 50 and 75 ohms systems in one datasheet
1v2	25-Oct-2011	P. Crama	Fix lower temperature limit
1v1	08 Jun 2011	P. Crama	Fix bitrate, temperature range, SDIP/SDIN description
0v4	28-Feb 2011	S.E. Ellwood	Internal Quality review, Removed preliminary status
0v3	26 Oct 2009	Maarten Kuijk	Technical Review, revised section 5.1
0v2	15 Oct 2009	S. E. Ellwood	Internal Review
0v1	15 Oct 2009	S. E. Ellwood	Taken from EQCO875SC IEEE1394 Datasheet

6.2 Document References

[1] IEEE 802.3 Ethernet Standard - IEEE
[2] AN0907 - IP Data/PoE COAX Adaptor reference design – EqcoLogic NV
[3] Patents & Patents Pending: EP2237419A1, US8164358B2, EP2237435B1 US8488685B2

6.3 Ordering Information

Order Code	Application	Production	Package Type	Operating Range
EQCO875SC.1	75 ohm Coax	End Of Life	16 Pin, 4mm QFN	-10°C…+70°C
EQCO850SC.1	50 ohm Coax	End Of Life	16 Pin, 4mm QFN	-10°C…+70°C
EQCO875SC.3	75 ohm Coax	In Qualification	16 Pin, 4mm QFN	-10°C…+70°C
EQCO850SC.3	50 ohm Coax	In Qualification	16 Pin, 4mm QFN	-10°C…+70°C

EQCO850SC.1 and EQCO850.3 consist of the same silicon and the same package.
EQCO875SC.1 and EQCO875.3 consist of the same silicon and the same package.

6.4 Disclaimer:

EQCOLOCIC MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Eqcologic reserves the right to make changes without further notice to the materials described herein. Eqcologic does not assume any liability arising out of the application or use of any product or circuit described herein. Eqcologic does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Eqcologic's product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Eqcologic against all charges.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Ethernet ICs ***category:***

Click to view products by Microchip ***manufacturer:***

Other Similar products are found below :

12200BS23MM DSL4510 S R15X BCM53115MIPBG BCM53115SIPB BCM54616C0KMLG BCM5461A1KPFG BCM5461SA1IPFG BCM5461SA3KFBG BCM54640EB2KFBG BCM5464SA1IRBG SBL2ECHIP-236IR BCM54210B0KMLG BCM54612EB1KMLG BCM8727MCIFBG KSZ8091RNDCA-TR LA2333T-TLM-E VSC7421XJQ-02 VSC8522XJQ-02 LAN91C93I-MU WGI219LM SLKJ3 VSC7389XHO 78Q2133S/F BCM5325EKQMG BCM54210EB1IMLG BCM54220B0KFBG BCM5720A0KFBG BCM54220SB0KFBG BCM54220SB0KQLEG MAX3956AETJ+ KSZ8441FHLI BCM53262MIPBG BCM54640EB2IFBG BCM5461SA1KPFG BCM53402A0IFSBG KSZ8091MNXCA JL82599ES S R1VN BCM53125MKMMLG F104X8A VSC7511XMY VSC7418XKT-01 VSC7432YIH-01 WGI219V SLKJ5 BCM84793A1KFSBG BCM56680B1KFSBLG FTX710-BM2 S LLKB 88E3082-C1-BAR1C000 WGI210CS S LKKL BCM56450B1IFSBG BCM56960B1KFSBG EZX557AT2 S LKVX