DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 320240E SBH-PW-N

4,7“ ¼-VGA

Product Specification ***Version: 1***

13/Jun/2008

GENERAL SPECIFICATION

MODULE NO. :

DEM 320240E SBH-PW-N

CUSTOMER P/N

VERSION NO.	CHANGE DESCRIPTION	DATE
0	ORIGINAL VERSION	15.05.2008
1	CHANGE BACKLIGHT SPECIFICATION AND ELECTRICAL CHARACTERISTICS	13.06.2008

PREPARED BY : HCL DATE: 13.06.2008

APPROVED BY : MH DATE: 13.06.2008

CONTENTS

1. FUNCTIONS & FEATURES

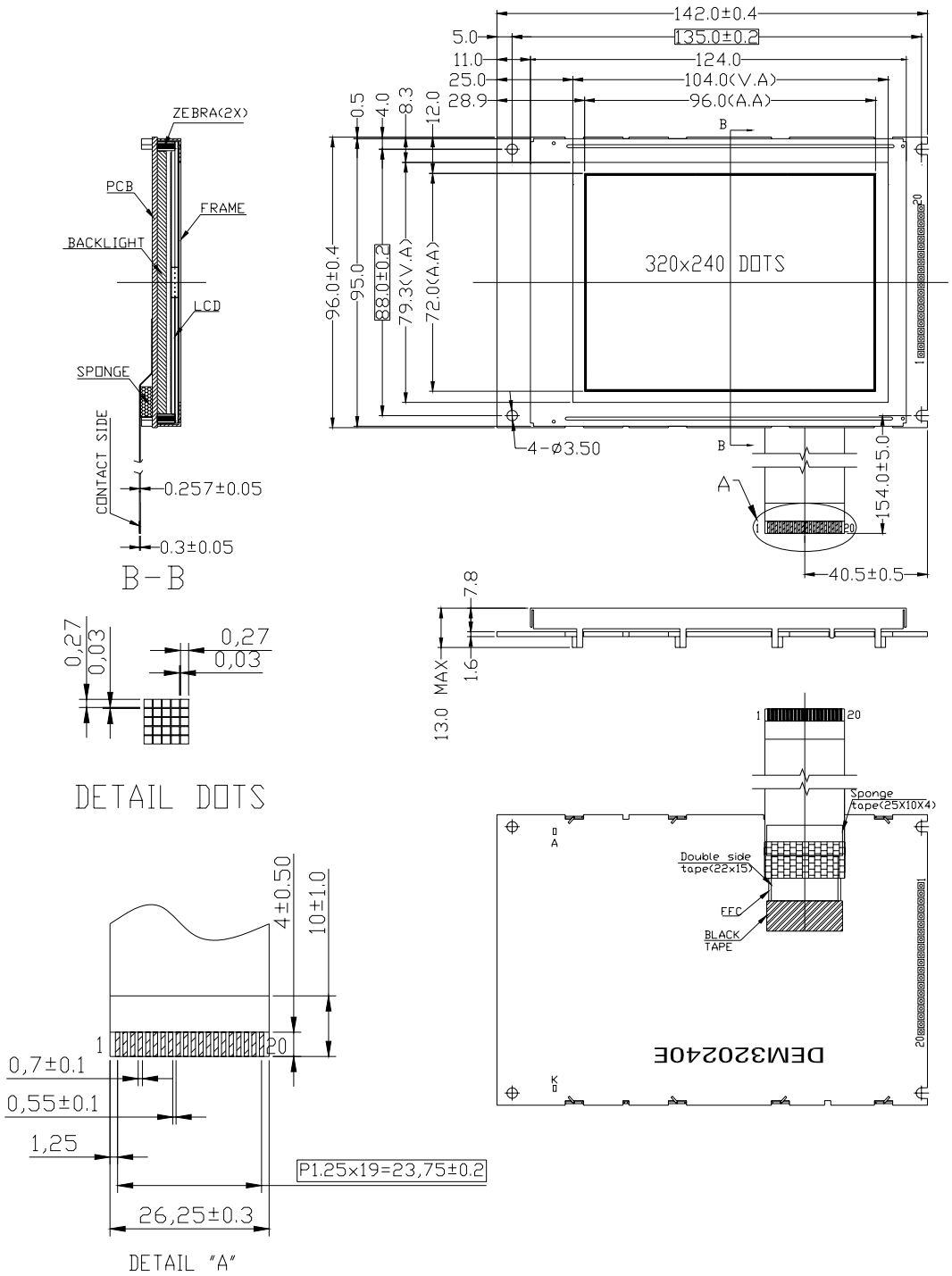
MODULE NAME	LCD TYPE
DEM 320240E SBH-PW-N	STN-BLUE Transmissive Negative Mode

- Viewing Direction : 6 o'clock
- Driving Scheme : 1/240 Duty Cycle, 1/13 Bias
- Display Content : 320x240 Dots
- Power Supply Voltage : 5.0 Volt (typ.)
- LCD Driving Voltage ($V_{LCD}=V_{DD}-V_0$) : 20.5 Volt (typ.)
- LCD-Controller : S1D13700 (Epson) on Board
- Negative Power generator : AIC1652
- Operating Temperature : -20°C to +70°C
- Storage Temperature : -30°C to +80°C

2. MECHANICAL SPECIFICATIONS

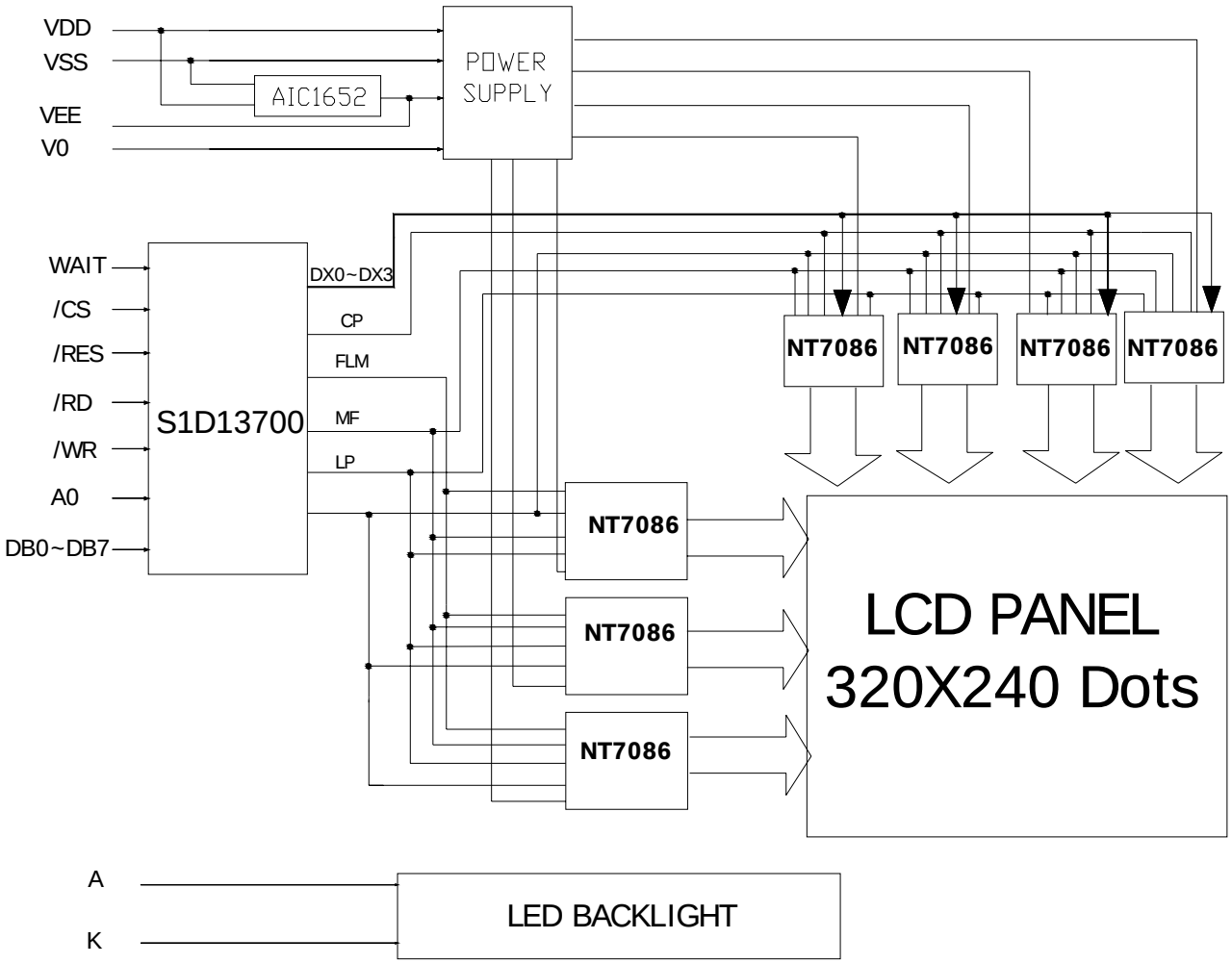
- Module Size : 142.00 x 96.00 x 13.00 mm
- Viewing Area : 104.00 x 79.30 mm
- Active Area : 96.00 x 72.00 mm
- Dot Size : 0.27 x 0.27 mm
- Dot Pitch : 0.30 x 0.30 mm

3. EXTERNAL DIMENSIONS (unit: mm)



Remarks:
1,Unmarked tolerance is ±0.30,
2,The material comply with RoHS.

4. BLOCK DIAGRAM



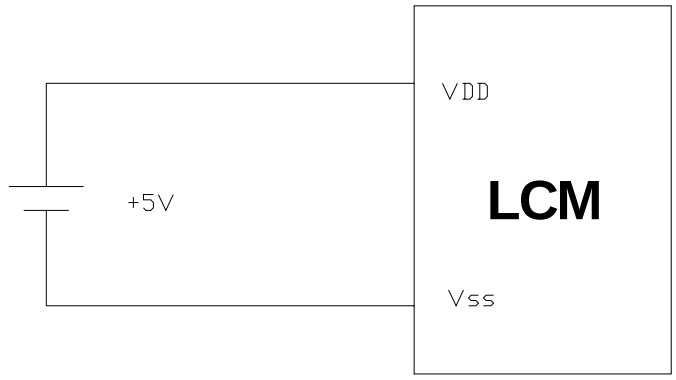
5. PIN ASSIGNMENT

Interface Connector

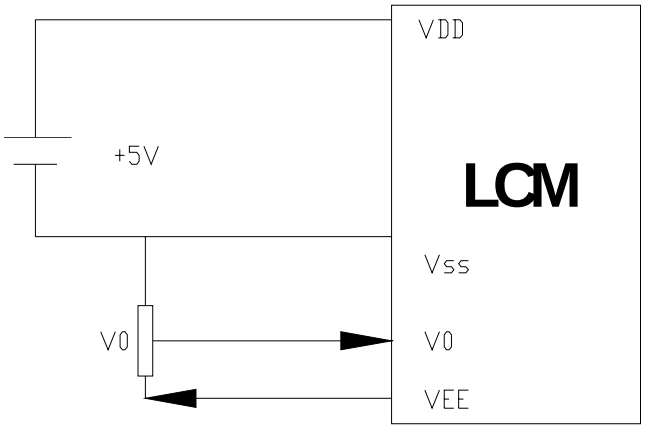
Pin No.	Symbol	Function
1	WAIT	Wait
2	VSS	Ground terminal of module
3	VEE	Supply voltage for LCD
4	VDD	Power terminal of module(TYP:5.0V)
5~12	DB7~ DB0	Data bus
13	/WR	Data Write
14	/RD	Data Read
15	A0	Command/Data select
16	V0	LCD contrast adjust voltage
17	/CS	Chip selection
18	/RES	Reset signal
19	A	LED+(TYP:5.0V ,using LED resistors on board)
20	K	LED-

6. POWER SUPPLY

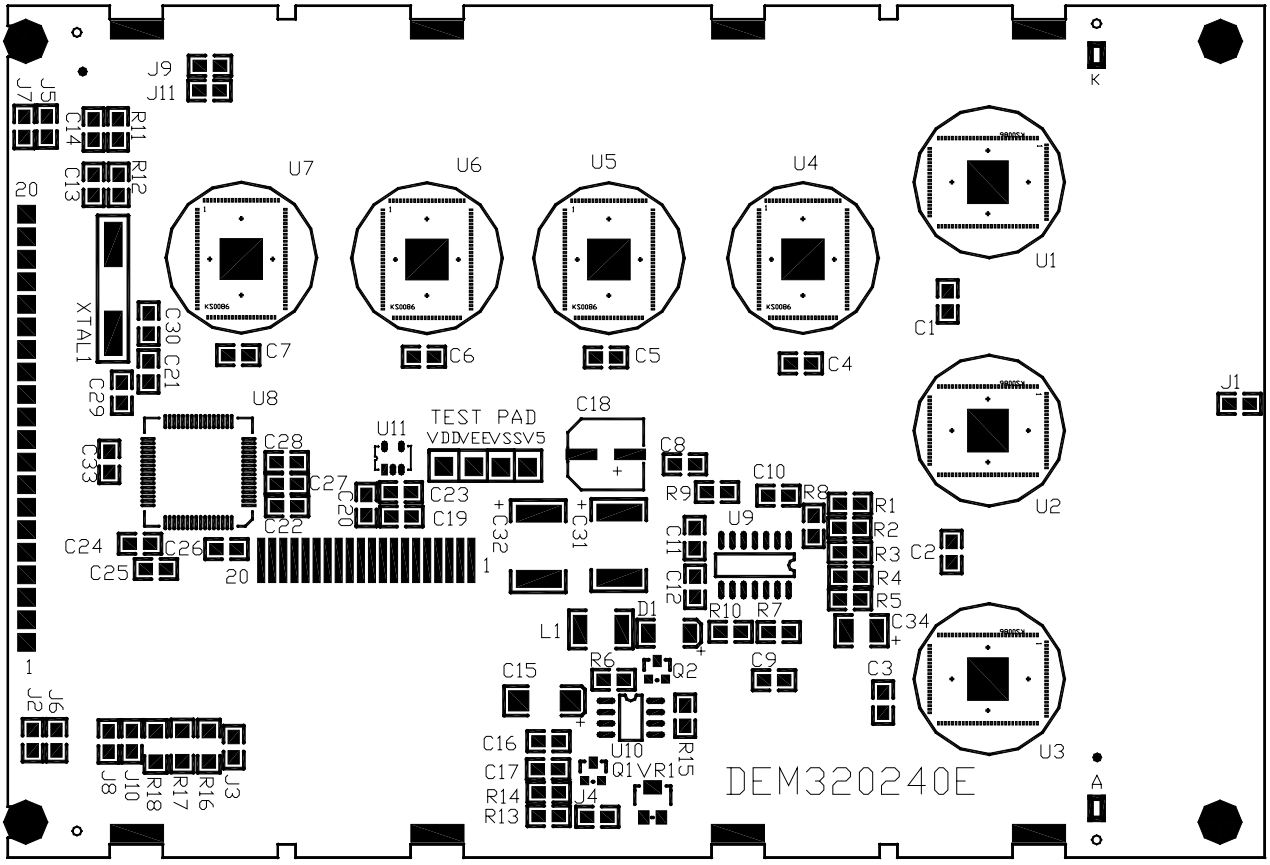
Mode(External contrast regulation)-J4 is open.



Mode(Internal contrast regulation)-J4 is close.



7. PCB DRAWING



DESCRIPTION:

7.1. If J5, J6 are closed, the metal-bezel will be on ground.

Note: In application module, J5= J6= 0 Ohm

7.2. If J1, J2, J7 are closed, the mounting-hole will be on ground.

Note: In application module, J1 = J2 = J7 = 0 Ohm

7.3. If J3 is closed, the LED resistors R16, R17 and R18 will be short.

Note: In application module, J3 = R18 =open, R16 = R17 =33 Ohm

7.4. If J4 is closed, the internal contrast regulation will be used.

If J4 is open, the external contrast regulation will be used.

The VR1 use to internal contrast regulation.

Note: In application module, VR1=10K Ohm, J4 = open

7.5. If pin19 is positive and 20 is negative, J8, J11 connect with 0 Ohm.

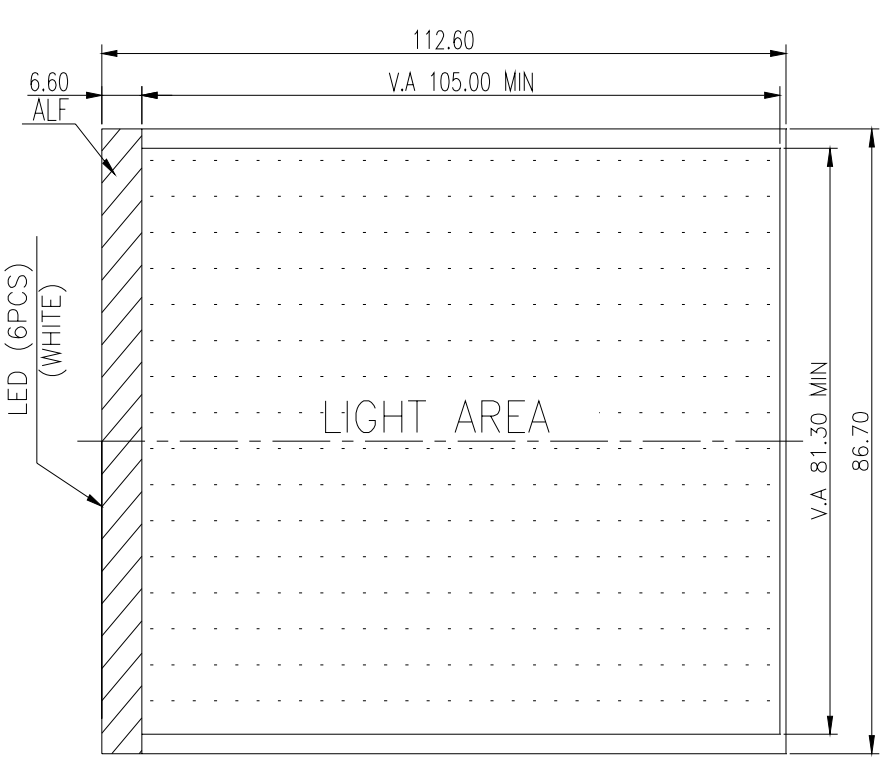
If pin19 is negative and 20 is positive, J9, J10 connect with 0 Ohm.

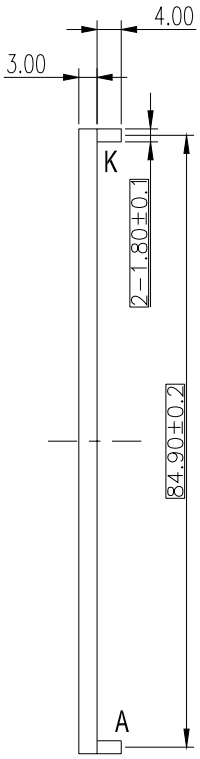
Note: In application module, J8= J11=0 Ohm, J9= J10= open.

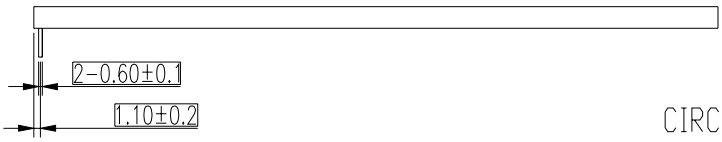
8. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATIONS(unit: mm)

Backlight life time: Longer than 30000 hours

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	Vf	2.8	3.1	3.4	V	If=120mA
Forward Current	If	90	120	150	mA	
Power Dissipation	Pd			0.408	W	If=120mA
Reverse Voltage	VR			5.0	V	
Reverse Current	IR			0.6	mA	
Luminous Intensity	IV	500			cd/m^2	If=120mA
Luminous Uniformity		70			%	If=120mA
Color Chromaticity	X	0.27	0.30	0.33		If=20mA,Ta=25℃ Each chip
	Y	0.27	0.30	0.34		

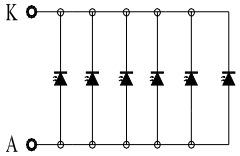






Remarks:
1,Unmarked tolerance is ±0.30,
2,The material comply with RoHS.

CIRCUIT DIAGRAM



1*6=6(Pcs)WHITE LED

9. ABSOLUTE MAXIMUM LIMIT

Item	Symbol	MIN	TYP.	MAX	UNIT
Supply voltage for logic	Vdd-Vss	-0.3	--	+7.0	V
Supply voltage for LCD	Vdd-V0	-0.3	--	+30.0	V
Input Voltage	Vi	-0.3	--	Vdd+0.3	V
Operating temperature	Top	-20	--	+70	°C
Storage temperature	Tst	-30	--	+80	°C

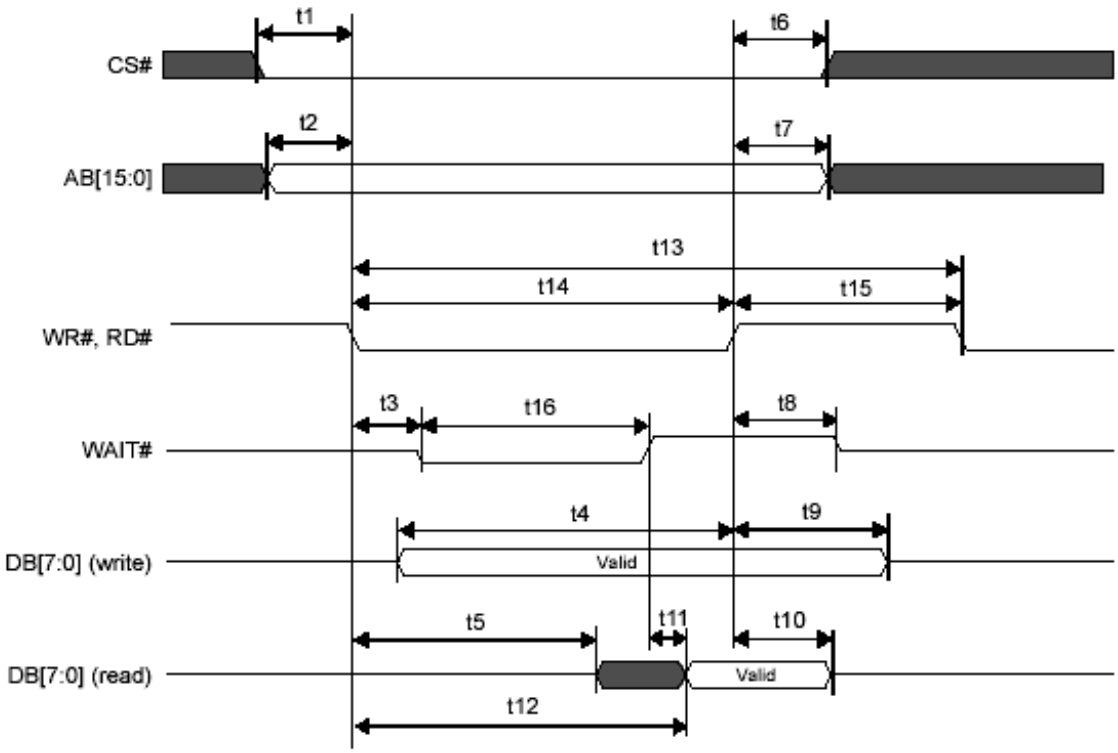
10. ELECTRICAL CHARACTERISTICS

Unless otherwise noted. V_{SS} = 0V

Item	Symbol	Standard Value			Unit
		Min	Typ.	Max	
Supply Voltage for logic	Vdd-Vss	4.5	5.0	5.5	V
Supply Voltage for LCD	Vdd -V0	18.0	20.5	24.0	V
Consumption current	Idd	--	TBD	--	mA

11. S1D13700 TIMING DIAGRAMS

Generic Bus Direct/Indirect Interface with WAIT # Timing



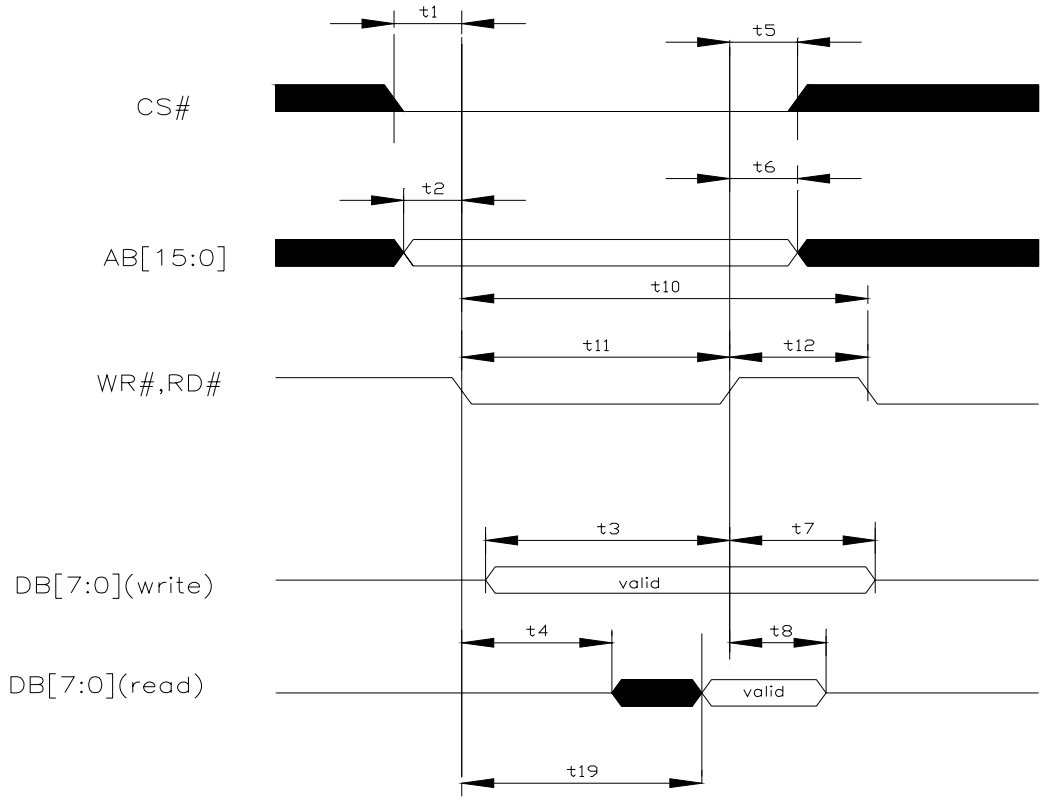
Generic Bus Direct/Indirect Interface with WAIT # Timing

Symbol	Parameter	Min	Max	Units
t1	CS# setup time	5	--	ns
t2	AB[15:0] setup time	5	--	ns
t3	WR#, RD# falling edge to WAIT# driven low	2	--	ns
t4	DB[7:0] setup time to WR# rising edge (write cycle)	Note1	15	ns
t5	RD# falling edge to DB[7:0] driven (read cycle)	3	--	ns
t6	CS# hold time	7	--	ns
t7	AB[15:0] hold time	7	--	ns
t8	RD#, WR# rising edge to WAIT# high impedance	2	10	ns
t9	DB[7:0] hold time from WR# rising edge (write cycle)	5	--	ns
t10	DB[7:0] hold time from RD# rising edge (read cycle)	3	14	ns
t11	WAIT# rising edge to valid Data if WAIT# is used	--	Note 2	ns
t12	RD# falling edge to valid Data if WAIT# is not used	--	Note 3	ns
t13	RD#, WR# cycle time	Note 4	--	ns
t14	RD#, WR# pulse active time	5	--	Ts
t15	RD#, WR# pulse inactive time	Note 5	--	ns
t16	WAIT# pulse active time	--	Note 6	ns

Note: (Ts = System clock period)

1. t4min = 2Ts + 5
2. t11max = 1Ts + 5 (for 3.3V)
   = 1Ts + 7 (for 5.0V)
3. t12max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
5. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
6. t16max = 4Ts + 2

Generic Bus Direct/Indirect Interface without WAIT # Timing

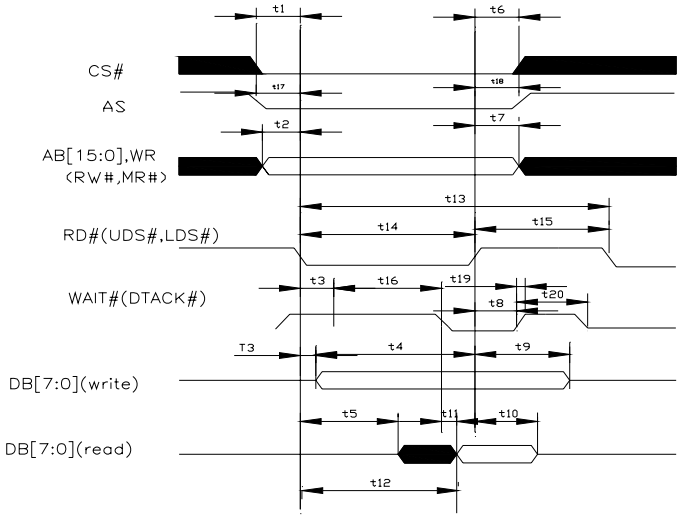


Symbol	Parameter	min	max	Unit
t1	CS# setup time	5	--	ns
t2	AB[15:0] setup time	5	--	ns
t3	DB[7:0] setup time to WR# rising edge (write cycle)	Note 1	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	--	ns
t5	CS# hold time	7	--	ns
t6	AB[15:0] hold time	7	--	ns
t7	DB[7:0] hold time from WR# rising edge (write cycle)	5	--	ns
t8	DB[7:0] hold time from RD# rising edge (read cycle)	3	14	ns
t9	RD# falling edge to valid Data (read cycle)	--	Note2	ns
t10	RD#, WR# cycle time	Note 3	--	ns
t11	RD#, WR# pulse active time	5	--	Ts
t12	RD#, WR# pulse inactive time	Note 4	--	ns

Note: (Ts = System clock period)

1. t3min = 2Ts + 5
2. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
3. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
4. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

MC68K Family Bus Indirect/Direct Interface with DTACK # Timing



Symbol	Parameter	Min	Max	Units
t1	CS# setup time	5	--	ns
t2	AB[15:0] setup time	5	--	ns
t3	AS# falling edge to WAIT# driven	2	15	ns
t4	DB[7:0] setup time to RD# rising edge (write cycle)	Note 1	--	ns
t5	RD# falling edge to DB[7:0] driven (read cycle)	3	--	ns
t6	CS# hold time	7	--	ns
t7	AB[15:0] hold time	7	--	ns
t8	RD# rising edge to WAIT# high impedance if Direct interface and in Power Save Mode	2	10	ns
t9	DB[7:0] hold time from RD# rising edge (write cycle)	5	--	ns
t10	DB[7:0] hold time from RD# rising edge (read cycle)	2	55	ns
t11	WAIT# falling edge to valid Data if WAIT# is used	--	Note 2	ns
t12	RD# falling edge to valid Data if WAIT# is not used	--	Note 3	ns
t13	RD# cycle time	Note 4	--	ns
t14	RD# pulse active time	5	--	Ts
t15	RD# pulse inactive time	Note 5	--	ns
t16	WAIT# pulse inactive time from WAIT# driven	--	Note 6	Ns
17	AS# setup time	0	--	ns
18	AS# hold time	0	--	ns
19	AS# rising edge to WAIT# high de-asserted if not Direct interface and not in Power Save Mode	--	10	ns
20	WAIT# pulse inactive time	0	Note 7	ns

Note: (Ts = System clock period)

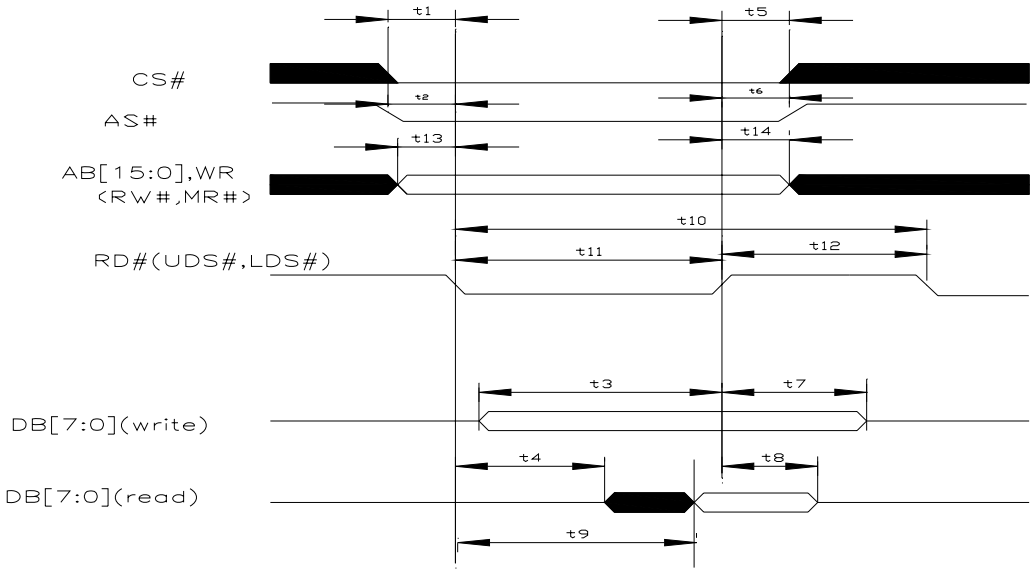
1. t4min = 2Ts + 5 2. t11max = 1Ts + 5 (for 3.3V)= 1Ts + 7 (for 5.0V) 3. t12max = 4Ts + 18 (for 3.3V)= 4Ts + 20 (for 5.0V)

4. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)

5. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

6. t16max = 4Ts + 2 7. t20max = 1Ts - 15

MC68K Family Bus Indirect/Direct Interface without DTACK # Timing

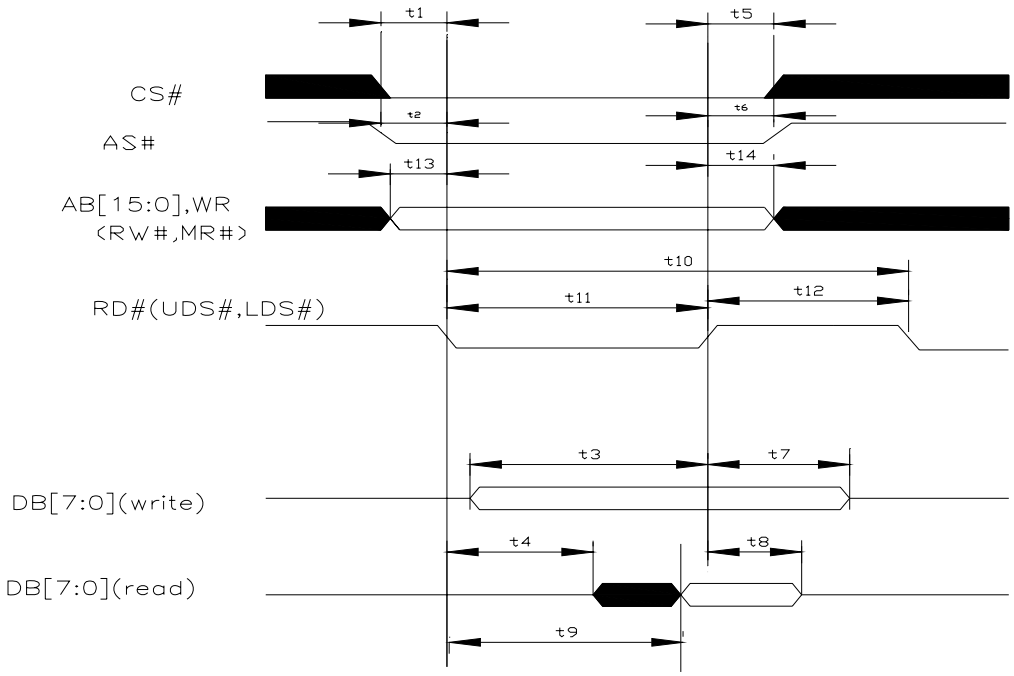


Symbol	Parameter	Min	Max	Units
t1	CS# setup time	5	--	ns
t2	AB[15:0] setup time	5	--	ns
t3	DB[7:0] setup time to RD# rising edge (write cycle)	Note 1	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	--	ns
t5	CS# hold time	7	--	ns
t6	AB[15:0] hold time	7	--	ns
t7	DB[7:0] hold time from RD# rising edge (write cycle)	5	--	ns
t8	DB[7:0] hold time from RD# rising edge (read cycle)	2	55	ns
t9	RD# falling edge to valid Data	--	Note 2	ns
t10	RD# cycle time	Note 3	--	ns
t11	RD# pulse active time	5	--	Ts
t12	RD# pulse inactive time	Note 4	--	ns
t13	AS# setup time	0	--	ns
t14	AS# hold time	0	--	ns

Note: (Ts = System clock period)

1. t3min = 2Ts + 5
2. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
3. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
4. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

M68K Family Bus Indirect Interface Timing



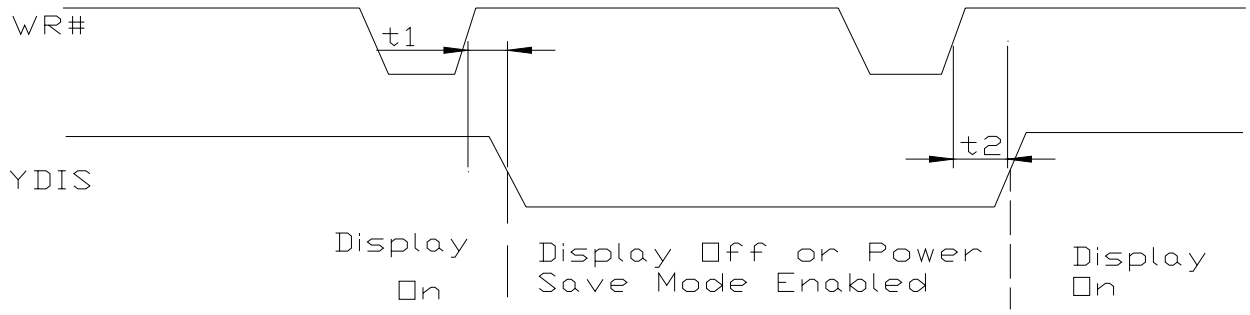
Note:CLK input to the M6800 interface must be driven synchronous to the host microprocessor.

Symbol	Parameter	Min	Max	Units
t1	CS# setup time	5	--	ns
t2	AB[15:0] setup time	5	--	ns
t3	DB[7:0] setup time to RD# falling edge (write cycle)	Note 1	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	--	ns
t5	CS# hold time	7	--	ns
t6	AB[15:0] hold time	7	--	ns
t7	DB[7:0] hold time from RD# falling edge (write cycle)	5	--	ns
t8	DB[7:0] hold time from RD# falling edge (read cycle)	2	55	ns
t9	RD# falling edge to valid Data	--	Note 2	ns
t10	RD# cycle time	Note 3	--	ns
t11	RD# pulse active time	5	--	Ts
t12	RD# pulse inactive time	Note 4	--	ns
t13	AS# setup time	0	--	ns
t14	AS# hold time	0	--	ns

Note: (Ts = System clock period)

1. t3min = 2Ts + 5
2. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
3. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
4. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

Power Save Mode/Display Enable Timing



Symbol	Parameter	Min	Max	Units
t1a	YDIS falling edge delay for Power Save Mode Enable in Indirect Mode (see Note 1)	--	2	Frames
t1b	YDIS falling edge delay for Display Off in Indirect Mode (58h)	--	1Ts+10	ns
t1c	YDIS falling edge delay for Display Off in Direct Mode (see Note 2)	--	2Ts+10	ns
t2	YDIS rising edge delay for Display On (see Note 2)	--	2Ts+10	ns

Note: (Ts = System Clock Period)

1. Power Save Mode is controlled by the Power Save Mode Enable bit, REG[08h] bit 0.
2. Display On/Off is controlled by the Display Enable bit, REG[09h] bit 0.

12. INDIRECT ADDRESSING COMMAND

Indirect Addressing Command

Class	Register Address	Command	Register Description	Control Byte Value	No. of Bytes
System Control	8000h - 8007h	SYSTEM SET	Initializes device and display	40h	8
	8008h	POWER SAVE	Enters standby mode	53h	0
Display Control	8009h - 800A	DISP ON/OFF	Enables/disables display and display attributes	58h 59h	1
	800Bh - 8014h	SCROLL	Sets screen block start addresses and sizes	44h	10
	8015h - 8016h	CSRFORM	Sets cursor type	5Dh	2
	8017h	CSRDIR	Sets direction of cursor movement	4Ch - 4Fh	0
	8018h	OVLAY	Sets display overlay format	5Bh	1
	8019h - 801Ah	CGRAM ADR	Sets start address of character generator RAM	5Ch	2
	801Bh	HDOT SCR	Sets horizontal scroll position	5A	1
Drawing Control	801Ch - 801Dh	CSRW	Sets cursor address	46h	2
	801Eh - 801Fh	CSRR	Reads cursor address	47h	2
	8020h	GRAYSCALE	Sets the Grayscale depth (bpp)	60h	1
Memory Control		MEMWRITE	Writes to memory	42h	n/a
		MEMREAD	Reads from memory	43h	

Command Set

- In general, the internal registers of the SED13700 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.
- 2-byte parameter (where two bytes are treated as 1 data item) are handled as follows:
  1. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
  2. System Set, Scroll, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.
- APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

13. CHARACTER GENERATOR

13.1 Character Generator Characteristics

Internal Character Generator

The internal character generator is recommended for minimum system configurations containing a S1D13700, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- • 5 x 7 pixel font
- • 160 JIS standard characters
- • Can be mixed with character generator RAM (maximum of 64 CGRAM characters)
- • Can be automatically spaced out up to 8 x 16 pixels

Character Generator RAM

The character generator RAM can be used for storing graphics characters. The character generator RAM can be mapped to any display memory location by the microprocessor, allowing effective usage of unused address space.

- • Up to 8 x 8 pixel characters when REG[00h] bit 2 = 0 and 8 x 16 characters when REG[00h] bit 2 = 1
- • Can be mapped anywhere in display memory address space if used with the character generator ROM (REG[00h] bit 0 = 0)

13.2 Setting the Character Generator Address

The CGRAM addresses in the display memory address space are not mapped directly from the address in the Character Generator RAM Start Address registers, REG[19h] -REG[1Ah]. The data to be displayed is at a CGRAM address calculated from (REG[19h] -REG[1Ah]) + character code + ROW select address.

The following tables show the address mapping for CGRAM addresses.

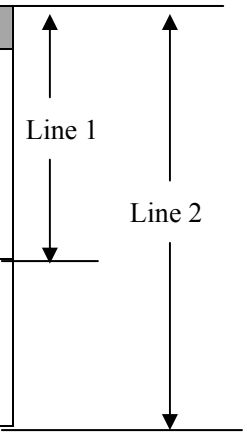
Character Fonts Where Number of Lines ≤ 8 (REG[00h] bit 2 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Character fonts, ≤ 9 number of lines ≤ 16 (M2=1, M1=0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

R_{OW}	R3	R2	R1	R0
$R_{OW}0$	0	0	0	0
$R_{OW}1$	0	0	0	1
$R_{OW}2$	0	0	1	0
↓	↓	↓	↓	↓
$R_{OW}7$	0	1	1	1
$R_{OW}8$	1	0	0	0
↓	↓	↓	↓	↓
$R_{OW}14$	1	1	1	0
$R_{OW}15$	1	1	1	1



Row select address

Note: Lines=1: lines in the character bitmap ≤ 8

Lines=2: lines in the character bitmap ≥ 9

3. Character Codes

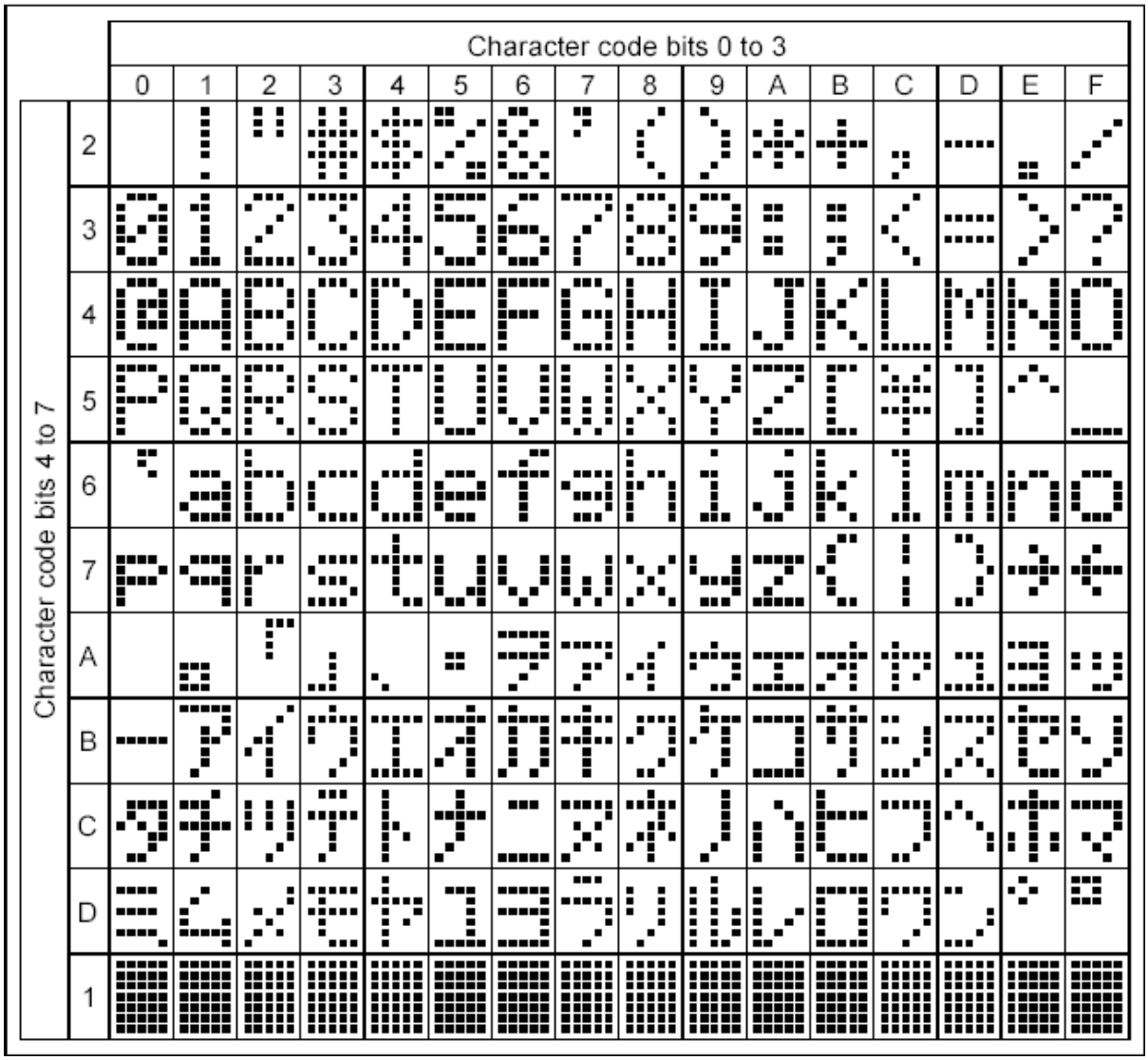
The following figure shows the character codes and the codes allocated to CG RAM. ALL codes can be used by the CG RAM if not using the internal ROM, but the CGRAM address must be set to 0.

	Upper 4 bits															
Lower 4 bits	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		■		0	@	P	'	p				ー	タ	三		
1		■	!	1	A	Q	a	q			。	ア	チ	ㄙ		
2		■	"	2	B	R	b	r			「	イ	ツ	メ		
3		■	#	3	C	S	c	s			」	ウ	テ	モ		
4		■	$	4	D	T	d	t			、	エ	ト	ヤ		
5		■	%	5	E	U	e	u			・	オ	ナ	ユ		
6		■	&	6	F	V	f	v			ヲ	カ	ニ	ヨ		
7		■	'	7	G	W	g	w			ァ	キ	ヌ	ラ		
8		■	(	8	H	X	h	x			ィ	ク	ネ	リ		
9		■	)	9	I	Y	i	y			ゥ	ケ	ノ	ル		
A		■	*	:	J	Z	j	z			ェ	コ	ハ	レ		
B		■	+	;	K	[	k	{			ォ	サ	ヒ	ロ		
C		■	,	<	L	¥	l	¦			ャ	シ	フ	ワ		
D		■	.	=	M	]	m	}			ュ	ス	ヘ	ン		
E		■	-	>	N	^	n	→			ョ	セ	ホ	゛		
F		■	/	?	O	_	o	←			ッ	ソ	マ	゜		

CGRAM1 CGRAM2

On- chip character codes

4. Internal Character Generator Font



Note:The shaded positions indicate characters that have the whole 6 · 8 bitmap blackened.

14. MICROPROCESSOR INTERFACE

14.1 System Bus Interface

CNF[4:0], A[15:1], A0, D[7:0], RD#, WR#, AS and CS are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. CNF[4:2] change the operation of the RD# and WR# pins to enable interfacing to either a Generic (Z80), M6800, or MC68K family bus, and should be pulled-up or pulled down

Generic

The following table shows the signal states for each function.

Generic Interface Signals

A0	**RD#**	**WR#**	**Function**
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

14.2 M6800 Series

M6800 Series interface signals

A0	R/W#	E	Function
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

14.3 MC68K Series

MC68K series interface signals

A0	RD/WR#	LDS#	Function
1	1	0	Display data and cursor address read
0	0	0	Display data and parameter write
1	0	0	Command write

15. LCD MODULES HANDLING PRECAUTIONS

- Please remove the protection foil of polarizer before using.

- Be sure that you are grounded when handing LCM

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

16. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for LCD Graphic Display Modules & Accessories ***category:***

Click to view products by Display Elektronik ***manufacturer:***

Other Similar products are found below :

NA57W001B HDM64GS12L-Y11S LCM-H12864GSFH-Y MGLS-240128-Z05 GLK19264A-7T-1U-TCI-LV-E DEM 128032A FGH RG12864F-FHW-M EGLK19264A-7T-WB-VPT-PL HG2G-V5FT22TF-W HG1G-4VT22TF-S HDM64GS24L-2-Y14S LTS-2301AP LTS-6760P LTS-6980HR RG12864A-GHC-V RG12864A-GHY-V RG12864A-TIG-V RG12864A-TIY-V RG12864A-YHY-X RG12864B-FHW-V RG12864B-GHW-V RG12864C-YHW-V RG12864K-BIW-VBG RG160128A-TIW-V RG240128B-YHY-M RG320240A1-BIW-V RG320240B-BIW-V RG320240B-FHW-V DEM 097032A SGH-PY DEM 122032A SYH-LY DEM 122032C SBH-PW-N-12 DEM 128064A SBH-PW-N DEM 128064B SBH-PW-N DEM 128064F FGH-P(RGB) DEM 128064G FGH-PW DEM 128064I FGH-PW DEM 128064J SBH-PW-N DEM 128064O FGH-PW DEM 128064O SBH-PW-N DEM 128064Q SBH-PW-N DEM 128128D FGH-PW DEM 240064B FGH-PW DEM 240064B SBH-PW-N DEM 240160A SBH-PW-N DEM 320240B FGH-PW-N DEM 320240C FGH-PW EA W240-7KHLW RX12864A1-BIW RX12864D3-BIW RX240128A-FGN