

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CFD2 650V

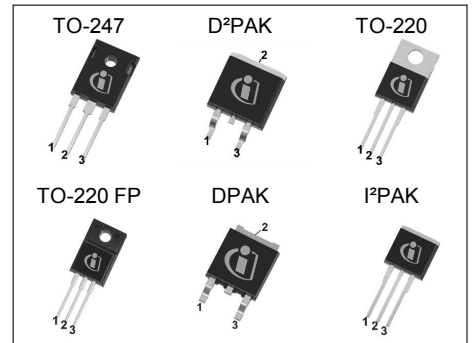
650V CoolMOS™ CFD2 Power Transistor
IPx65R420CFD

Data Sheet

Rev. 2.4
Final

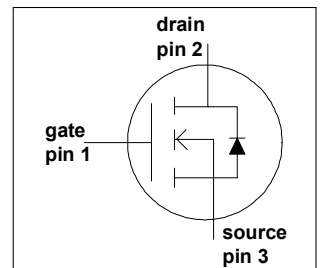
1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.



Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Easy to use/drive
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Pb-free plating, Halogen free mold compound (except PG-TO252)



Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server and Telecom



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j \max}$	700	V
$R_{DS(on),max}$	0.42	Ω
Q_g,typ	31.5	nC
$I_D,pulse$	27	A
$E_{oss} @ 400V$	2.8	μJ
Body diode di/dt	900	A/ μs
Q_{rr}	0.3	μC
t_{rr}	90	ns
I_{rrm}	6.2	A

Type / Ordering Code	Package	Marking	Related Links
IPW65R420CFD	PG-TO 247	65F6420	see Appendix A
IPB65R420CFD	PG-TO 263		
IPP65R420CFD	PG-TO 220		
IPA65R420CFD	PG-TO 220 FullPAK		
IPD65R420CFD	PG-TO 252		
IPI65R420CFD	PG-TO 262		



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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			8.7	A	$T_C = 25^\circ\text{C}$
				5.5		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			27	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			227	mJ	$I_D = 1.8\text{A}$, $V_{DD} = 50\text{V}$ (see table 22)
Avalanche energy, repetitive	E_{AR}			0.34	mJ	$I_D = 1.8\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			1.8	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{Hz}$)
Power dissipation (non FullPAK) TO-247, TO-220, I ² PAK	P_{tot}			83.3	W	$T_C = 25^\circ\text{C}$
Power dissipation (FullPAK) TO-220 FP	P_{tot}			31.2	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Mounting torque (non FullPAK) TO-247, TO-220, I ² PAK				60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220 FP				50	Ncm	M2.5 screws
Continuous diode forward current	I_S			8.7	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			27	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ (see table 20)
Maximum diode commutation speed	di_r/dt			900	A/ μs	

¹⁾ Limited by $T_{j\text{max}}$.

²⁾ Pulse width t_p limited by $T_{j\text{max}}$

³⁾ $V_{peak} < V_{(BR)DSS}$, $T_j < T_{j\text{max}}$, identical low side and high side switch with same R_g

3 Thermal characteristics

Table 3 Thermal characteristics TO-247, TO-220, I²PAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			1.5	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics TO-220 FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			4	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 5 Thermal characteristics D²PAK, DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			1.5	°C/W	
Thermal resistance, junction - ambient ¹⁾	R_{thJA}			62	°C/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL

¹⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}, I_D = 0.3mA$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
			100			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ C$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.378	0.42	Ω	$V_{GS} = 10V, I_D = 3.4A, T_j = 25^\circ C$
			0.983			$V_{GS} = 10V, I_D = 3.4A, T_j = 150^\circ C$
Gate resistance	R_G		4		Ω	$f = 1MHz, \text{open drain}$

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		870		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	C_{oss}		45		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		36		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		161		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Turn-on delay time	$t_{d(on)}$		10		ns	$V_{DD} = 480V, V_{GS} = 13V, I_D = 5.2A, R_G = 3.4\Omega$ (see table 21)
Rise time	t_r		7		ns	
Turn-off delay time	$t_{d(off)}$		38		ns	
Fall time	t_f		8		ns	

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		6.4		nC	$V_{DD} = 480V, I_D = 5.2A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		18.6		nC	
Gate charge total	Q_g		31.5		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V



Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 5.2A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		90		ns	$V_R = 400V, I_F = 5.2A,$ $di_F/dt = 100A/\mu s$ (see table 20)
Reverse recovery charge	Q_{rr}		0.3		μC	
Peak reverse recovery current	I_{rrm}		6.2		A	

5 Electrical characteristics diagrams

Table 10

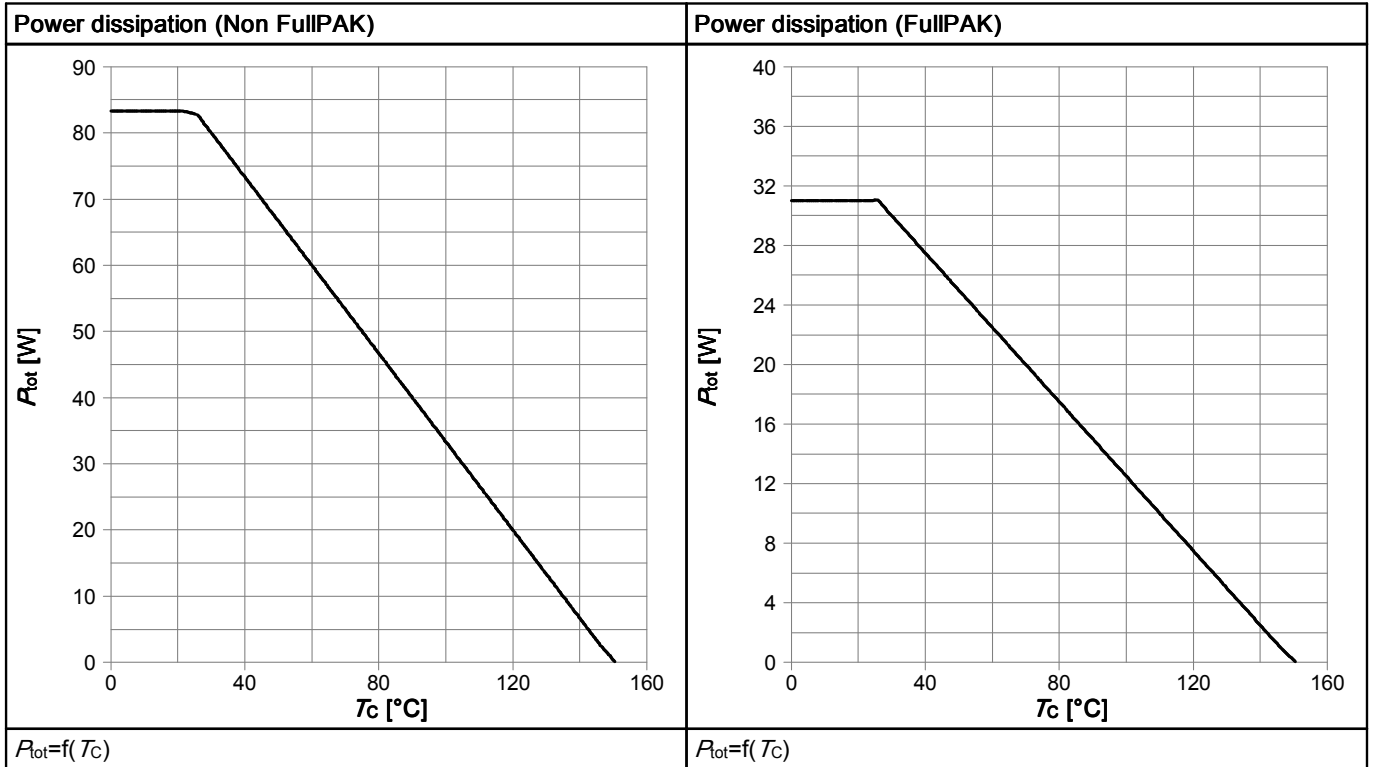


Table 11

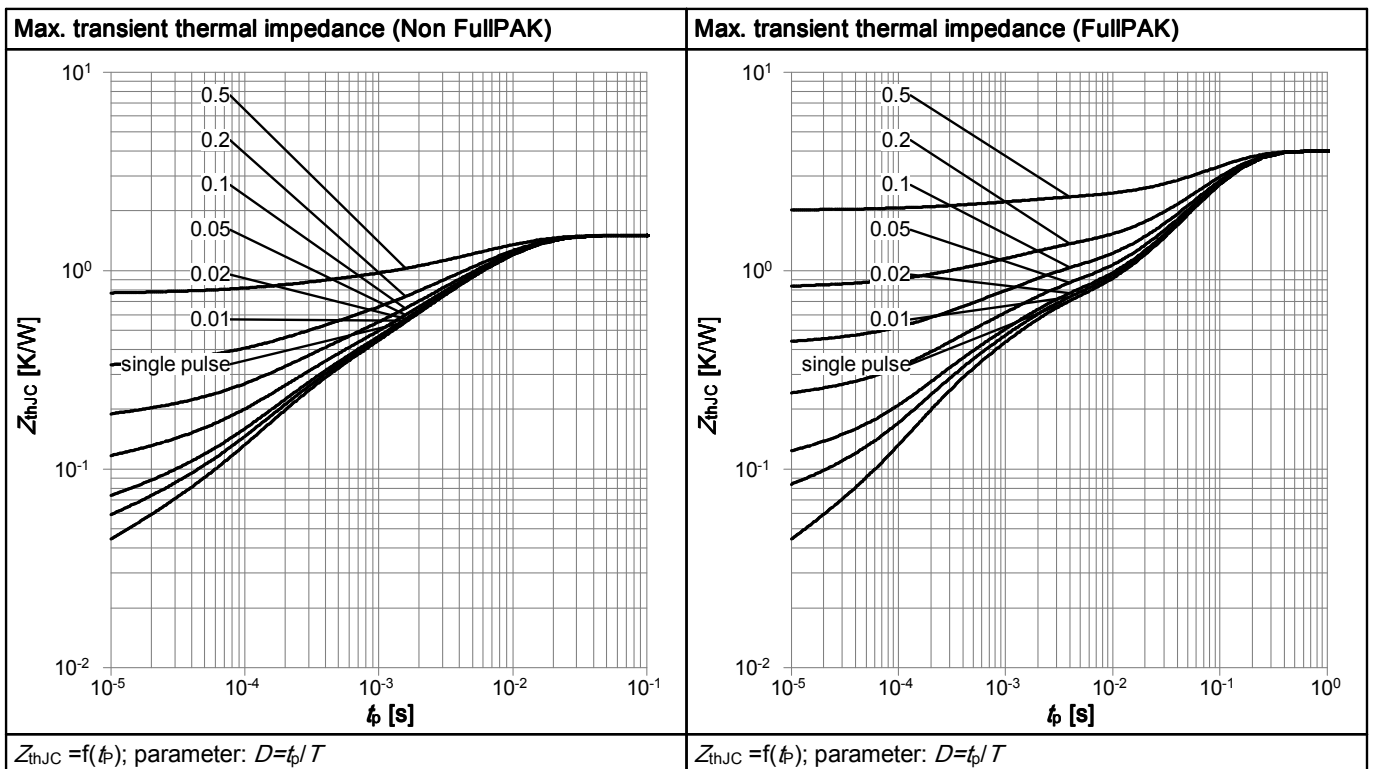


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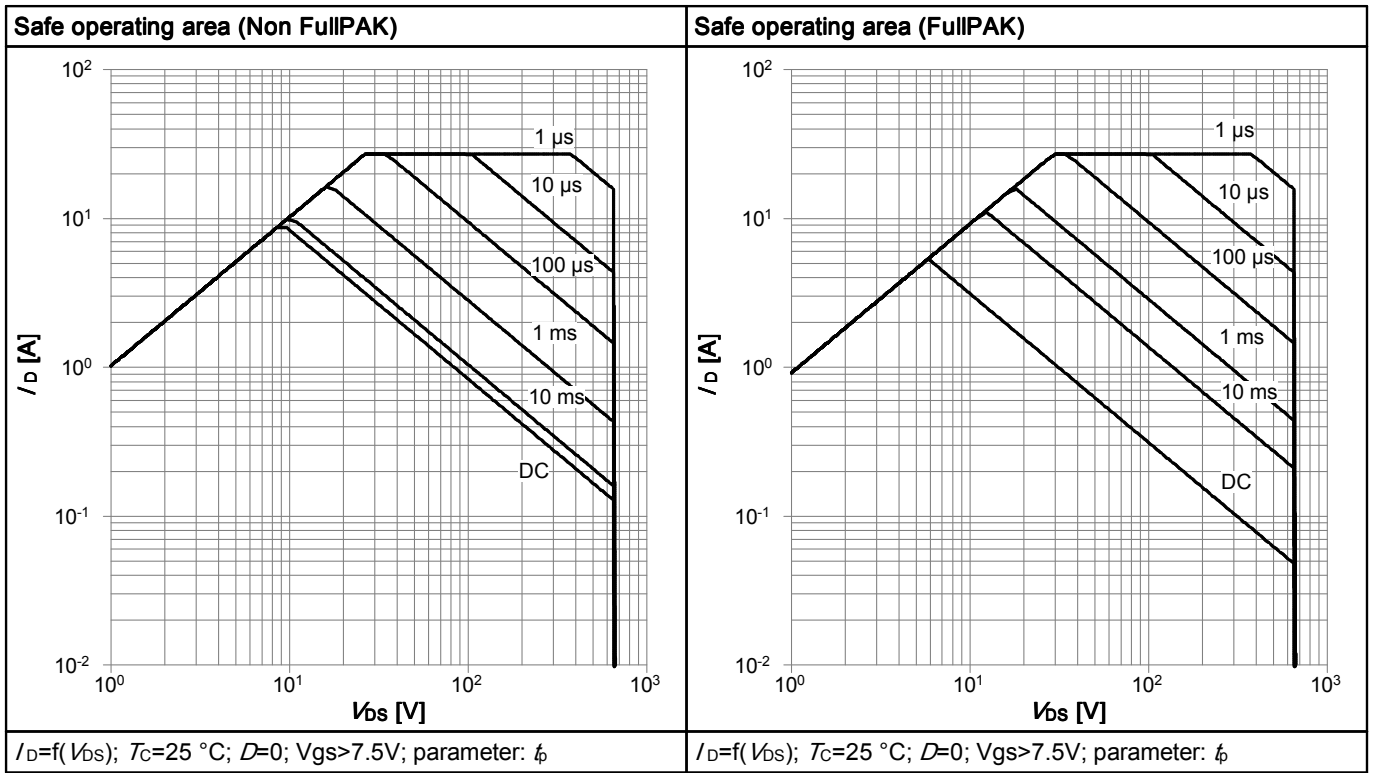


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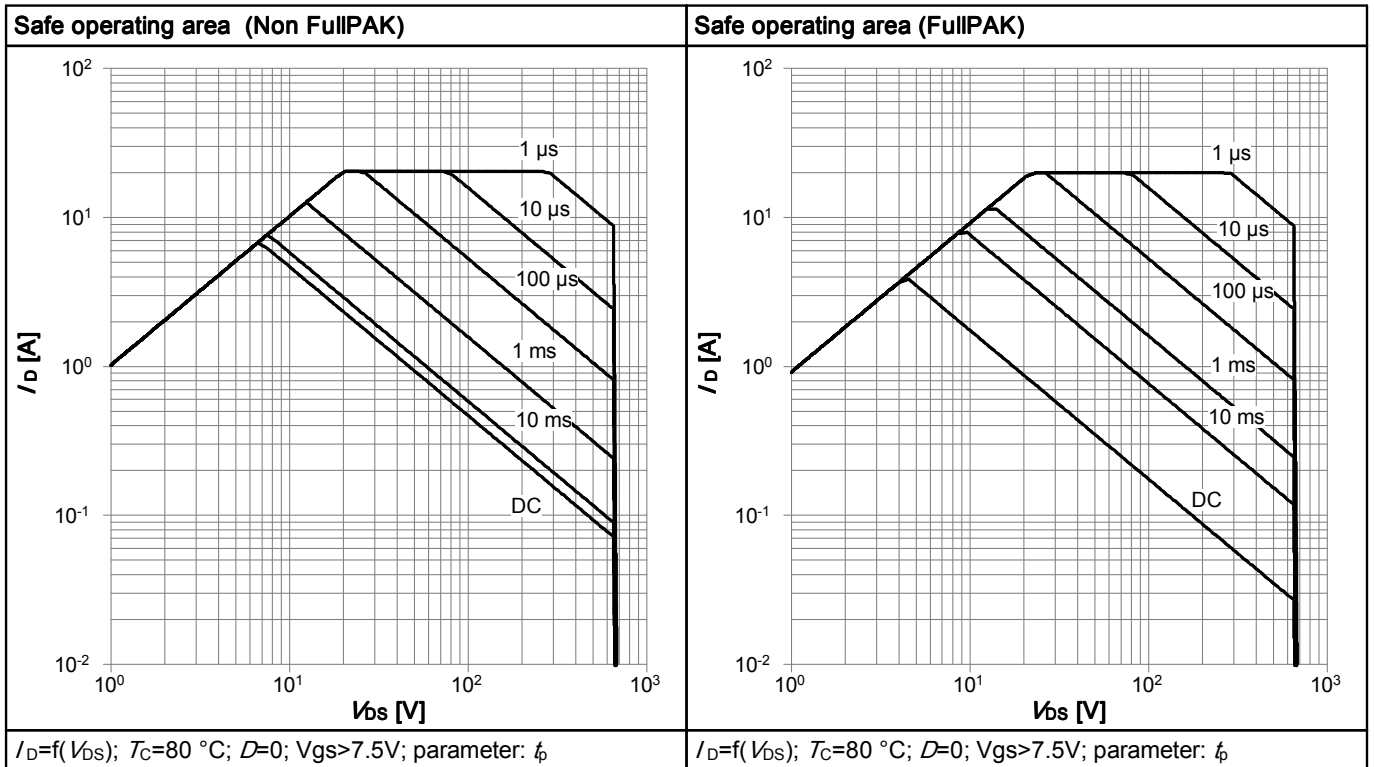


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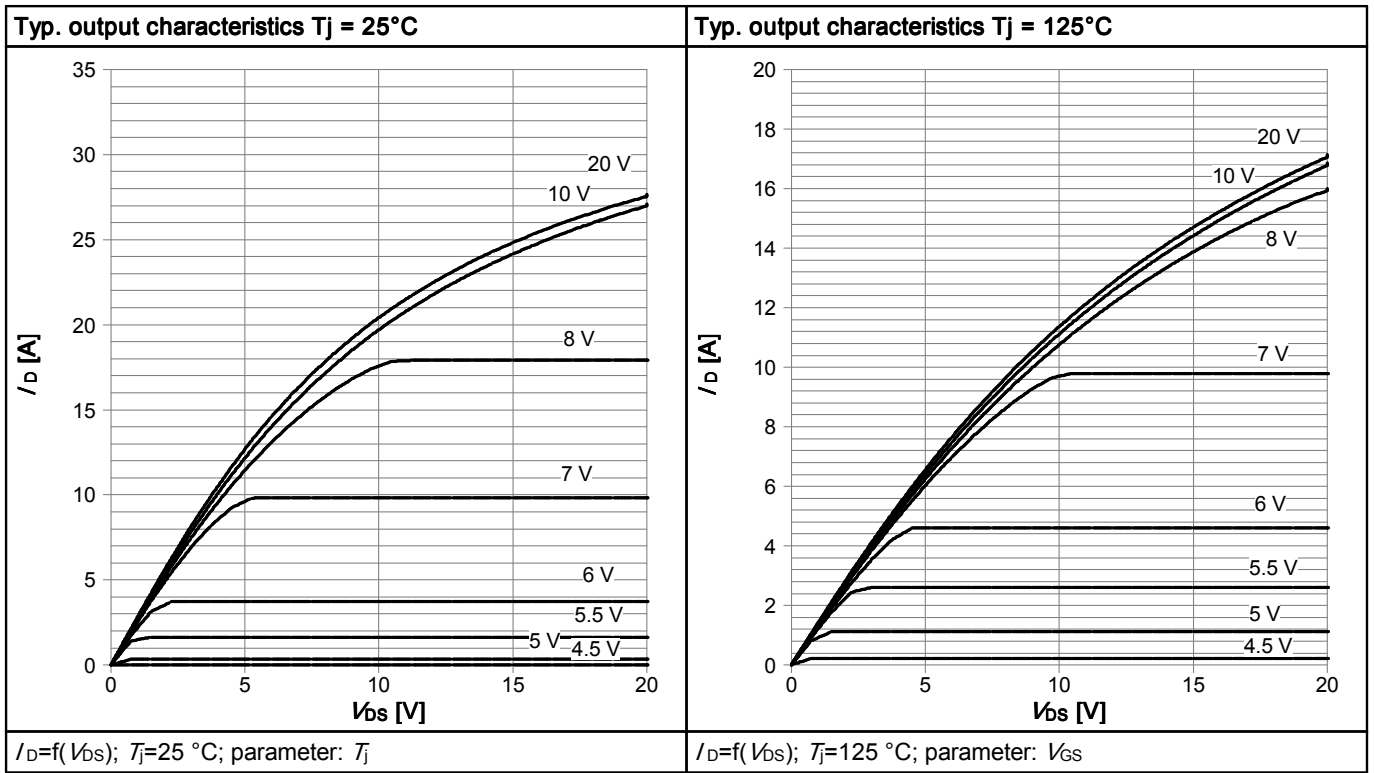


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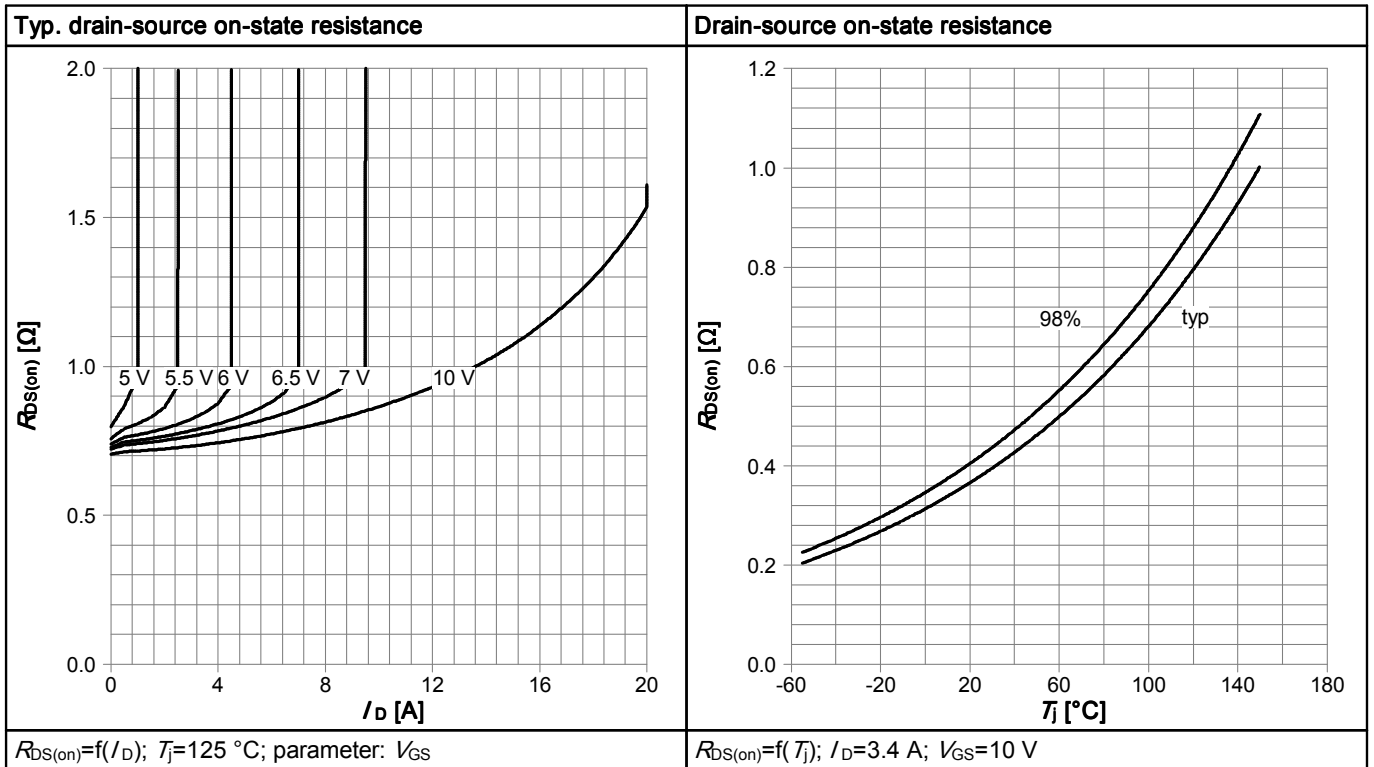


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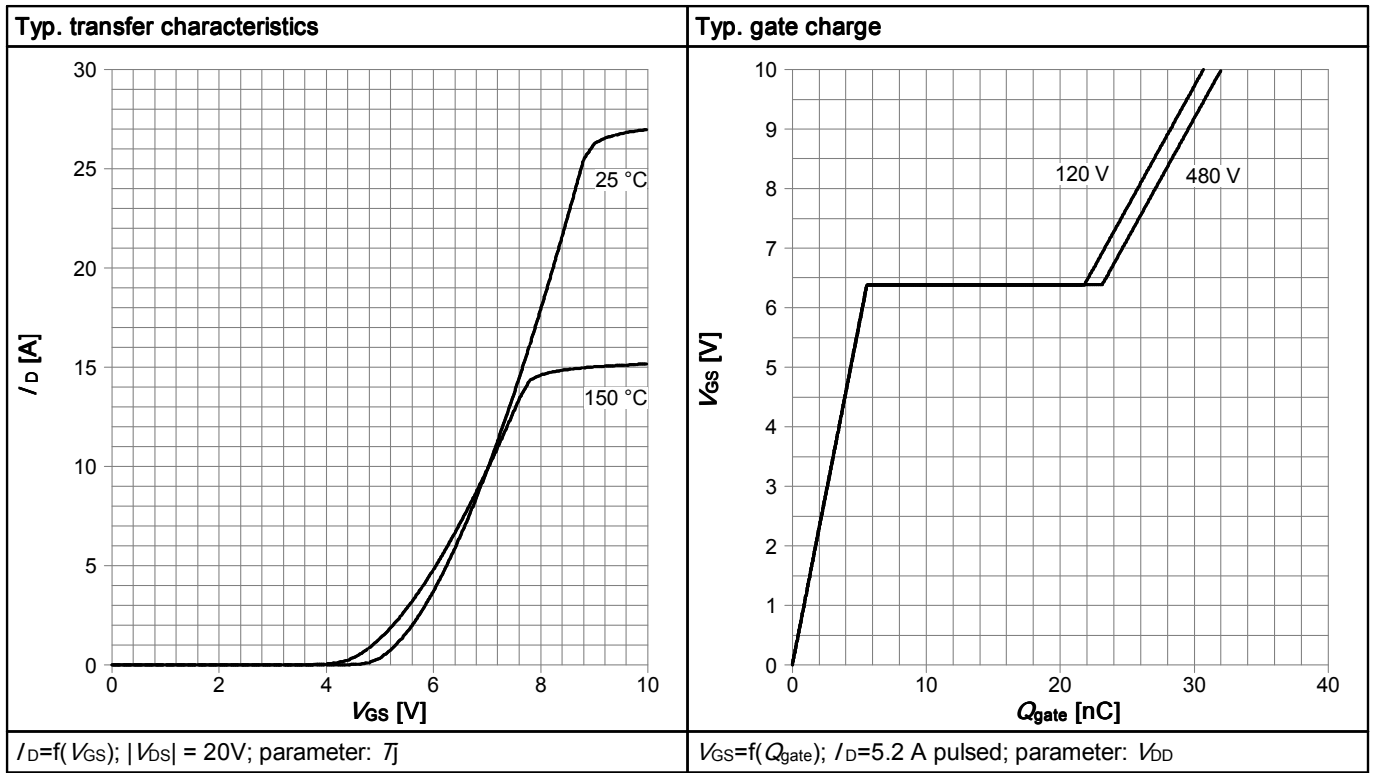


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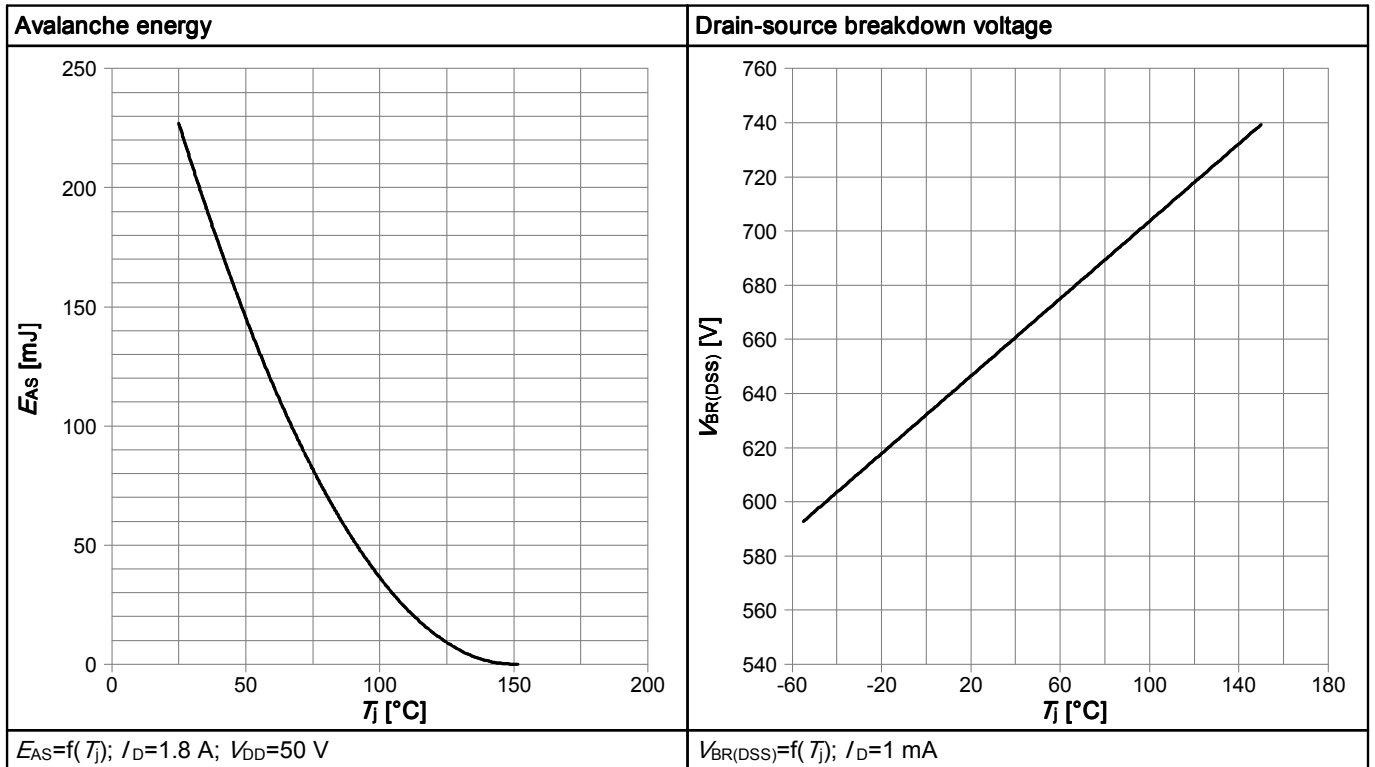


Table 18

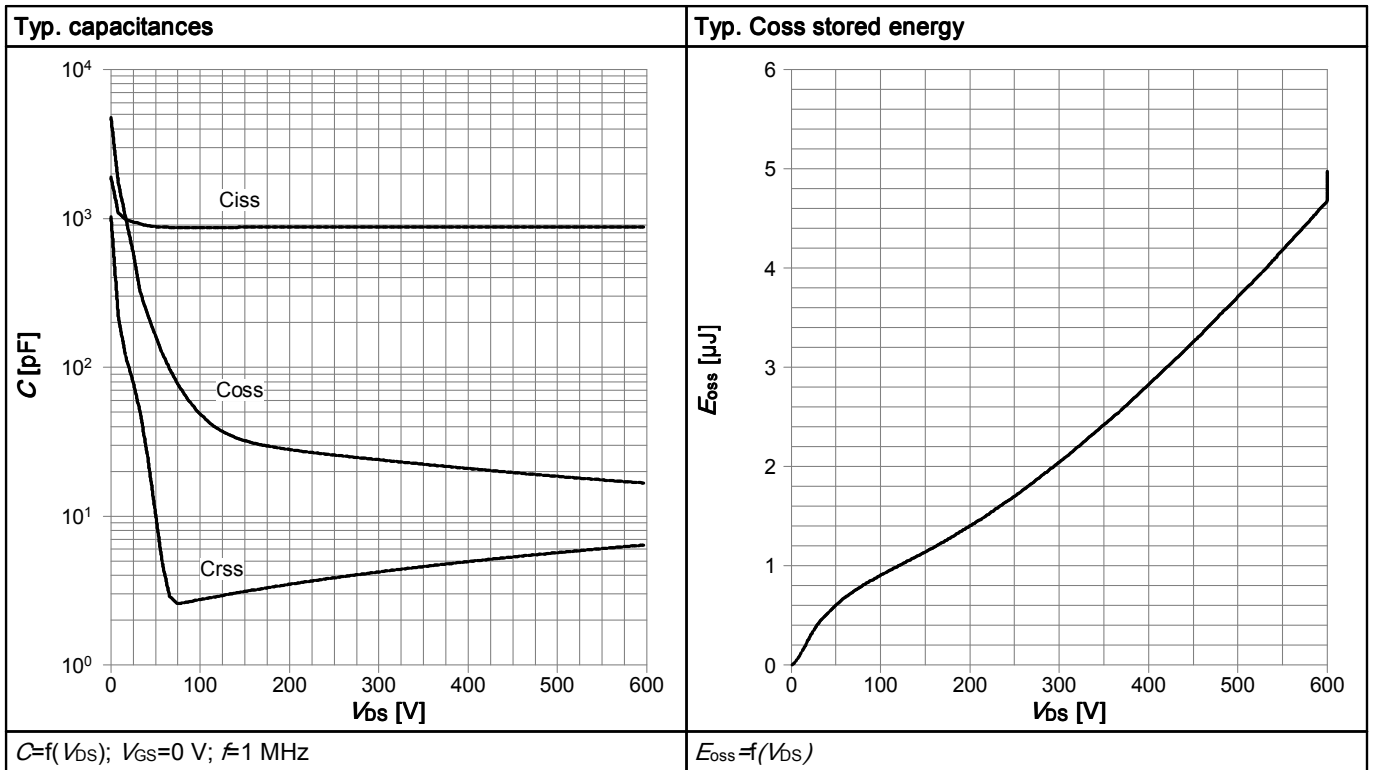
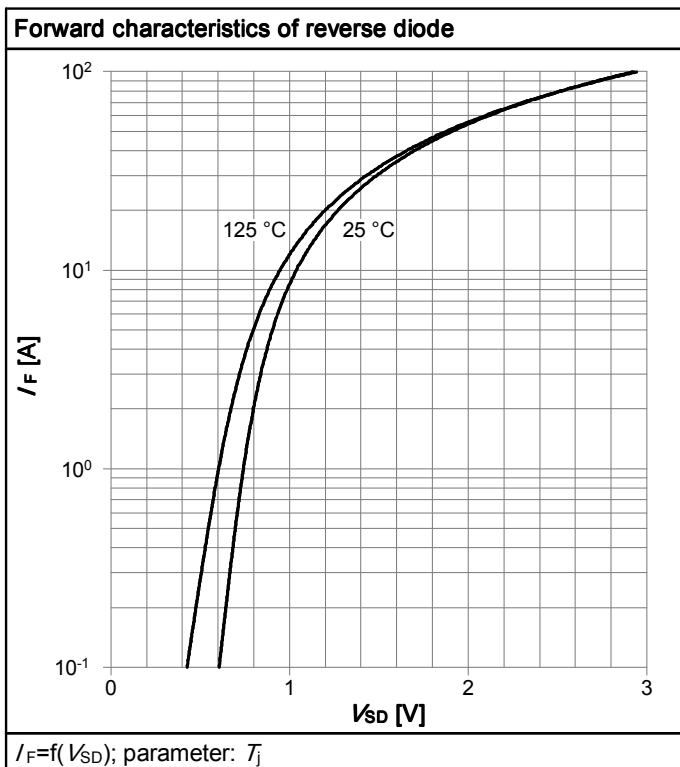


Table 19



6 Test Circuits

Table 20 Diode characteristics

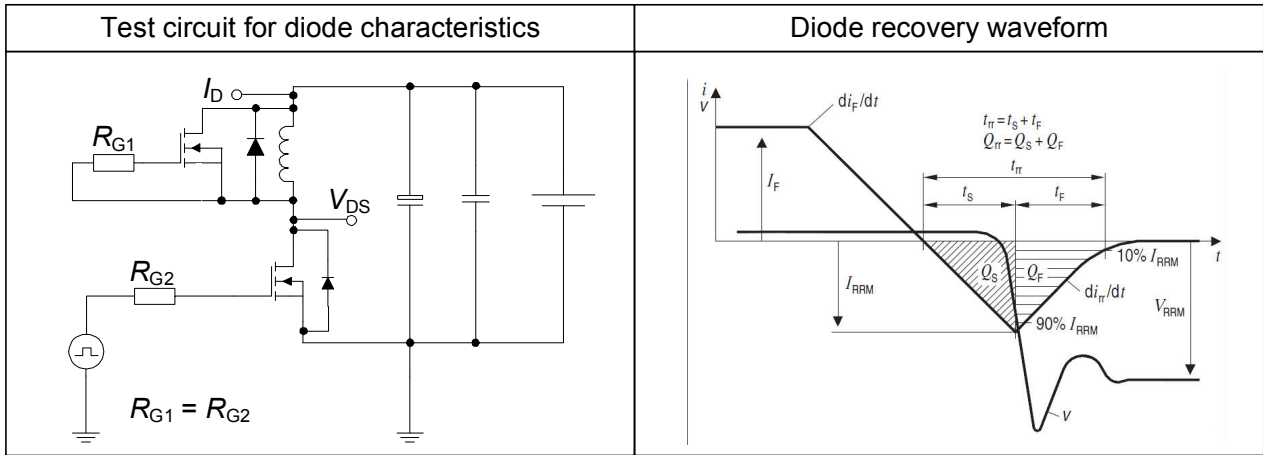


Table 21 Switching times

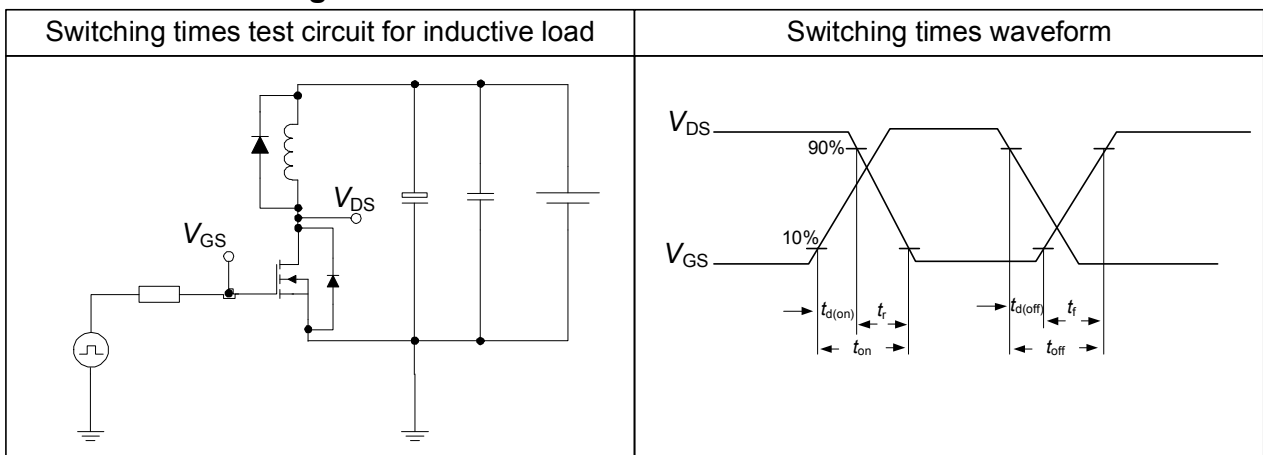
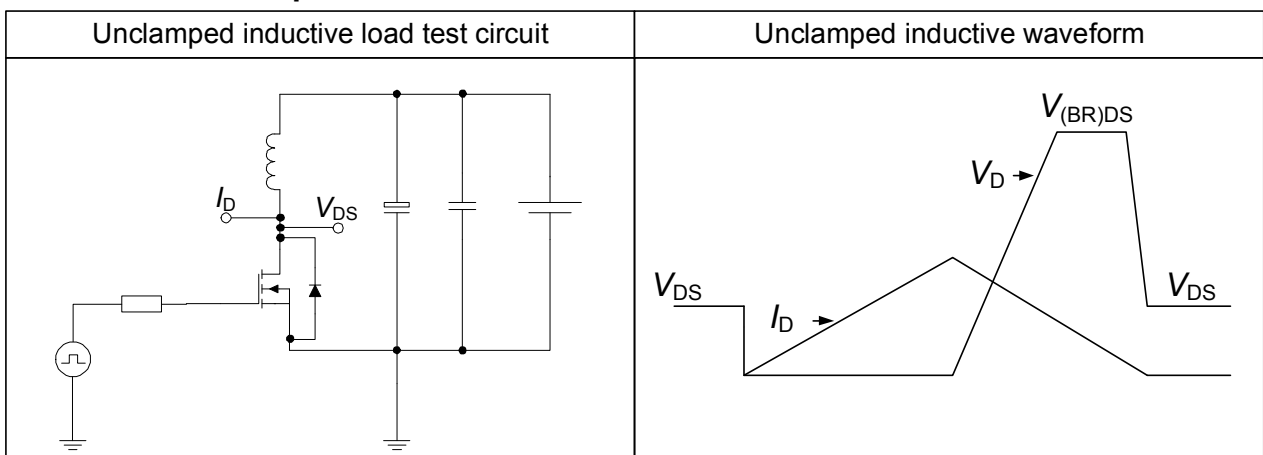


Table 22 Unclamped inductive



7 Package Outlines

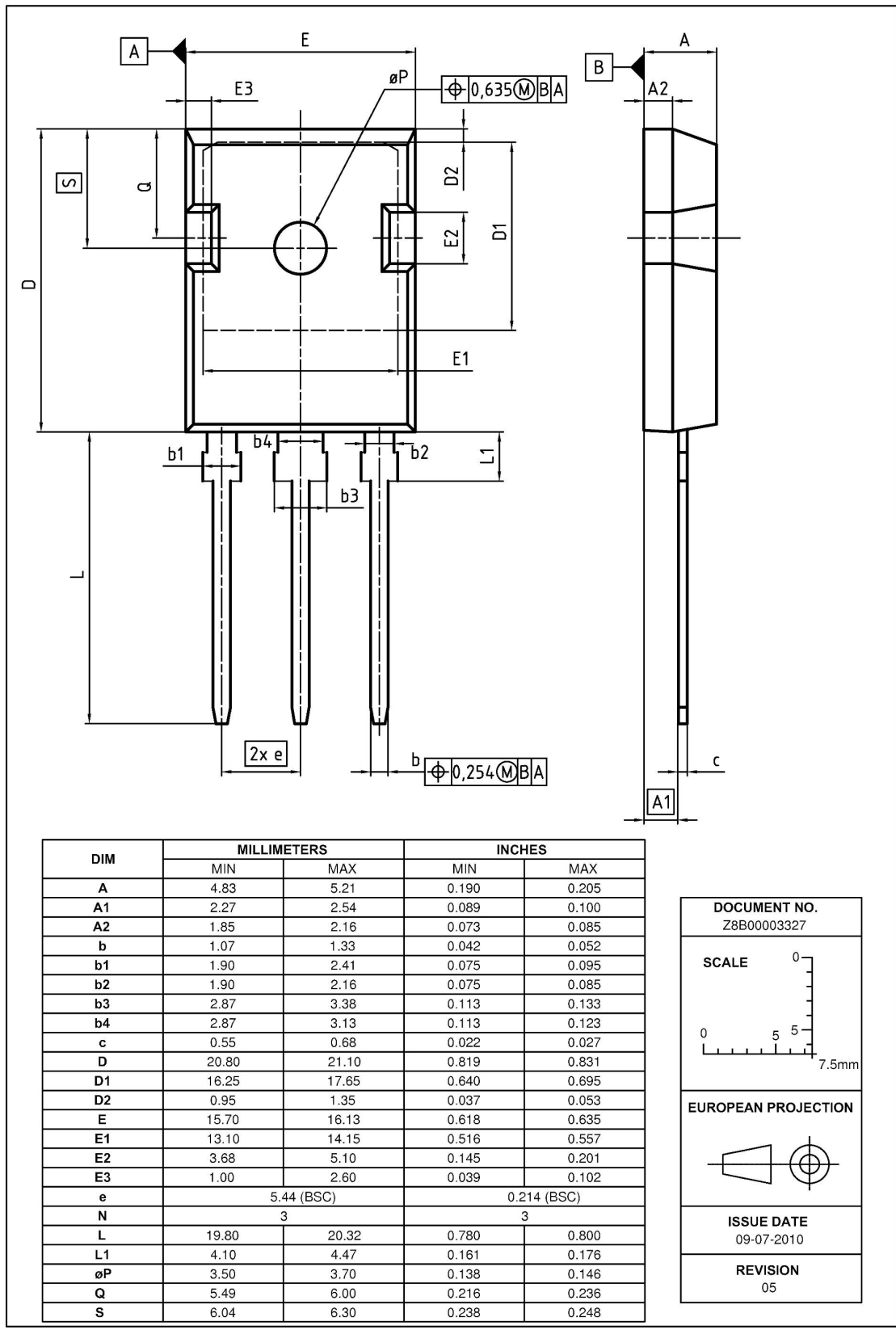


Figure 1 Outline PG-TO 247, dimensions in mm/inches



Figure 2 Outline PG-TO 263, dimensions in mm/inches



Figure 3 Outline PG-TO 220, dimensions in mm/inches

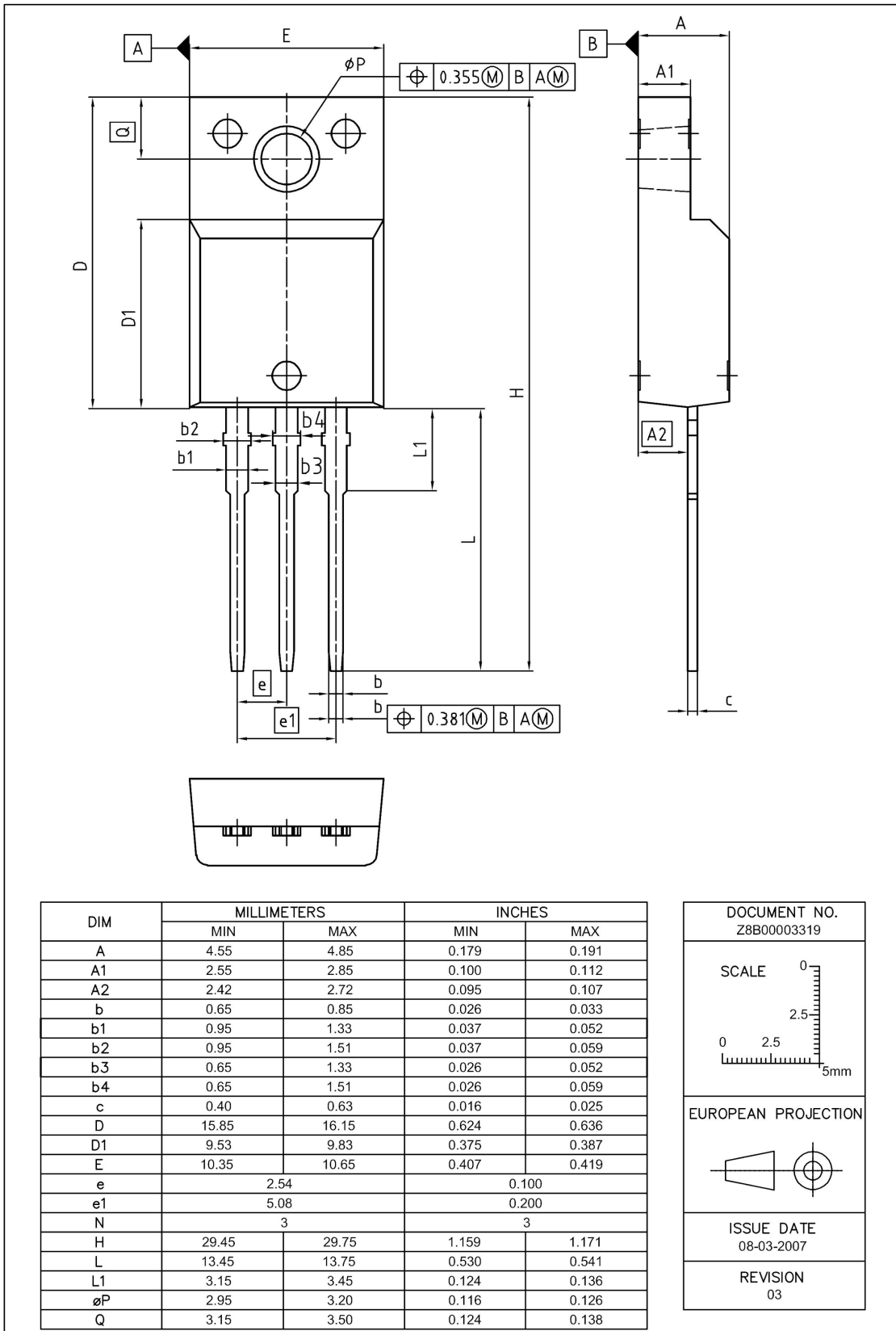


Figure 4 Outline PG-TO 220 FullPAK, dimensions in mm/inches

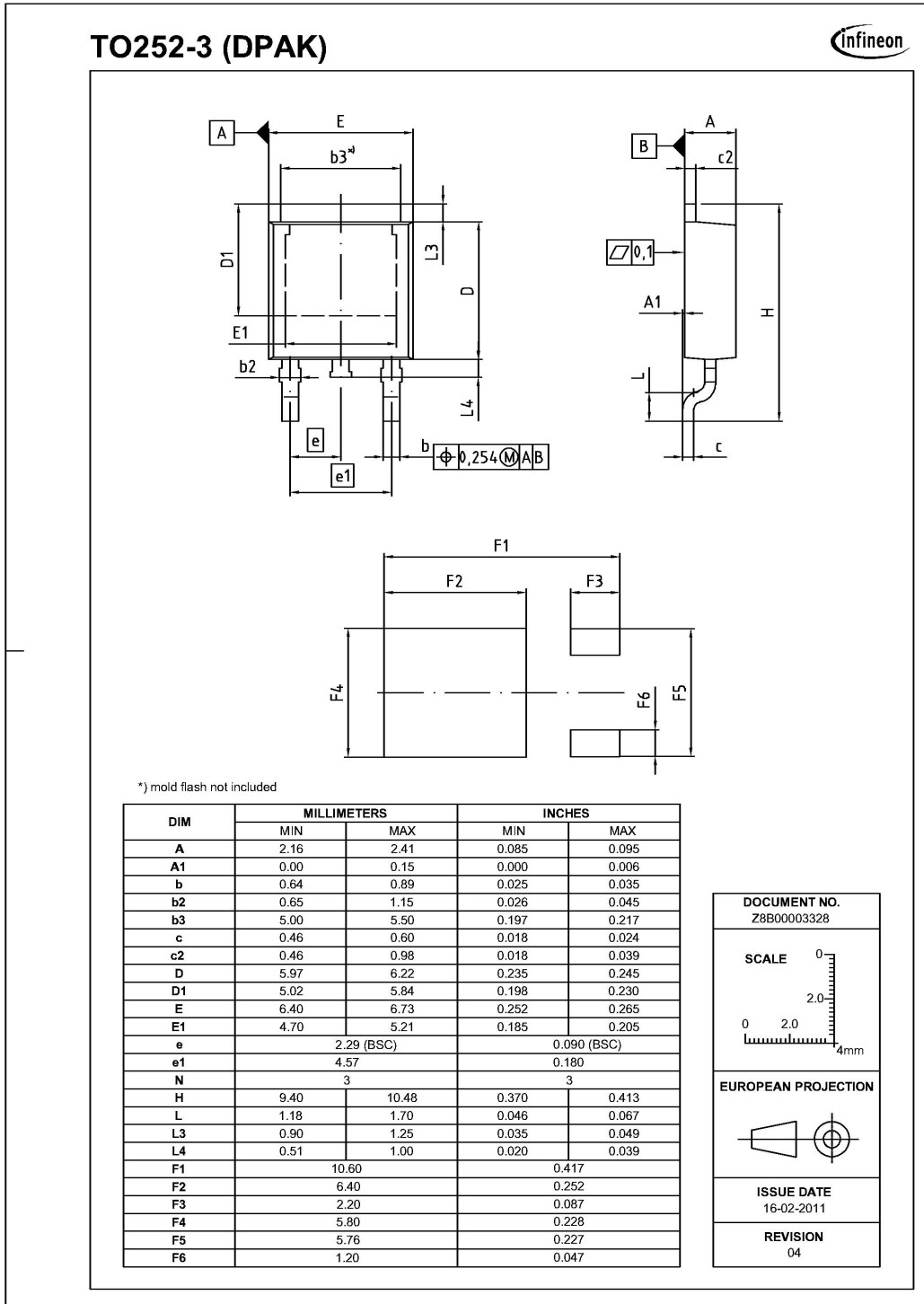


Figure 5 Outline PG-TO 252, dimensions in mm/inches

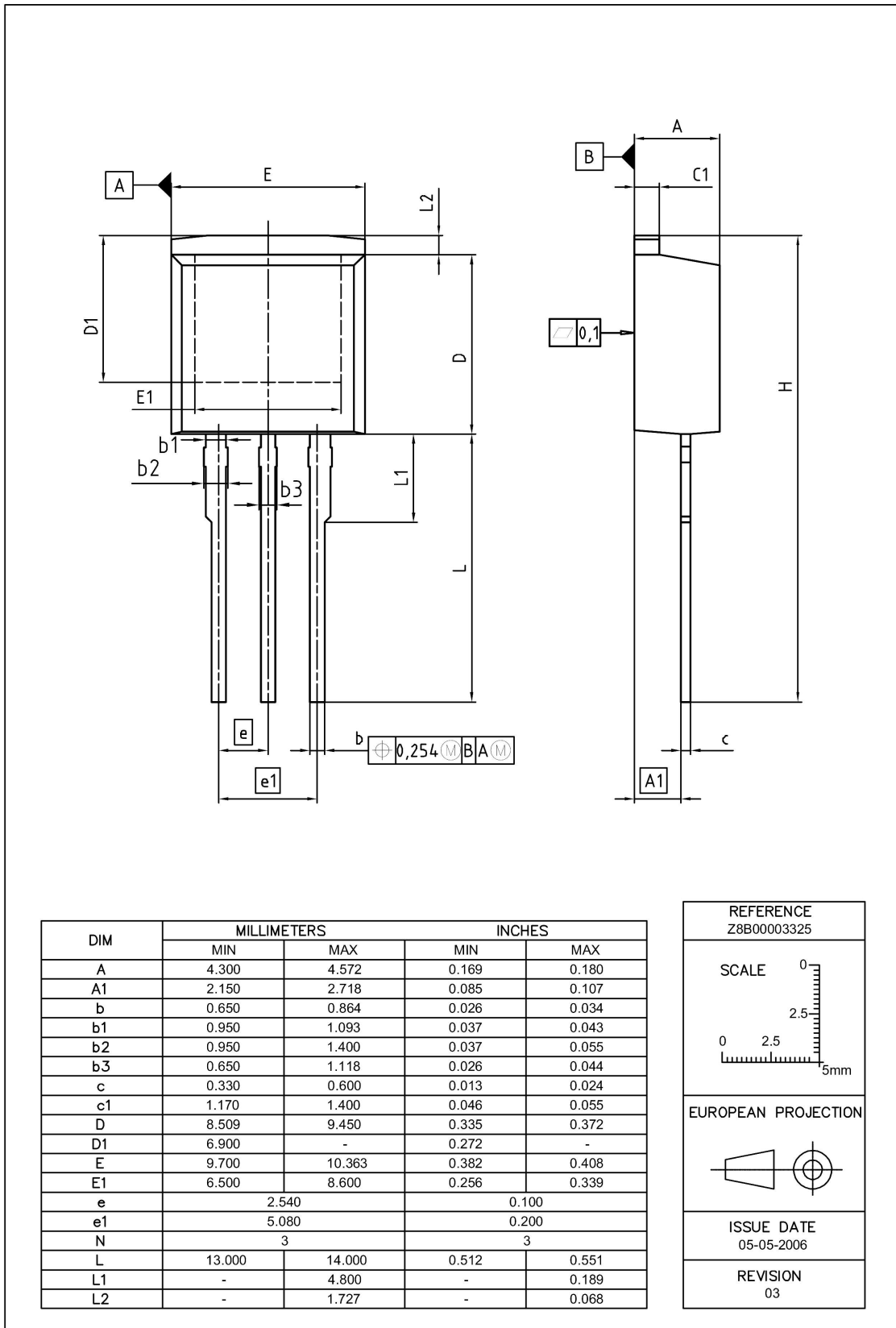


Figure 6 Outline PG-TO 262, dimensions in mm/inches



8 Appendix A

Table 23 Related Links

- **IFX Design Tools:**
<http://www.infineon.com/cms/en/product/promopages/designtools/index.html>
- **IFX CoolMOS Webpage:**
<http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8>



Revision History

IPW65R420CFD , IPB65R420CFD , IPP65R420CFD , IPA65R420CFD , IPD65R420CFD , IPI65R420CFD

Revision: 2012-06-01, Rev. 2.7

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2011-05-04	Release of final datasheet
2.1	2011-05-05	release of final datasheet
2.2	2011-06-07	Update V_{DS} @ $T_{j\ max}$
2.3	2011-08-29	update to CFD2 standard
2.4	2011-09-14	update pin naming
2.5	2011-09-16	release of new pin naming
2.6	2011-09-26	update the Igss test condition
2.7	2012-06-01	update SOA, AE, Typ. Gate Charge

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

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