

## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## CoolMOS™ CFD2 650V Thinpak

650V CoolMOS™ CFD2 Power Transistor  
IPL65R210CFD

## Data Sheet

Rev. 2.0  
Final

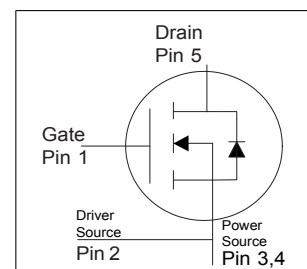
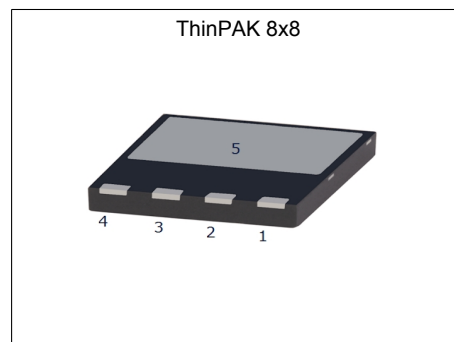
Industrial & Multimarket

## 1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.

### ThinPAK

ThinPAK is a new leadless SMD package for HV MOSFETs. The new package has a very small footprint of only 64mm<sup>2</sup> (vs. 150mm<sup>2</sup> for the D<sup>2</sup>PAK) and a very low profile with only 1mm height (vs. 4.4mm for the D<sup>2</sup>PAK). The significantly smaller package size, combined with benchmark low parasitic inductances, provides designers with a new and effective way to decrease system solution size in power-density driven designs.



## Features

- Reduced board space consumption
- Increased power density
- Short commutation loop
- Smooth switching waveform
- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM  $R_{ds(on)} \cdot Q_g$  and  $E_{oss}$
- Easy to use/drive
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Pb-free plating, Halogen free mold compound



## Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching stages for e.g. PC Silverbox, LCD TV, Lighting, Server and Telecom.

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{Jmax}$	700	V
$R_{DS(on),max}$	0.21	$\Omega$
$Q_g,typ$	68	nC
$I_D,pulse$	53	A
$E_{oss} @ 400V$	5.7	$\mu J$
Body diode $di/dt$	900	A/ $\mu s$
$Q_{rr}$	0.5	$\mu C$
$t_{rr}$	120	ns
$I_{rrm}$	7.5	A

Type / Ordering Code	Package	Marking	Related Links
IPL65R210CFD	PG-VSON-4	65F6210	see Appendix A

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## 2 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$			16.6	A	$T_C = 25^\circ\text{C}$
				10.5		$T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$			53	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$			484	mJ	$I_D = 3.3\text{A}$ , $V_{DD} = 50\text{V}$ (see table 10)
Avalanche energy, repetitive	$E_{AR}$			0.70	mJ	$I_D = 3.3\text{A}$ , $V_{DD} = 50\text{V}$
Avalanche current, repetitive	$I_{AR}$			3.3	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	$V_{GS}$	-20		20	V	static
		-30		30		AC ( $f > 1\text{ Hz}$ )
Operating and storage temperature	$T_j, T_{stg}$	-40		150	$^\circ\text{C}$	
Continuous diode forward current	$I_S$			16.6	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			53	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_D$ ,
Maximum diode commutation speed	di <sub>i</sub> /dt			900	A/ $\mu\text{s}$	$T_j = 25^\circ\text{C}$ (see table 8)
Power dissipation	$P_{tot}$			151	W	$T_C = 25^\circ\text{C}$

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup>  $V_{peak} < V_{(BR)DSS}$ ,  $T_j < T_{j,max}$ , identical low side and high side switch with same  $R_g$

### 3 Thermal characteristics

**Table 3 Thermal characteristics ThinPAK 8x8**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$			0.83	°C/W	
Thermal resistance, junction - ambient <sup>1)</sup>	$R_{thJA}$			62	°C/W	SMD version, device on PCB, minimal footprint
				45		SMD version, device on PCB, 6cm <sup>2</sup> cooling area
Soldering temperature, wave- & reflowsoldering allowed	$T_{sold}$			260	°C	reflow MSL 3

<sup>1)</sup> Device on 40mm\*40mm\*1.5mm one layer epoxy PCB FR4 with 6cm<sup>2</sup> copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

## 4 Electrical characteristics

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}, I_D = 0.7mA$
Zero gate voltage drain current	$I_{DSS}$			1	$\mu A$	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
			200			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ C$
Gate-source leakage current	$I_{GSS}$			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.189	0.21	$\Omega$	$V_{GS} = 10V, I_D = 7.3A, T_j = 25^\circ C$
			0.491			$V_{GS} = 10V, I_D = 7.3A, T_j = 150^\circ C$
Gate resistance	$R_G$		1		$\Omega$	$f = 1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$		1850		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	$C_{oss}$		86		pF	
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$		70		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$		336		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Turn-on delay time	$t_{d(on)}$		12		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 11.0A, R_G = 3.4\Omega$ (see table 9)
Rise time	$t_r$		8.4		ns	
Turn-off delay time	$t_{d(off)}$		53.2		ns	
Fall time	$t_f$		6.4		ns	

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$		12		nC	$V_{DD} = 480V, I_D = 11A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$		37		nC	
Gate charge total	$Q_g$		68		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$		0.9		V	$V_{GS} = 0V, I_F = 11.0A, T_j = 25^\circ C$
Reverse recovery time	$t_{rr}$		120		ns	$V_R = 400V, I_F = 11.0A,$ $di_F/dt = 100A/\mu s$ (see table 8)
Reverse recovery charge	$Q_{rr}$		0.5		$\mu C$	
Peak reverse recovery current	$I_{rrm}$		7.6		A	

### 5 Electrical characteristics diagrams

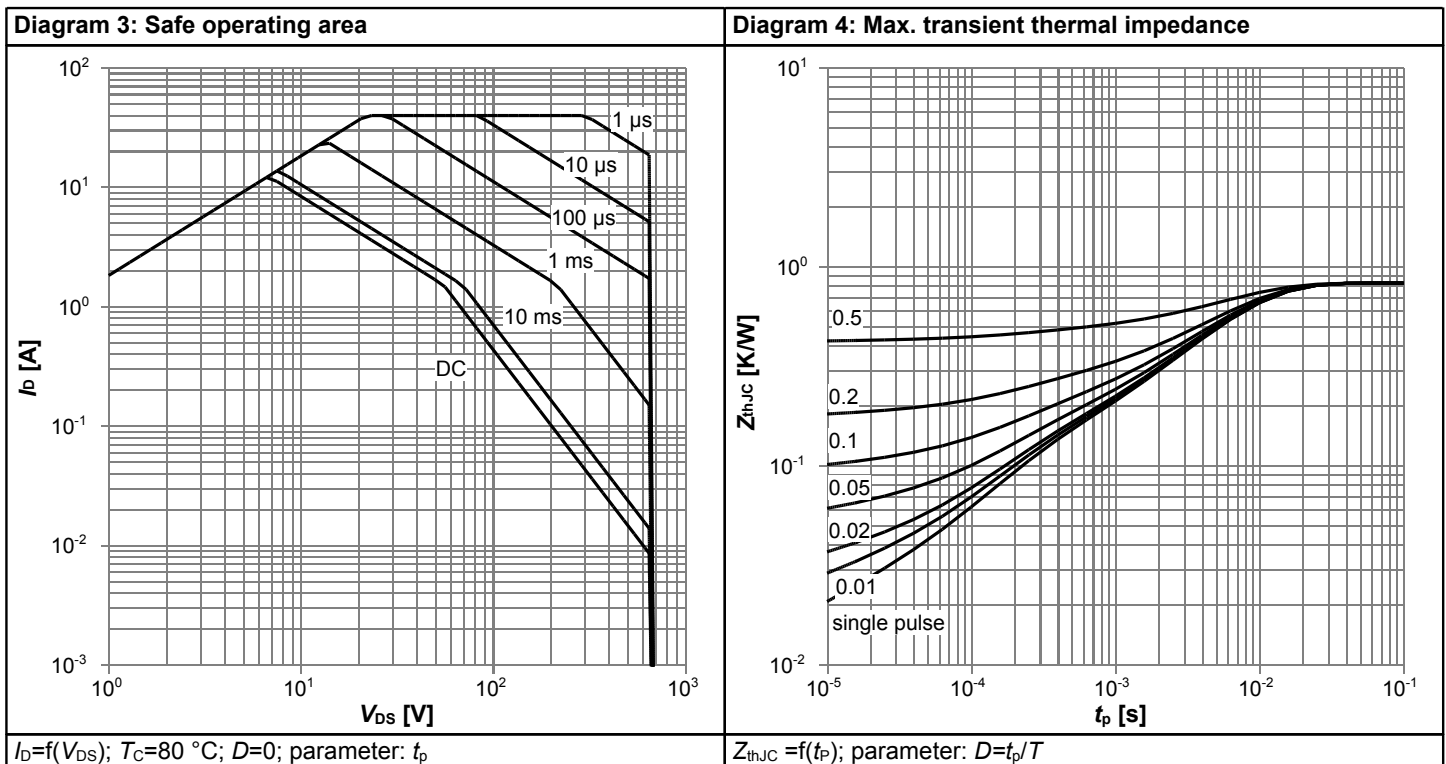
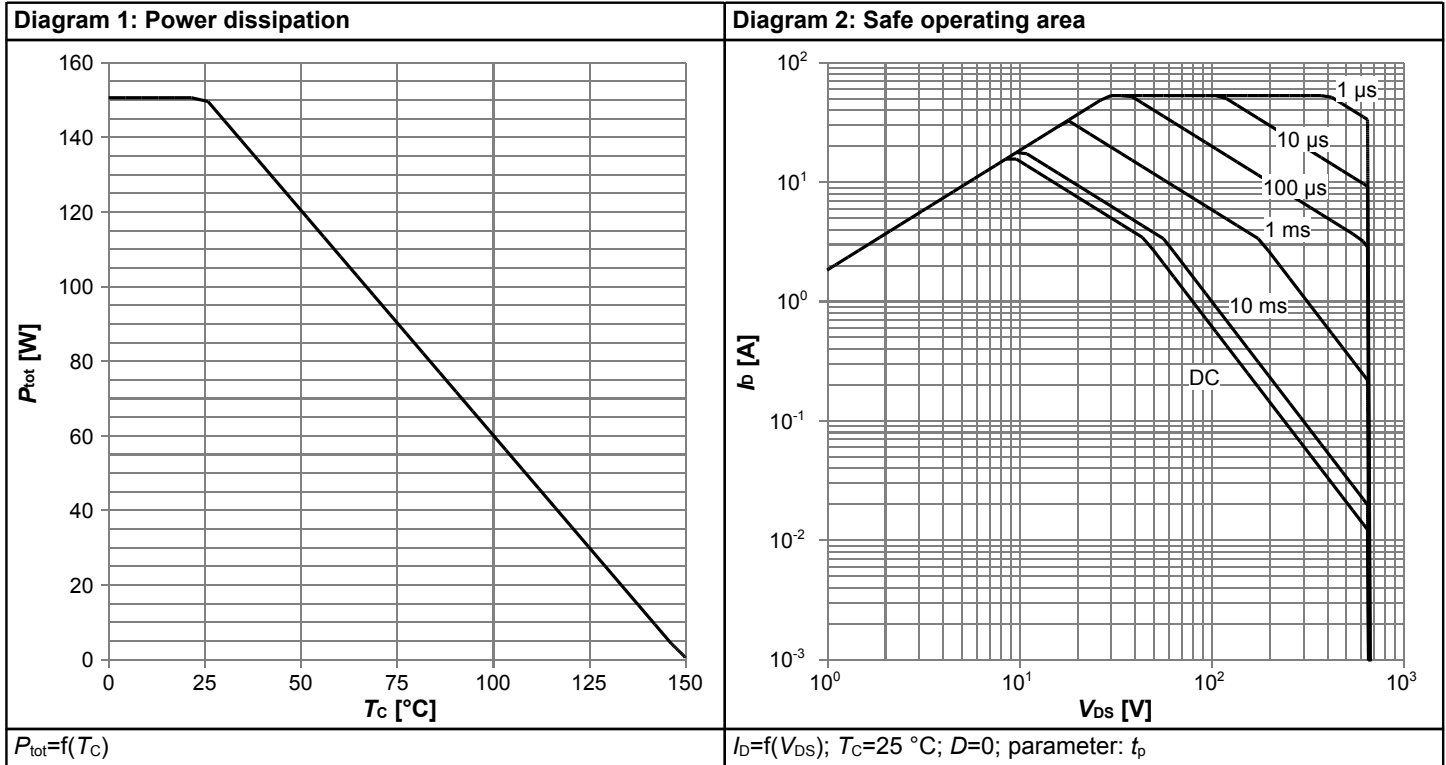
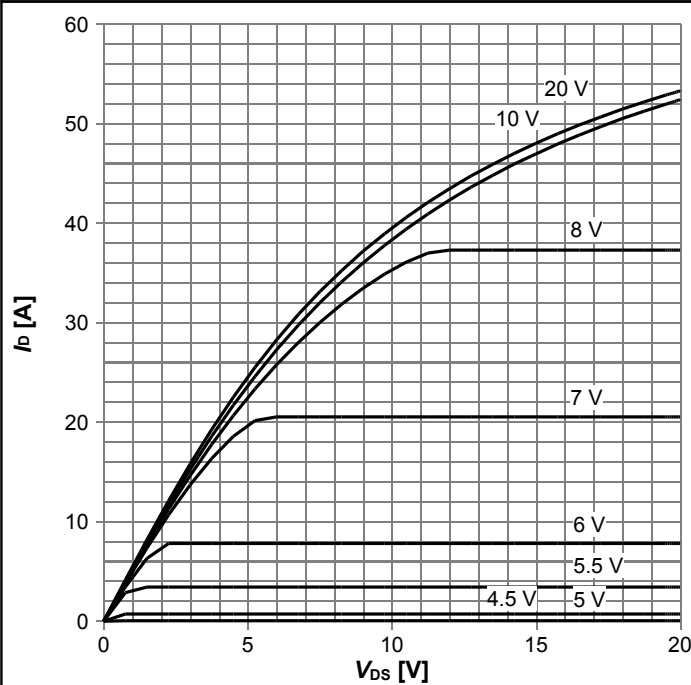


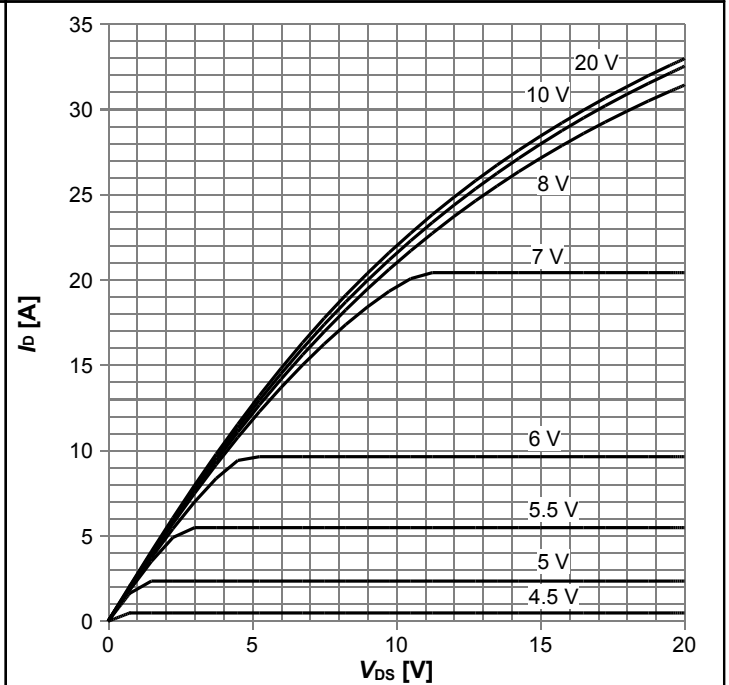


Diagram 5: Typ. output characteristics



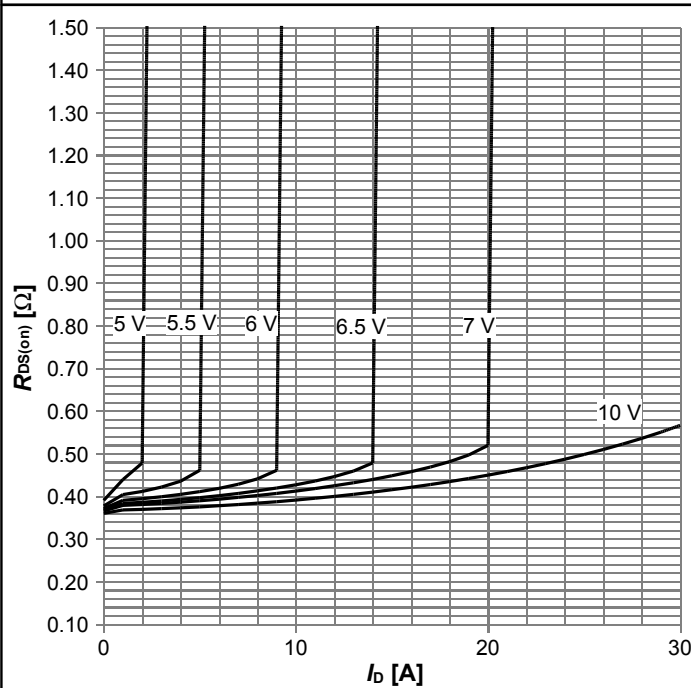
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



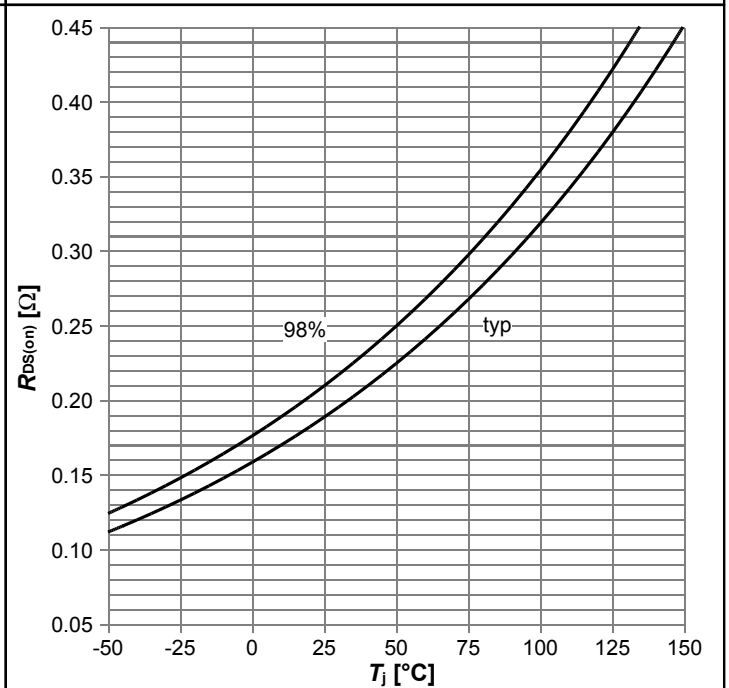
$I_D = f(V_{DS})$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



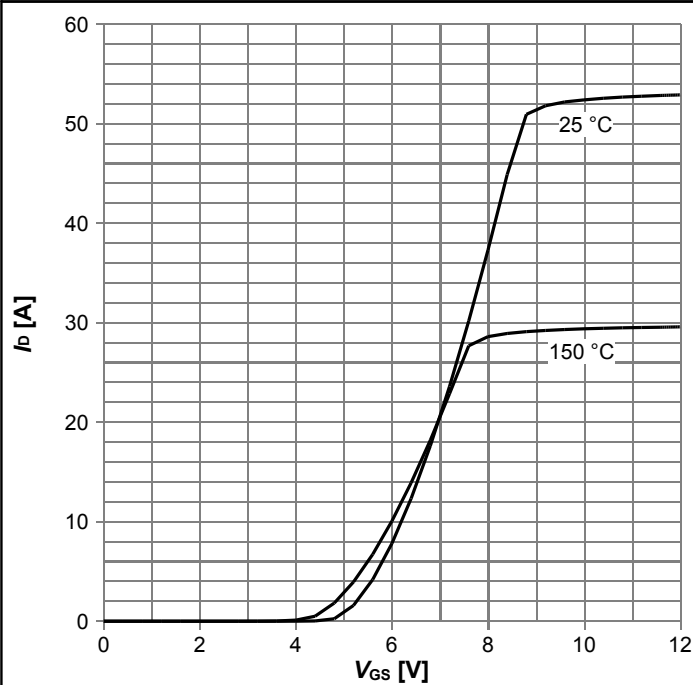
$R_{DS(on)} = f(I_D)$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



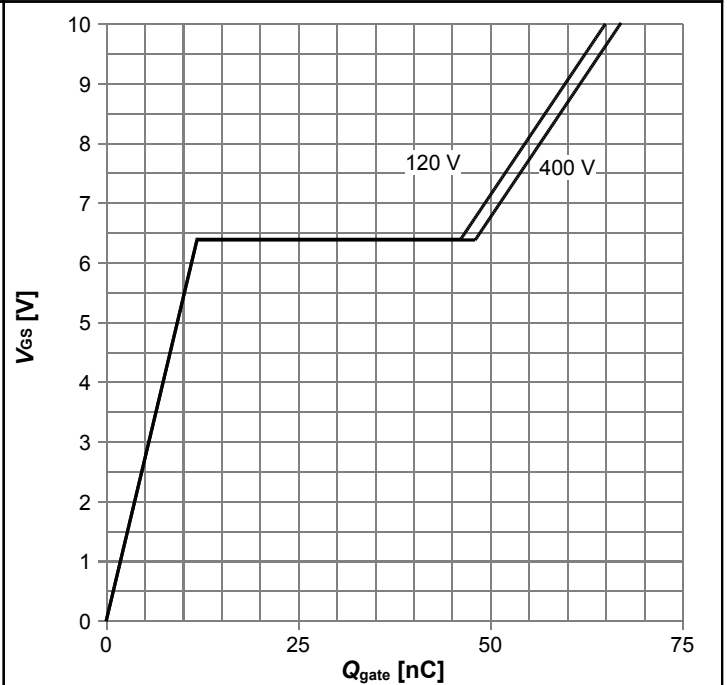
$R_{DS(on)} = f(T_j)$ ;  $I_D = 7.3\text{ A}$ ;  $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



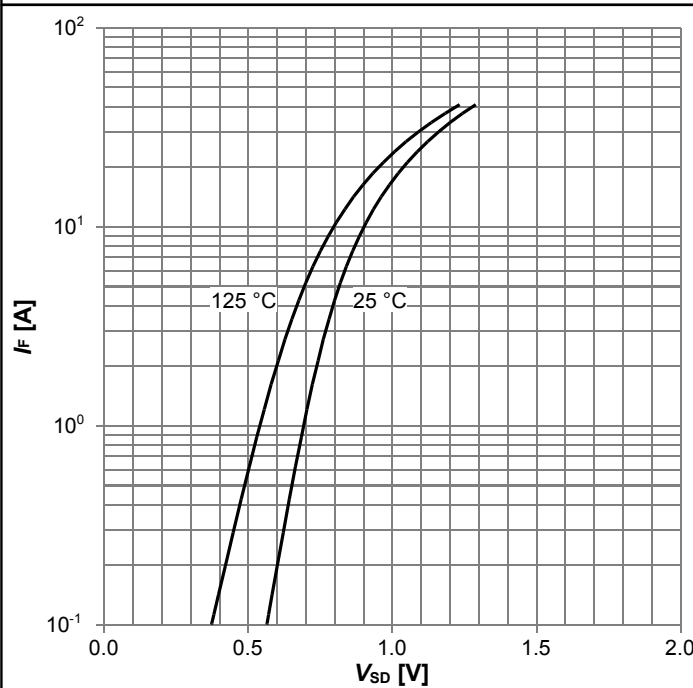
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



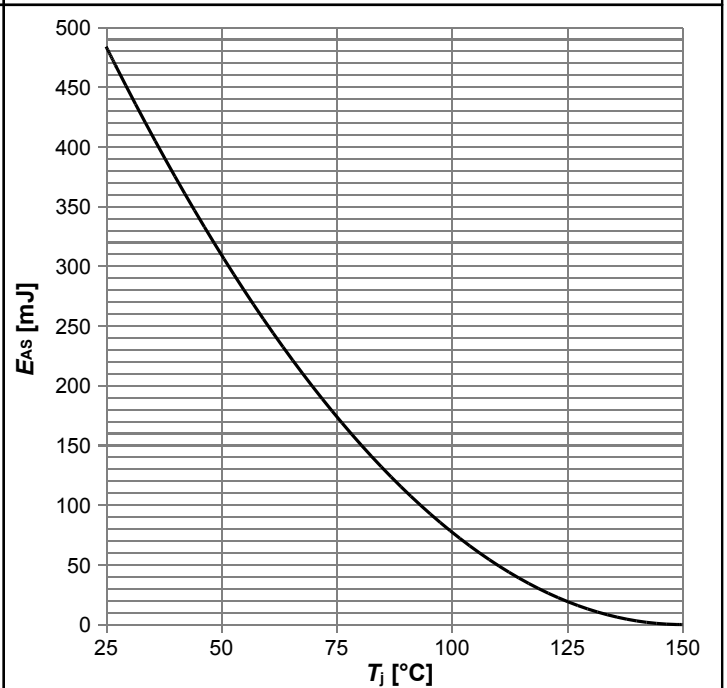
$V_{GS}=f(Q_{gate}); I_D=11 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



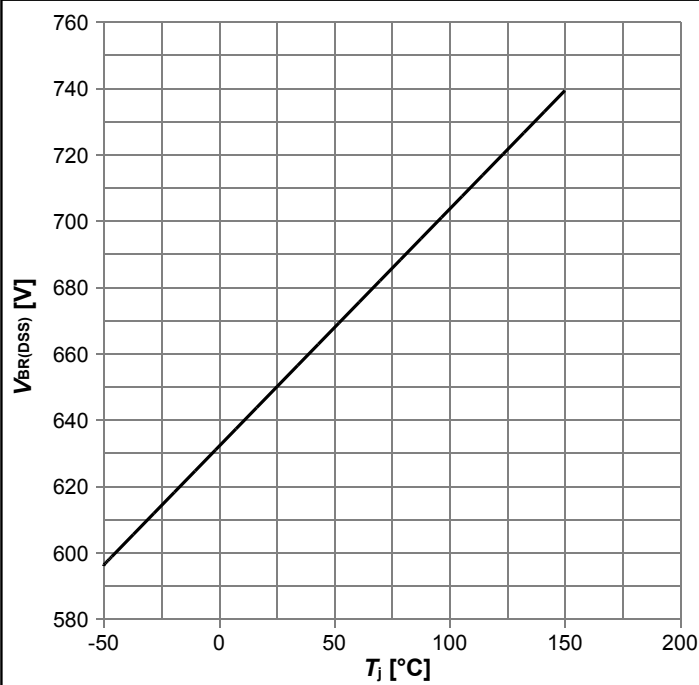
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



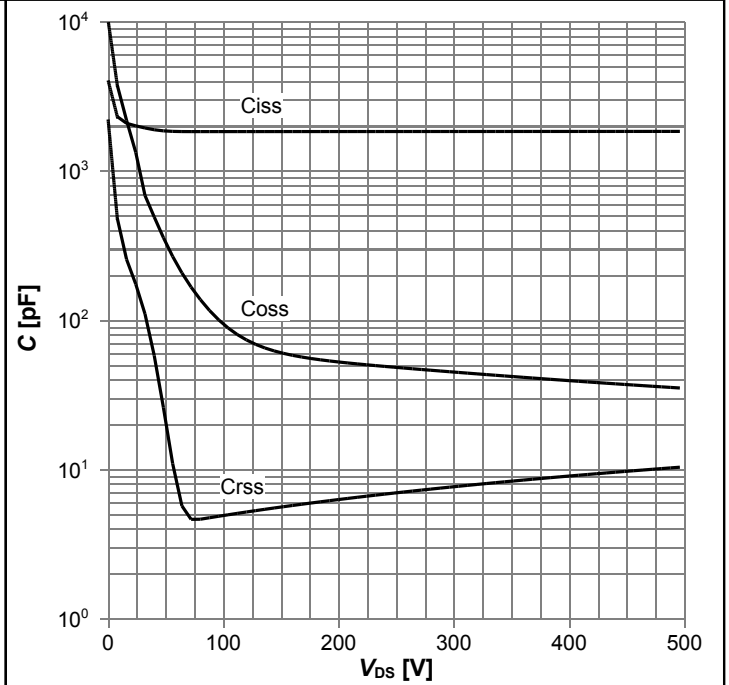
$E_{AS}=f(T_j); I_D=3.3 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



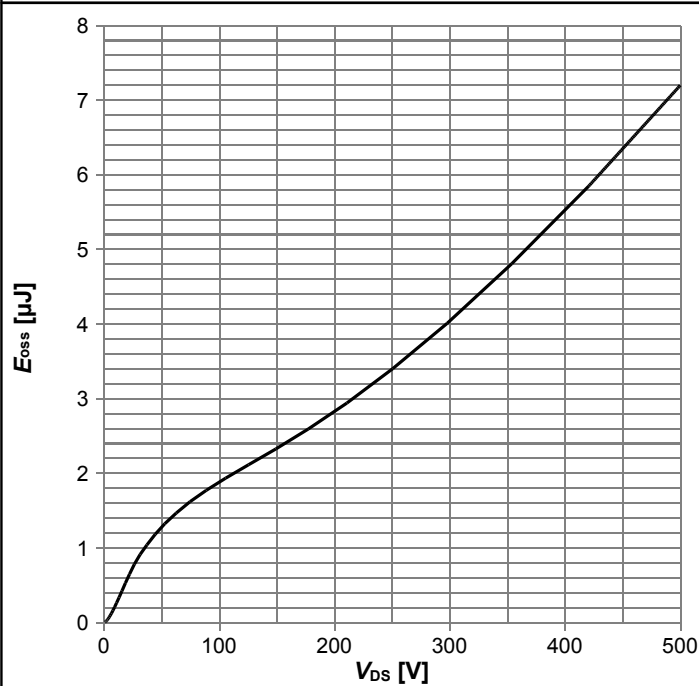
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1\text{MHz}$

Diagram 15: Typ. Coss stored energy



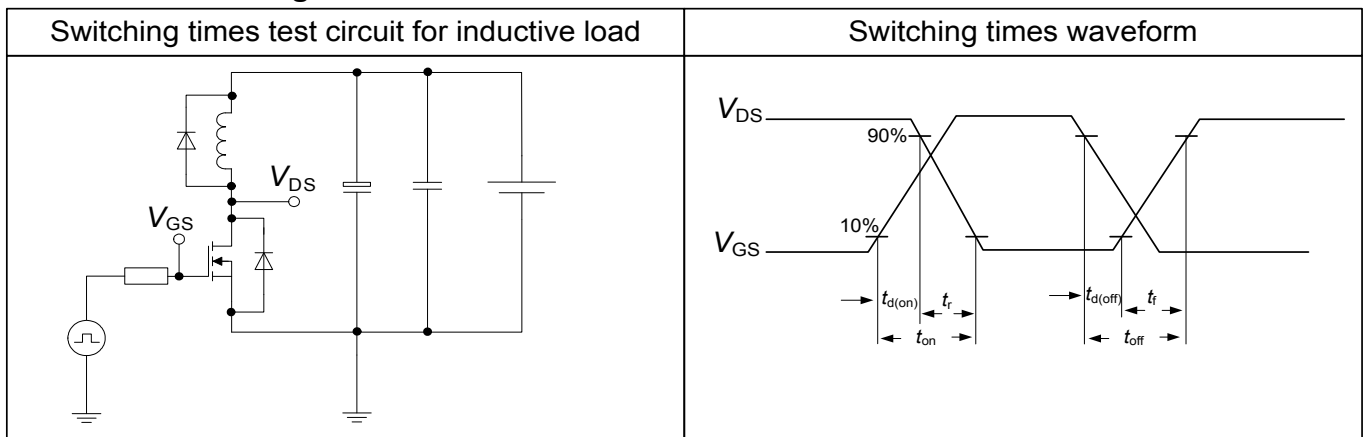
$E_{oss}=f(V_{DS})$

## 6 Test Circuits

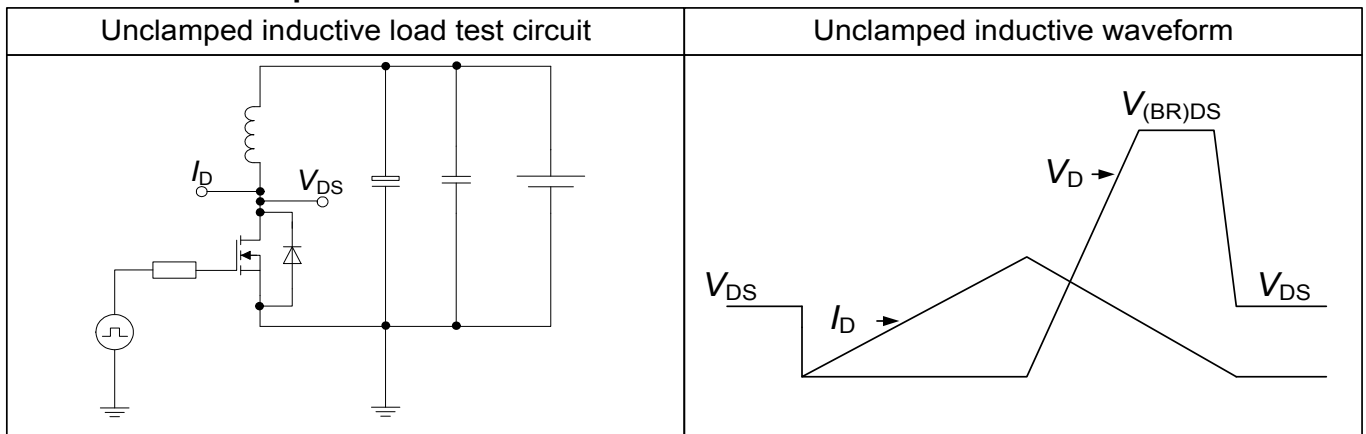
**Table 8 Diode characteristics**



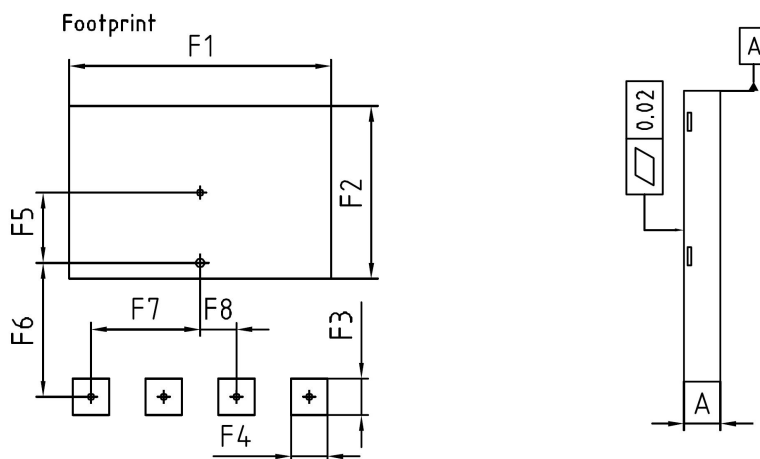
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

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Figure 1 Outline PG-VSON-4, dimensions in mm/inches

## 8 Appendix A

### Table 11 Related Links

- IFX Design Tools: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS Webpage: [www.infineon.com](http://www.infineon.com)

## Revision History

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IPL65R210CFD

**Revision: 2014-03-19, Rev. 2.0**

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Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-03-19	Release of final version

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