

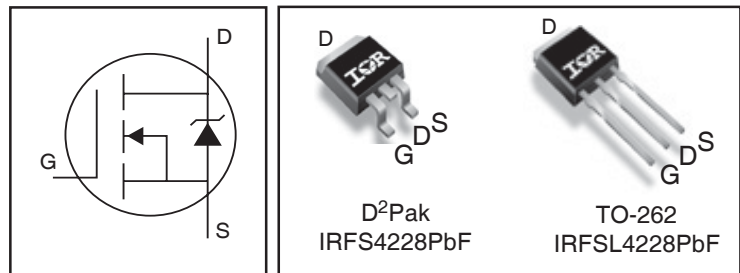
**PDP SWITCH**

**IRFS4228PbF**  
**IRFSL4228PbF**

**Features**

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $E_{PULSE}$  Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $Q_G$  for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Key Parameters		
$V_{DS}$ min	150	V
$V_{DS}$ (Avalanche) typ.	180	V
$R_{DS(ON)}$ typ. @ 10V	12	mΩ
$I_{RP}$ max @ $T_C = 100^\circ\text{C}$	170	A
$T_J$ max	175	°C



G	D	S
Gate	Drain	Source

**Description**

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low  $E_{PULSE}$  rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	±30	V
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	83	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	59	
$I_{DM}$	Pulsed Drain Current ①	330	
$I_{RP}$ @ $T_C = 100^\circ\text{C}$	Repetitive Peak Current ⑤	170	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	330	W
$P_D$ @ $T_C = 100^\circ\text{C}$	Power Dissipation	170	
	Linear Derating Factor	2.2	W/°C
$T_J$	Operating Junction and	-40 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

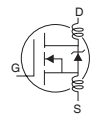
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.45*	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D²Pak ⑥	—	40	

\*  $R_{\theta JC}$  (end of life) for D²Pak and TO-262 = 0.65°C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wearout of the die attach medium.

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	150	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12	15	mΩ	$V_{GS} = 10V, I_D = 33A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-14	—	mV/°C	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	170	—	—	S	$V_{DS} = 25V, I_D = 50A$
$Q_g$	Total Gate Charge	—	71	107	nC	$V_{DD} = 75V, I_D = 50A, V_{GS} = 10V$ ③
$Q_{gd}$	Gate-to-Drain Charge	—	21	—	nC	
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 75V, V_{GS} = 10V$ ③ $I_D = 50A$ $R_G = 2.5\Omega$ See Fig. 22
$t_r$	Rise Time	—	59	—		
$t_{d(off)}$	Turn-Off Delay Time	—	24	—		
$t_f$	Fall Time	—	33	—		
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{DD} = 120V, V_{GS} = 15V, R_G = 5.1\Omega$
$E_{PULSE}$	Energy per Pulse	—	58	—	μJ	$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DS} = 120V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$
		—	110	—		$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DS} = 120V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$
$C_{iss}$	Input Capacitance	—	4530	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	550	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	100	—		$f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance	—	480	—		$V_{GS} = 0V, V_{DS} = 0V\ to\ 120V$
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		

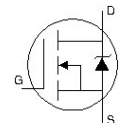


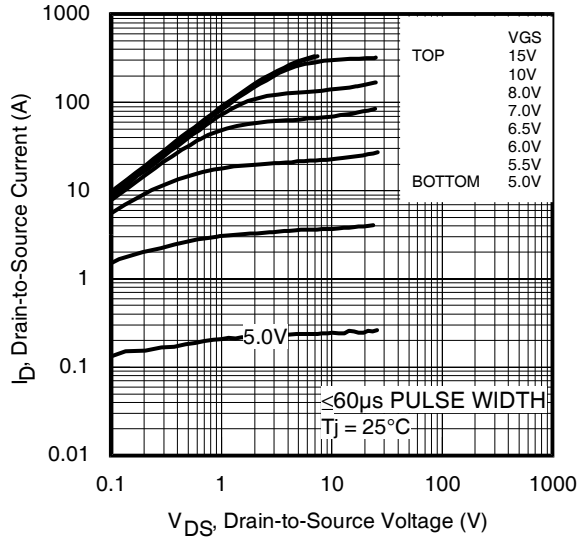
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	120	mJ
$E_{AR}$	Repetitive Avalanche Energy ①	—	33	mJ
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	180	—	V
$I_{AS}$	Avalanche Current ②	—	50	A

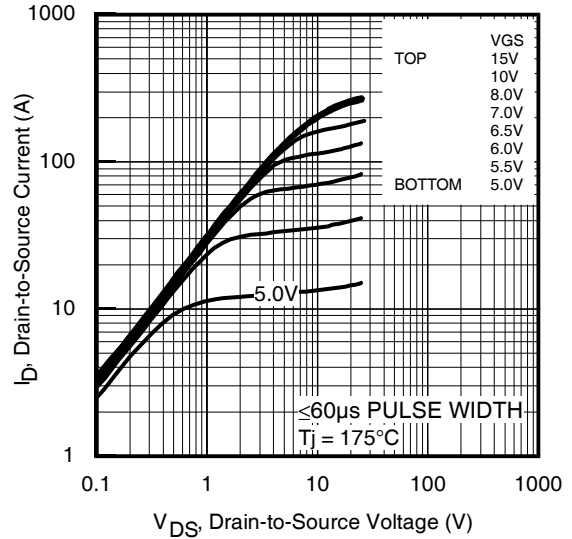
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	83	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	330		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	76	110	ns	$T_J = 25^\circ\text{C}, I_F = 50A, V_{DD} = 50V$
$Q_{rr}$	Reverse Recovery Charge	—	230	350	nC	$di/dt = 100A/\mu s$ ③

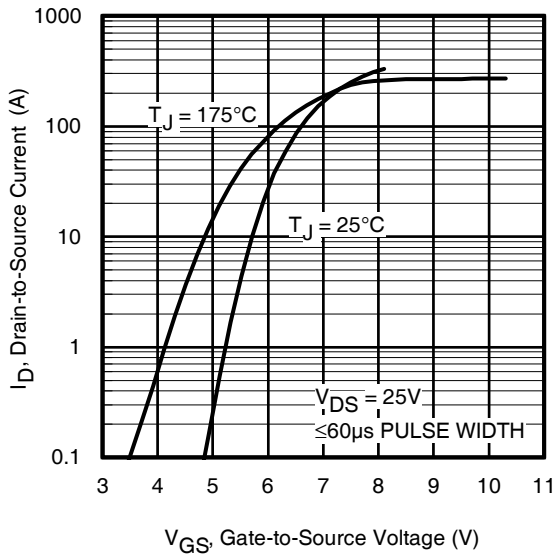




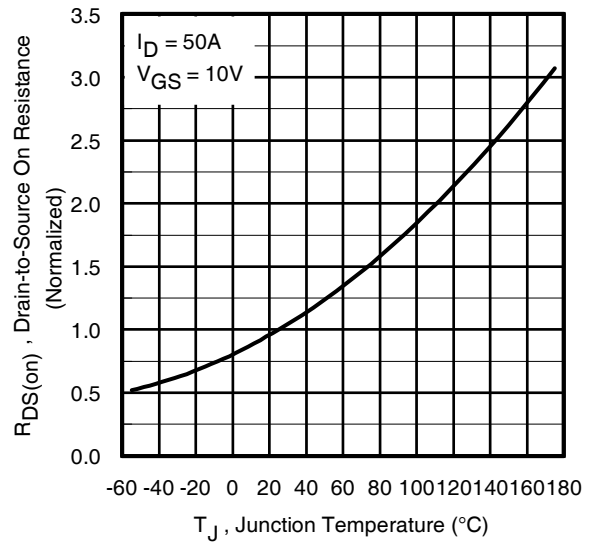
**Fig 1.** Typical Output Characteristics



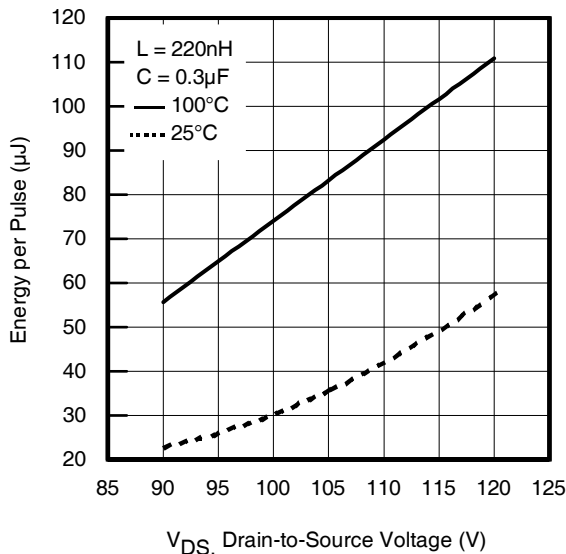
**Fig 2.** Typical Output Characteristics



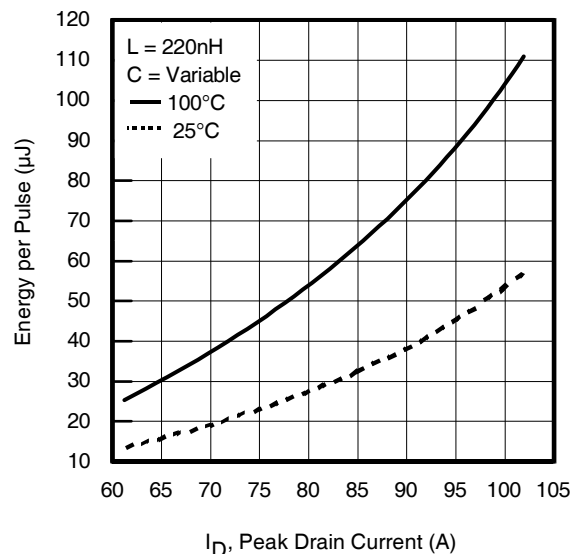
**Fig 3.** Typical Transfer Characteristics



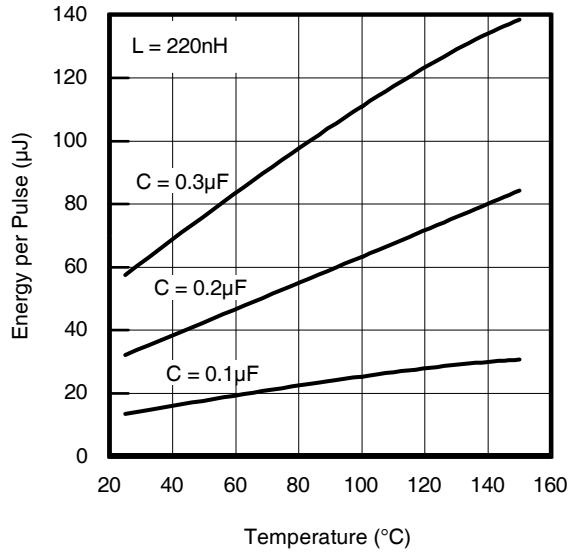
**Fig 4.** Normalized On-Resistance vs. Temperature



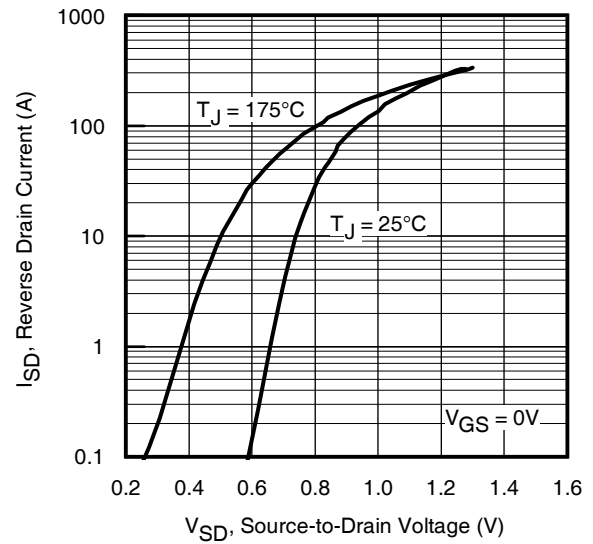
**Fig 5.** Typical  $E_{PULSE}$  vs. Drain-to-Source Voltage



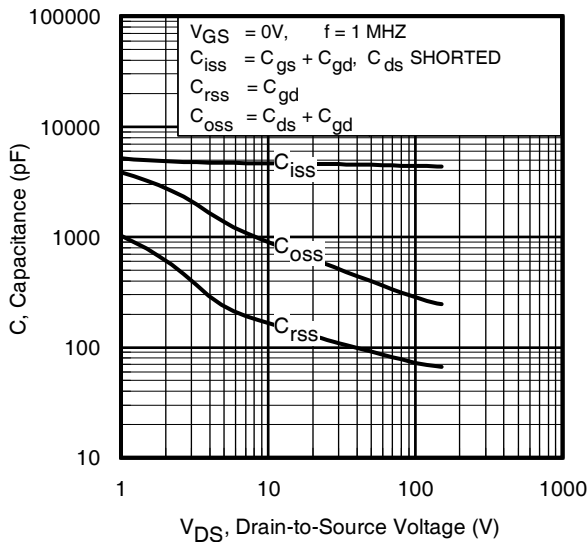
**Fig 6.** Typical  $E_{PULSE}$  vs. Drain Current



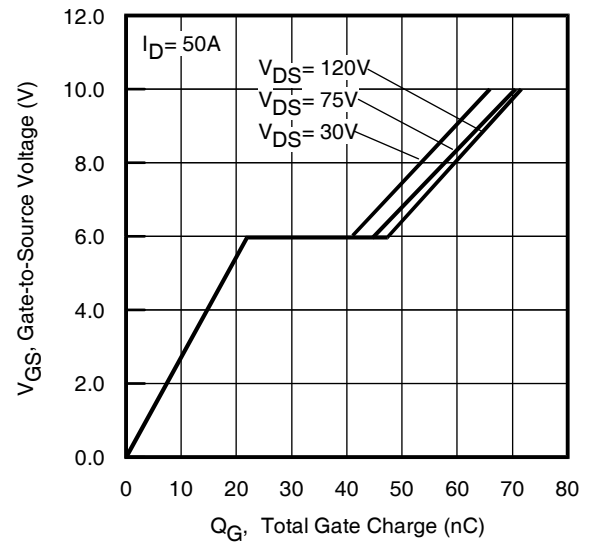
**Fig 7.** Typical  $E_{PULSE}$  vs. Temperature



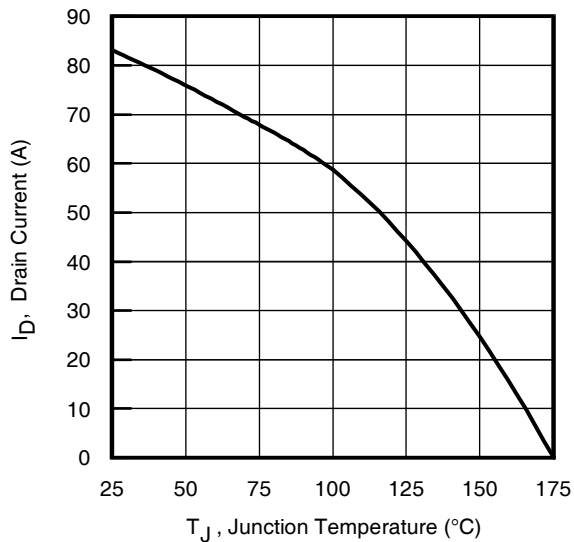
**Fig 8.** Typical Source-Drain Diode Forward Voltage



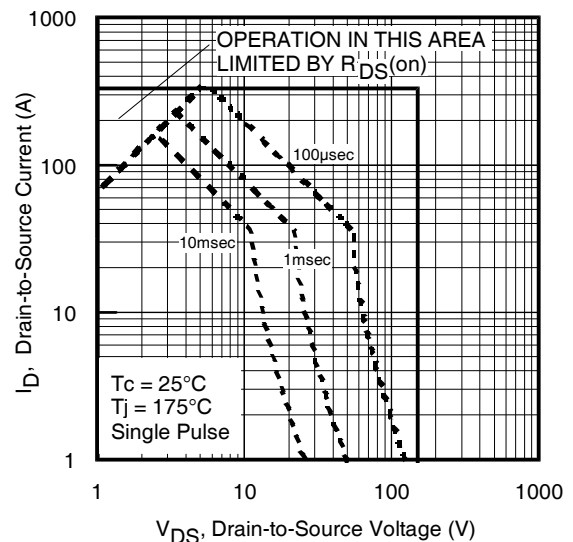
**Fig 9.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 10.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig 11.** Maximum Drain Current vs. Case Temperature



**Fig 12.** Maximum Safe Operating Area

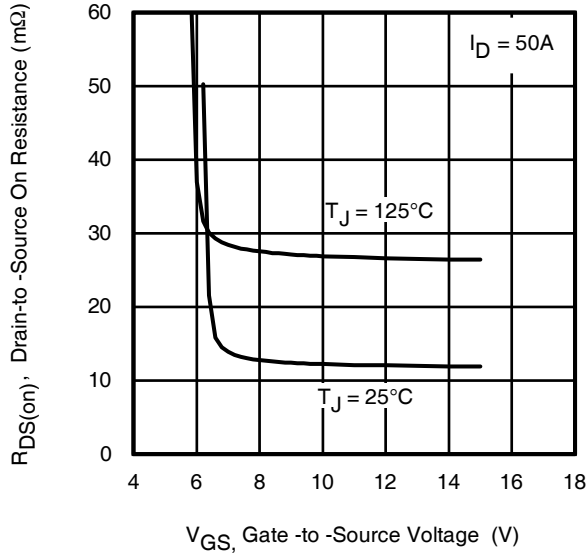


Fig 13. On-Resistance vs. Gate Voltage

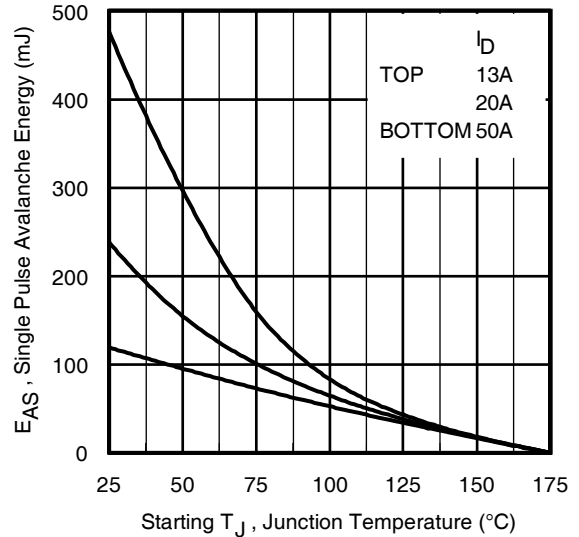


Fig 14. Maximum Avalanche Energy vs. Temperature

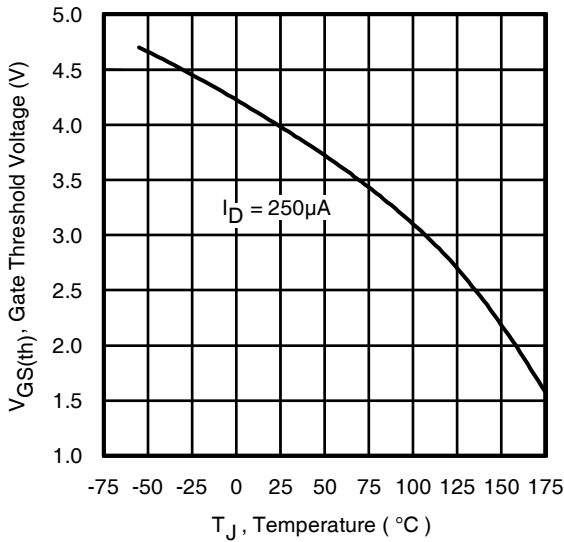


Fig 15. Threshold Voltage vs. Temperature

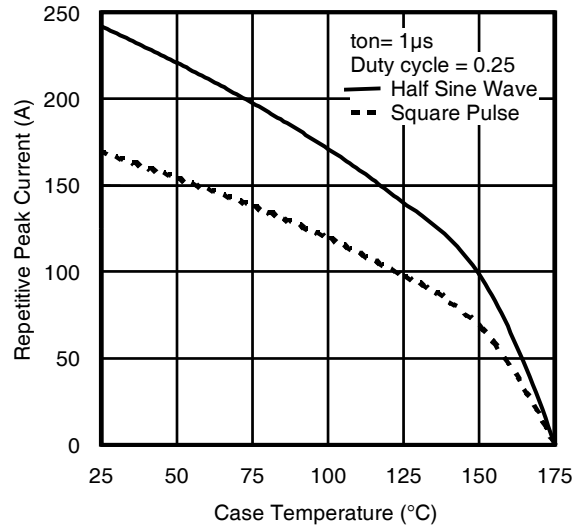


Fig 16. Typical Repetitive peak Current vs. Case temperature

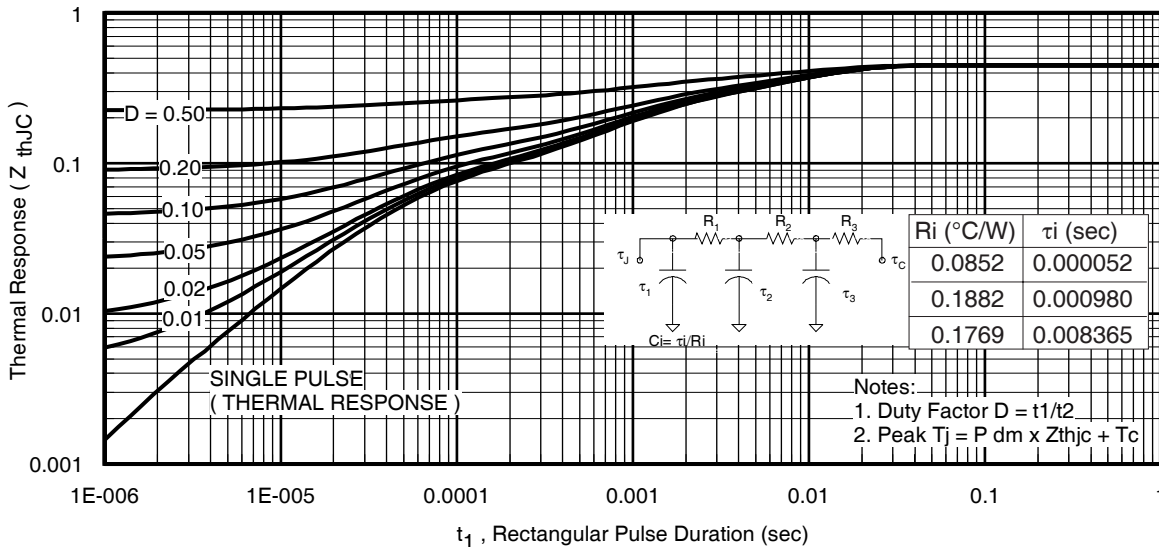
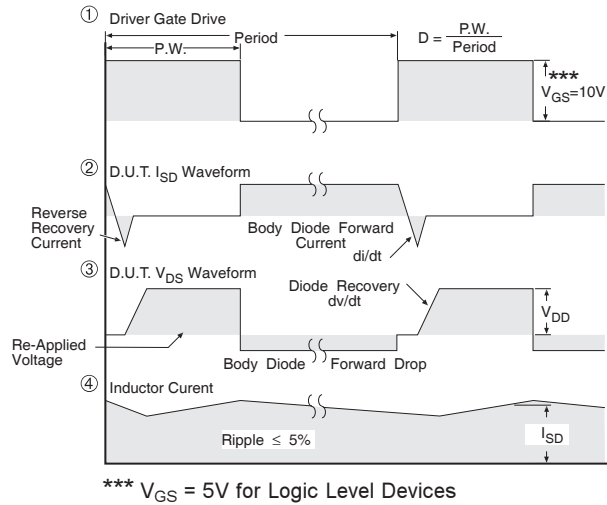
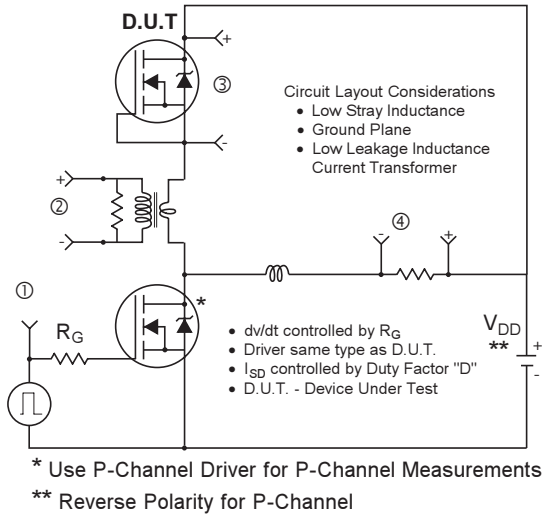
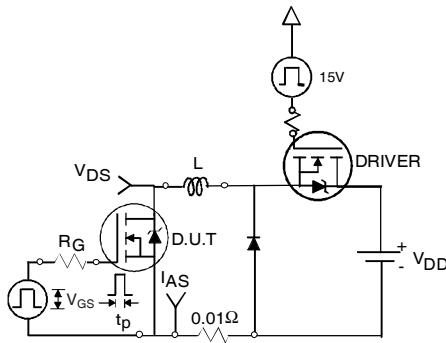


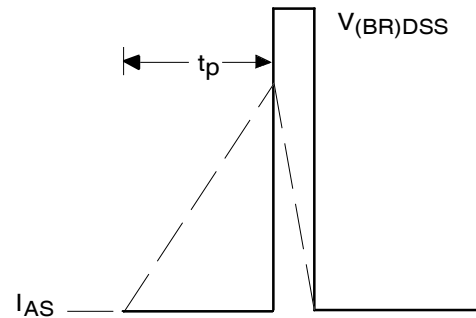
Fig 17. Maximum Effective Transient Thermal Impedance, Junction-to-Case



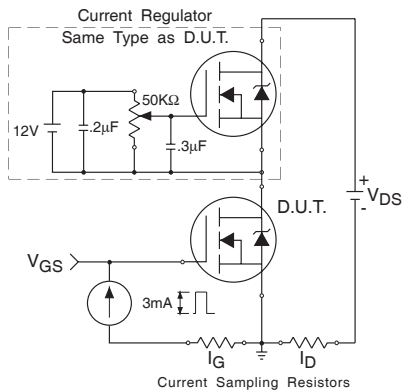
**Fig 18.** Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs



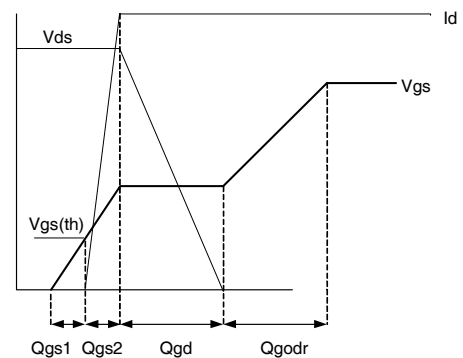
**Fig 19a.** Unclamped Inductive Test Circuit



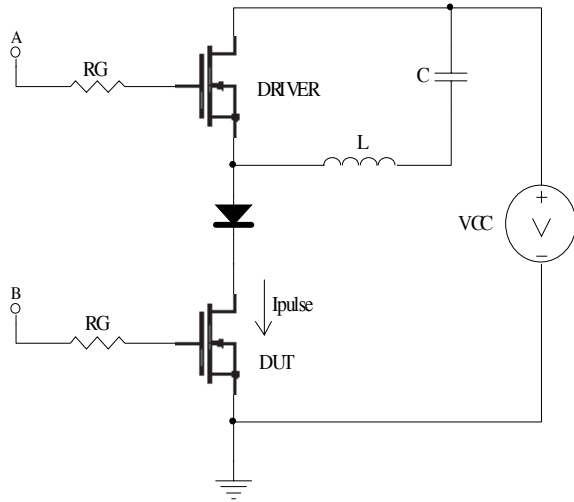
**Fig 19b.** Unclamped Inductive Waveforms



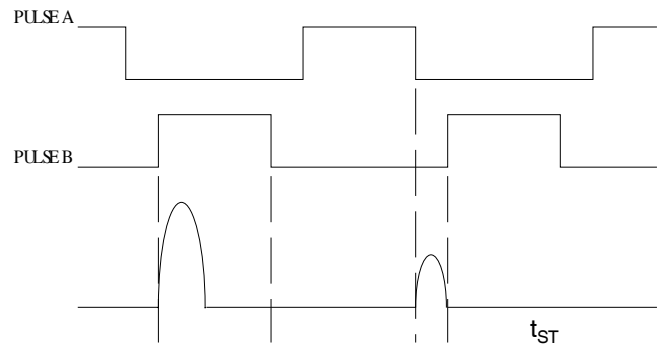
**Fig 20a.** Gate Charge Test Circuit



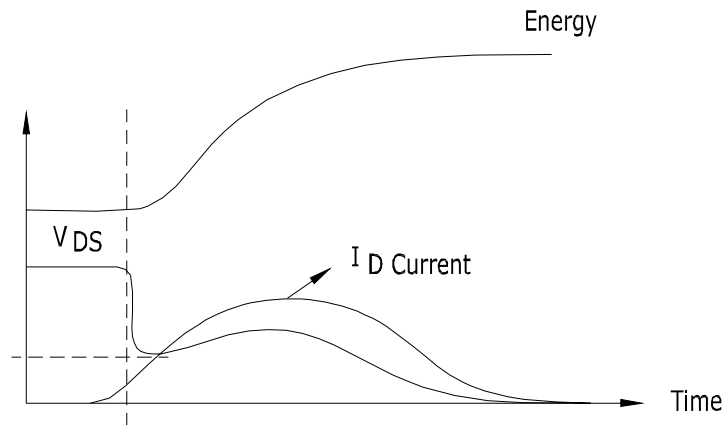
**Fig 20b.** Gate Charge Waveform



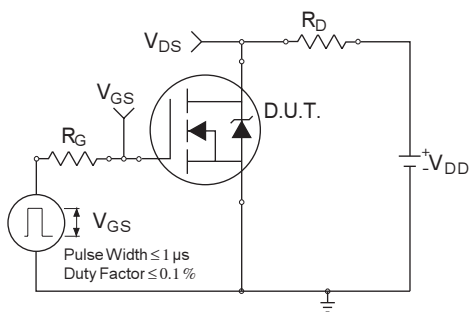
**Fig 21a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit



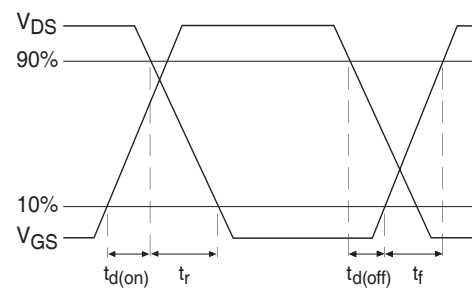
**Fig 21b.**  $t_{st}$  Test Waveforms



**Fig 21c.**  $E_{PULSE}$  Test Waveforms



**Fig 22a.** Switching Time Test Circuit



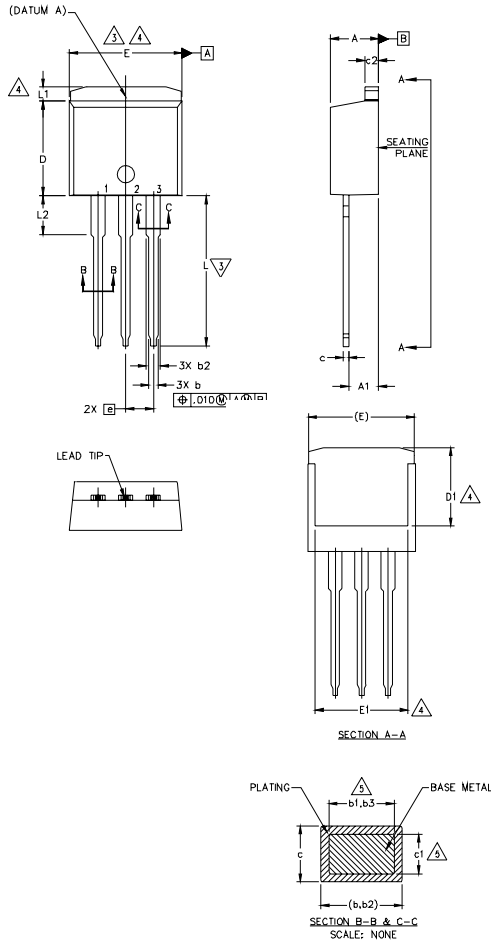
**Fig 22b.** Switching Time Waveforms





## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54	BSC	.100	BSC	
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

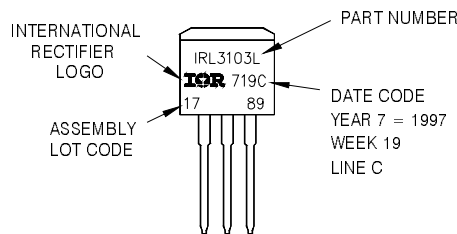
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

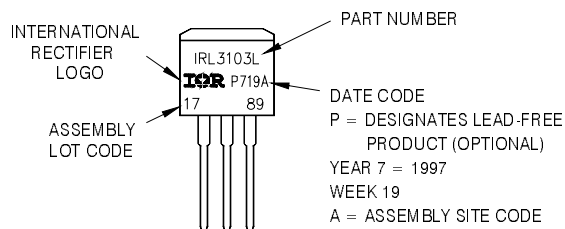
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE 'C'

Note: "P" in assembly line position indicates "Lead - Free"



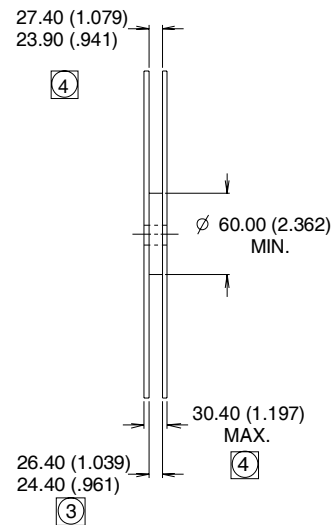
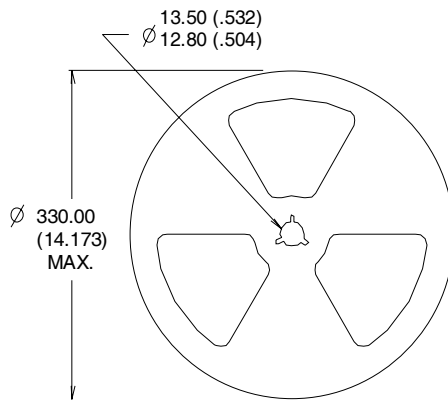
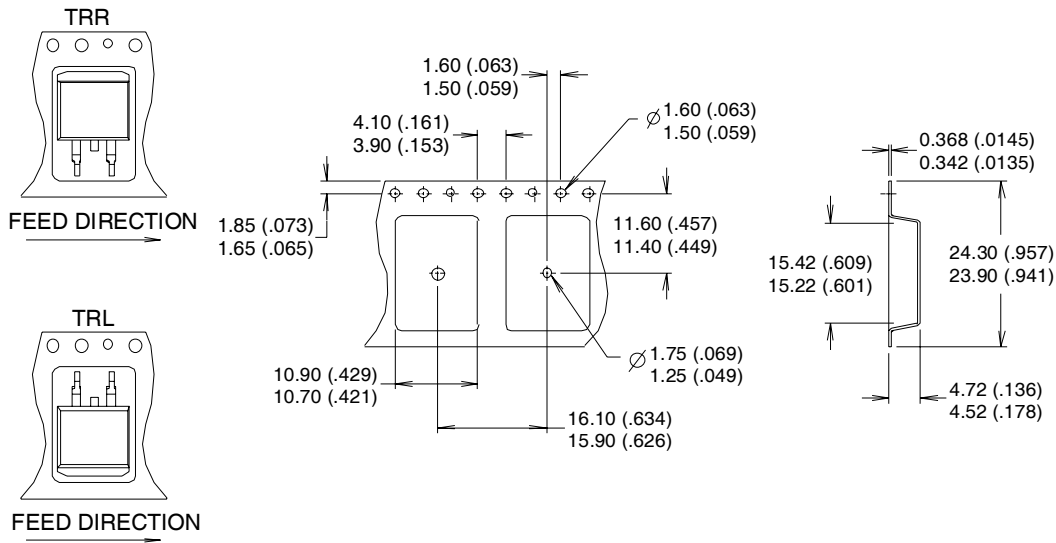
OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

# IRFS/SL4228PbF

## D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information



**NOTES :**

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.096\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 50\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ Half sine wave with duty cycle = 0.25,  $t_{on} = 1\mu\text{sec}$ .
- ⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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