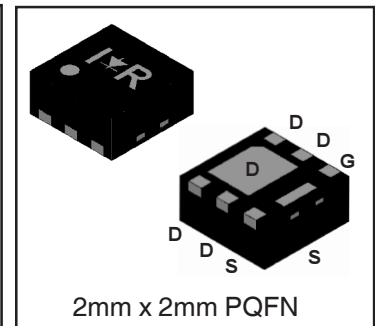
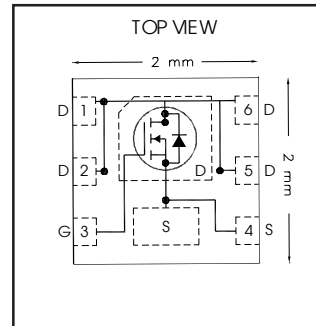


# IRLHS6342PbF

HEXFET® Power MOSFET

$V_{DS}$	<b>30</b>	<b>V</b>
$V_{GS}$	<b>±12</b>	<b>V</b>
$R_{DS(on) max}$ (@ $V_{GS} = 4.5V$ )	<b>15.5</b>	<b>mΩ</b>
$Q_g$ (typical)	<b>11</b>	<b>nC</b>
$I_D$ (@ $T_{C(Bottom)} = 25°C$ )	<b>12</b> Ⓣ	<b>A</b>



## Applications

- Charge and discharge switch for battery application
- System/Load Switch

## Features and Benefits

### Features

Low $R_{DS(on)}$ ( $\leq 15.5m\Omega$ )
Low Thermal Resistance to PCB ( $\leq 13°C/W$ )
Low Profile ( $\leq 1.0$ mm)
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Consumer Qualification

results in

### Resulting Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLHS6342TRPBF	PQFN 2mm x 2mm	Tape and Reel	4000	
IRLHS6342TR2PBF	PQFN 2mm x 2mm	Tape and Reel	400	

## Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±12	
$I_D @ T_A = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	8.7	A
$I_D @ T_A = 70°C$	Continuous Drain Current, $V_{GS} @ 10V$	6.9	
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	19Ⓣ	
$I_D @ T_{C(Bottom)} = 70°C$	Continuous Drain Current, $V_{GS} @ 10V$	15Ⓣ	
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$ (Wirebond Limited)	12Ⓣ	
$I_{DM}$	Pulsed Drain Current ①	76	
$P_D @ T_A = 25°C$	Power Dissipation ⑤	2.1	W
$P_D @ T_A = 70°C$	Power Dissipation ⑤	1.3	
	Linear Derating Factor ⑤	0.02	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑤ are on page 2

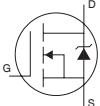
## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	22	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12.0	15.5	mΩ	$V_{GS} = 4.5V, I_D = 8.5A$ ③
		—	15.0	19.5		$V_{GS} = 2.5V, I_D = 8.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	0.5	—	1.1	V	$V_{DS} = V_{GS}, I_D = 10\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-4.2	—	mV/°C	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -12V$
$g_{fs}$	Forward Transconductance	39	—	—	S	$V_{DS} = 10V, I_D = 8.5A$
$Q_g$	Total Gate Charge	—	11	—	nC	$V_{DS} = 15V$
$Q_{gs}$	Gate-to-Source Charge	—	0.5	—		$V_{GS} = 4.5V$
$Q_{gd}$	Gate-to-Drain Charge	—	4.6	—		$I_D = 8.5A$ (See Fig. 6 & 17)
$R_G$	Gate Resistance	—	2.1	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	4.9	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$
$t_r$	Rise Time	—	13	—		$I_D = 8.5A$
$t_{d(off)}$	Turn-Off Delay Time	—	19	—		$R_G = 1.8\Omega$
$t_f$	Fall Time	—	13	—		See Fig. 18
$C_{iss}$	Input Capacitance	—	1019	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	97	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	70	—		$f = 1.0\text{MHz}$

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	14	mJ
$I_{AR}$	Avalanche Current ①	—	8.5	A

## Diode Characteristics

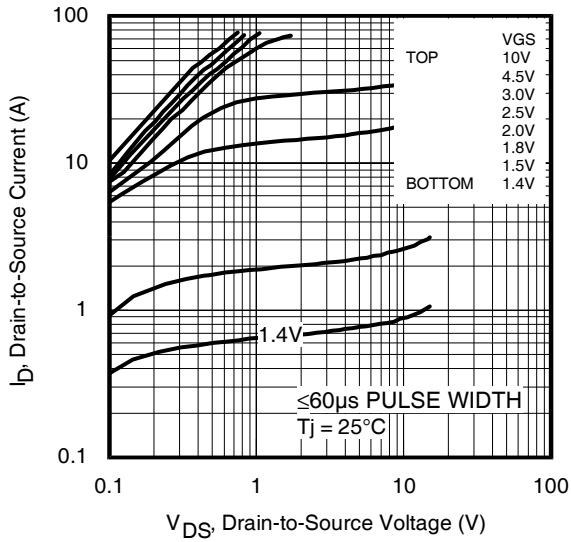
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	12 <sup>⑦</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	76		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 8.5A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	11	17	ns	$T_J = 25^\circ\text{C}, I_F = 8.5A, V_{DD} = 15V$
$Q_{rr}$	Reverse Recovery Charge	—	13	20	nC	$di/dt = 300\text{A}/\mu\text{s}$ ③
$t_{on}$	Forward Turn-On Time	Time is dominated by parasitic Inductance				

## Thermal Resistance

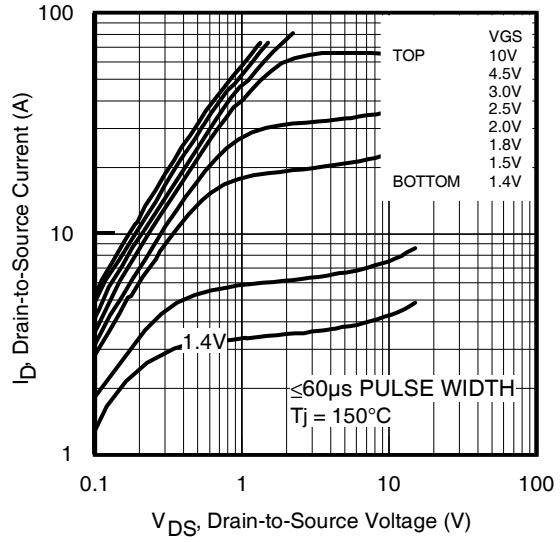
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑤	—	13	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ⑤	—	90	
$R_{\theta JA}$	Junction-to-Ambient ④	—	60	
$R_{\theta JA}$	Junction-to-Ambient (<10s) ④	—	42	

### Notes:

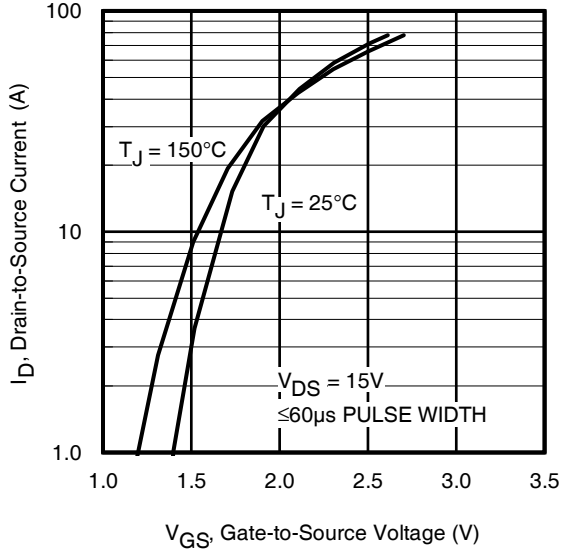
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.39\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 8.5A$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Package is limited to 12A by die-source to lead-frame bonding technology



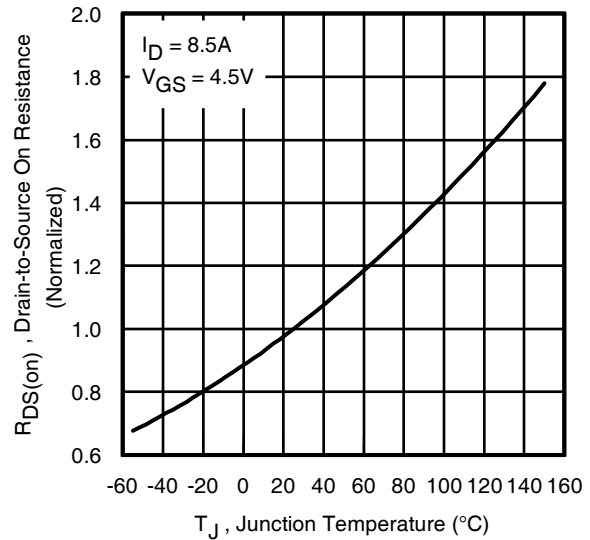
**Fig 1.** Typical Output Characteristics



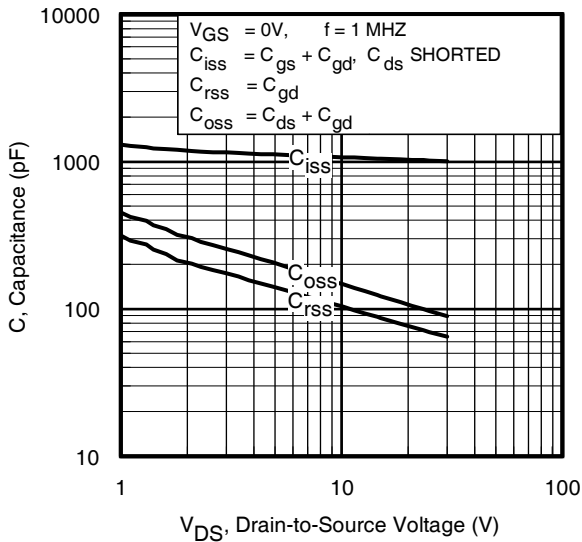
**Fig 2.** Typical Output Characteristics



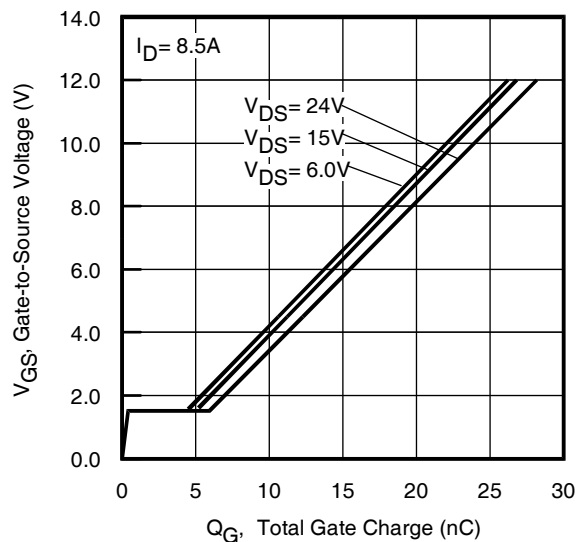
**Fig 3.** Typical Transfer Characteristics



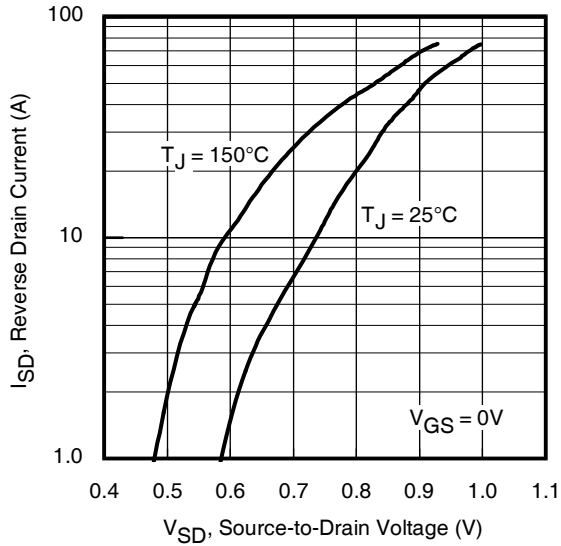
**Fig 4.** Normalized On-Resistance vs. Temperature



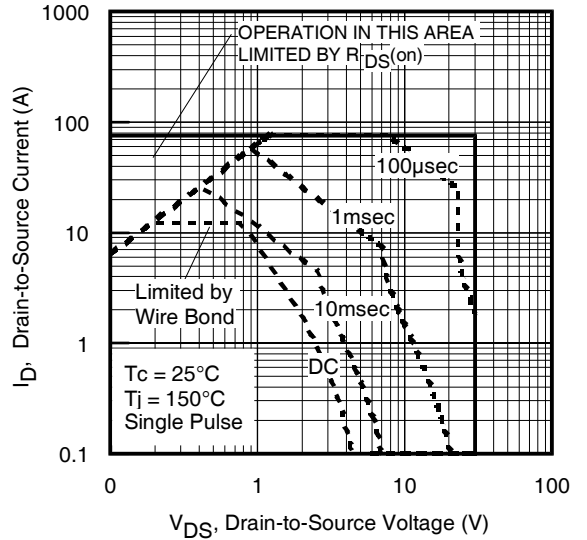
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage  
[www.irf.com](http://www.irf.com)



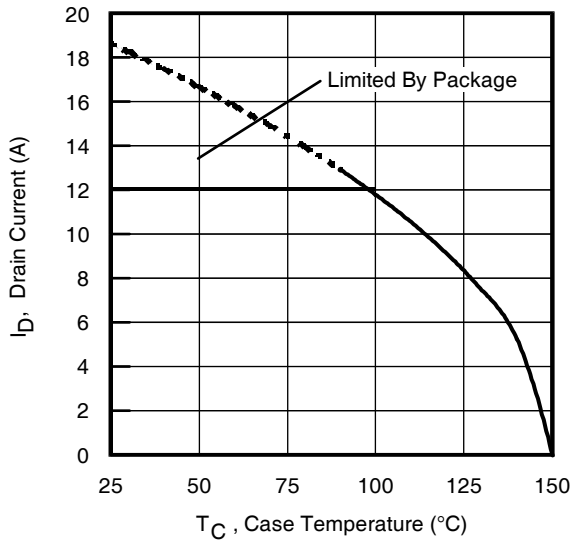
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



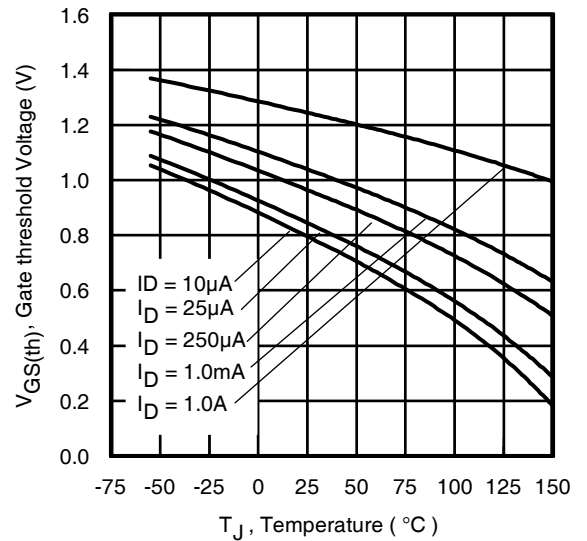
**Fig 7.** Typical Source-Drain Diode Forward Voltage



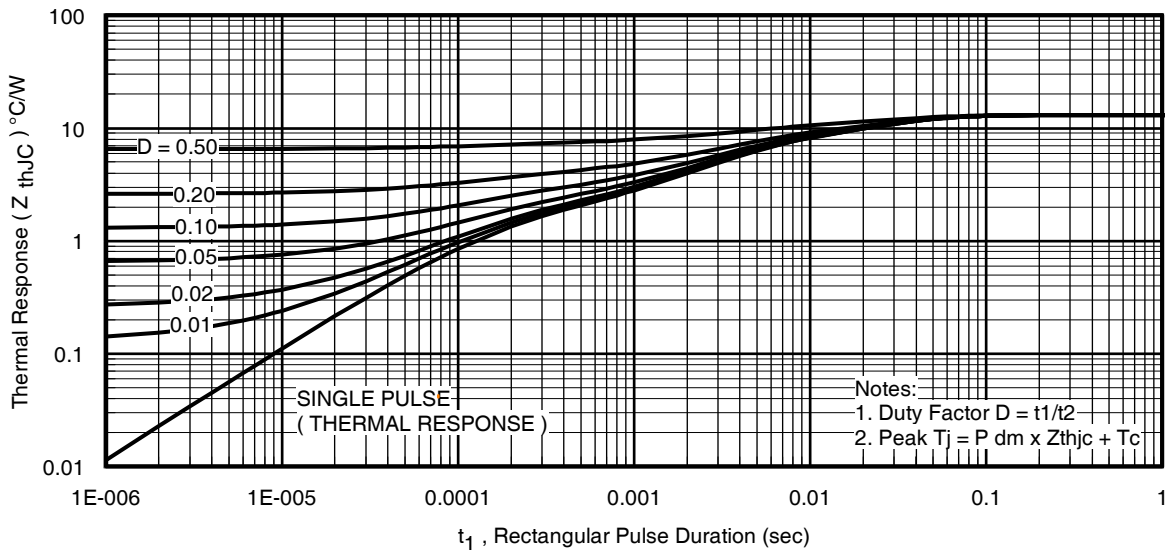
**Fig 8.** Maximum Safe Operating Area



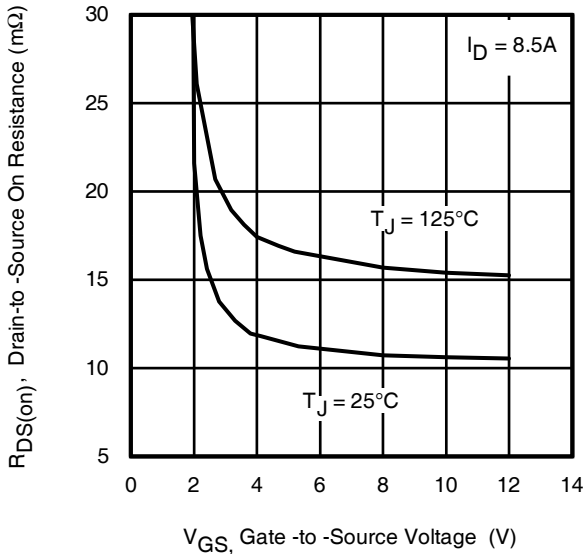
**Fig 9.** Maximum Drain Current vs. Case (Bottom) Temperature



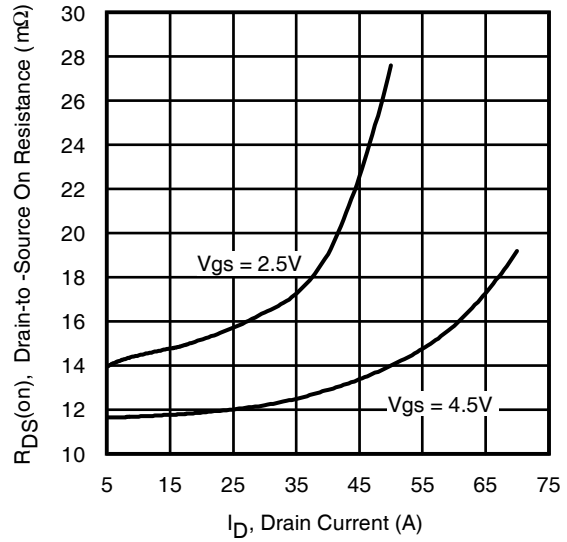
**Fig 10.** Threshold Voltage vs. Temperature



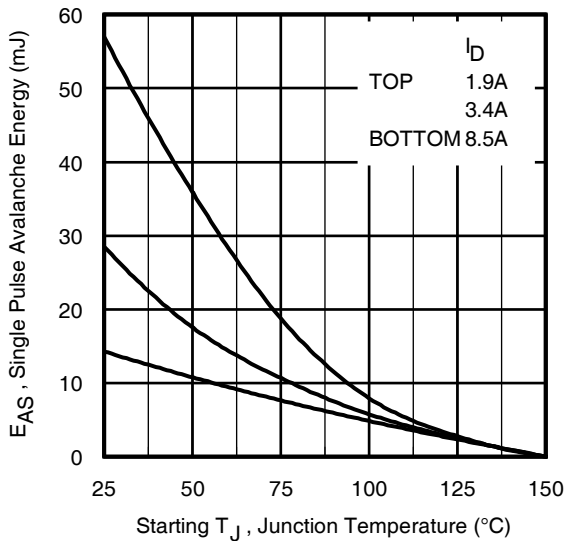
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)



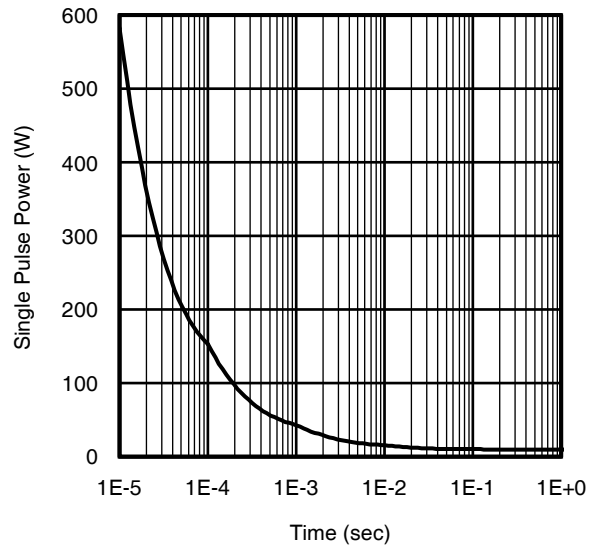
**Fig 12.** On-Resistance vs. Gate Voltage



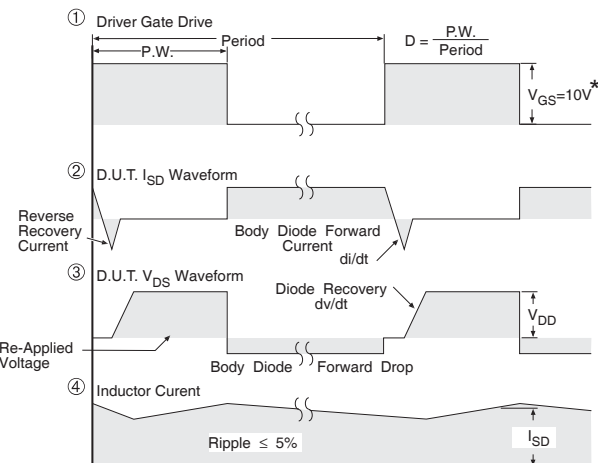
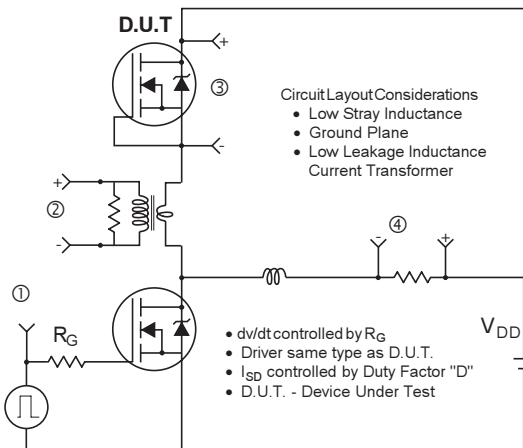
**Fig 13.** Typical On-Resistance vs. Drain Current



**Fig 14.** Maximum Avalanche Energy vs. Drain Current

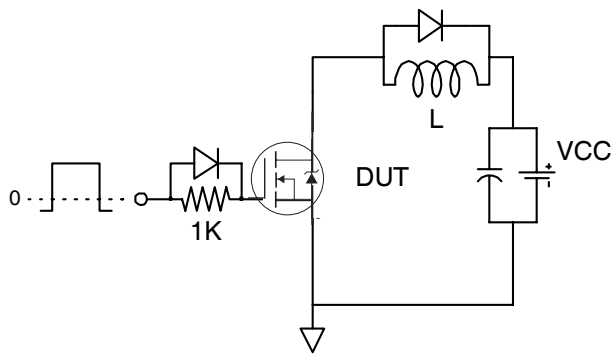


**Fig 15.** Typical Power vs. Time

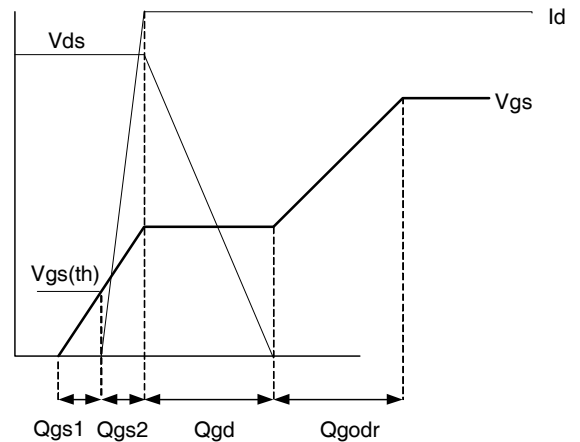


\*  $V_{GS} = 5V$  for Logic Level Devices

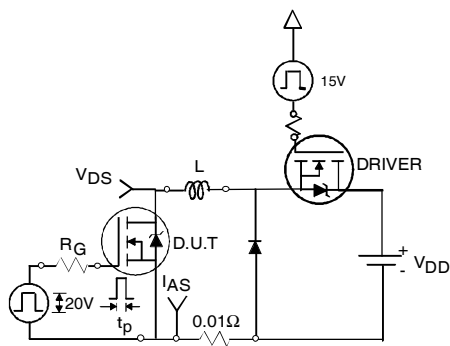
**Fig 16.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel  
HEXFET<sup>®</sup> Power MOSFETs



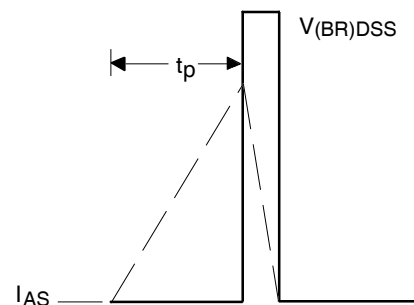
**Fig 17a.** Gate Charge Test Circuit



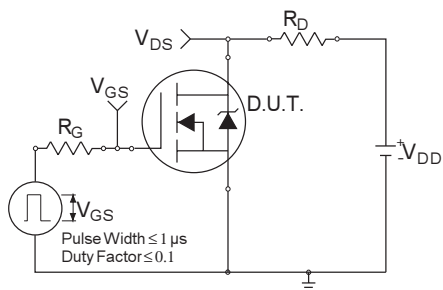
**Fig 17b.** Gate Charge Waveform



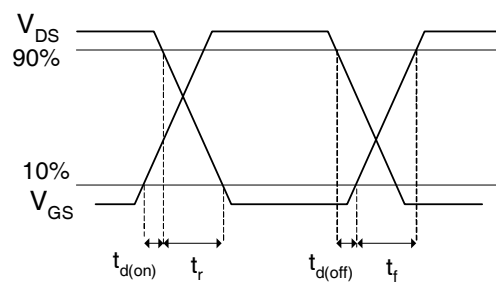
**Fig 18a.** Unclamped Inductive Test Circuit



**Fig 18b.** Unclamped Inductive Waveforms

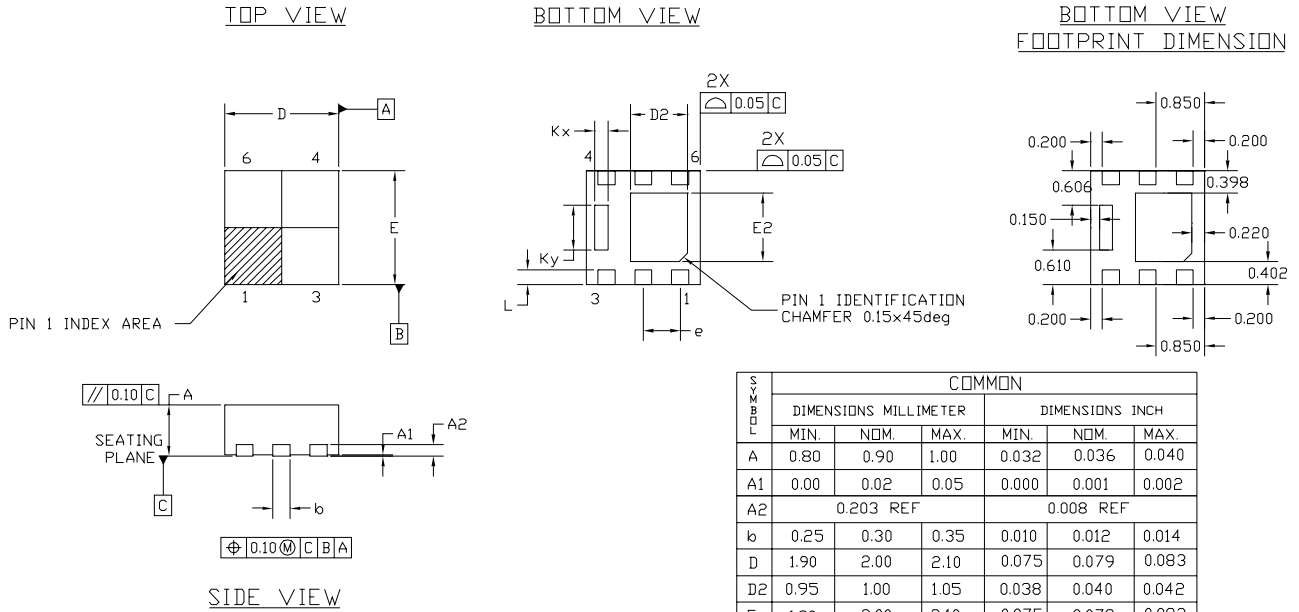


**Fig 19a.** Switching Time Test Circuit



**Fig 19b.** Switching Time Waveforms

## PQFN 2x2 Outline Package Details

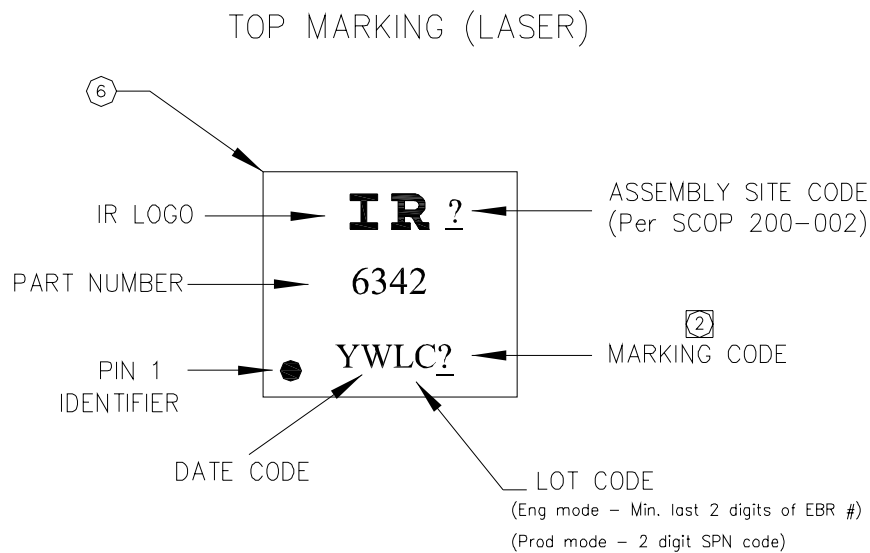


NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER
3. DIMENSION *b* APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm. FROM TERMINAL TIP.

For footprint and stencil design recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

## PQFN 2x2 Outline Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

## PQFN 2x2 Outline Tape and Reel

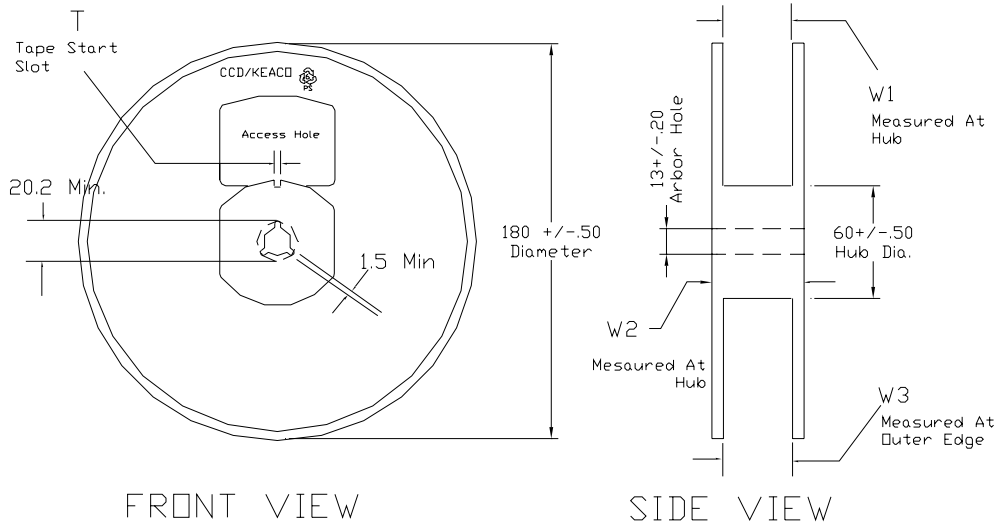
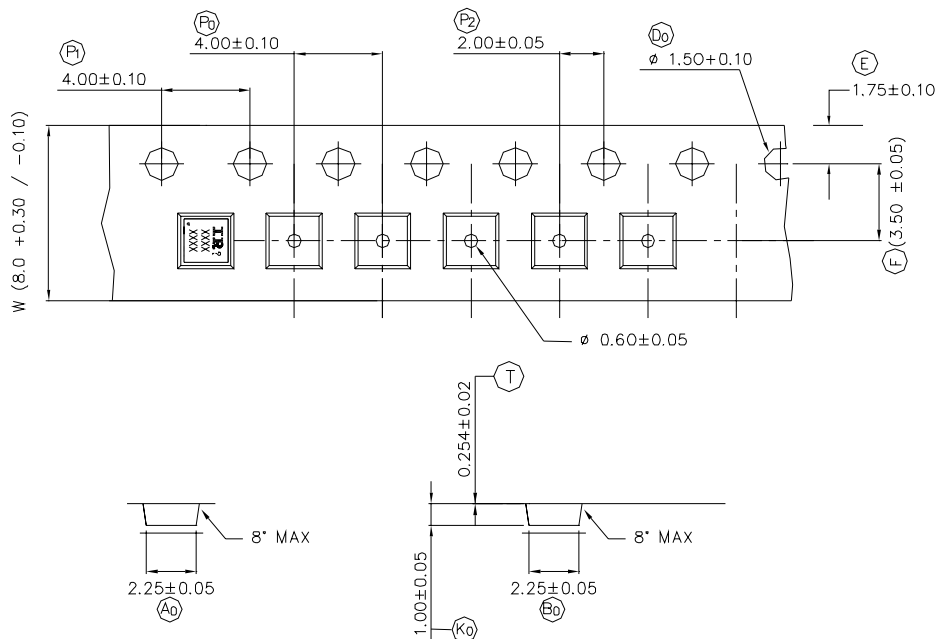


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is  $\geq 1 \times 10^5$  but  $< 1 \times 10^{12}$  ohm/sq.



NOTE: The Surface Resistivity is  $10^4 - 10^8$  OHM/SQ



**Qualification information<sup>†</sup>**

Qualification level	Consumer <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines )	
Moisture Sensitivity Level	PQFN 2mm x 2mm	MSL 1 (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site  
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.  
 Please contact your International Rectifier sales representative for further information:  
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

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