Data Sheet No. PD60299

IRS212(7, 71, 8, 81)(S)PbF

CURRENT SENSING SINGLE CHANNEL DRIVER

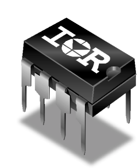
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600 V
  Tolerant to negative transient voltage dV/dt immune
- Application-specific gate drive range:
  Motor Drive: 12 V to 20 V (IRS2127/IRS2128)
  Automotive: 9 V to 20 V (IRS21271/IRS21281)
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V input logic compatible
- $\overline{\text{FAULT}}$ lead indicates shutdown has occured
- Output in phase with input (IRS2127/IRS21271)
- Output out of phase with input (IRS2128/IRS21281)
- RoHS compliant

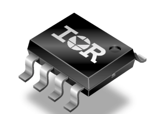
Product Summary

V_{OFFSET}	600 V max.	
I_O+/-	200 mA / 420 mA	
V_{OUT}	12 V - 20V (IRS2127/IR2128)	9 V - 20 V (IRS21271/IR21281)
V_{CSth}	250 mV or 1.8 V	
$t_{on/off}$ (typ.)	150 ns & 150 ns	

Packages



8-Lead PDIP

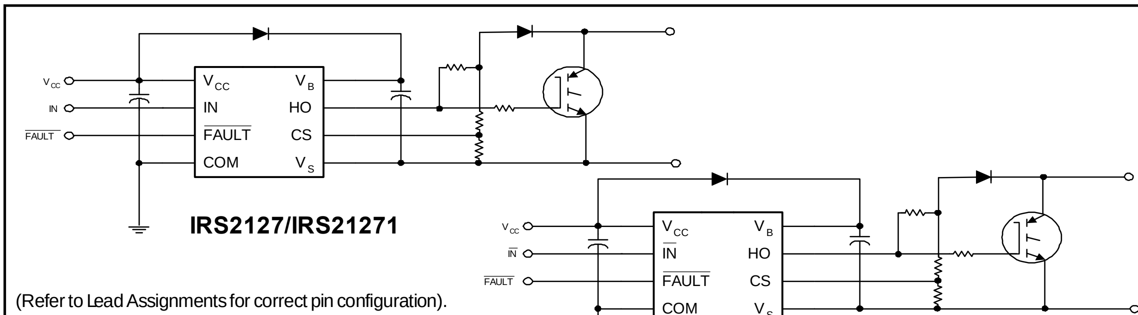


8-Lead SOIC

Description

The IRS2127/IRS2128/IRS21271/IRS21281 are high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3 V. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side or low-side configuration which operates up to 600 V.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). These diagrams show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating supply voltage		-0.3	625	V
V_S	High-side floating offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Logic supply voltage		-0.3	25	
V_{IN}	Logic input voltage		-0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ output voltage		-0.3	V_{CC} + 0.3	
V_{CS}	Current sense voltage		V_S - 0.3	V_B + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \le$ +25 °C	8-Lead DIP	—	1.0	W
		8-Lead SOIC	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	8-Lead DIP	—	125	°C/W
		8-Lead SOIC	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating supply voltage	(IRS2127/IRS2128)	V_S + 12	V_S + 20	V
		(IRS21271/IRS21281)	V_S + 9	V_S + 20	
V_S	High-side floating offset voltage		Note 1	600	
V_{HO}	High-side floating output voltage		V_S	V_B	
V_{CC}	Logic supply voltage		10	20	
V_{IN}	Logic input voltage		0	V_{CC}	
V_{FLT}	$\overline{\text{FAULT}}$ output voltage		0	V_{CC}	
V_{CS}	Current sense signal voltage		V_S	V_S + 5	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25 °C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

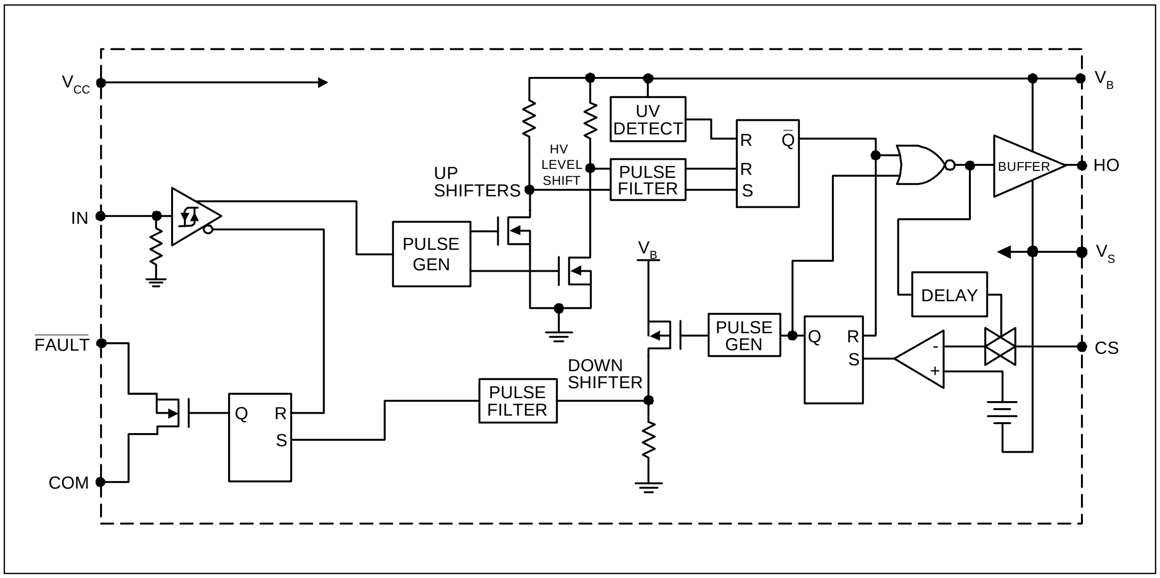
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	150	200	ns	V_S = 0 V
t_{off}	Turn-off propagation delay	—	150	200		V_S = 600 V
t_r	Turn-on rise time	—	80	130		
t_f	Turn-off fall time	—	40	65		
t_{bl}	Start-up blanking time	550	750	950		
t_{cs}	CS shutdown propagation delay	—	65	360		
t_{flt}	CS to $\overline{\text{FAULT}}$ pull-up propagation delay	—	270	510		

Static Electrical Characteristics

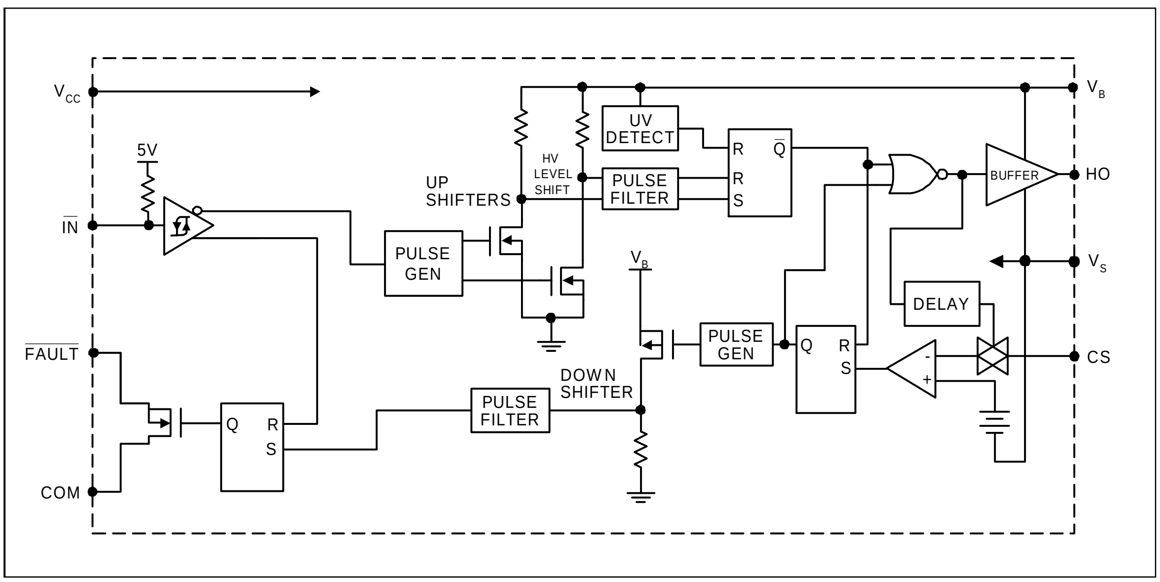
V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25 °C unless otherwise specified. The V_{IN}, $V_{TH,}$ and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage (IRS2127/IRS21271) Logic "0" input voltage (IRS2128/IRS21281)	2.5	—	—	V	V_{CC} = 10 V to 20 V
V_{IL}	Logic "0" input voltage (IRS2127/IRS21271) Logic "1" input voltage (IRS2128/IRS21281)	—	—	0.8		
V_{CSTH+}	CS input positive going threshold (IRS2127/IRS2128)	180	250	320	mV	
	CS input positive going threshold (IRS21271/IRS21281)	1.5	1.8	2.1	V	
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	300	800		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	—	60	120		
I_{IN+}	Logic "1" input bias current	—	7.0	15		V_{IN} = 5 V
I_{IN-}	Logic "0" input bias current	—	—	5.0		V_{IN} = 0 V
I_{CS+}	"High" CS bias current	—	—	5.0		V_{CS} = 3 V
I_{CS-}	"High" CS bias current	—	—	5.0		V_{CS} = 0 V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold (IRS2127/IRS2128)	8.8	10.3	11.8	V	
	V_{BS} supply undervoltage positive going threshold (IRS21271/IRS21281)	6.3	7.2	8.2		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold (IRS2127/IRS2128)	7.5	9.0	10.6		
	V_{BS} supply undervoltage negative going threshold (IRS21271/IRS21281)	6.0	6.8	7.7		
I_{O+}	Output high short circuit pulsed current	200	290	—	mA	V_O = 0 V, V_{IN} = 5 V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	420	600	—		V_O = 15 V, V_{IN} = 0 V PW ≤ 10 µs
$R_{on,FLT}$	FAULT - low on resistance	—	125	—	Ω	

Functional Block Diagram IRS2127/IRS21271



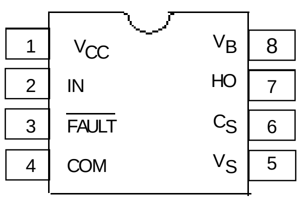
Functional Block Diagram IRS2128/IRS21281



Lead Definitions

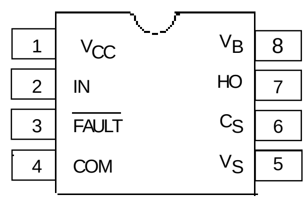
Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IRS2127/IRS21271) out of phase with HO (IRS2128/IRS21281)
$\overline{FAULT}$	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



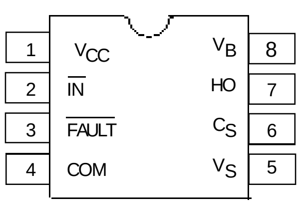
8 Lead PDIP

IRS2127/IRS21271



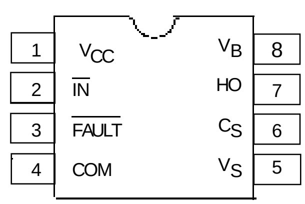
8 Lead SOIC

IRS2127S/IRS21271S



8 Lead PDIP

IRS2128/IRS21281



8 Lead SOIC

IRS2128S/IRS21281S

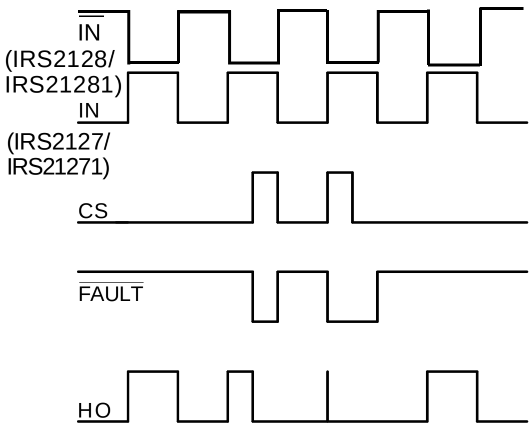


Figure 1. Input/Output Timing Diagram

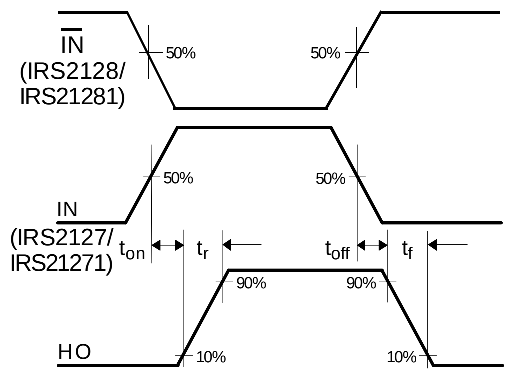


Figure 2. Switching Time Waveform Definition

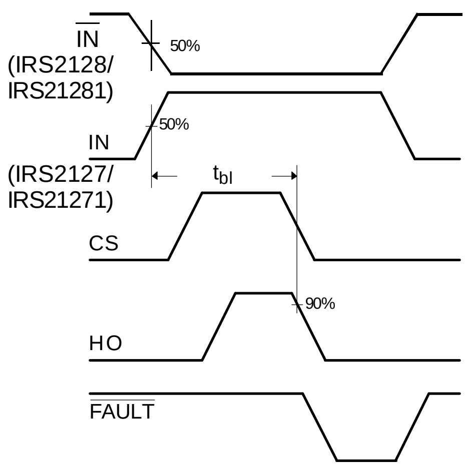


Figure 3. Start-Up Blanking Time Waveform Definitions

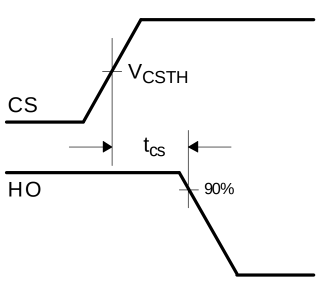


Figure 4. CS Shutdown Waveform Definitions

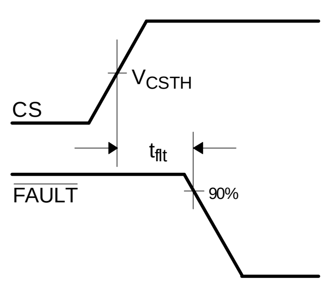


Figure 5. CS to FAULT Waveform Definitions

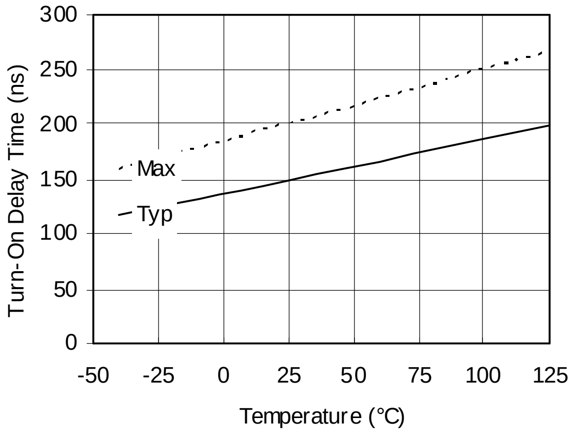


Figure 6A. Turn-On Delay Time vs. Temperature

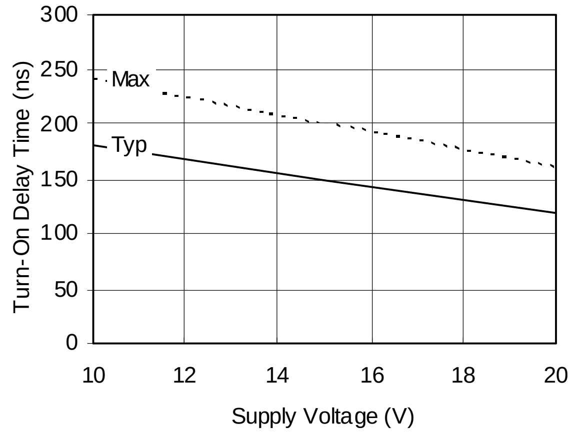


Figure 6B. Turn-On Delay Time vs. Voltage

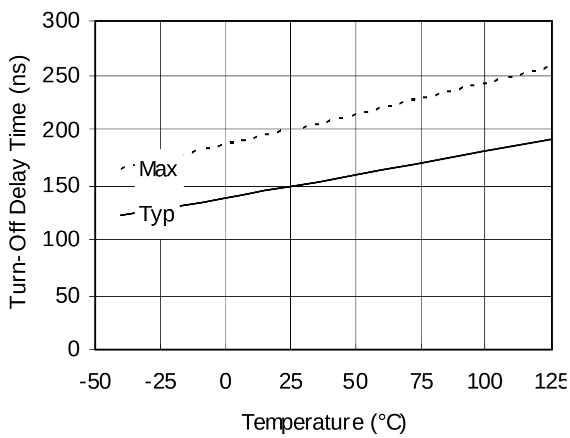


Figure 7A. Turn-Off Delay Time vs. Temperature

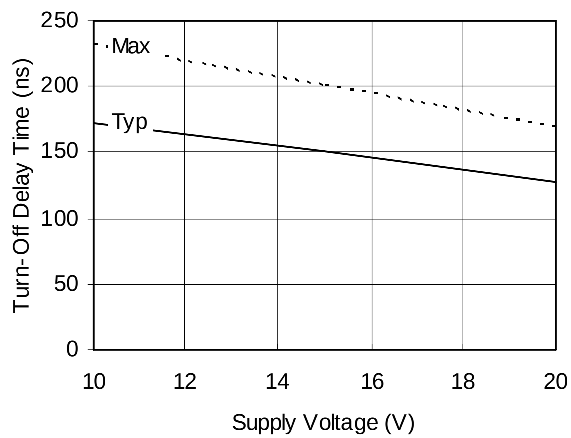


Figure 7B. Turn-Off Delay Time vs. Voltage

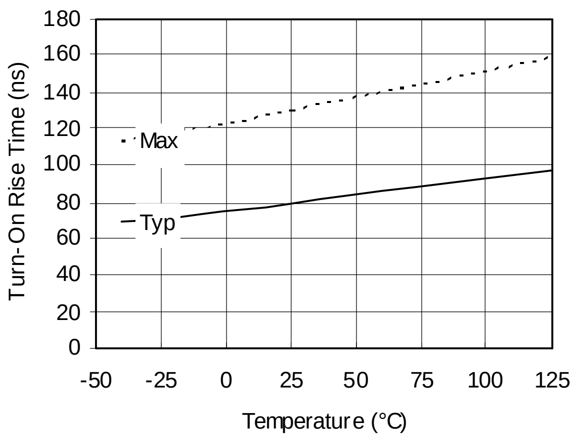


Figure 8A. Turn-On Rise Time vs. Temperature

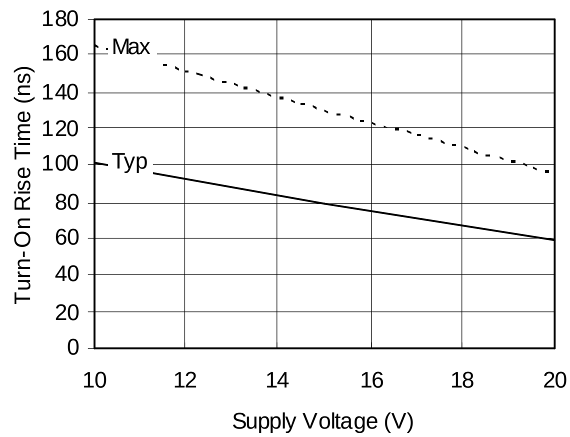


Figure 8B. Turn-On Rise Time vs. Voltage

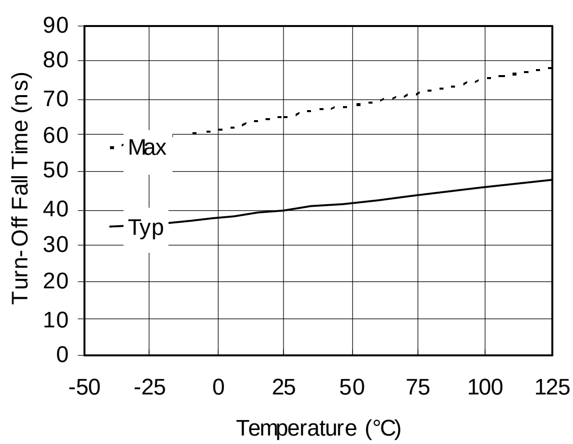


Figure 9A. Turn-Off Fall Time vs. Temperature

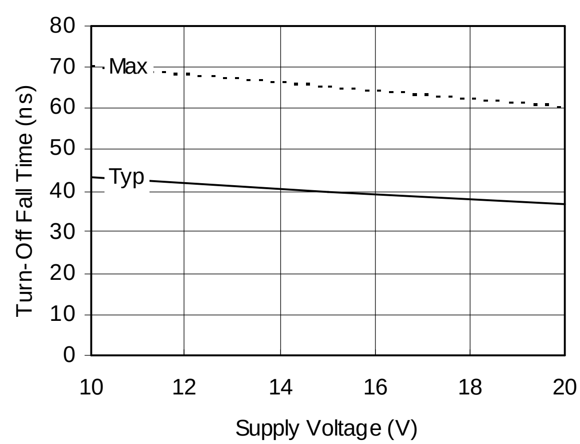


Figure 9B. Turn-Off Fall Time vs. Voltage

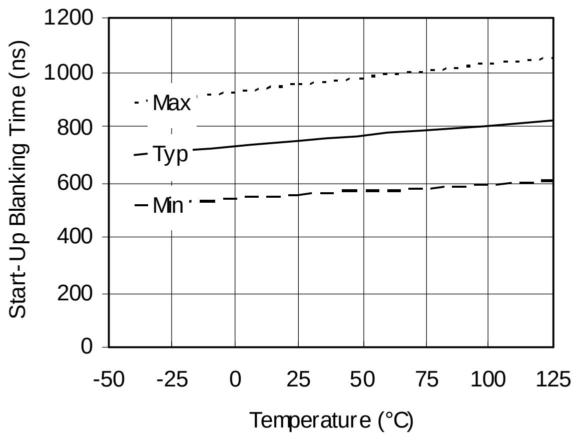


Figure 10A. Start-Up Blanking Time vs. Temperature

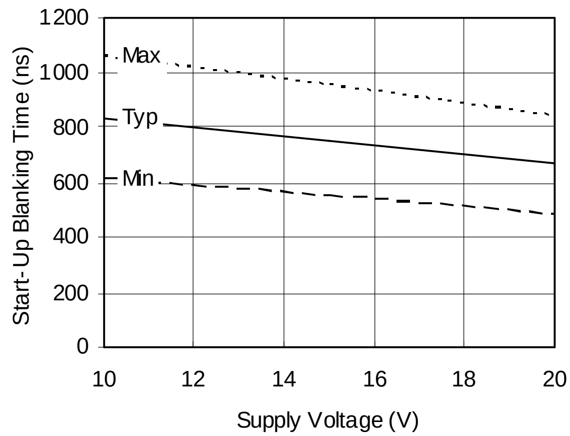


Figure 10B. Start-Up Blanking Time vs. Voltage

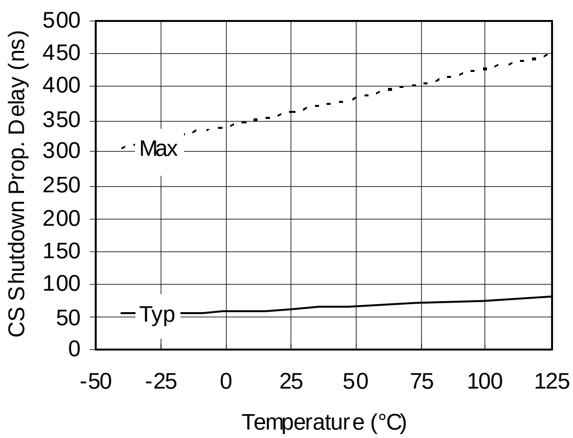


Figure 11A. CS Shutdown Prop. Delay vs. Temperature

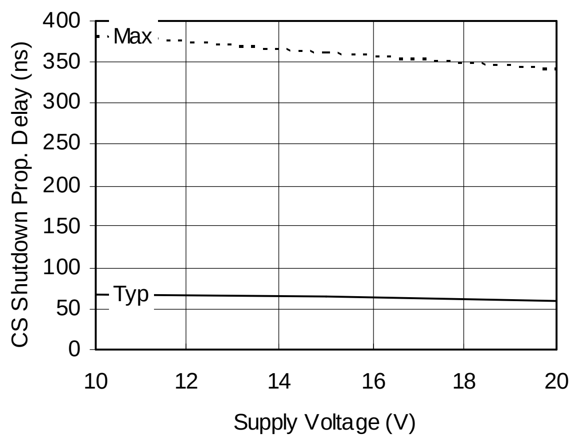


Figure 11B. CS Shutdown Prop. Delay vs. Voltage

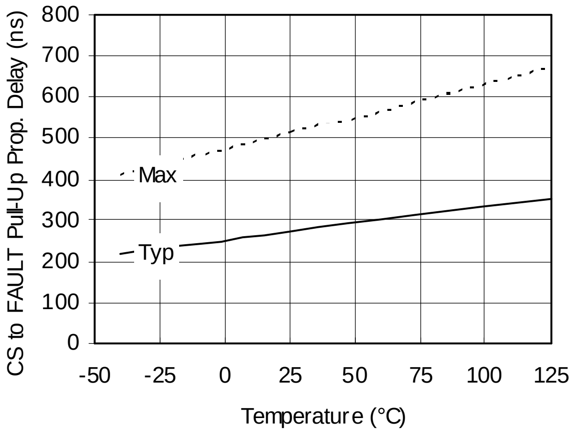


Figure 12A. CS to FAULT Pull-Up Prop. Delay vs. Temperature

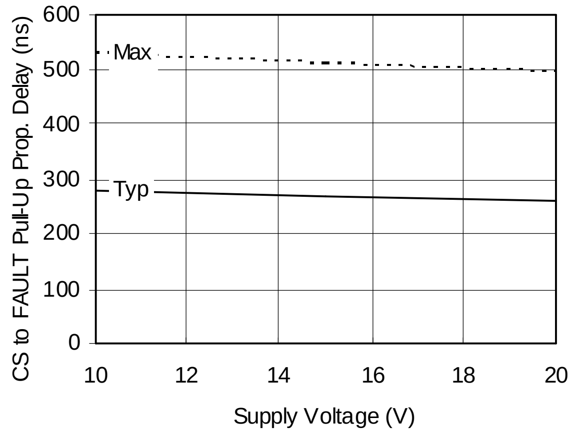


Figure 12B. CS to FAULT Pull-Up Prop. Delay vs. Voltage

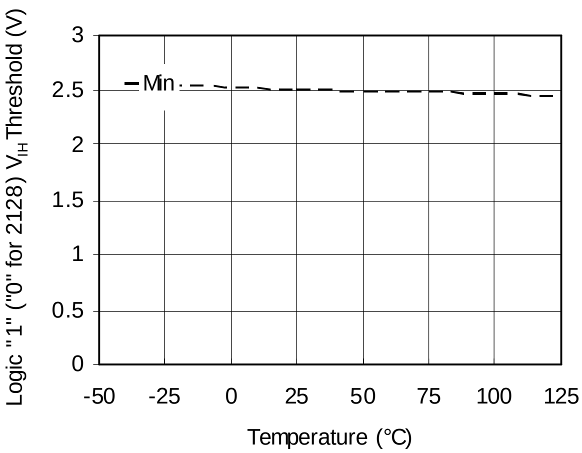


Figure 13A. Logic "1" ("0" for 2128) V_{IH} Threshold vs. Temperature

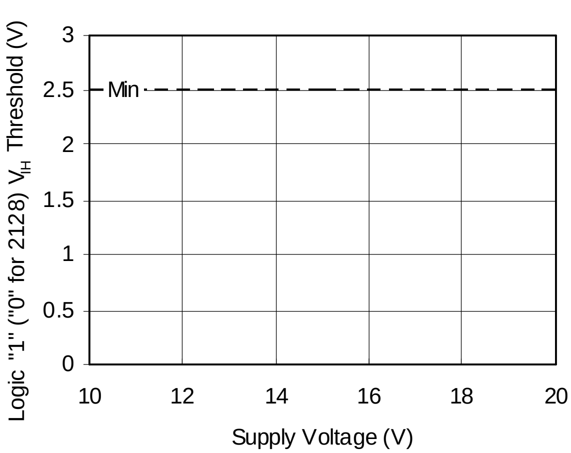


Figure 13B. Logic "1" ("0" for 2128) V_{IH} Threshold vs. Voltage

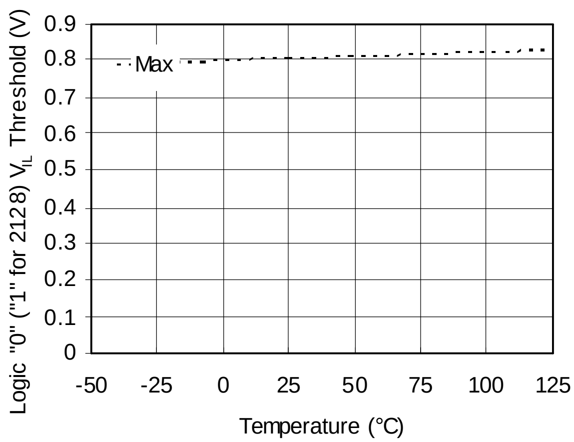


Figure 14A. Logic "0" ("1" for 2128) V_{IL} Threshold vs. Temperature

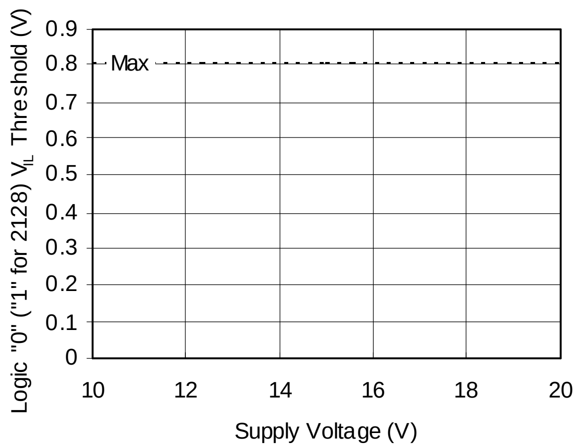


Figure 14B. Logic "0" ("1" for 2128) V_{IL} Threshold vs. Voltage

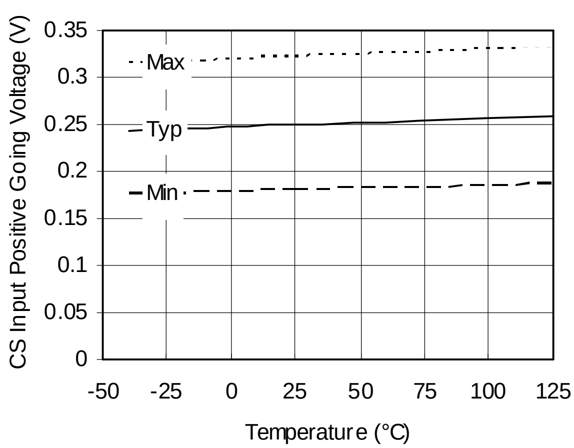


Figure 15A. CS Input Positive Going Voltage vs. Temperature

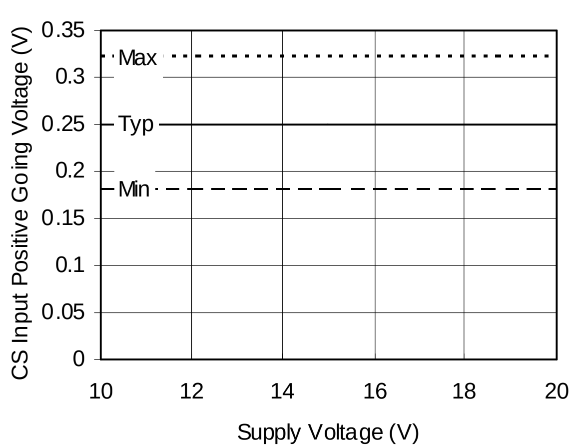


Figure 15B. CS Input Positive Going Voltage vs. Voltage

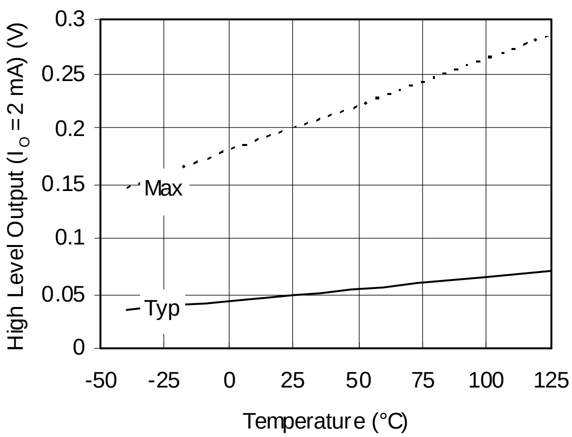


Figure 16A. High Level Output (I_O = 2 mA) vs. Temperature

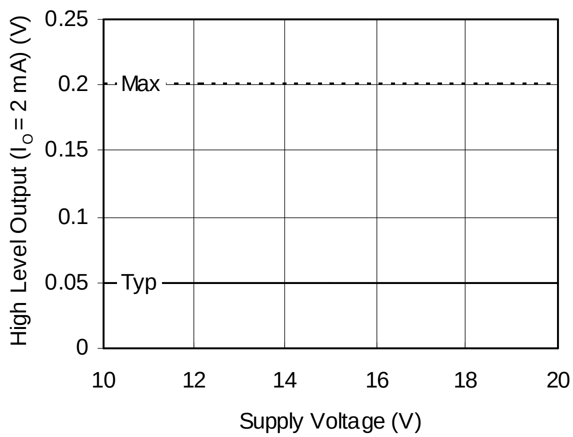


Figure 16B. High Level Output (I_O = 2 mA) vs. Voltage

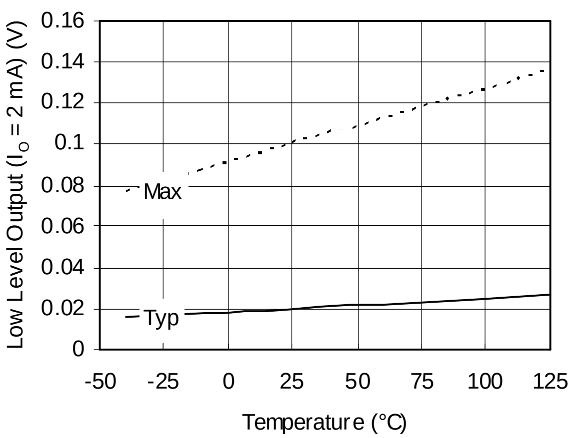


Figure 17A. Low Level Output (I_O = 2 mA) vs. Temperature

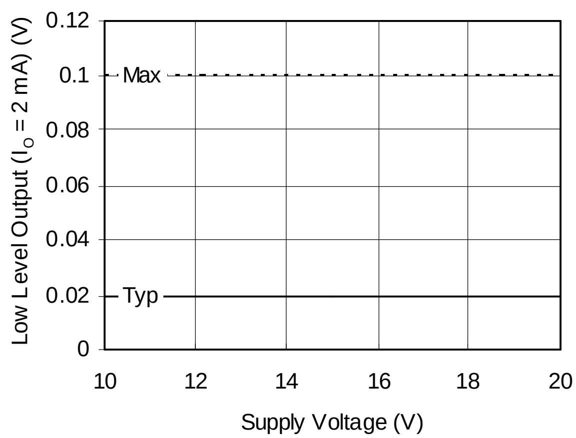


Figure 17B. Low Level Output (I_O = 2 mA) vs. Voltage

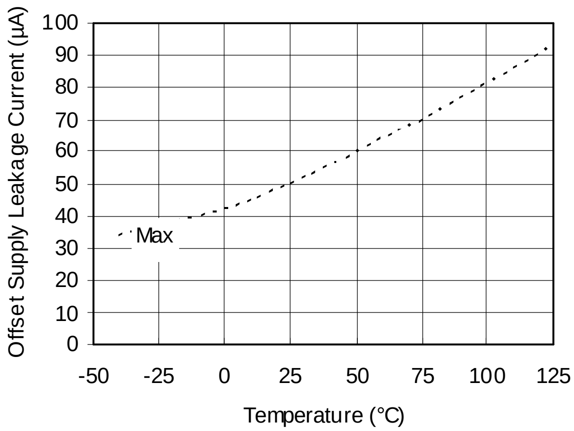


Figure 18A. Offset Supply Leakage Current vs. Temperature

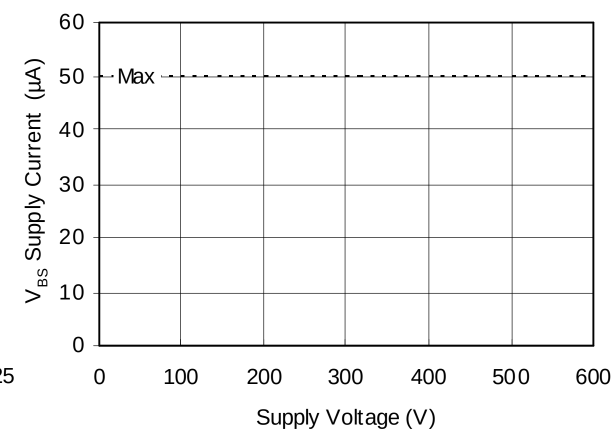


Figure 18B. High-Side Floating Well Offset Supply Leakage vs. Voltage

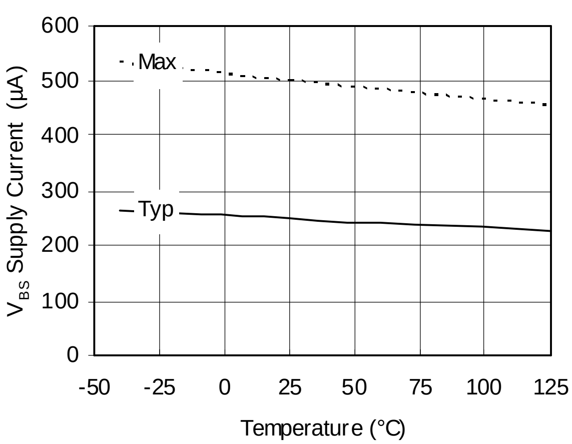


Figure 19A. V_{BS} Supply Current vs. Temperature

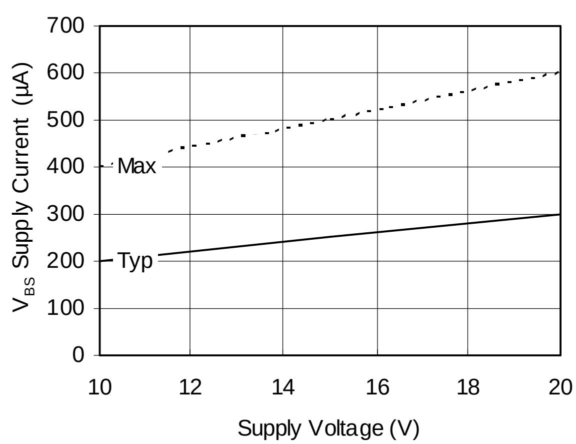


Figure 19B. V_{BS} Supply Current vs. Voltage

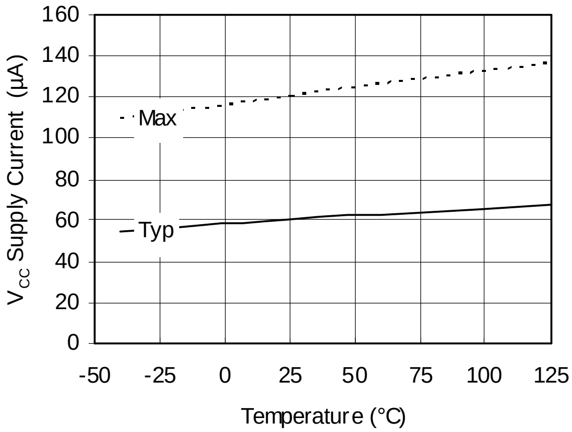


Figure 20A. V_{CC} Supply Current vs. Temperature

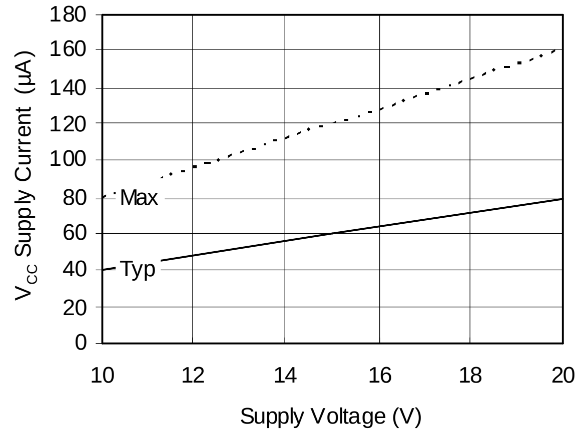


Figure 20B. V_{CC} Supply Current vs. Voltage

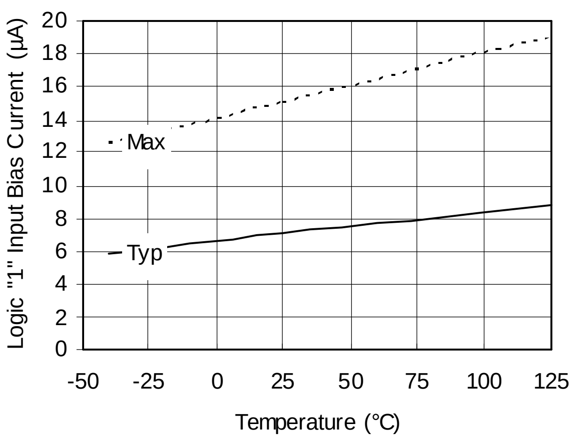


Figure 21A. Logic "1" Input Bias Current vs. Temperature

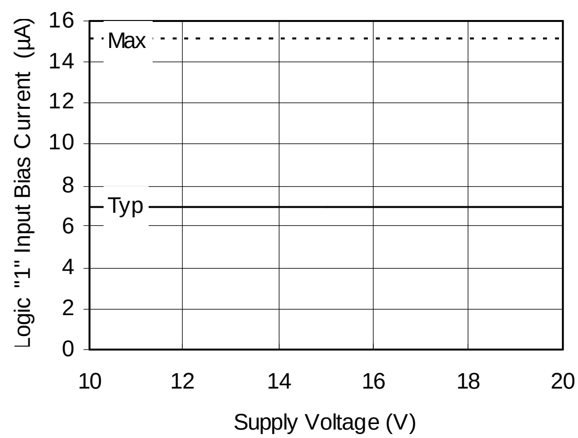


Figure 21B. Logic "1" Input Bias Current vs. Voltage

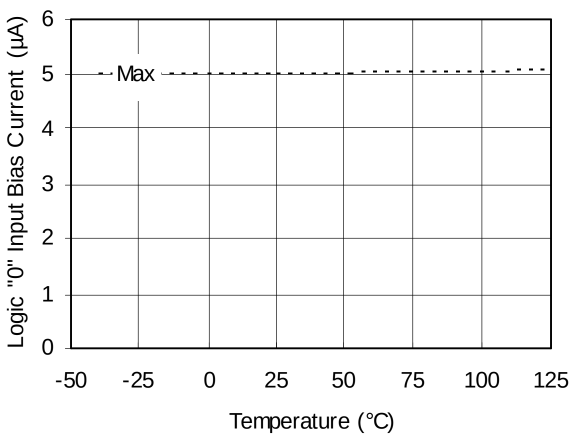


Figure 22A. Logic "0" Input Bias Current vs. Temperature

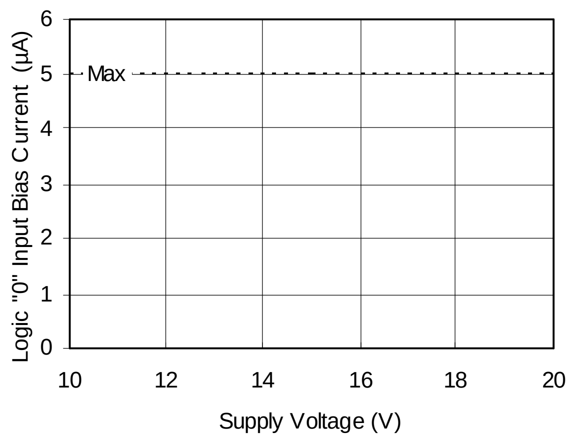


Figure 22B. Logic "0" Input Bias Current vs. Voltage

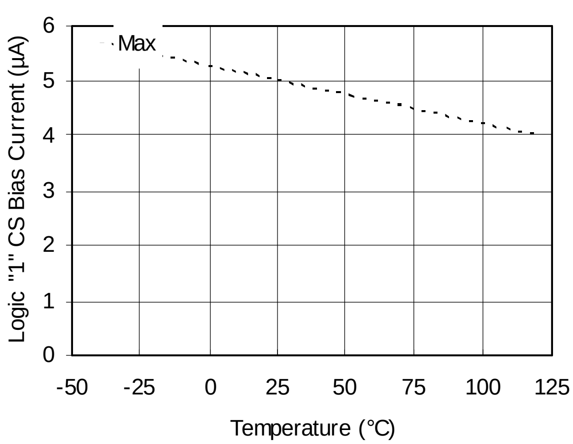


Figure 23A. Logic "1" CS Bias Current vs. Temperature

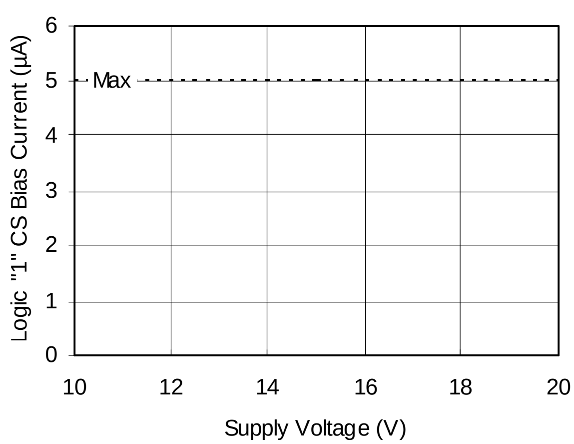


Figure 23B. Logic "1" CS Bias Current vs. Voltage

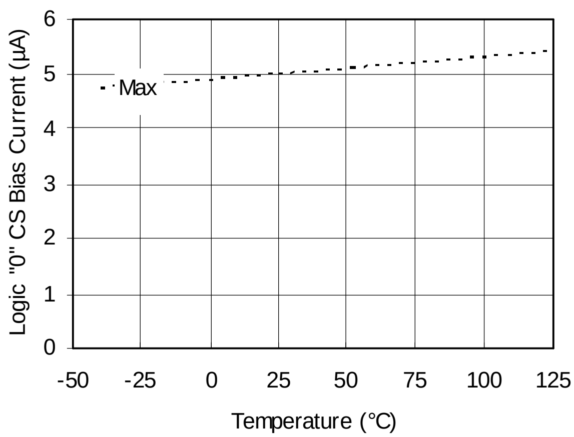


Figure 24A. Logic "0" CS Bias Current vs. Temperature

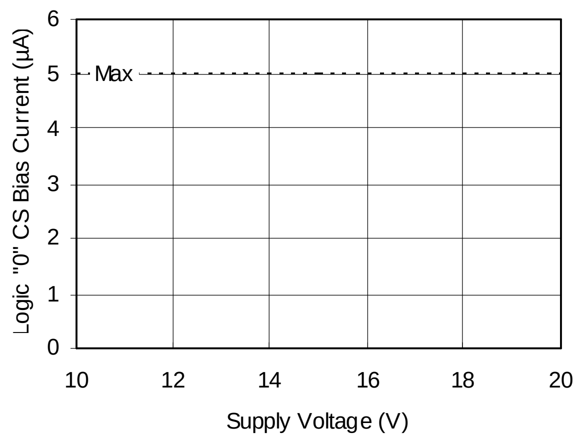


Figure 24B. Logic "0" CS Bias Current vs. Voltage

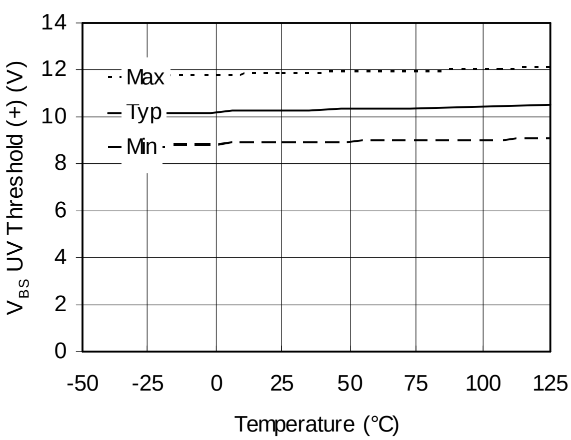


Figure 25A. V_{BS} UV Threshold (+) vs. Temperature

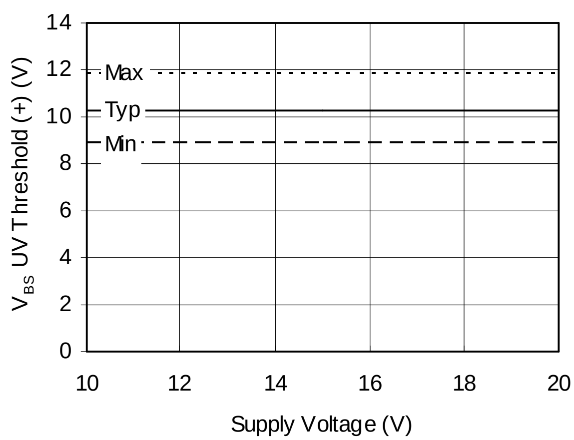


Figure 25B. V_{BS} UV Threshold (+) vs. Voltage

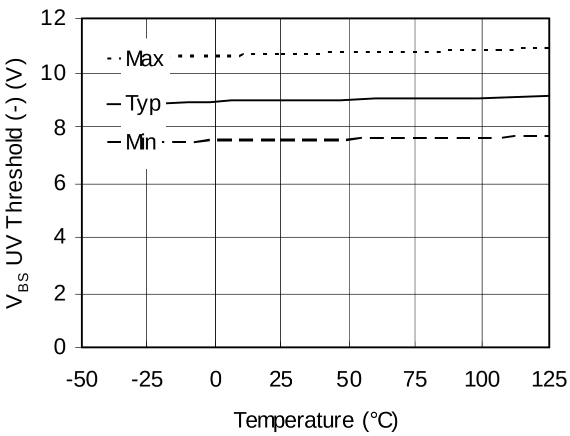


Figure 26A. V_{BS} UV Threshold (-) vs. Temperature

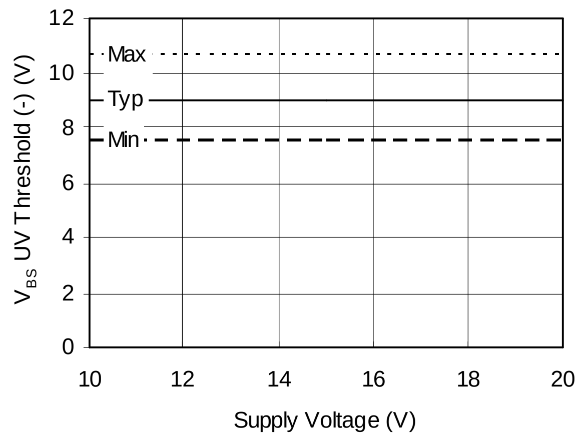


Figure 26B. V_{BS} UV Threshold (-) vs. Voltage

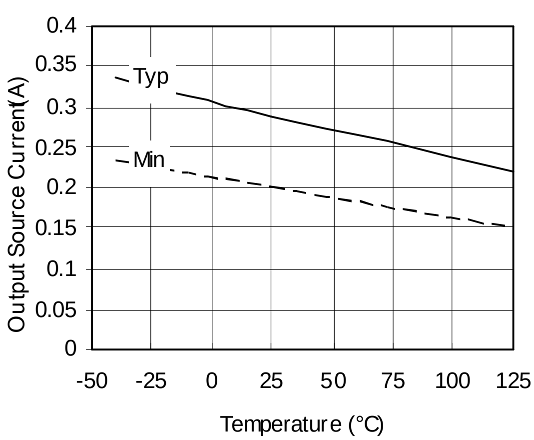


Figure 27A. Output Source Current vs. Temperature

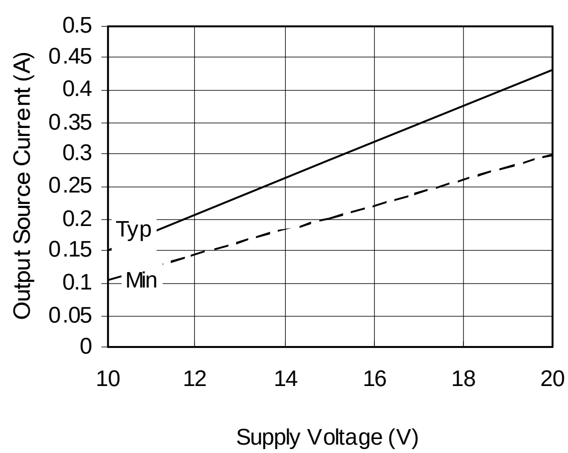


Figure 27B. Output Source Current vs. Voltage

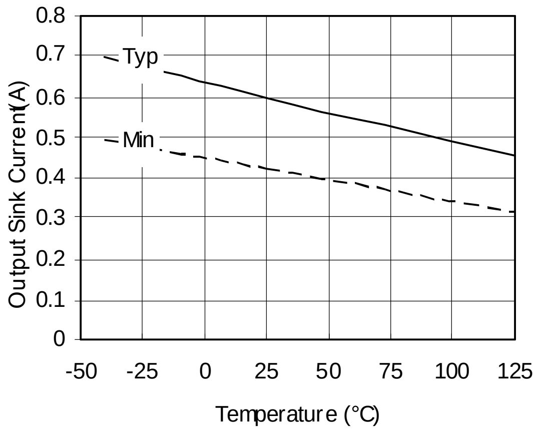


Figure 28A. Output Sink Current vs. Temperature

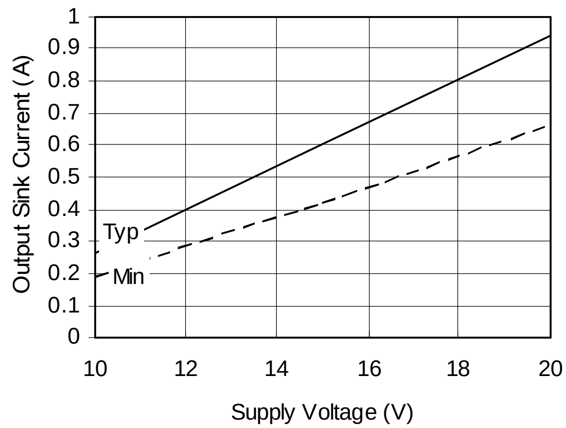
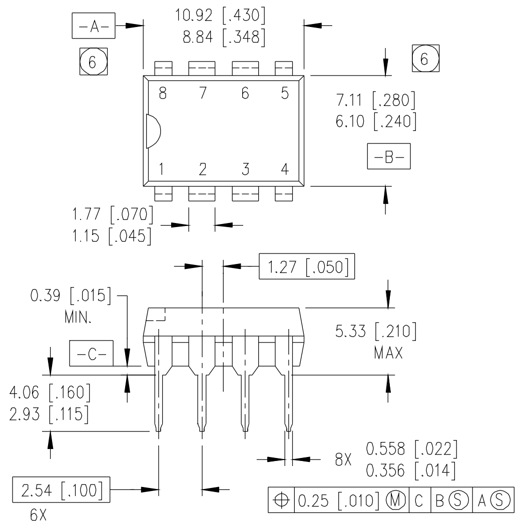


Figure 28B. Output Sink Current vs. Voltage

Case outlines

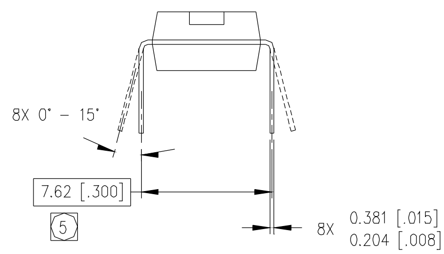


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

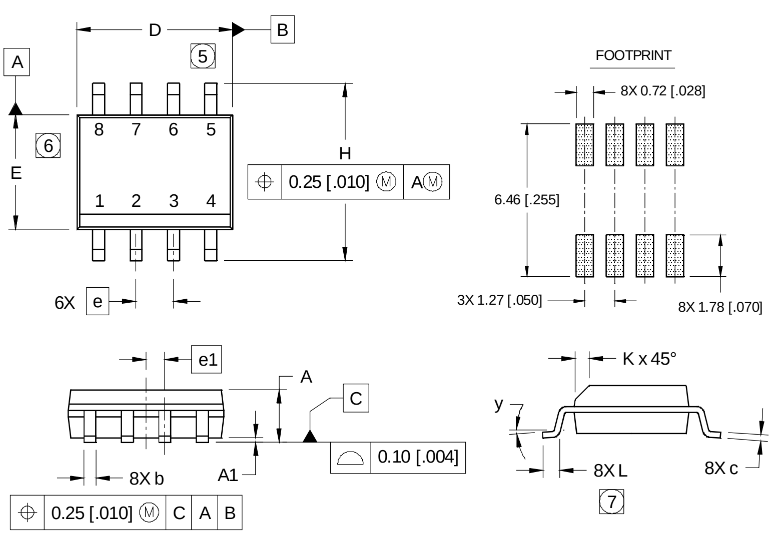
5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

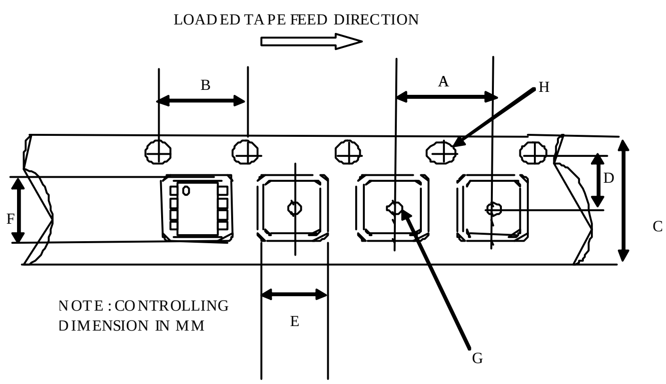
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

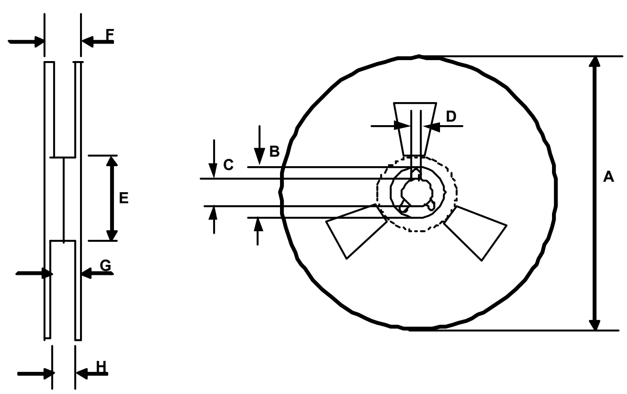
01-6027
01-0021 11 (MS-012AA)

Tape & Reel
8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

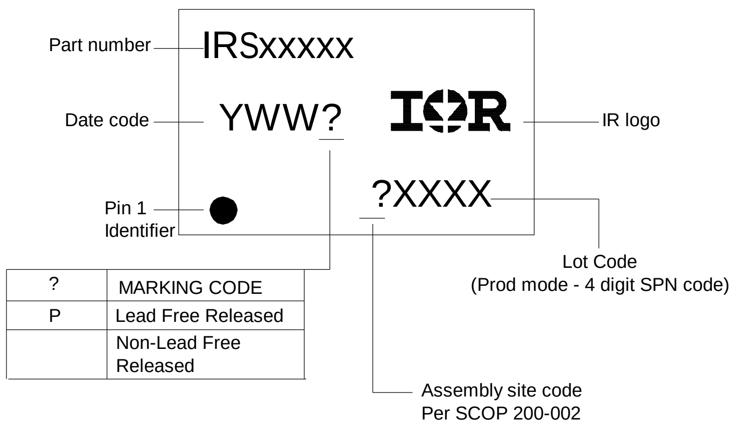
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

8-Lead PDIP IRS2127PbF	8-Lead PDIP IRS2128PbF
8-Lead PDIP IRS21271PbF	8-Lead PDIP IRS21281PbF
8-Lead SOIC IRS2127SPbF	8-Lead SOIC IRS2128SPbF
8-Lead SOIC IRS21271SPbF	8-Lead SOIC IRS21281SPbF
8-Lead SOIC Tape & Reel IRS2127STRPbF	8-Lead SOIC Tape & Reel IRS2128STRPbF
8-Lead SOIC Tape & Reel IRS21271STRPbF	8-Lead SOIC Tape & Reel IRS21281STRPbF

International Rectifier

The SOIC-8 is MSL2 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 6/27/2007