4M-BIT [512K x 8] SINGLE VOLTAGE 5V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Single Power Supply Operation
  - 4.5 to 5.5 volt for read, erase, and program operations
- 524288 x 8 only
- Sector Structure
  - 64K-Byte x 8
- Latch-up protected to 100mA from -1V to Vcc + 1V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Access time: 70/90ns
  - Program time: 9us (typical)
  - Erase time: 0.7s/sector, 4s/chip (typical)
- Low Power Consumption
  - Low active read current: 30mA (maximum) at 5MHz
  - Low standby current: 1uA (typical)
- Minimum 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion

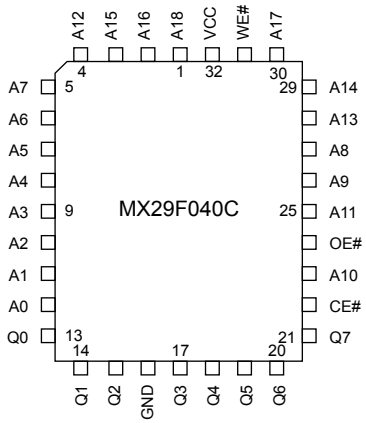
PACKAGE

- 32-Pin PLCC
- 32-Pin TSOP
- **All devices are RoHS Compliant**

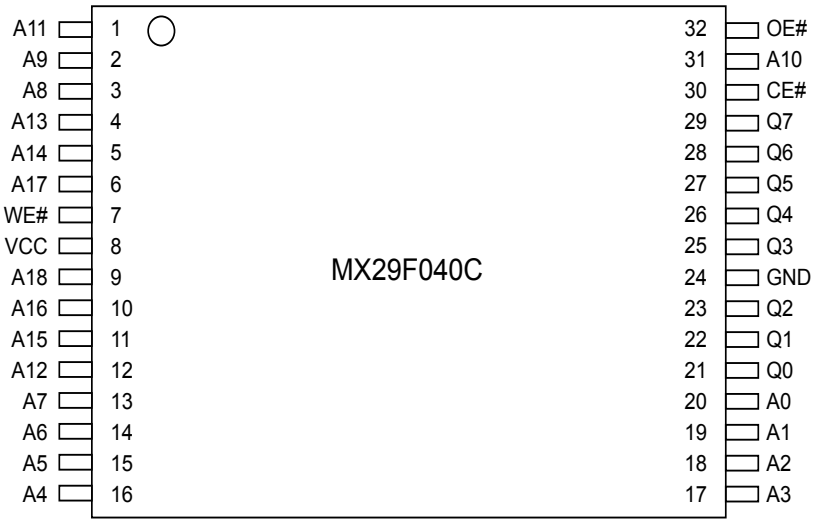
Contents

PIN CONFIGURATIONS

32 PLCC



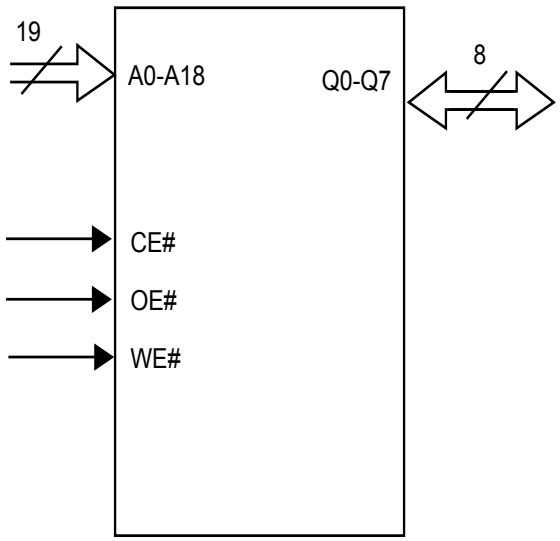
32 TSOP (Standard Type) (8mm x 20mm)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
GND	Ground Pin
VCC	+5.0V single power supply

LOGIC SYMBOL



BLOCK DIAGRAM

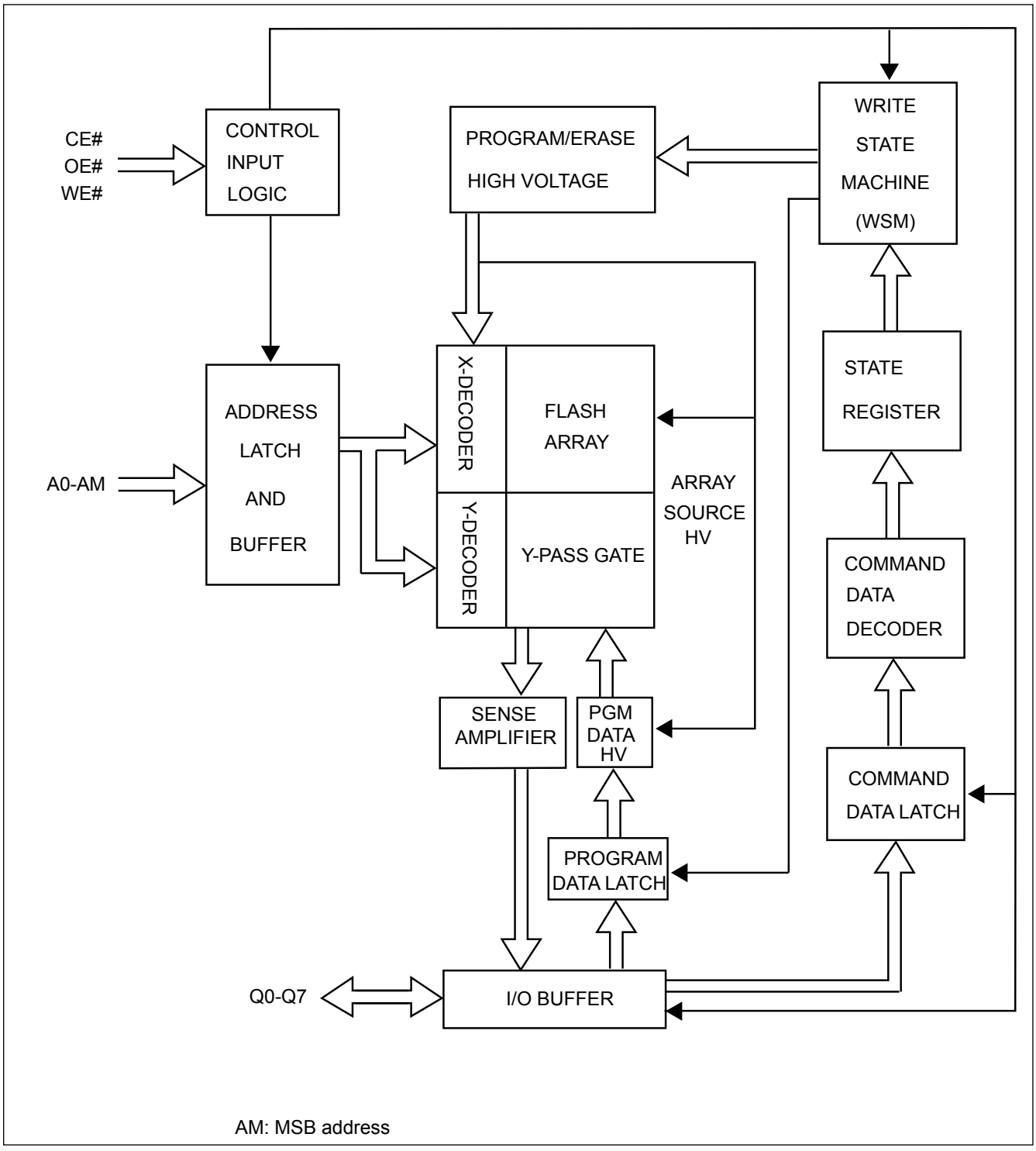


Table 1. SECTOR STRUCTURE

MX29F040C SECTOR ADDRESS TABLE

Sector	Sector Address			Address Range
	A18	A17	A16	
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

Note: All sectors are 64 Kbytes in size.

Table 2. BUS OPERATION

Mode / Pins	CE#	OE#	WE#	A0	A1	A6	A9	Q0 ~ Q7
Read Silicon ID Manufacture Code	L	L	H	L	L	X	Vhv	C2H
Read Silicon ID Device Code	L	L	H	H	L	X	Vhv	A4H
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}

Notes:
1. Vhv is the very high voltage, 11.5V to 12.5V.
2. X means input high (Vih) or input low (Vil).

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array out. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped after a period of time no more than Treadyand the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

"Figure 1. COMMAND WRITE OPERATION" illustrates the AC timing waveform of a write command, and *"TABLE 3. MX29F040C COMMAND DEFINITIONS"* defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode or erase-suspended read array mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE# and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29F040C is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29F040C COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select		Program	Chip Erase	Sector Erase	Erase Suspend	Erase Resume
				Manufacturer ID	Device ID					
1st Bus Cycle	Addr	Addr	XXX	555	555	555	555	555	XXX	XXX
	Data	Data	F0	AA	AA	AA	AA	AA	B0	30
2nd Bus Cycle	Addr			2AA	2AA	2AA	2AA	2AA		
	Data			55	55	55	55	55		
3rd Bus Cycle	Addr			555	555	555	555	555		
	Data			90	90	A0	80	80		
4th Bus Cycle	Addr			X00	X01	Addr	555	555		
	Data			C2	ID	Data	AA	AA		
5th Bus Cycle	Addr						2AA	2AA		
	Data						55	55		
6th Bus Cycle	Addr						555	Sector		
	Data						10	30		

Notes:

1. Device ID: A4H.
2. It is not allowed to adopt any other code which is not in the above command definition table.

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

	Address	Data (Hex)
Manufacturer ID	X00	C2
Device ID	X01	A4

There is an alternative method to that shown in *"Table 2. BUS OPERATION"*, which is intended for EPROM programmers and requires Vhv on address bit A9.

AUTOMATIC PROGRAMMING

The MX29F040Ccan provide the user program function. As long as the users enter the right cycle defined in the *"TABLE 3. MX29F040C COMMAND DEFINITIONS"* (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

With the internal write state controller, the device requires the user to write the program command and data only. The typical chip program time at room temperature of the MX29F040C is 4.5 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5
In progress*1	Q7#	togging	0
Finished	Q7	Stop toggling	0
Exceed time limit	Q7#	Toggling	1

*1: The status "in progress" means both program mode and erase-suspended program mode.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware rests or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2
In progress	0	Togging	0	Toggling
Finished	1	Stop toggling	0	1
Exceed time limit	0	Toggling	1	Toggling

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2
Time-out period	0	Toggling	0	0	Toggling
In progress	0	Togging	0	1	Toggling
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	1	Toggling

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1(<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, and Q7.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	toggle
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, program, and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 400us interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage Range
Vcc . . . . . .-0.5V to +7.0 V
A9 . . . . . .-0.5V to +13.5 V
The other pins. . . . . .-0.5V to Vcc +0.7 V
Output Short Circuit Current (less than one second) . . . . . .200 mA

Note:
1. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to Vcc +2V during during transition and for less than 20ns during transitions.

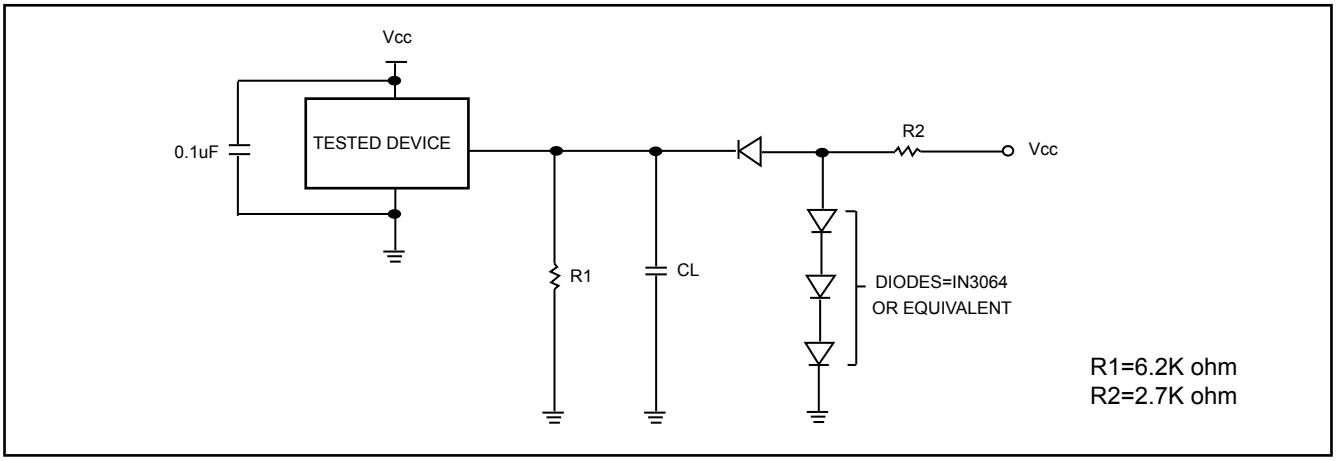
OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade
Surrounding Temperature (T_A). . . . . 0°C to +70°C
Industrial (I) Grade
Surrounding Temperature (T_A). . . . . -40°C to +85°C
V_{CC} Supply Voltages
V_{CC} range. . . . . +4.5V to 5.5V

DC CHARACTERISTICS

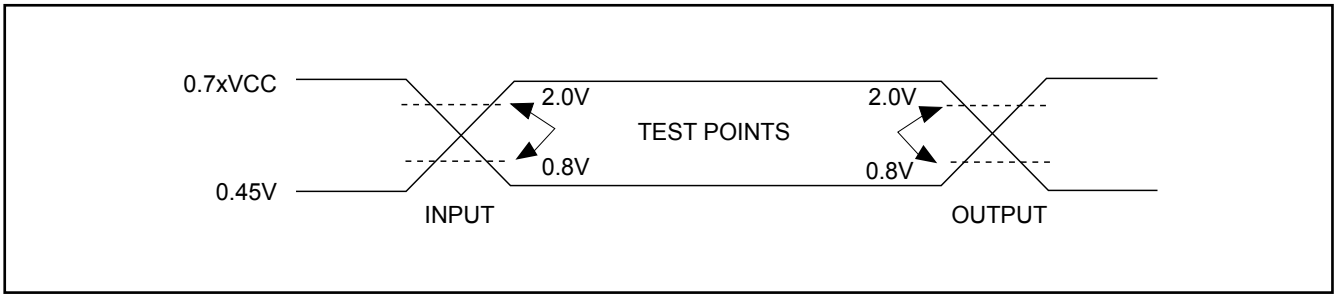
Symbol	Description	Min	Typ	Max	Remark
Iilk	Input Leak			± 1.0uA	
Iolk	Output Leak			10uA	
Icr1	Read Current(10MHz)			50mA	CE#=Vil, OE#=Vih
Icr2	Read Current(5MHz)			40mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	30mA	CE#=Vil, OE#=Vih, WE#=ViL
Isb1	Standby Current (TTL)			1mA	Vcc=Vcc max, CE#=Vih other pin disable
Isb2	Standby current (CMOS)		1uA	5uA	Vcc=Vcc max, CE#=vcc +0.3V, other pin disable
Vil	Input Low Voltage	-0.3V		0.8V	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for Auto Select	11.5V	12V	12.5V	
Vol	Output Low Voltage			0.45V	Iol=2.1mA, Vcc=Vcc min
Voh1	Ouput High Voltage (TTL)	2.4V			Ioh1=-2mA
Voh2	Ouput High Voltage (CMOS)	Vcc-0.4V			Ioh2=-100uA

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance, CL: 100PF for 90ns, 30PF for 70ns
Rise/Fall Times : 10nS
Input/Output reference levels: 0.8V, 2.0V

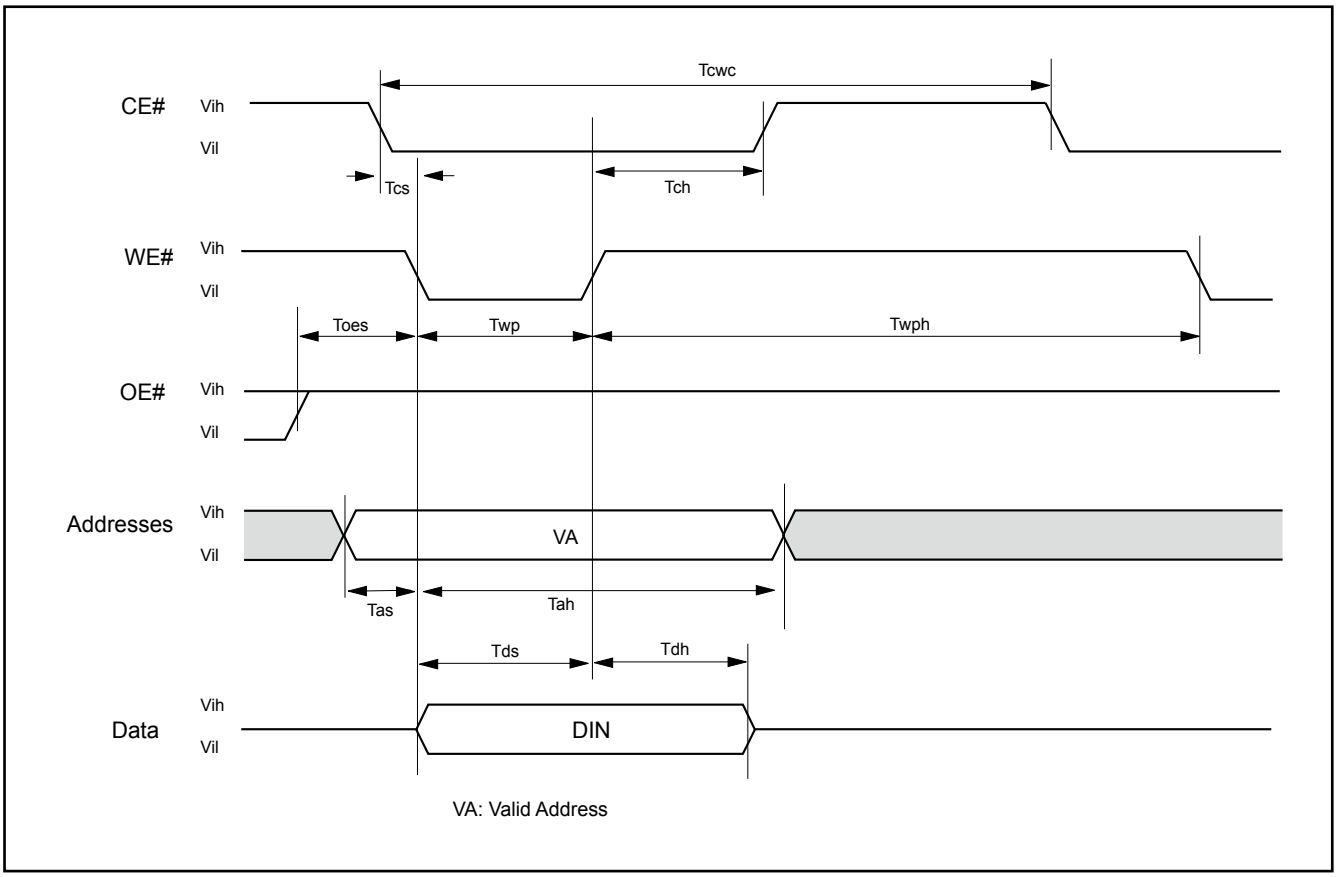
SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

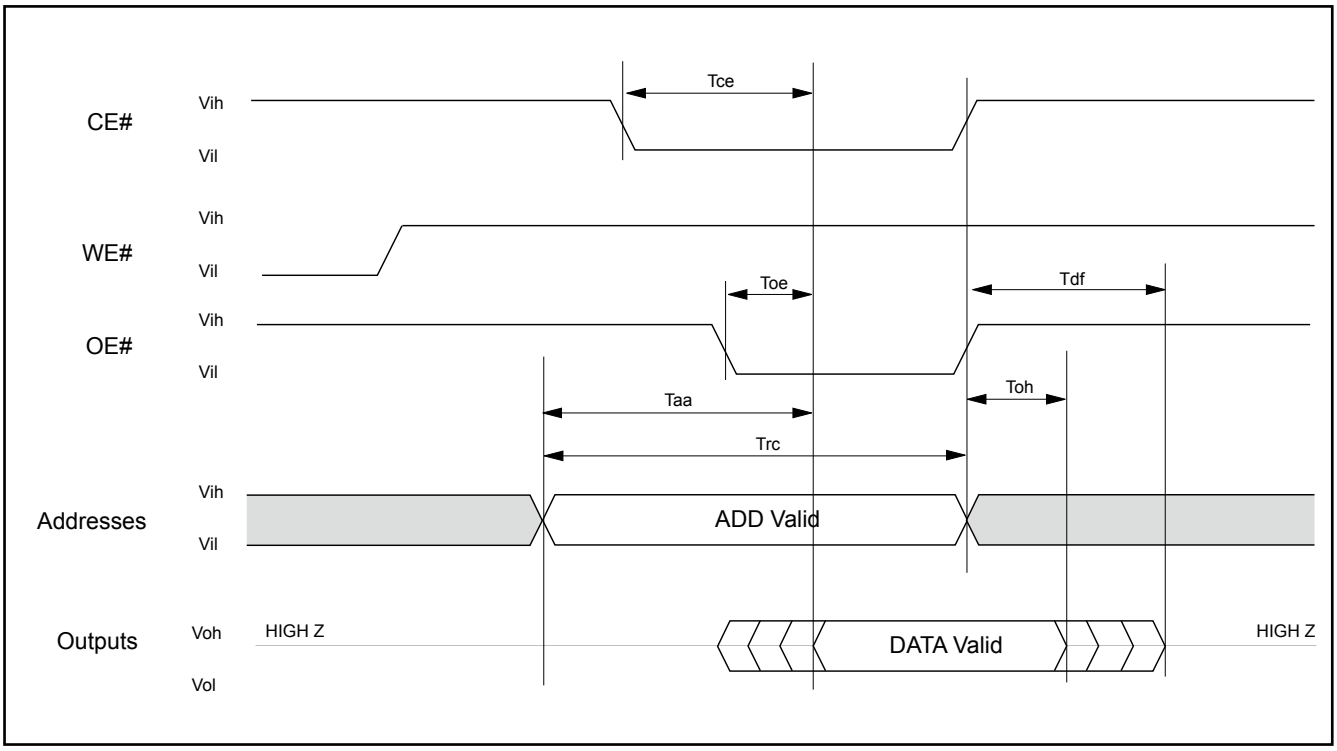
Symbol	Description	Speed Option -70/90			Unit
		Min	Typ	Max	
Taa	Valid data output after address			70/90	ns
Tce	Valid data output after CE# low			70/90	ns
Toe	Valid data output after OE# low			30/35	ns
Tdf	Data output floating after OE# high or CE# high			20	ns
Toh	Output hold time from the earliest rising edge of Addrss, CE#, OE#	0			ns
Trc	Read period time	70/90			ns
Twp	WE# pulse width	35			ns
Twph	WE# pulse with high	30			ns
Tghwl	Read recover time before write	0			ns
Twc	Write period time	70/90			ns
Tcwc	Command write period time	70/90			ns
Tas	Address setup time	0			ns
Tah	Address hold time	45			ns
Tds	Data setup time	30/45			ns
Tdh	Data hold time	0			ns
Tcs	CE# Setup time	0			ns
Tch	CE# hold time	0			ns
Toes	OE# setup time	0			ns
Tcep	CE# pulse width	35/45			ns
Tceph	CE# pulse width high	20			ns
Tavt	Program operation		9	300	us
Taetc	Chip Erase Operation		4	32	sec
Taetb	Sector Erase Operation		0.7	8	sec
Tbal	Sector Address hold time			50	us

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

Figure 2. READ TIMING WAVEFORMS



ERASE/PROGRAM OPERATION

Figure 3. AUTOMATIC CHIP ERASE TIMING WAVEFORM

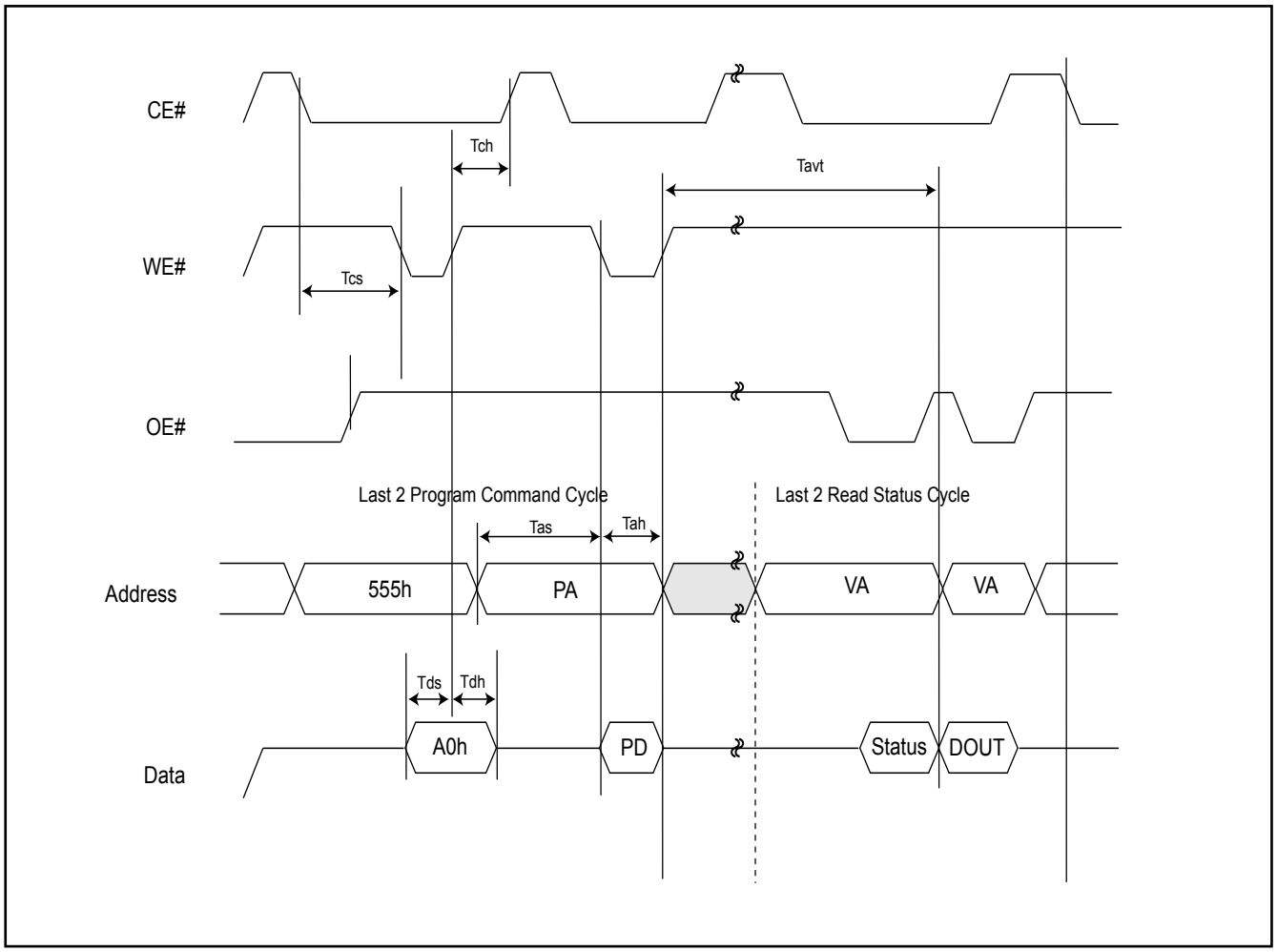


Figure 4. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

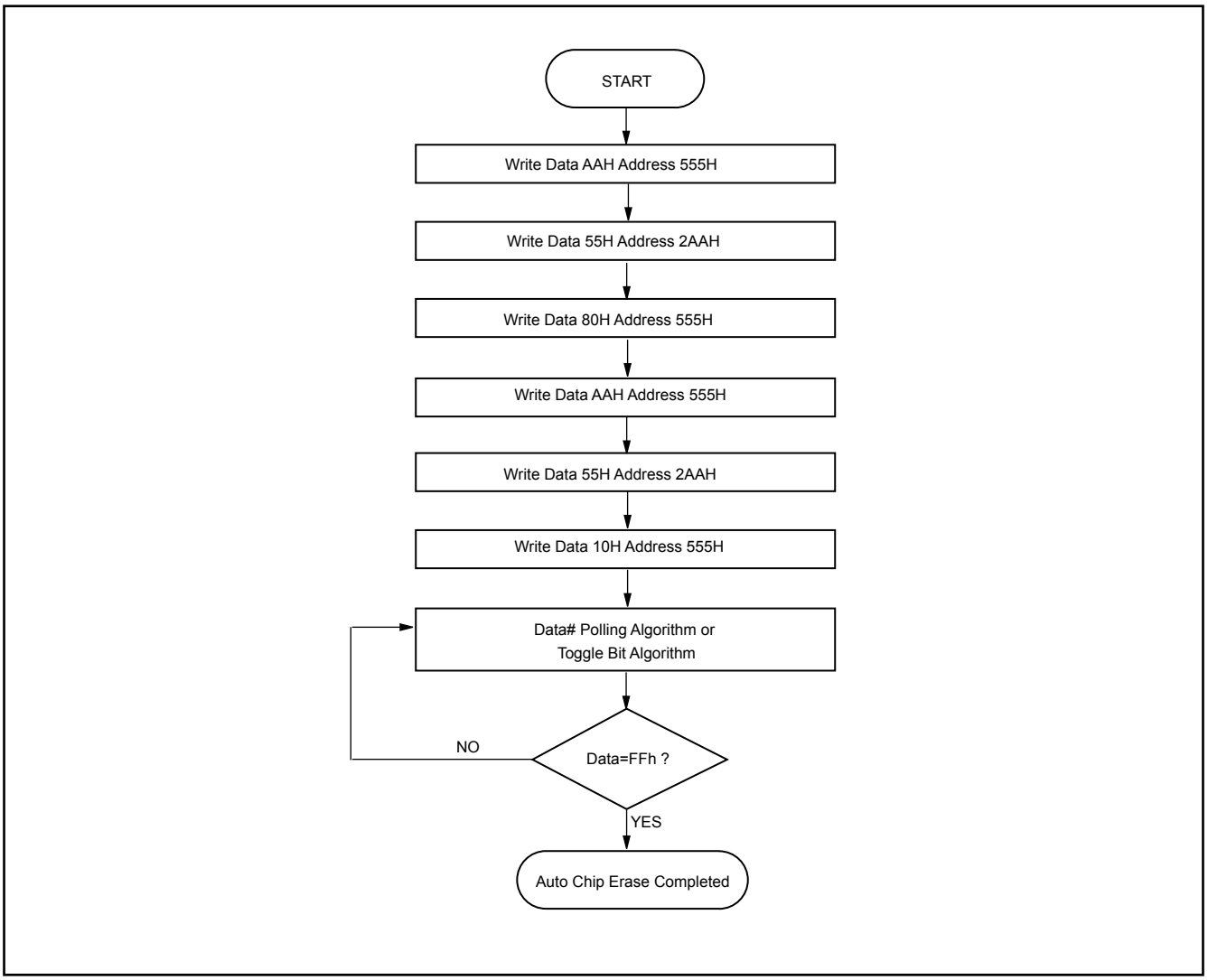


Figure 5. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

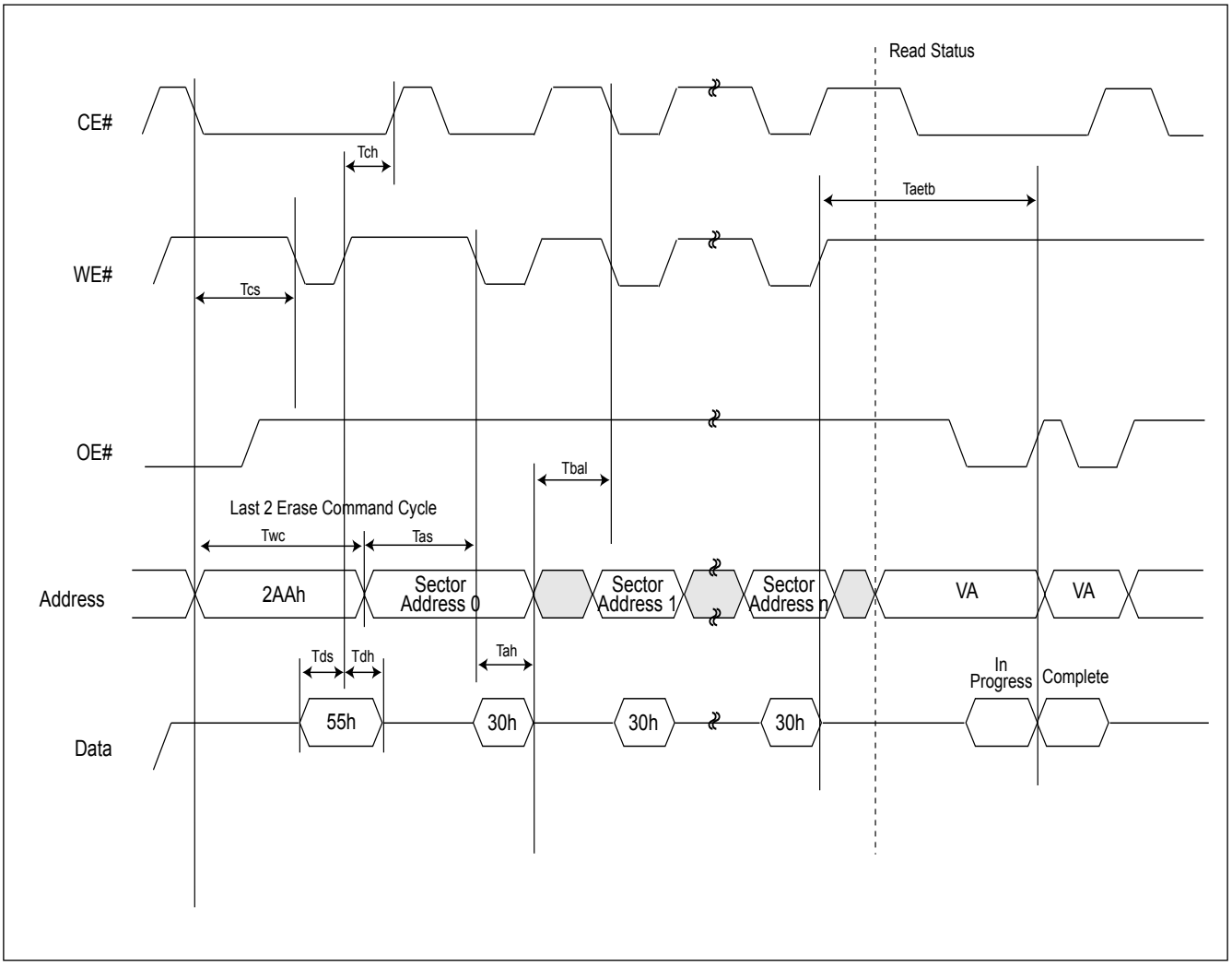


Figure 6. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

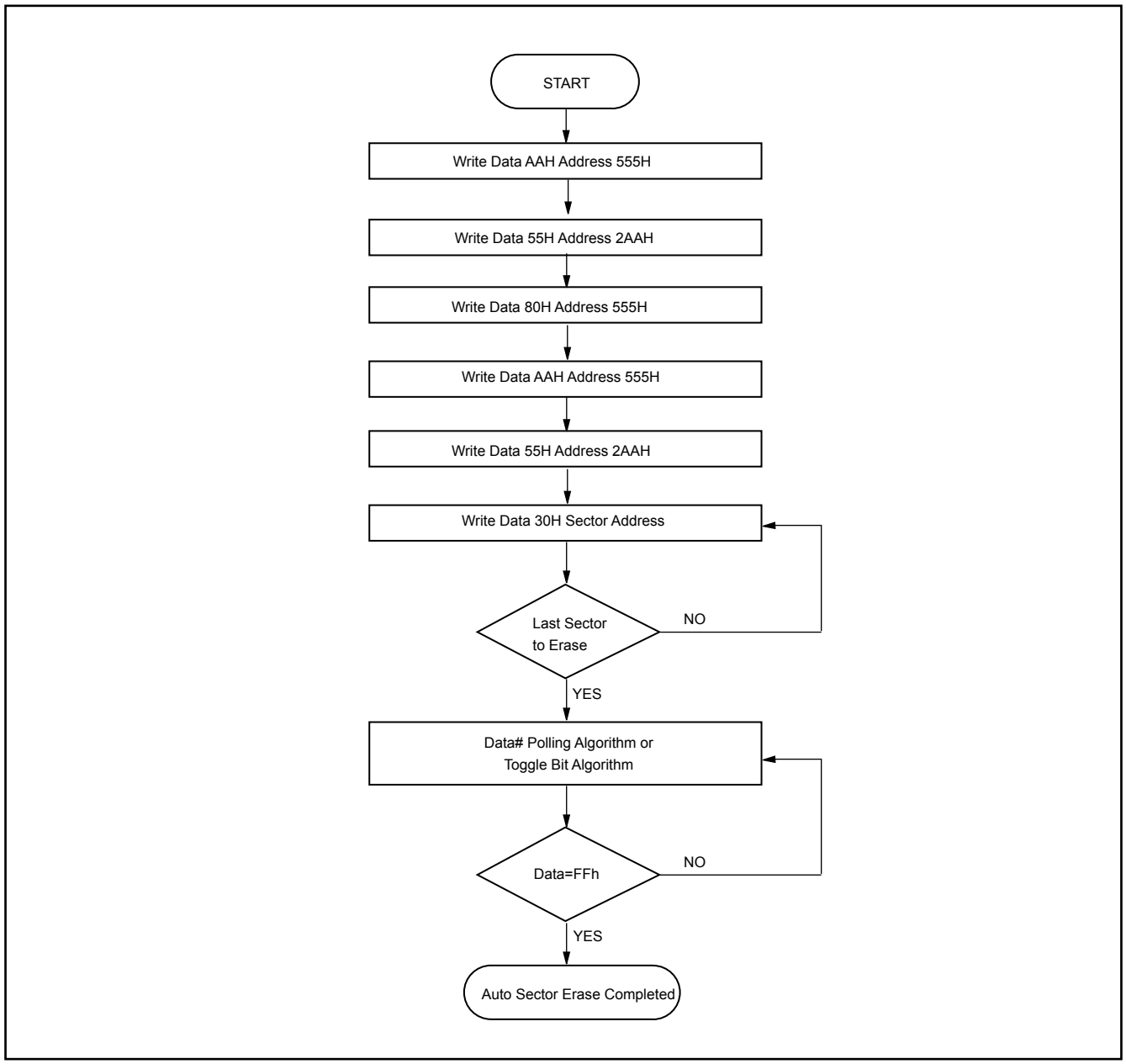


Figure 7. ERASE SUSPEND/RESUME FLOWCHART

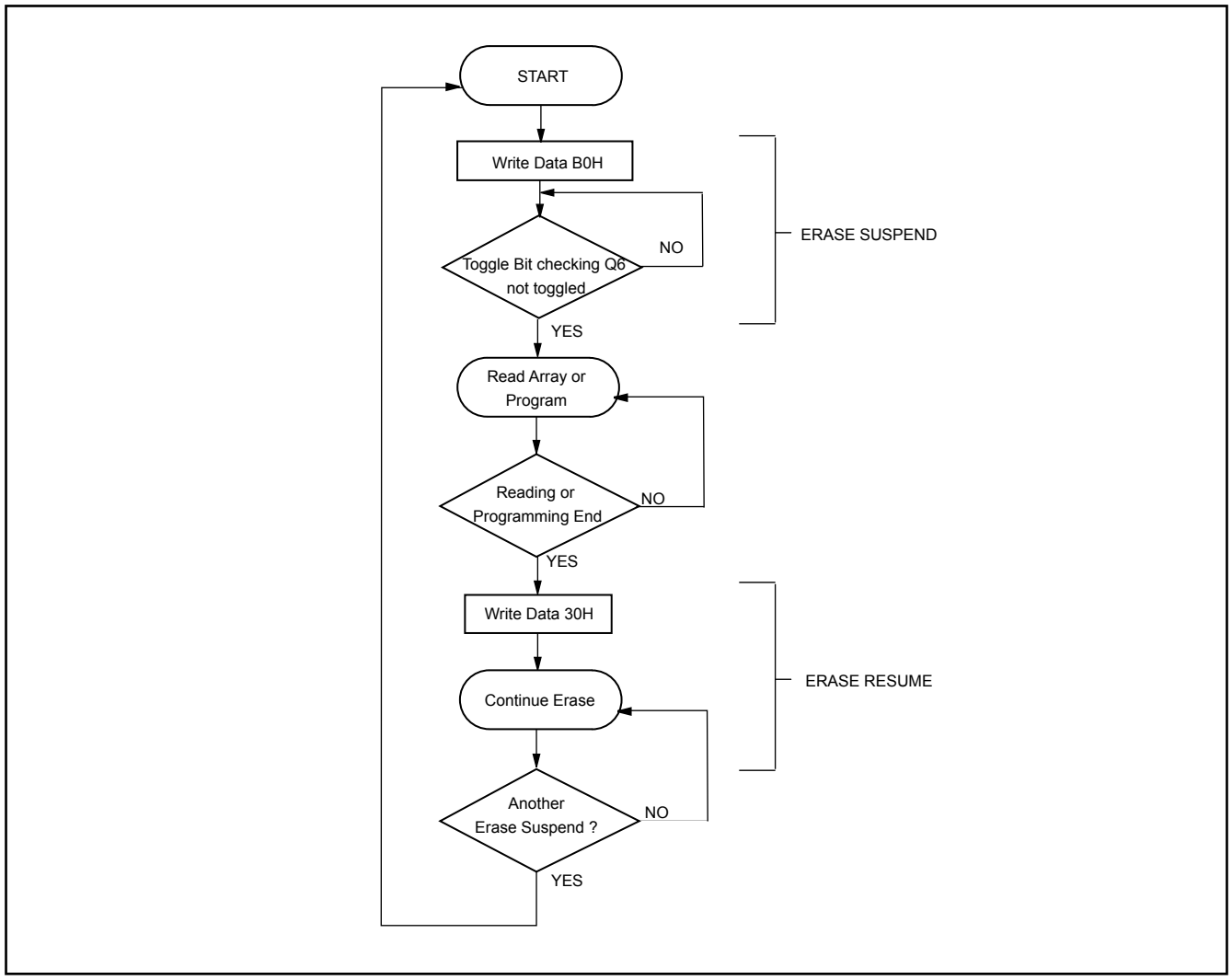


Figure 8. AUTOMATIC PROGRAM TIMING WAVEFORMS

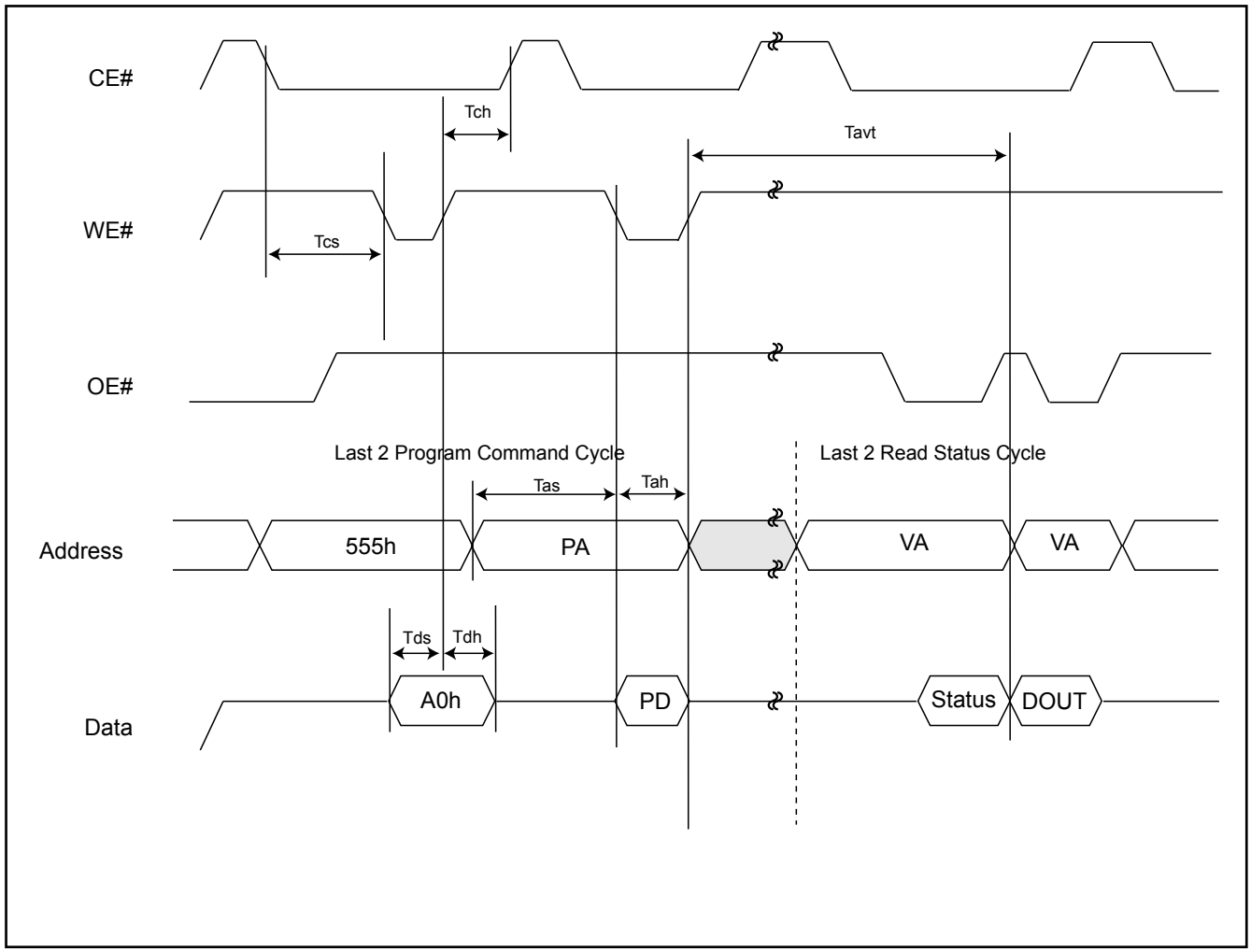


Figure 9. CE# CONTROLLED WRITE TIMING WAVEFORM

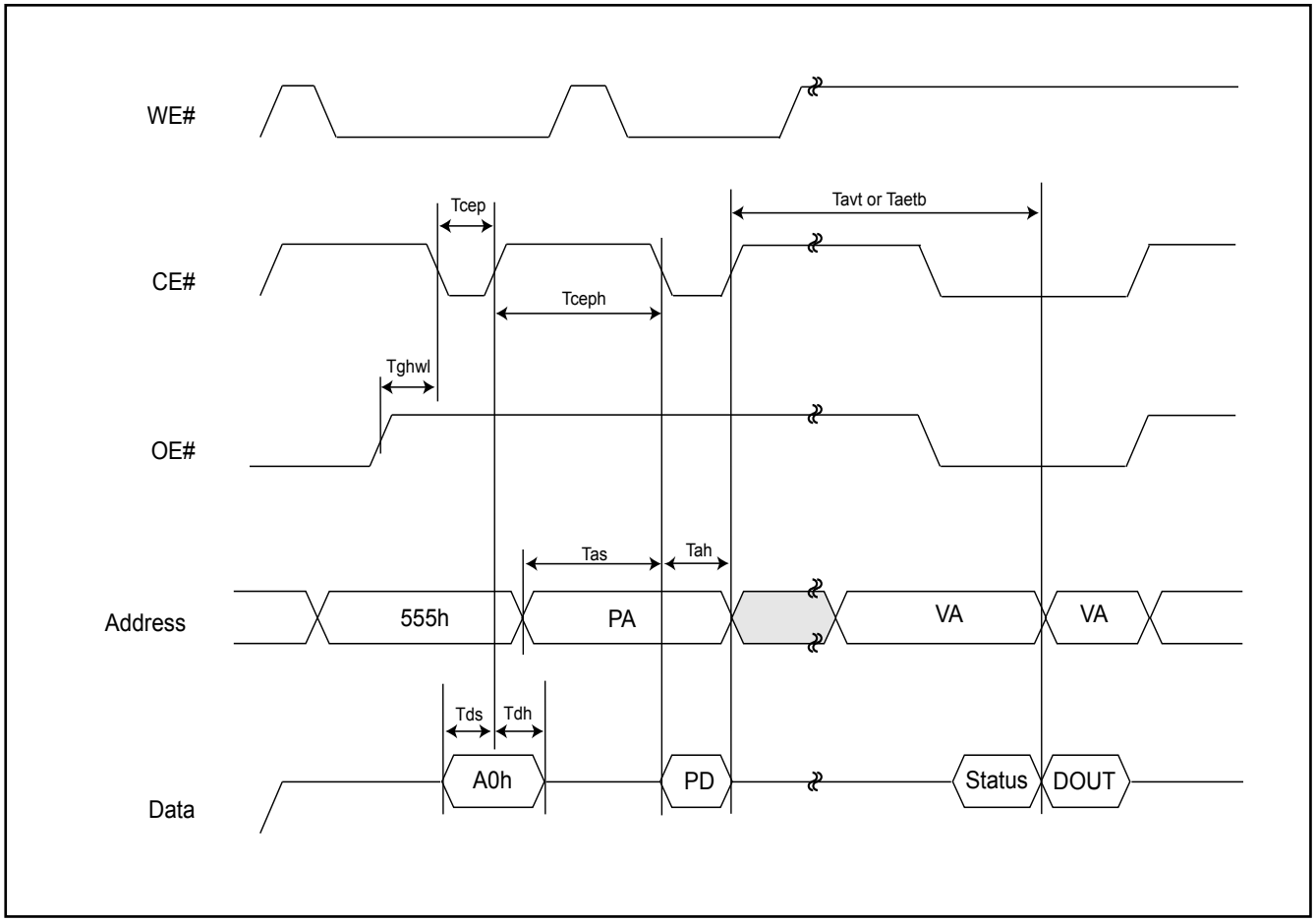


Figure 10. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

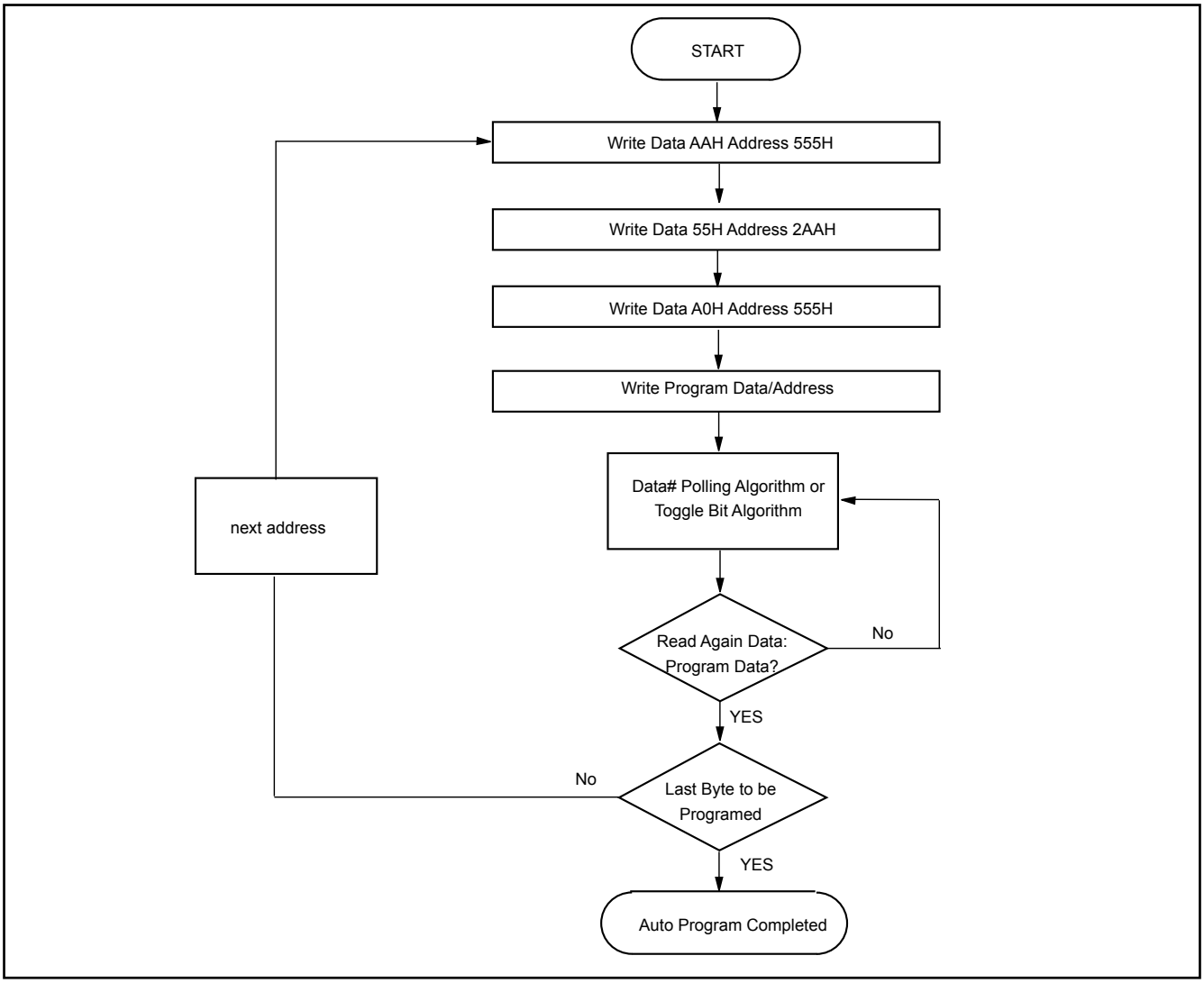
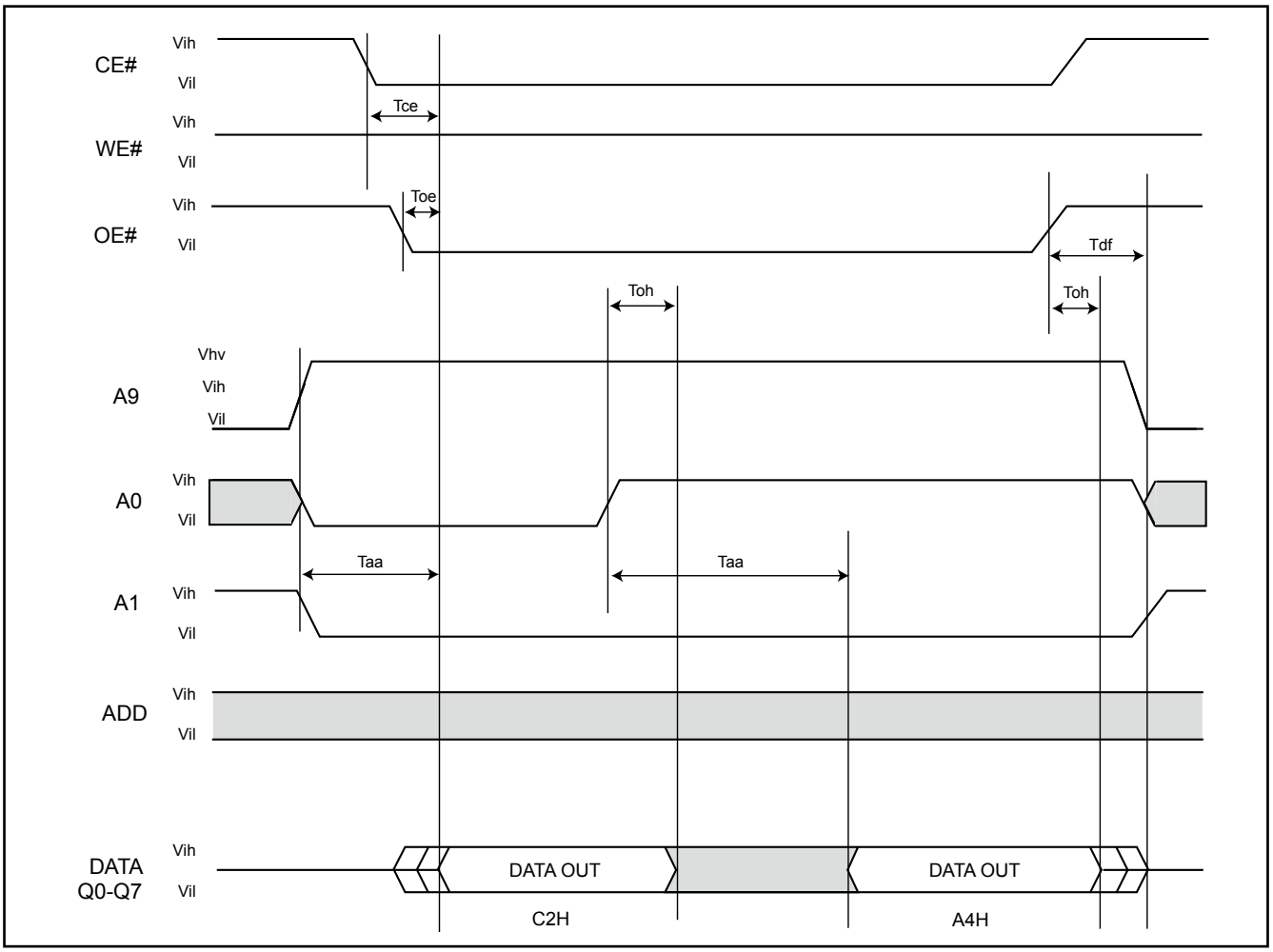


Figure 11. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 12. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

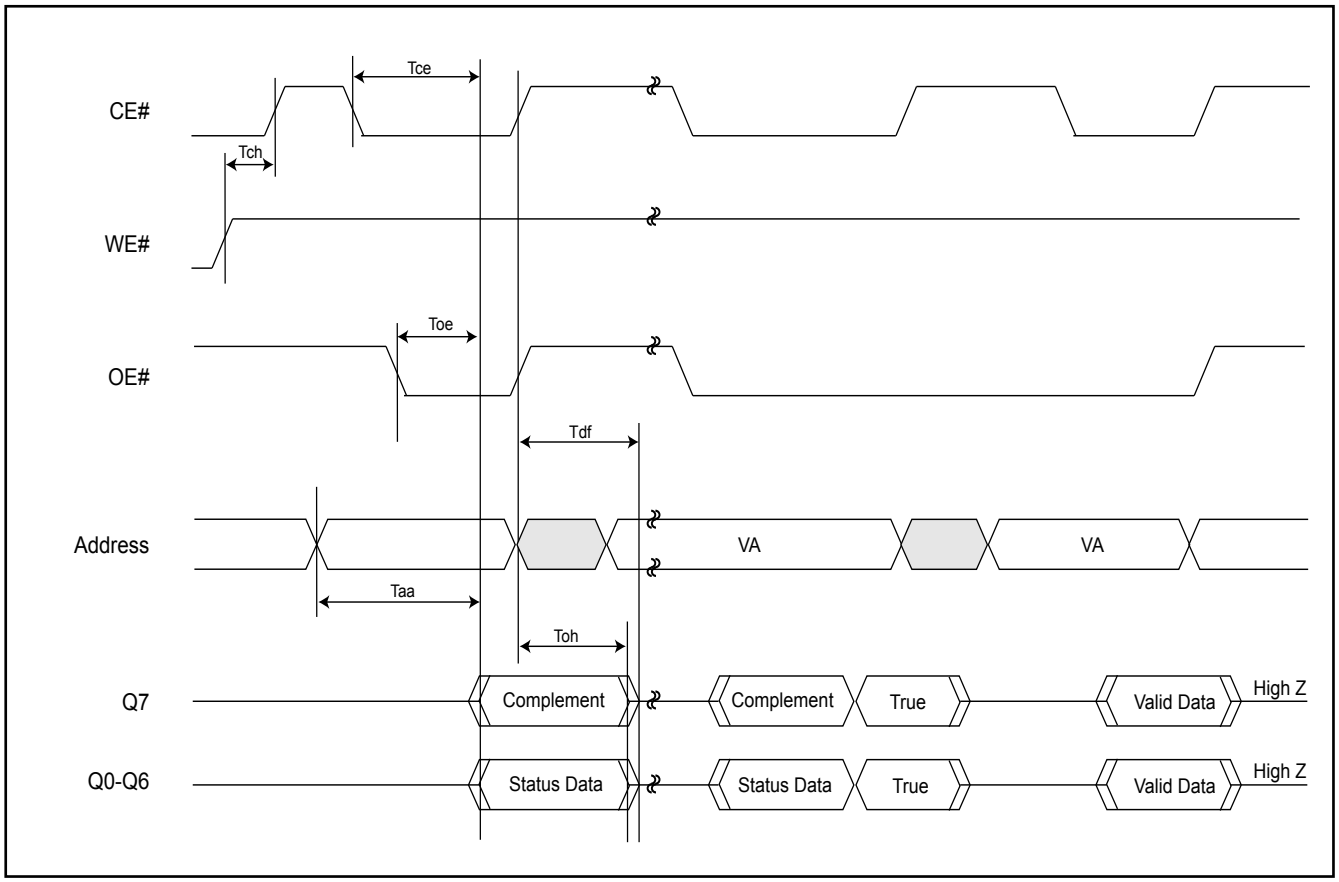
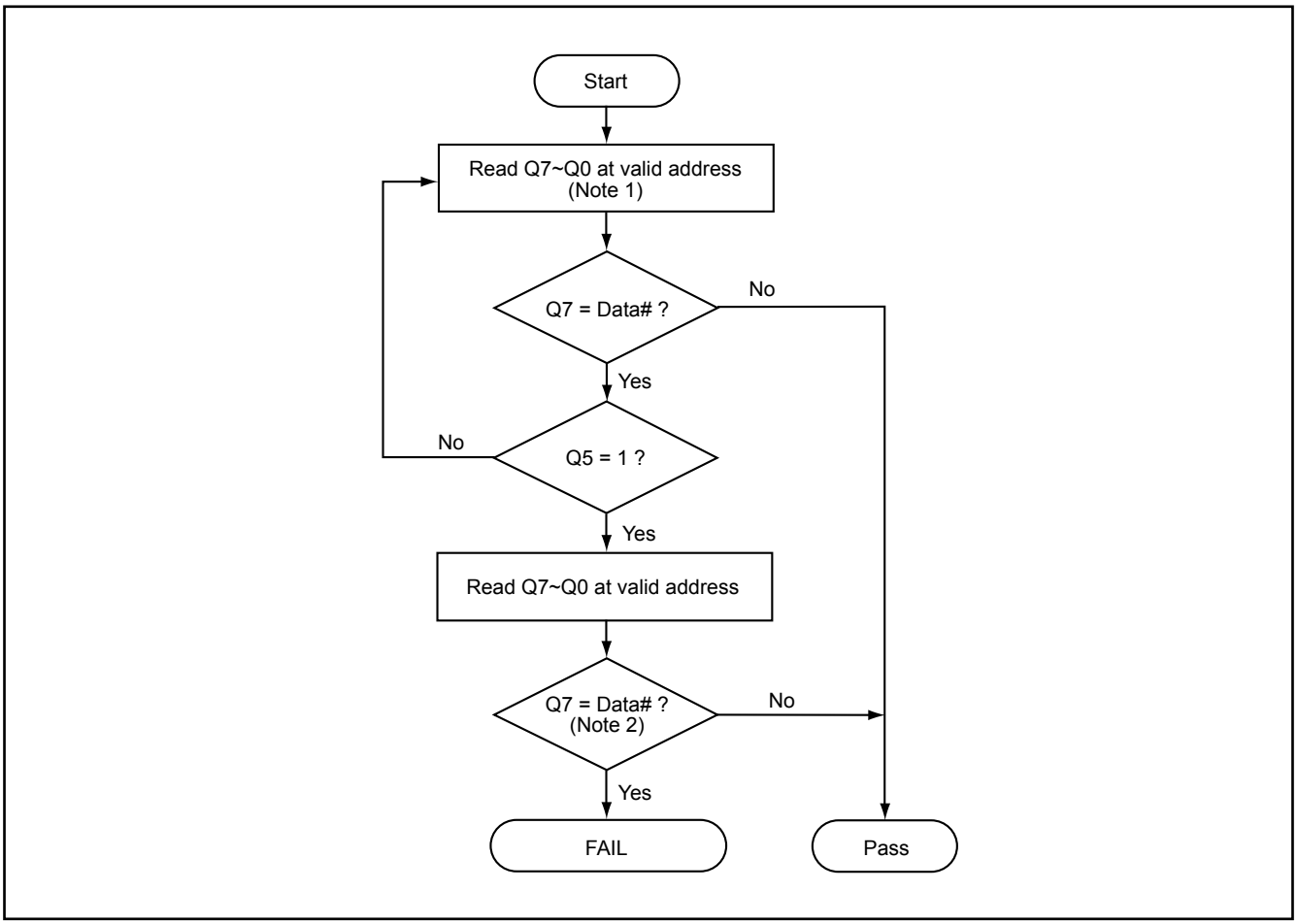
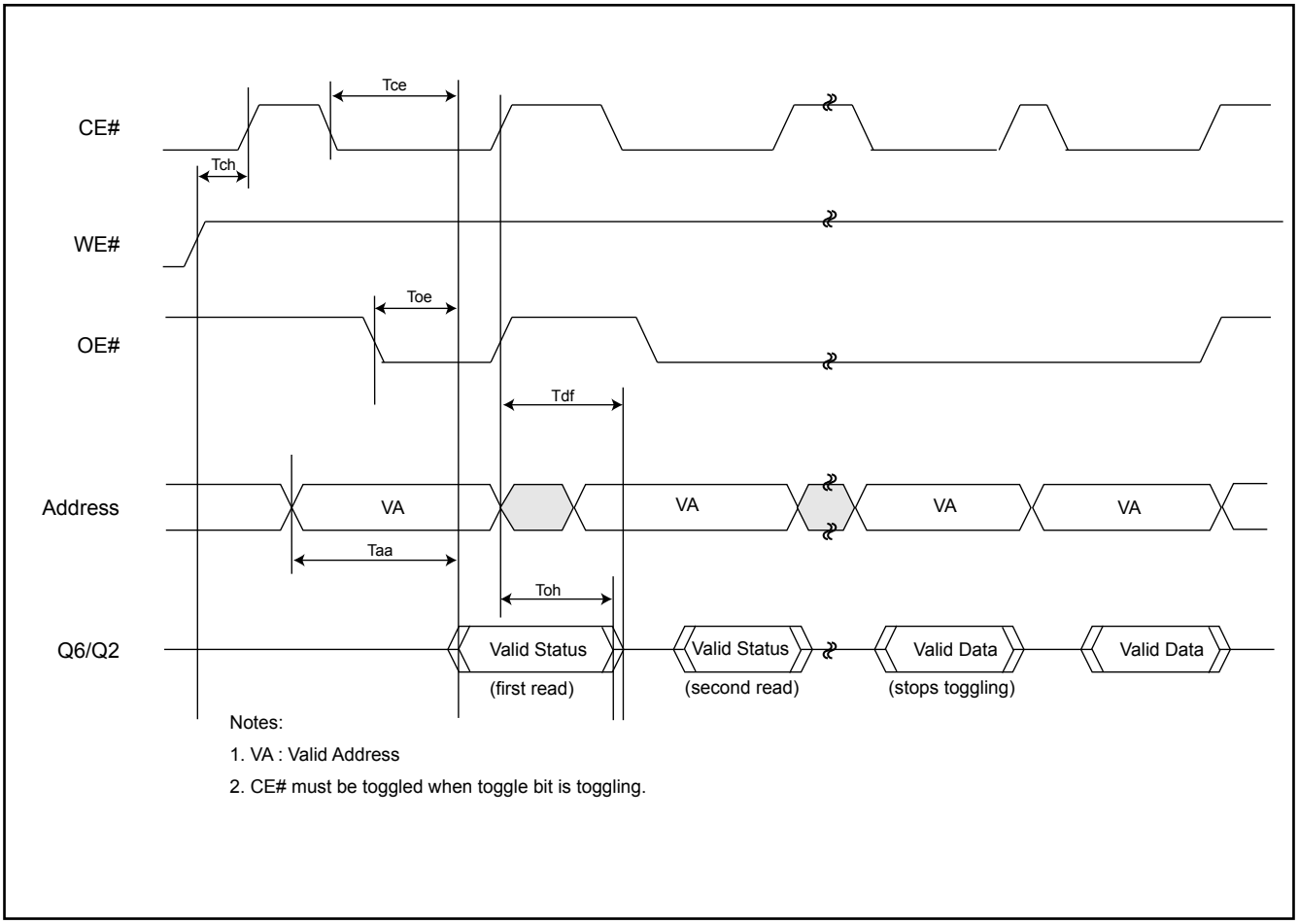


Figure 13. DATA# POLLING ALGORITHM



Notes:
1. For programming, valid address meas program address.
   For erasing, valid address meas erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

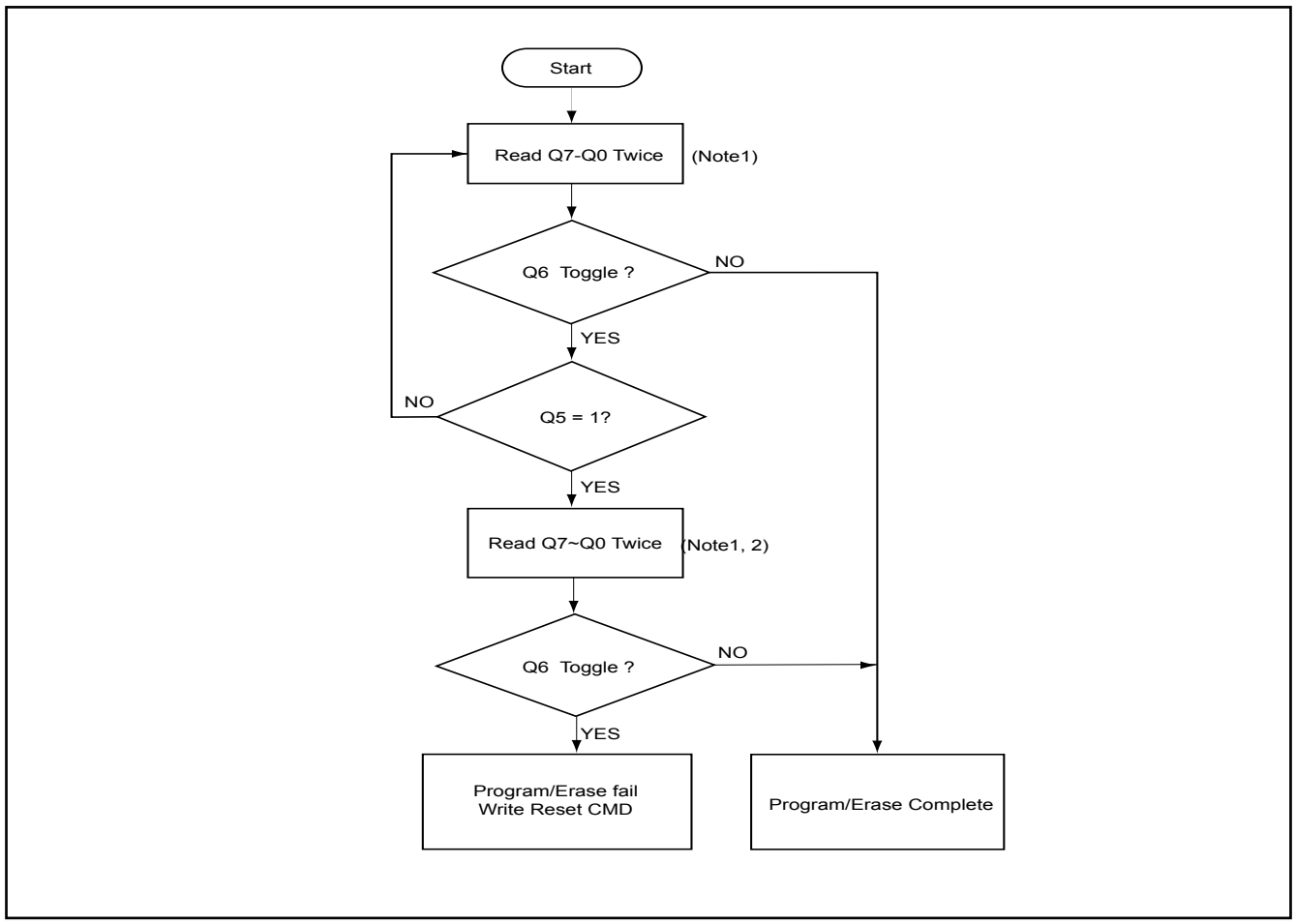
Figure 14. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



Notes:

1. VA : Valid Address
2. CE# must be toggled when toggle bit is toggling.

Figure 15. TOGGLE BIT ALGORITHM



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in *"Figure A. AC Timing at Device Power-Up"* is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

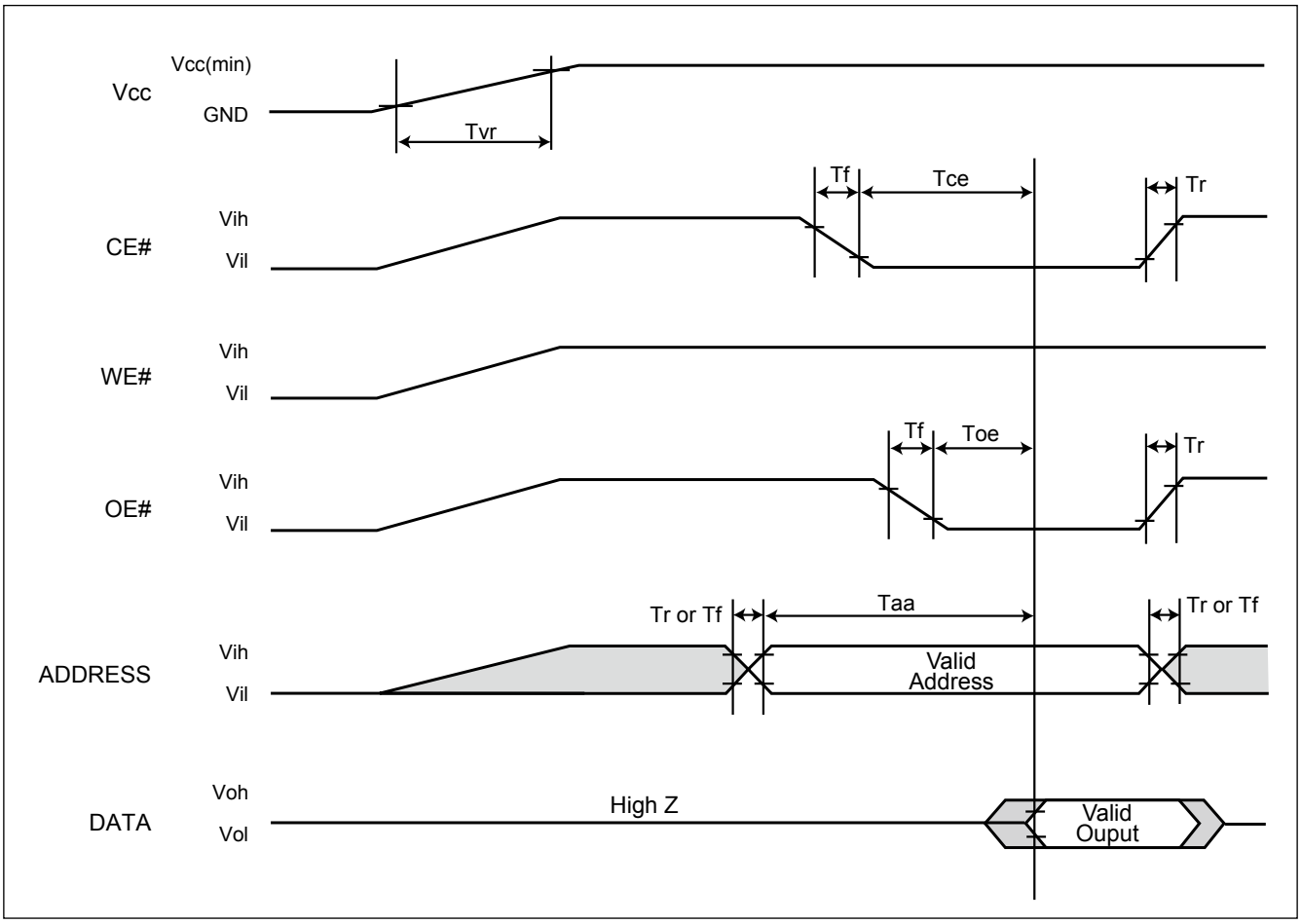


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	uS/V
Tr	Input Signal Rise Time		20	uS/V
Tf	Input Signal Fall Time		20	uS/V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			
	MIN.	TYP.	MAX.	UNITS
Byte Programming Time		9	300	us
Sector Erase Time		0.7	8	sec
Chip Erase Time		4	32	sec
Chip Programming Time		4.5	13.5	sec
Erase/Program Cycles	100,000			Cycles

Note: 1. Typical condition means 25°C, 5V.
2. Maximum condition means 90°C, 4.5V, 100K cycles.

DATA RETENTION

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55˚C	20		years

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage difference with GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage difference with GND on all I/O pins	-1.0V	VCC + 1.0V
Vcc Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 5V, one pin per testing		

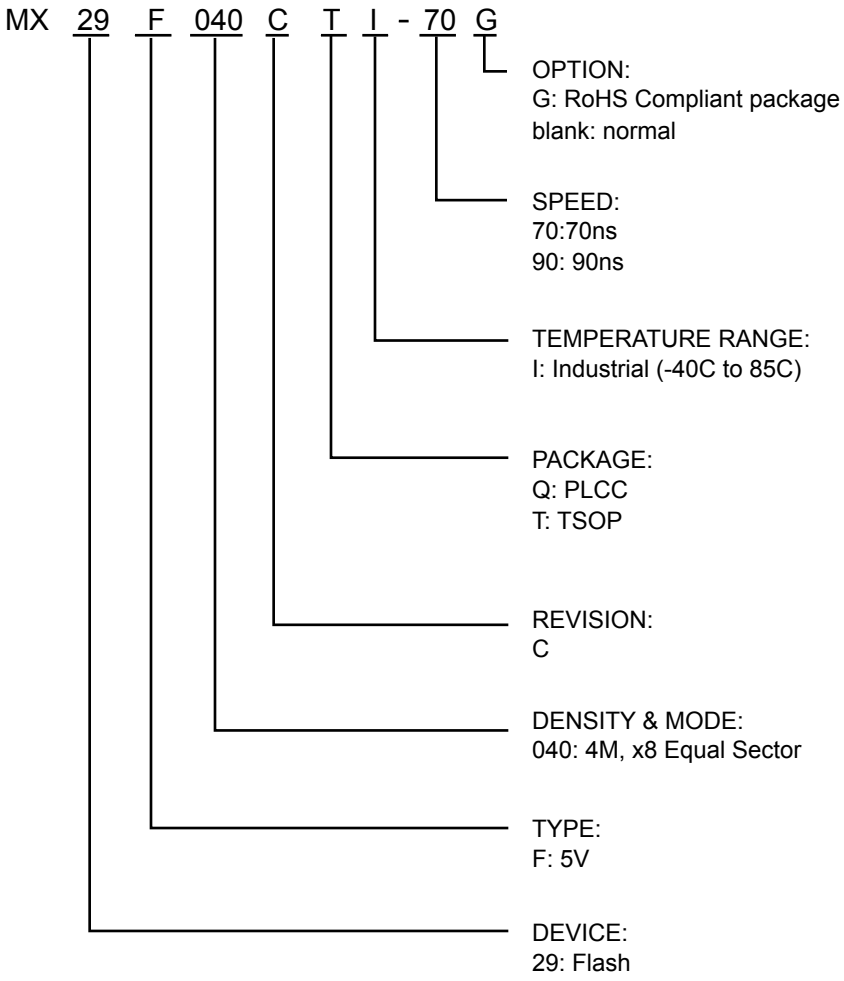
TSOP AND PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0		12	pF
COUT	Output Capacitance	VOUT=0		12	pF
CIN	Input Capacitance	VIN=0		8	pF

ORDERING INFORMATION

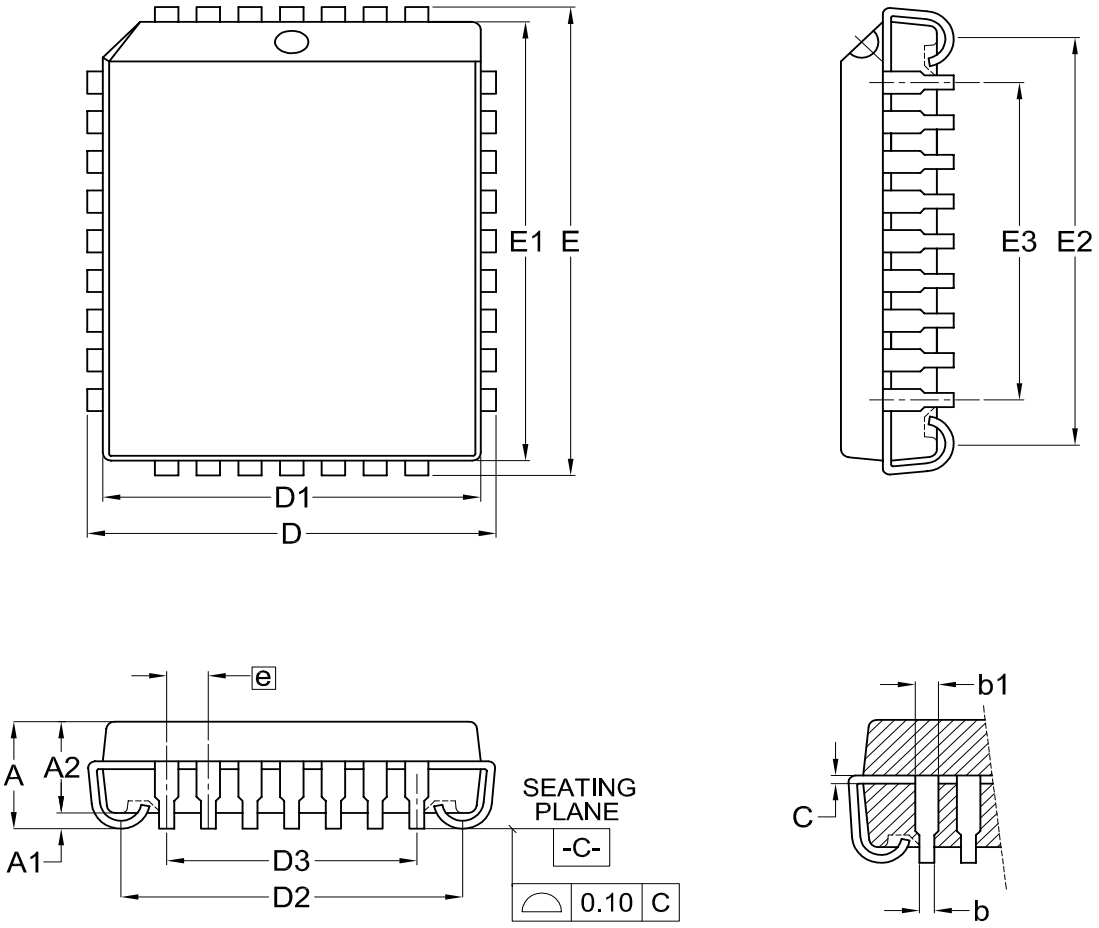
PART NO.	Access Time (ns)	Operating Current MAX.(mA)	Standby Current MAX.(uA)	Temperature Range	PACKAGE	Remark
MX29F040CQC-70G	70	30	5	0°C~70°C	32 Pin PLCC	
MX29F040CQC-90G	90	30	5	0°C~70°C	32 Pin PLCC	
MX29F040CTC-70G	70	30	5	0°C~70°C	32 Pin TSOP (Normal Type)	
MX29F040CTC-90G	90	30	5	0°C~70°C	32 Pin TSOP (Normal Type)	
MX29F040CQI-70G	70	30	5	-40°C~85°C	32 Pin PLCC	
MX29F040CQI-90G	90	30	5	-40°C~85°C	32 Pin PLCC	
MX29F040CTI-70G	70	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	
MX29F040CTI-90G	90	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	

PART NAME DESCRIPTION



PACKAGE INFORMATION

Doc. Title: Package Outline for 32L PLCC

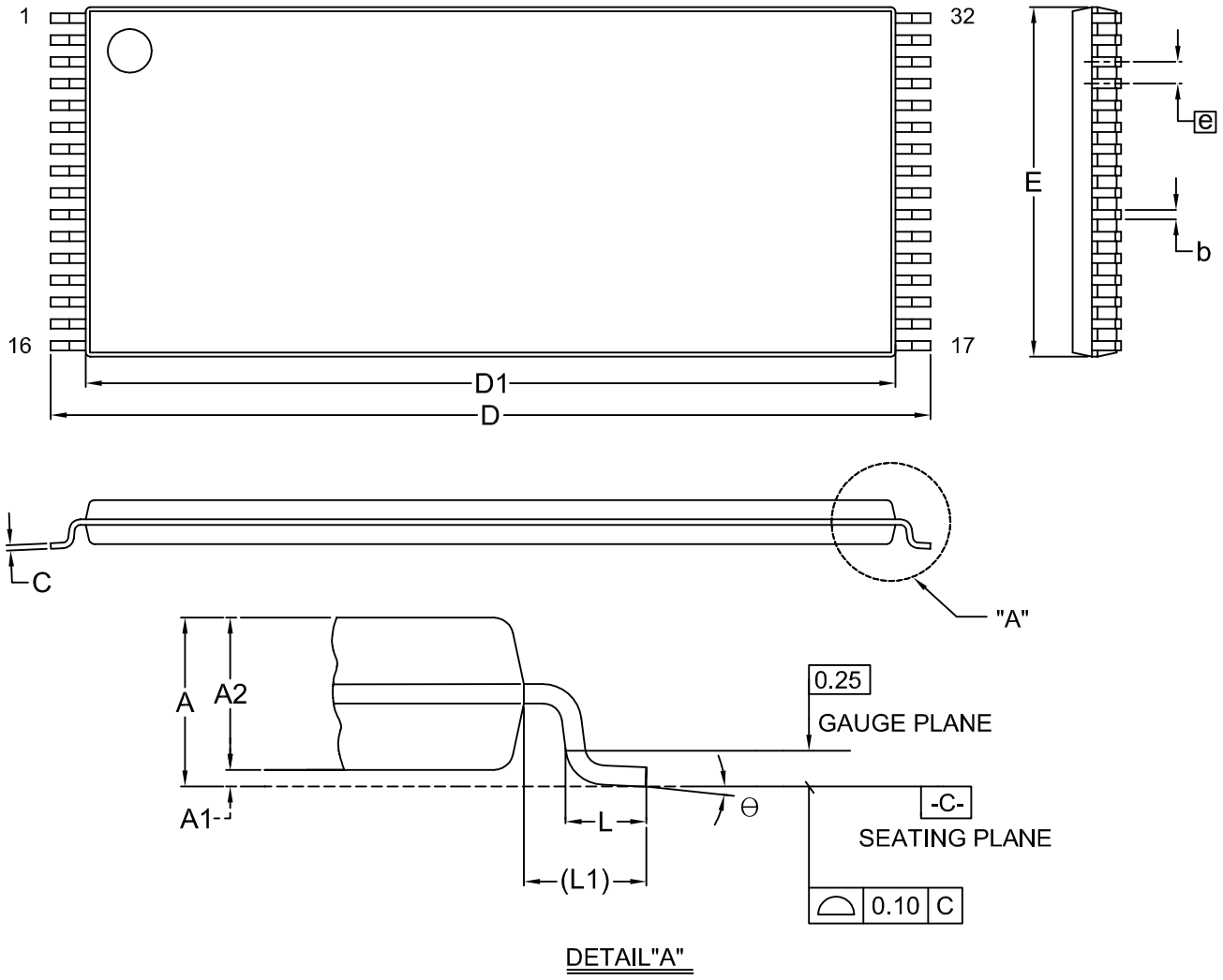


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	—	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	—	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-2002	8	MS-016			

Doc. Title: Package Outline for TSOP(I) 32L (8X20mm)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	—	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1604	10	MO-142			

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary" title	P1	DEC/20/2005
	2. Removed commercial grade	All	
	3. Added access time: 55ns; Removed access time: 120ns	All	
1.1	1. Removed access time: 55ns	P1,13,15,16 P29,30	JUN/21/2006
	2. Removed sector protect/chip unprotect feature	P1,5~7,10,12 P26~29	
	3. Added data# polling, toggle bit algorithm	P20,21	
1.2	1. DataSheet format changed	All	AUG/15/2006
1.3	1. Data modification	All	AUG/17/2006
1.4	1. Added statement	P40	NOV/06/2006
1.5	1. Removed PDIP package option	P1,2,34,35	JAN/18/2007
	2. Added recommedation for non RoHS compliant devices	P1,34	
1.6	1. Added note 1 into *"TABLE 3. MX29F040C COMMAND DEFINITIONS"*	P8	JAN/17/2008
1.7	1. Modified *"Figure 9. CE# CONTROLLED WRITE TIMING WAVEFORM"*	P25	FEB/21/2008
1.8	1. Removed non Pb-free EPNs	P1,34,35	SEP/15/2008
	2. Added C-grade EPNs	P34,35	
1.9	1. Modified Figure 10. CE# Controlled Write Timing Waveform (Changed "Twhwh1 or Twhwh2" into "Tavt or Taetb")	P25	MAR/09/2009
	2. Modified *"Figure 12. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)"*	P28	
2.0	1. Added Note of maximum/minimum voltage during transition into DC characteristics	P13	MAY/26/2009
	2. Added DC: Icw spec and modify Max. Icr1	P14	
	3. Added AC: Twp/Twph/Tghwl spec	P16	
2.1	1. Added *"DATA RETENTION"* table	P33	JUN/30/2009
	2. Modified the sector erase time max from 15s to 8s	P16,33	
2.2	1. Modified description for RoHS compliance	P1,36,37	DEC/04/2012
	2. Modified Output Load Capatitance	P17	

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