RoHS
2002/95/EC

NTE5368
Silicon Controlled Rectifier (SCR)
for High Speed Switching,
135 Amp, TO83

Absolute Maximum Ratings: (T_J = +125°C unless otherwise specified)

Repetitive Peak Voltages, V_{DRM}, V_{RRM} 600V

Non–Repetitive Peak Reverse Blocking Voltage, V_{RSM} 700V

Average On–State Current (180° Conduction, Half Sine Wave, T_C = +85°C), $I_{T(AV)}$ 85A

RMS On–State Current (DC, T_C = +77°C), $I_{T(RMS)}$ 135A

Continuous On–State Current, I_T 175A

Peak One Half Cycle, Non–Repetitive Surge Current, I_{TSM}
  (No Voltage Reapplied, Sinusoidal Half Wave)
    t = 10ms 2450A
    t = 8.3ms 2560A
  (100% V_{RRM} Reapplied, Sinusoidal Half Wave)
    t = 10ms 2060A
    t = 8.3ms 2160A

Maximum I^2t for Fusing, I^2t
  (No Voltage Reapplied, Sinusoidal Half Wave)
    t = 10ms .... $30KA^2s$
    t = 8.3ms .... $27KA^2s$
  (100% V_{RRM} Reapplied, Sinusoidal Half Wave), I^2t
    t = 10ms .... $21KA^2s$
    t = 8.3ms .... $19KA^2s$

Maximum $I^2\sqrt{t}$ for Fusing (t = 0.1 to 10ms, No Voltage Reapplied), $I^2\sqrt{t}$ .... $300KA^2\sqrt{s}$

Max. Peak Positive Gate Current ($t_p \leq$ 5ms), I_{GM} 5A

Max. Peak Positive Gate Voltage ($t_p \leq$ 5ms), $+V_{GM}$ 20V

Max. Peak Negative Gate Voltage ($t_p \leq$ 5ms), $-V_{GM}$ 5V

Average Gate Power (f = 50Hz, d% = 50), $P_{G(AV)}$ 5W

Max. Peak Gate Power (f = 50Hz, d% = 50), P_{GM} 40W

Max. Critical Rate of Rise of Off–State Voltage (To 80% V_{DRM}), dv/dt 500V/μs

Max. Non–Repetitive Rate of Rise of Turned On Current, di/dt
  (V_{DRM} = 600V, I_{TM} = 2 x di/dt) 1000A/μs

Operating Temperature Range, T_{hs} .... −40° to +125°C

Storage Temperature Range, T_{stg} .... −40° to +150°C

Thermal Resistance, Junction–to–Case, R_{thJC}
  (DC Operation) 0.195K/W

Thermal Resistance, Case–to–Heatsink, R_{thCS}
  (Mounting surface, smooth, flat and greased) 0.08K/W

Absolute Maximum Ratings (Cont'd): (T_J = +125°C unless otherwise specified)

Max. Peak On–State Voltage (I_{TM} = 300A, t_p = 10ms Sine Wave Pulse), V_{TM} 2.15V
Low Level Threshold Voltage ([16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$]), $V_{T(TO)1}$ 1.46V
High Level Threshold Voltage ([I > π x $I_{T(AV)}$]), $V_{T(TO)2}$ 1.52V
Low level Forward Slope Resistance ([16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$]), r_{t1} 2.32mΩ
High level Forward Slope Resistance ([I > π x $I_{T(AV)}$]), r_{t2} 2.34mΩ
Repetitive Peak Off–State Current (Rated V_{DRM} Applied), I_{DRM} 30mA
Repetitive Peak Reverse Current (Rated V_{RRM} Applied), I_{RRM} 30mA
Max. Gate Current (V_A = 12V, R_a = 6Ω, T_J = +25°C), I_{GT} 200mA
Max. Gate Voltage (V_A = 12V, R_a = 6Ω, T_J = +25°C), V_{GT} 3V
Max. Holding Current (I_T > 30A, T_J = +25°C), I_H 600mA
Typical Latching Current (T_J = +25°C, V_A = 12V, R_a = 6Ω, I_G = 1A), I_L 1000mA
Max. DC Gate Current Not to Trigger (Rated V_{DRM} Applied), I_{GD} 20mA
Max. DC Gate Voltage Not to Trigger (Rated V_{DRM} Applied), V_{GD} 0.25V
Typical Delay Time, t_d
      (T_J = +25°C, V_{DM} = 600V, I_{TM} = 50A DC, t_p = 1µs, Resistive Load,
      Gate Pulse: 10V, 5Ω Source) 0.80µs
Max. Turn–Off Time (I_{TM} = 100A, Commutating di/dt = 10A/µs, V_R = 50V, t_p = 200µs), t_q . . . 10–20µs
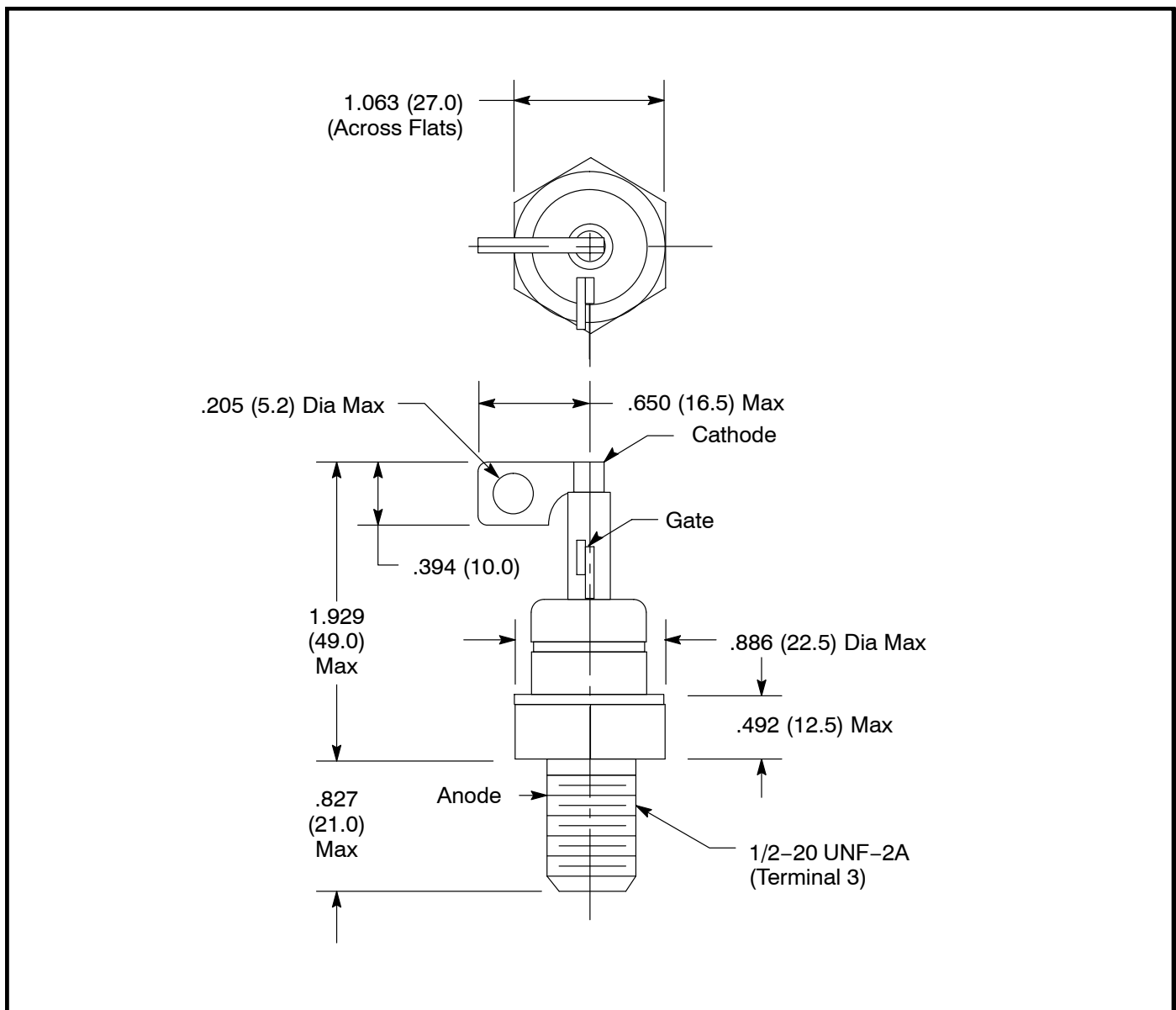
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