ELECTRONICS, INC.
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NTE5380
Silicon Controlled Rectifier (SCR) for High Speed Switching, 600V, 400 Amp, TO200AB

Absolute Maximum Ratings:

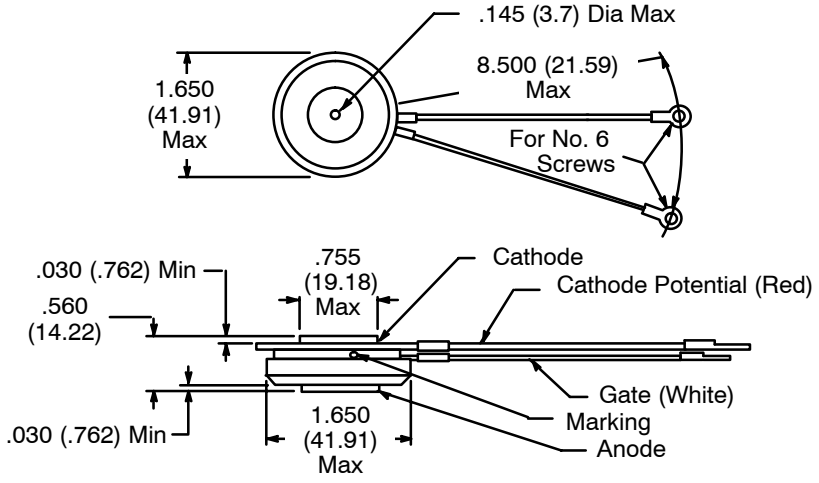
Maximum Repetitive Peak Voltage, V_{DRM}, V_{RRM} 800V
Maximum Non–Repetitive Peak Voltage, V_{RSM} 900V
Repetitive Peak Off–State Current (T_J = +125°C), I_{DRM}, I_{RRM} 40mA
Maximum Operating Temperature Range, T_J . . . . . –40° to +125°C
Storage Temperature Range, T_{stg} . . . . . –40° to +150°C
Maximum Thermal Resistance, Junction–to–Heatsink, R_{thJHS}
DC Operation Single Side Cooled 0.17K/W
DC Operation Double Side Cooled 0.08K/W
Maximum Thermal Resistance, Case–to–Heatsink, R_{thCHS}
DC Operation Single Side Cooled 0.033K/W
DC Operation Double Side Cooled 0.017K/W
Mounting Torque (±10%), F 4900N (500Kg)

Electrical Characteristics:

Parameter	Symbol	Test Conditions			Rating	Unit
On–State Conduction						
Max. Average On–State Current at Heatsink Temperature	$I_{T(AV)}$	180° Conduction, Half Sine Wave		Single Side Cooled, +85°C	130	A
				Double Side Cooled, +55°C	370	A
Max. RMS On–State Current	$I_{T(RMS)}$	DC @ +25°C Heatsink Temperature, Double Side Cooled			690	A
Max. Peak, One Half Cycle, Non–Repetitive Surge Current	I_{TSM}	t = 10ms	No Voltage Reapplied	Sinusoidal Half Wave, Initial T_J = +125°C	4900	A
		t = 8.3ms			5130	A
		t = 10ms	100% V_{RRM} Reapplied		4120	A
		t = 8.3ms			4310	A
Max. I^2t for Fusing	I^2t	t = 10ms	No Voltage Reapplied	Sinusoidal Half Wave, Initial T_J = +125°C	120	KA^2s
		t = 8.3ms			110	KA^2s
		t = 10ms	100% V_{RRM} Reapplied		85	KA^2s
		t = 8.3ms			78	KA^2s
Max. Peak On–State Voltage	V_{TM}	I_{TM} = 600V, T_J = +125°C, t_p = 10ms Sine Wave Pulse			1.8	V
Threshold Voltage, Low Level	$V_{T(TO)1}$	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = +125°C			1.40	V
Threshold Voltage, High Level	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), T_J = +125°C			1.45	V

Electrical Characteristics (Cont'd):

Parameter	Symbol	Test Conditions	Rating	Unit
On−State Conduction (Cont'd)				
Forward Slope Resistance, Low Level	r_{t1}	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = +125°C	0.67	mΩ
Forward Slope Resistance, High Level	r_{t2}	(I > π x $I_{T(AV)}$), T_J = +125°C	0.58	mΩ
Maximum Holding Current	I_H	T_J = +25°C, I_T > 30A	600	mA
Typical Latching Current	I_L	T_J = +25°C, V_A = 12V, R_a = 6Ω, I_G = 1A	1000	mA
Switching				
Max. Non−Repetitive Rate of Rise of Turned−On Current	di/dt	T_J = +125°C, V_{DRM} = 600V, I_{TM} = 2 x di/dt	1000	A/µs
Typical Delay Time	t_d	T_J = +125°C, V_{DRM} = 600V, I_{TM} = 50A DC, t_p = 1µs, Resistive Load, gate Pulse: 10V, 5Ω Source	1.1	µs
Max. Turn−Off Time	t_p	T_J = +125°C, I_{TM} = 30A, Commutating di/dt = 20A/µs, V_R = 50V, t_p = 500µs, dv/dt = 500V/µs	10 – 20	µs
Blocking				
Maximum Critical Rate of Rise of Off−State Voltage	dv/dt	T_J = +125°C, Linear to 80% V_{DRM}	500	V/µs
Max. Peak Reverse and Off−State Leakage Current	I_{RRM}, I_{DRM}	T_J = +125°C, V_{DRM}/V_{RRM} Applied	40	mA
Triggering				
Maximum Peak Gate Power	P_{GM}	T_J = +125°C, f = 50Hz, d% = 50	60	W
Maximum Average Gate Power	$P_{G(AV)}$		10	W
Max. Peak Positive Gate Current	I_{GM}	T_J = +125°C, $t_p \le$ 5ms	10	A
Max. Peak Positive Gate Voltage	$+V_{GM}$	T_J = +125°C, $t_p \le$ 5ms	20	V
Max. Peak Negative Gate Voltage	$-V_{GM}$		5	V
Max. DC Gate Current Required to Trigger	I_{GT}	T_J = +25°C, V_A = 12V, R_a = 6Ω	150	mA
Max. DC Gate Voltage Required to Trigger	V_{GT}	T_J = +25°C, V_A = 12V, R_a = 6Ω	3	V
Max. DC Gate Current not to Trigger	I_{GD}	T_J = +125°C, Rated V_{DRM} Applied	20	mA
Max. DC Gate Voltage not to Trigger	V_{GD}	T_J = +125°C, Rated V_{DRM} Applied	0.25	V



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