

OT408

1 A Four-quadrant triac, high surge capability

Rev. 01 — 30 July 2008

Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate triac in a SOT223 surface-mountable plastic package

1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- High surge capability
- Gate triggering in four quadrants
- Direct interfacing to low power gate drive circuits
- High blocking voltage of 800 V

1.3 Applications

- Home appliances
- Small lamp control
- Low power motor control
- Low power loads in industrial process control

1.4 Quick reference data

- $V_{DRM} \leq 800$ V
- $I_{TSM} \leq 12.5$ A ($t = 20$ ms)
- $I_{T(RMS)} \leq 1$ A
- $I_{GT} \leq 5$ mA
- $I_{GT} \leq 7$ mA (T2– G+)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	main terminal 1 (T1)	<p>SOT223</p>	<p>sym051</p>
2	main terminal 2 (T2)		
3	gate (G)		
4	mounting base; main terminal 2 (T2)		

3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
OT408	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
V_{RRM}	repetitive peak reverse voltage		-	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{sp}} \leq 103\text{ °C}$; see Figure 4 and 5	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j}} = 25\text{ °C}$ prior to surge; see Figure 2 and 3			
		$t = 20\text{ ms}$	-	12.5	A
		$t = 16.7\text{ ms}$	-	13.8	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$	-	0.78	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{TM}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $di_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$			
		T2+ G+	-	50	$\text{A}/\mu\text{s}$
		T2+ G-	-	50	$\text{A}/\mu\text{s}$
		T2- G-	-	50	$\text{A}/\mu\text{s}$
		T2- G+	-	10	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	$^{\circ}\text{C}$
T_{j}	junction temperature		-	125	$^{\circ}\text{C}$

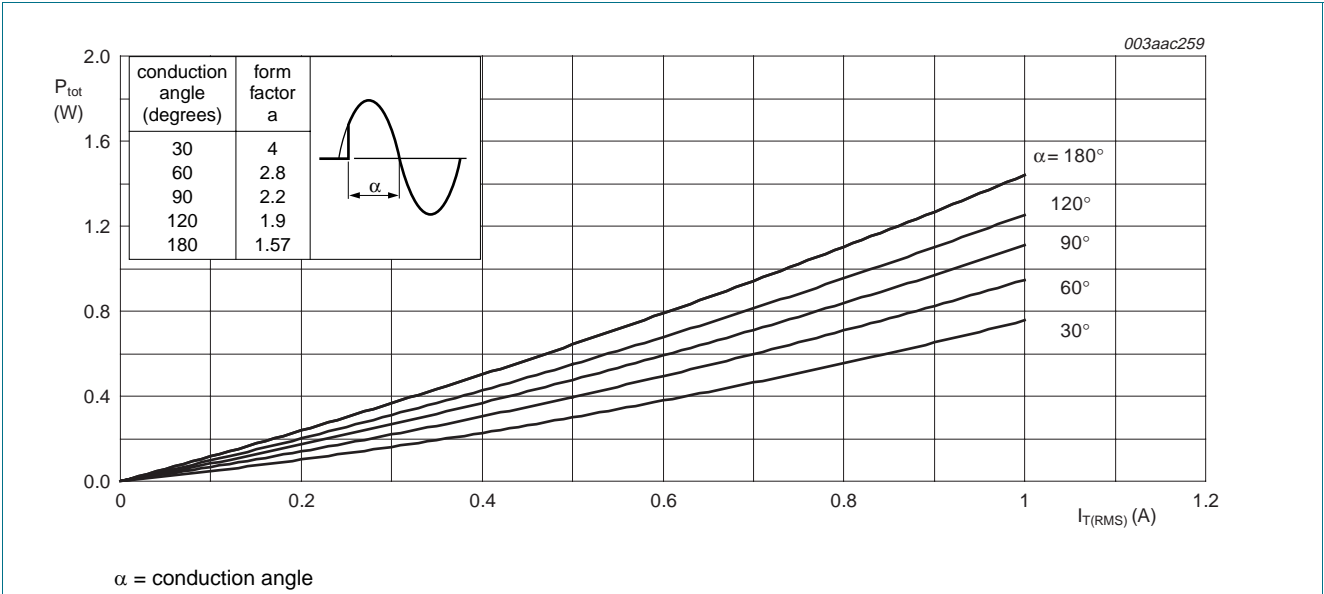


Fig 1. Total power dissipation as a function of RMS on-state current; maximum values

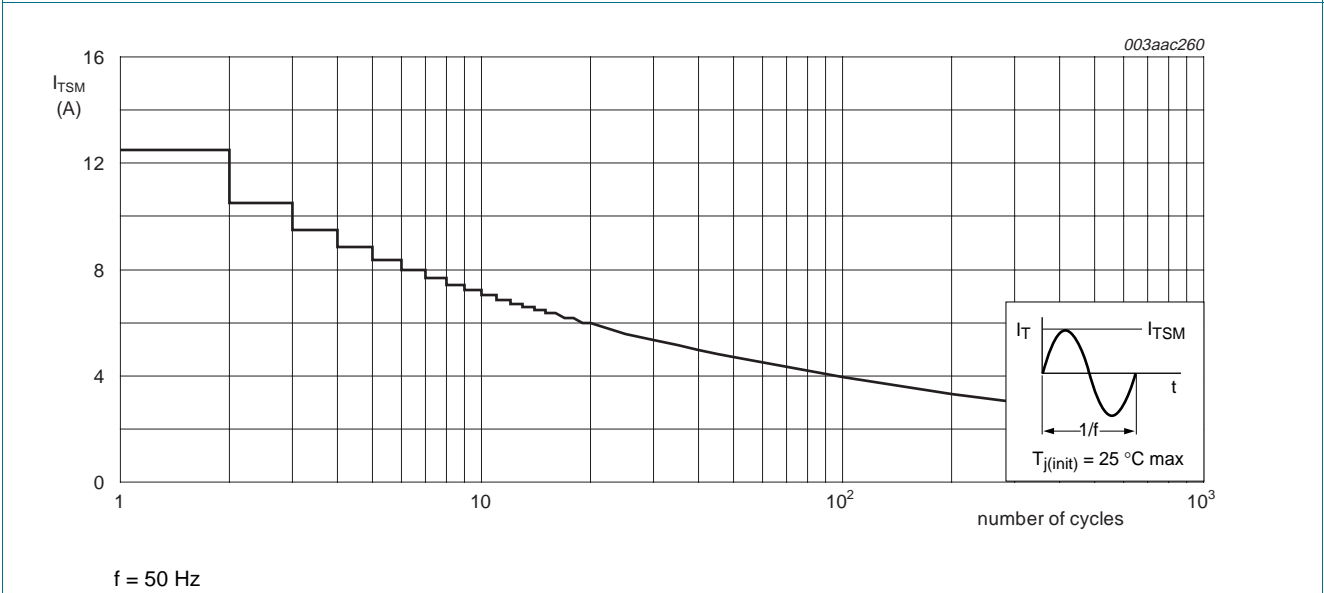


Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

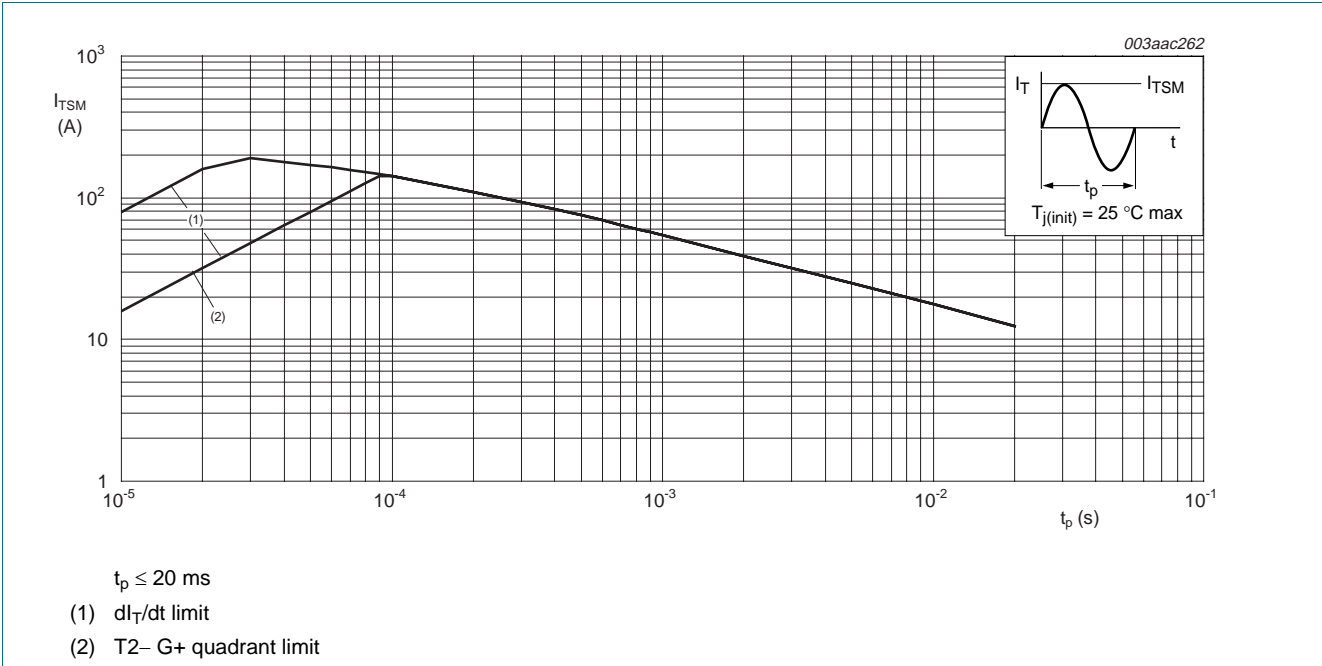


Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

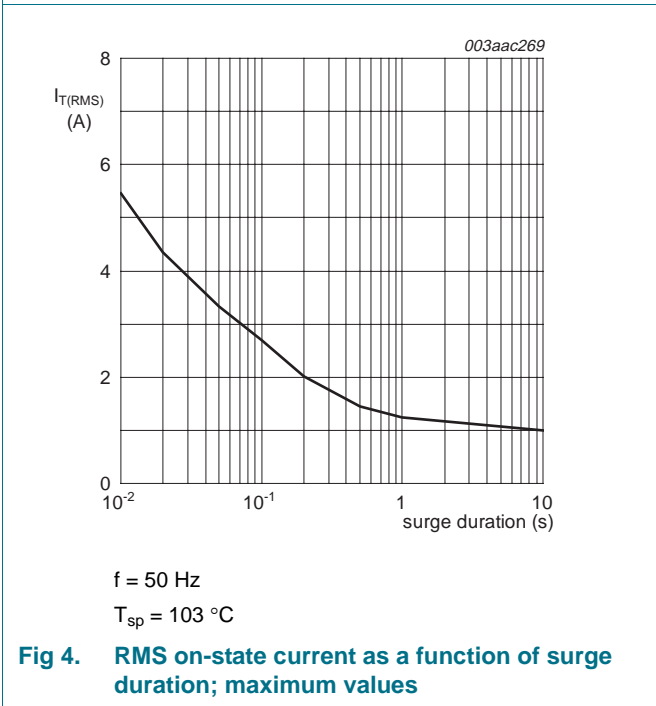


Fig 4. RMS on-state current as a function of surge duration; maximum values

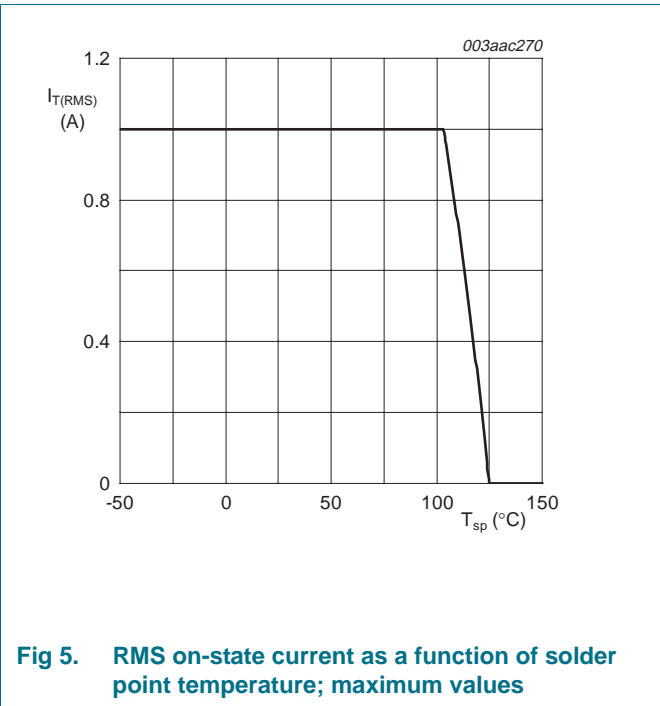


Fig 5. RMS on-state current as a function of solder point temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle; see Figure 6	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle				
		for minimum footprint see Figure 13	-	156	-	K/W
		for pad area see Figure 14	-	70	-	K/W

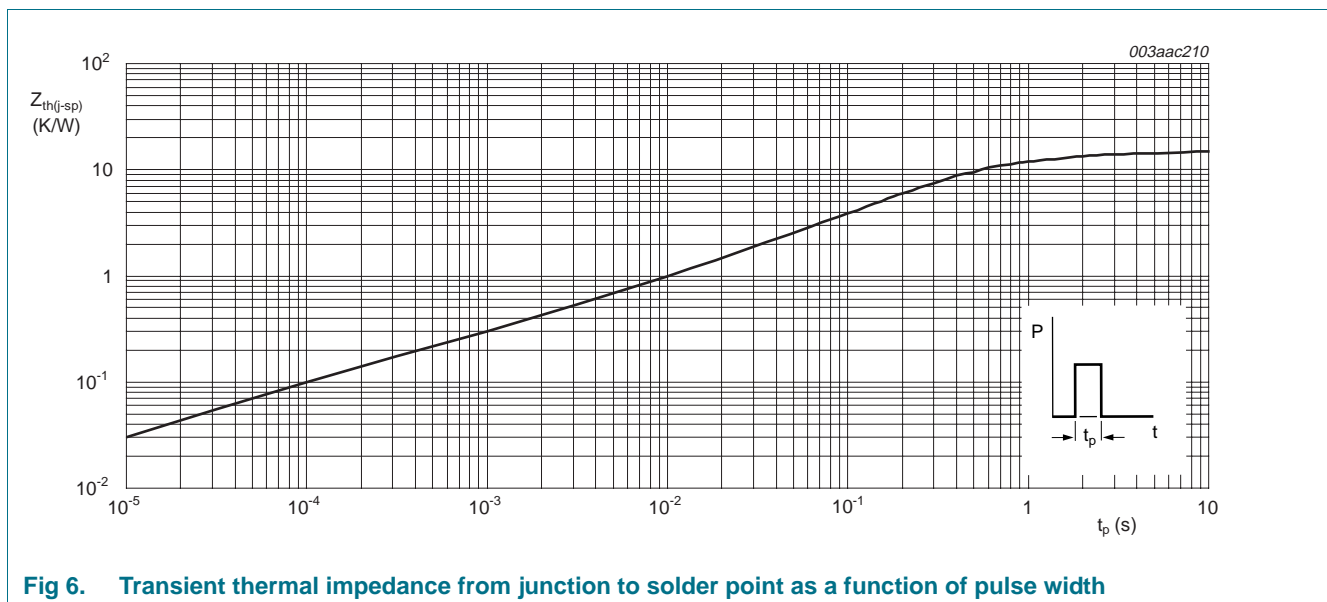


Fig 6. Transient thermal impedance from junction to solder point as a function of pulse width

6. Static characteristics

Table 5. Static characteristics

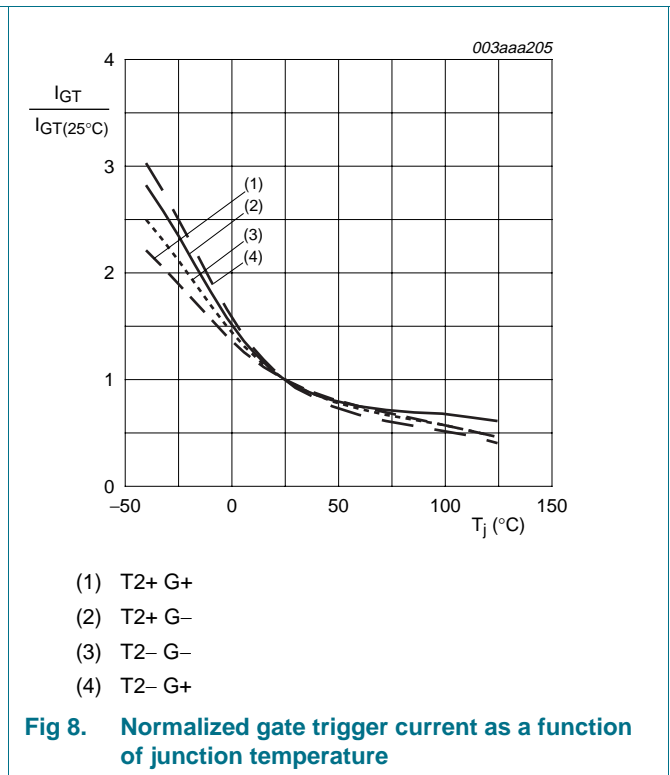
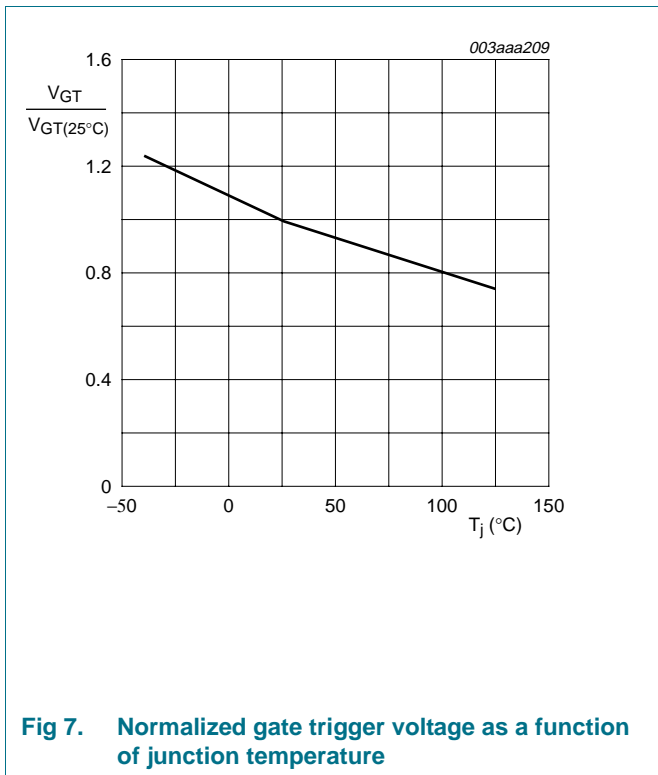
$T_j = 25\text{ °C}$ unless otherwise specified.

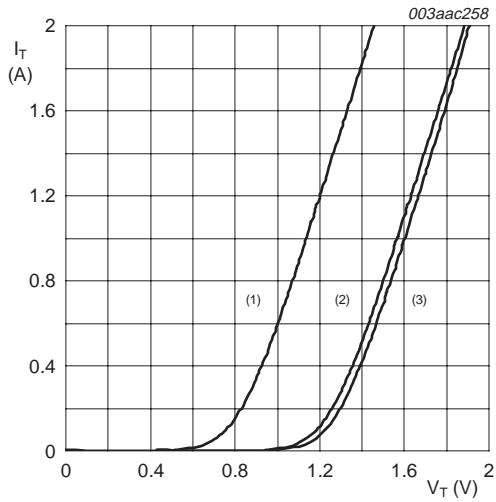
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 8				
		T2+ G+	-	-	5	mA
		T2+ G-	-	-	5	mA
		T2- G-	-	-	5	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; see Figure 10				
		T2+ G+	-	-	10	mA
		T2+ G-	-	-	20	mA
		T2- G-	-	-	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; see Figure 11	-	-	10	mA
		T2- G+	-	-	10	mA
		$I_T = 1\text{ A}$; see Figure 9	-	1.3	1.6	V
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 7	-	-	1.3	V
V_{GT}	gate trigger voltage	$V_D = V_{DRM}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$	0.2	-	-	V
		$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	-	-	0.5	mA

7. Dynamic characteristics

Table 6. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67V_{DRM(max)}$; $T_j = 110\text{ }^\circ\text{C}$; exponential waveform; gate open circuit	20	-	-	V/ μs
dV_{com}/dt	rate of change of commutating voltage	$V_{DM} = 400\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; $I_{TM} = 1\text{ A}$; $di_{com}/dt = 0.44\text{ A/ms}$	1	-	-	V/ μs





- $V_o = 1.254 \text{ V}; R_s = 0.31 \Omega$
- (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
 - (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
 - (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig 9. On-state current as a function of on-state voltage

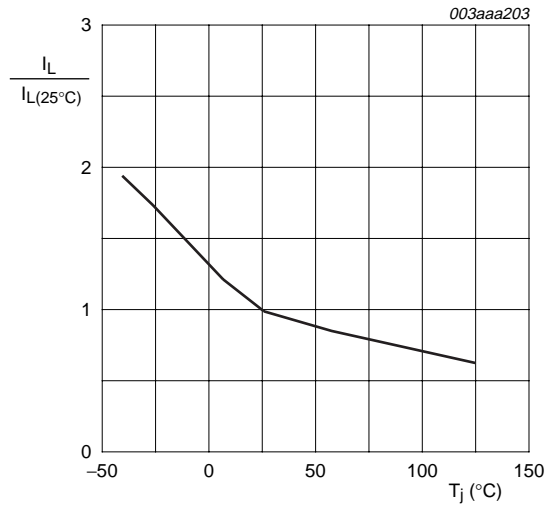


Fig 10. Normalized latching current as a function of junction temperature

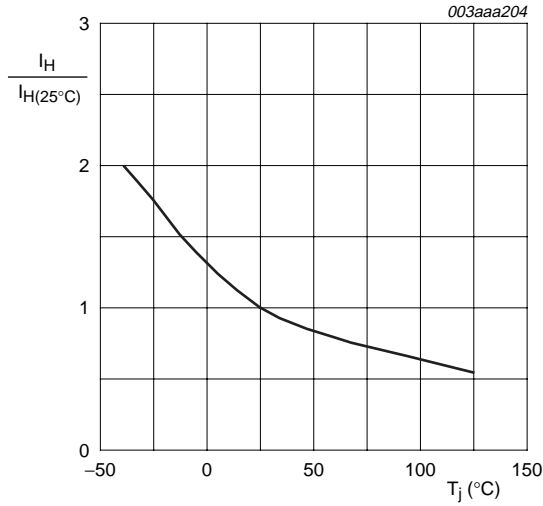


Fig 11. Normalized holding current as a function of junction temperature

8. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

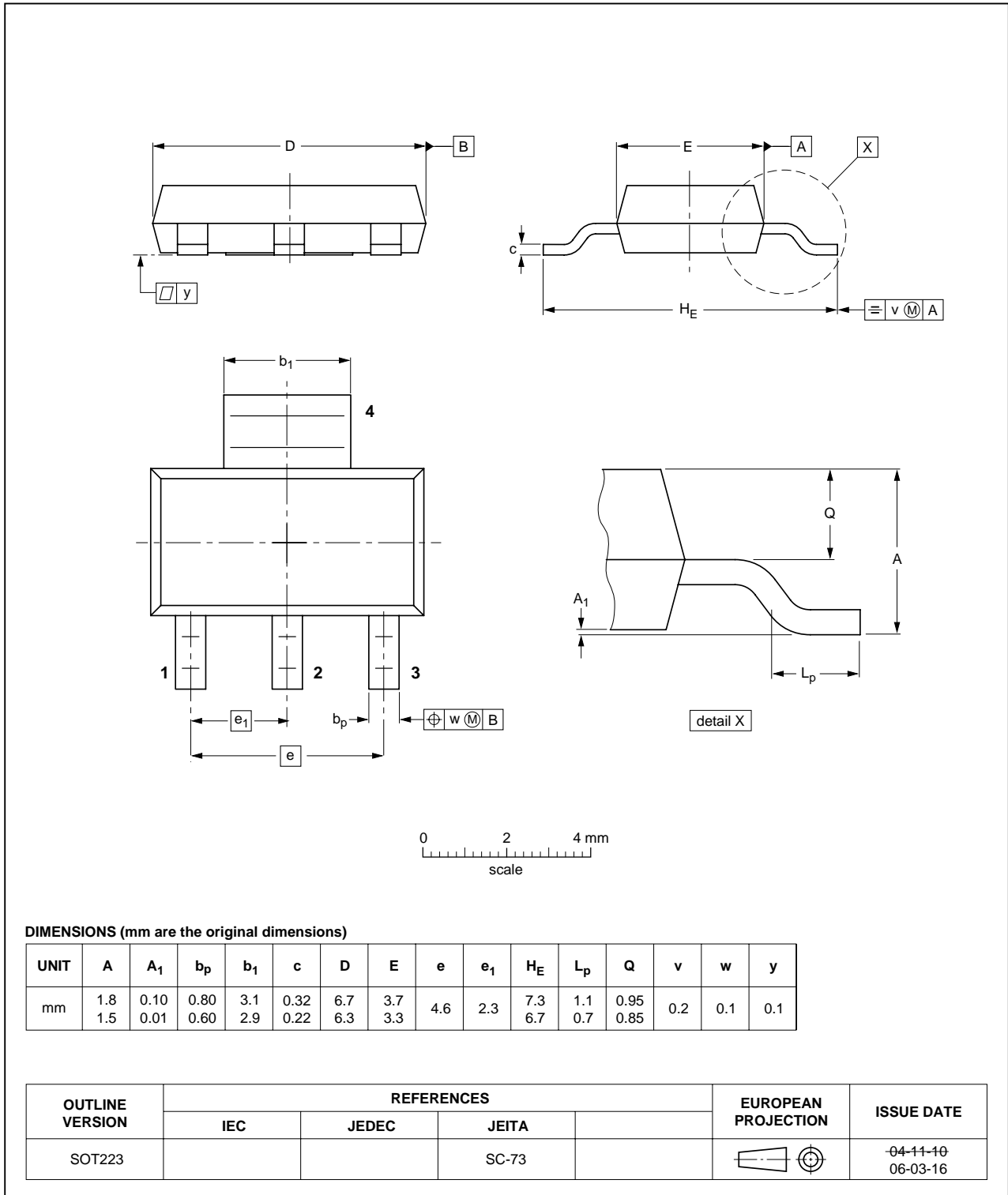
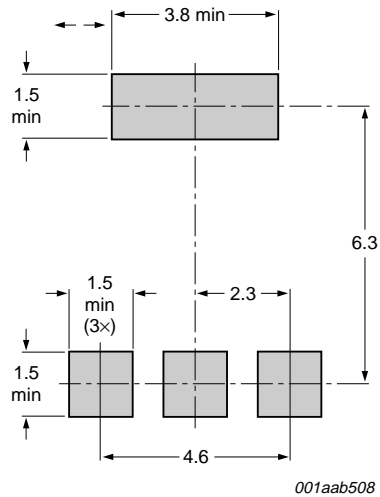


Fig 12. Package outline SOT223 (SC-73)

9. Mounting

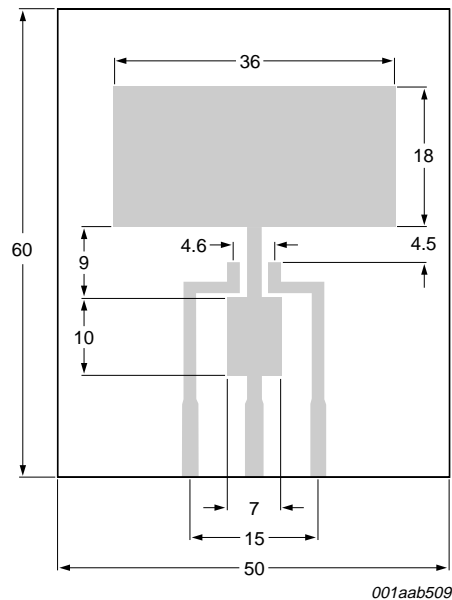
9.1 Mounting instructions



All dimensions are in mm

Fig 13. Minimum footprint SOT223

9.2 Printed-circuit board



All dimensions are in mm

Printed-circuit board: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μ m thick)

Fig 14. Printed-circuit board pad area SOT223

10. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
OT408_1	20080730	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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