PIC16(L)F191XX

LCD Control with Core Independent Peripherals, 28/40/48/64-Pin Microcontroller Product Brief

Description:

PIC16(L)F191XX microcontrollers offer eXtreme Low-Power (XLP) LCD drive coupled with Core Independent Peripherals and Intelligent Analog. They are especially suited for battery powered LCD applications due to an integrated charge pump, high current I/O drive for backlighting, and battery backup of the Real Time Clock/Calendar (RTCC). Active clock tuning of the HFINTOSC provides a highly accurate clock source over voltage and temperature. The family also features new 12-bit ADC^2 automating Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and automatic threshold comparison. Other new features include low-power IDLE and DOZE modes, Device Information Area (DIA), and Memory Access Partition (MAP). These low-power products will be offered in a broad range of pin counts from 28- to 64-pins to support the customer in various LCD and general purpose applications.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - Two 8-bit (TMR2) with Hardware Limit Timer (HLT) Extension
  - 16-bit (TMR0/1)
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software
- Programmable Code Protection

Memory:

- Up to 56 KB Flash Program Memory
- Up to 4 KB Data SRAM Memory
- 256 Bytes DataEE
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Right protect
  - Custom Partition
- Device Information Area (DIA)

Operating Characteristics:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF191XX)
  - 2.3V to 5.5V (PIC16F191XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality:

- **DOZE mode**: Ability to run CPU core slower than the system clock
- **IDLE mode**: Ability to halt CPU core while internal peripherals continue operating
- **Sleep mode**: Lowest power consumption
- **Peripheral Module Disable (PMD)**: Ability to disable hardware module to minimize power consumption of unused peripherals

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 µA @ 32 kHz, 1.8V, typical
  - 32 µA/MHz @ 1.8V, typical

Digital Peripherals:

- LCD Controller:
  - Up to 360 segments
  - Charge pump for low-voltage/current operation
  - Contrast control
- Four Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic

- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Two Capture/Compare/PWM (CCP) module
- Two 10-bit PWMs
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Communication:
  - Two EUSART, RS-232, RS-485, LIN compatible
  - One SPI
  - One I^2C, SMBus, PMBus™ compatible
- Up to 59 I/O Pins
- Individually Programmable Pull-ups
- Slew Rate Control
- Interrupt-on-Change with Edge-Select
- Input Level Selection Control (ST or TTL)
- Digital Open-Drain Enable
- Current-mode Enable

Analog Peripherals:

- Analog-to-Digital Converter with Computation (ADC^2):
  - 12-bit with up to 47 external channels
  - Automated post-processing
  - Automates math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
  - Conversion available during Sleep
- Two Comparators:
  - (1) Low-Power Comparator
  - (1) High-Speed Comparator
  - Fixed Voltage Reference at non-inverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Flexible Oscillator Structure:

- High-Precision Internal Oscillator:
  - Active clock tuning of HFINTOSC over voltage and temperature
  - Selectable frequency range up to 32 MHz
  - ±1% typical
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External Oscillator Block with:
  - Three external clock modes up to 20 MHz
  - Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripherals clock stops
  - Oscillator Start-up Timer (OST)
  - Ensures stability of crystal oscillator sources

TABLE 1: PIC16(L)F191XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (kW/KB)	DataEE (bytes)	Data SRAM (bytes)	I/O Pins	12-bit ADC (ch)	5-bit DAC	Comparator	8-bit/ (with HLT) Timer	16-bit Timer	Window Watchdog Timer (WWDT)	CCP/10-bit PWM	CWG	CLC	Zero-Cross Detect	Temperature Sensor	Memory Access Partition	Device Information Area	EUSART/ I^2C/SPI	Peripheral Pin
PIC16(L)F19155	**(A)**	8/14	256	1024	24	22	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19156	**(A)**	16/28	256	2048	24	22	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19175	**(A)**	8/14	256	1024	35	32	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19176	**(A)**	16/28	256	2048	35	32	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19185	**(A)**	8/14	256	1024	43	40	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19186	**(A)**	16/28	256	2048	43	40	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19195	**(B)**	8/14	256	1024	59	44	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19196	**(B)**	16/28	256	2048	59	44	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y
PIC16(L)F19197	**(B)**	32/56	256	4096	59	44	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y

Note 1: I – Debugging integrated on chip.

Data Sheet Index:

A. Future Release PIC16(L)F191XX Data Sheet, 28/40/44/48-Pin

B. Future Release PIC16(L)F1919X Data Sheet, 64-Pin

Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

TABLE 2: PACKAGES

Device	28 SPDIP	28 SOIC	28 SSOP	28 UQFN (4x4)	40 PDIP	40 UQFN (5x5)	44 TQFP	44 QFN (8x8)	48 UQFN (6x6)	48 TQFP (7x7)	64 TQFP	64 QFN (9x9)
PIC16(L)F19155	X	X	X	X								
PIC16(L)F19156	X	X	X	X								
PIC16(L)F19175					X	X	X	X				
PIC16(L)F19176					X	X	X	X				
PIC16(L)F19185									X	X		
PIC16(L)F19186									X	X		
PIC16(L)F19195											X	X
PIC16(L)F19196											X	X
PIC16(L)F19197											X	X

Note: Pin details are subject to change.

PIN DIAGRAMS

FIGURE 1: 28-PIN SSOP, SPDIP AND SOIC PACKAGE DIAGRAM FOR PIC16(L)F19155/56

28-Pin

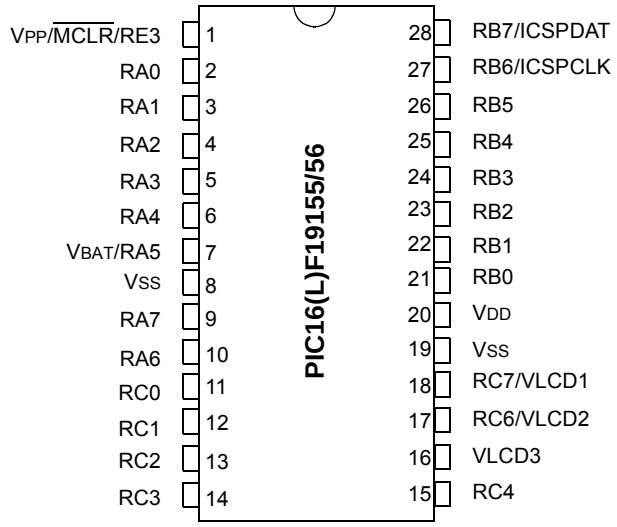


FIGURE 2: 28-PIN UQFN PACKAGE DIAGRAM FOR PIC16(L)F19155/56

UQFN 4x4x0.5mm

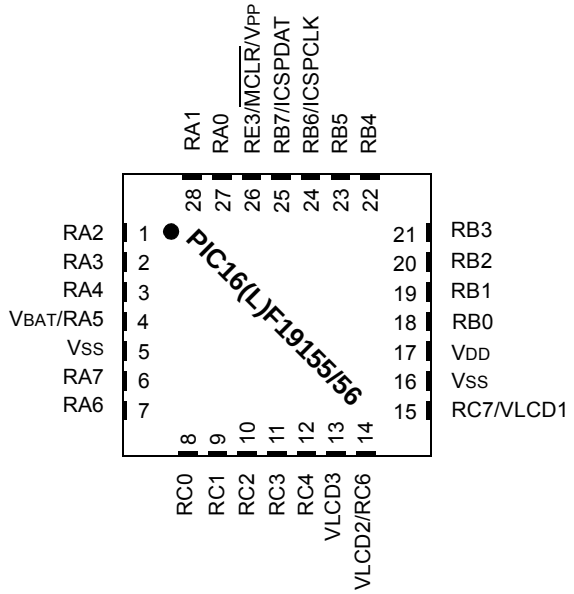


FIGURE 3: 40-PIN PDIP PACKAGE DIAGRAM FOR PIC16(L)F19175/76

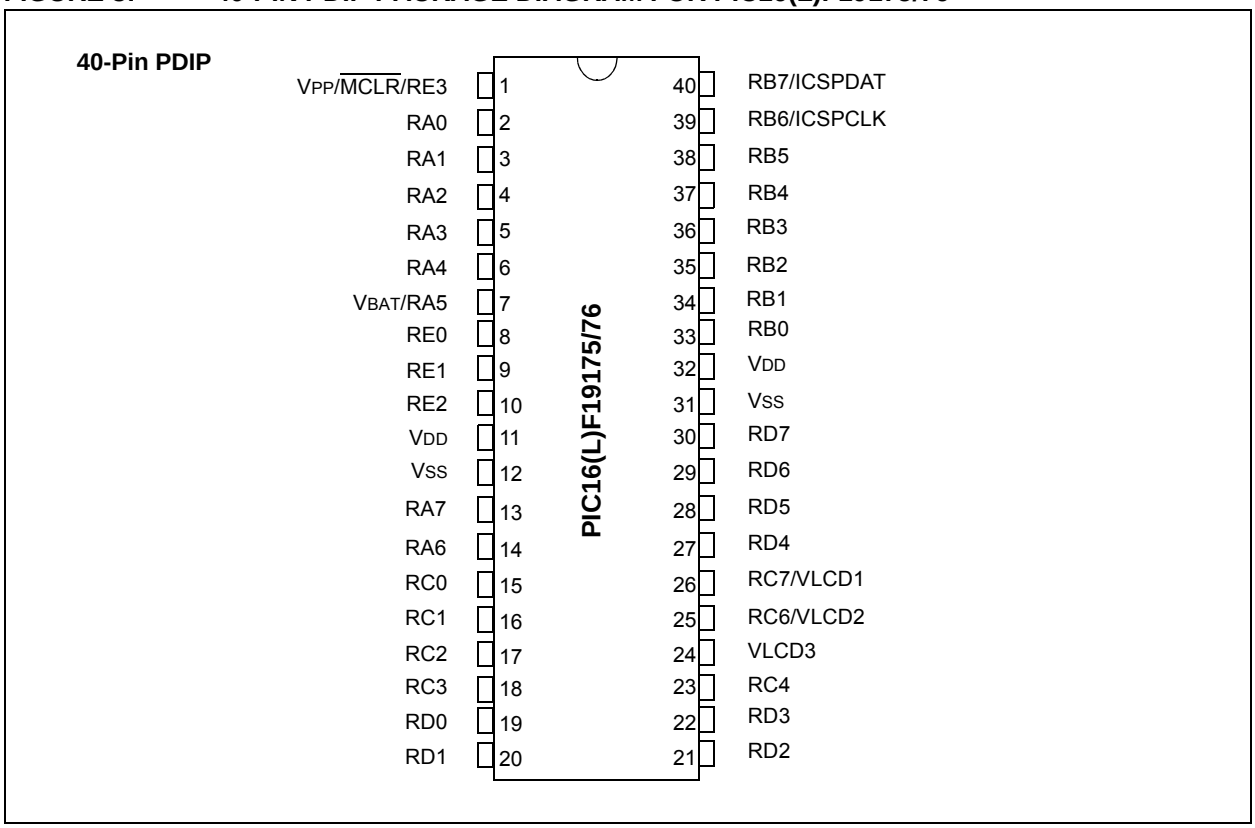


FIGURE 4: 40-PIN UQFN (5X5X0.5) PACKAGE DIAGRAM FOR PIC16(L)F19175/76

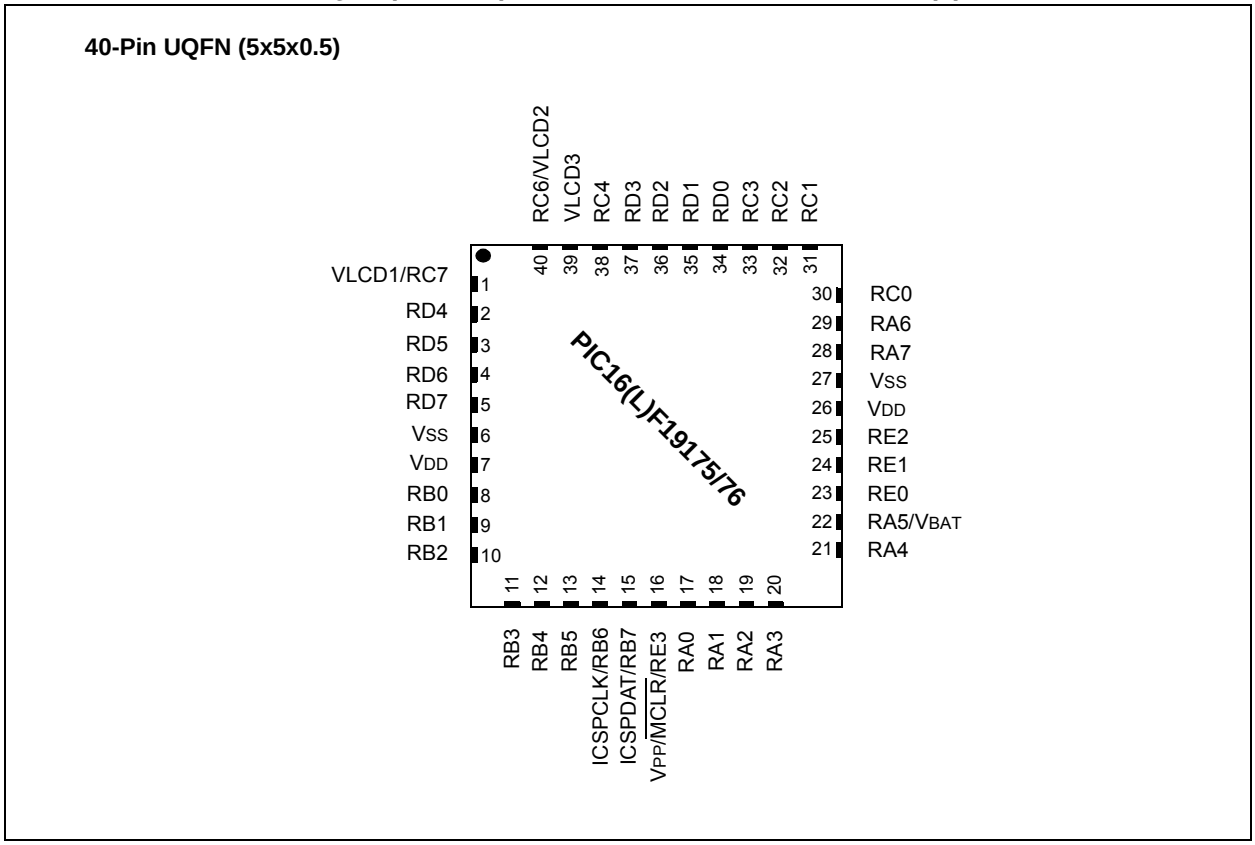


FIGURE 5: 44-PIN TQFP PACKAGE DIAGRAM FOR PIC16(L)F19175/76

44-Pin TQFP (10x10x1)

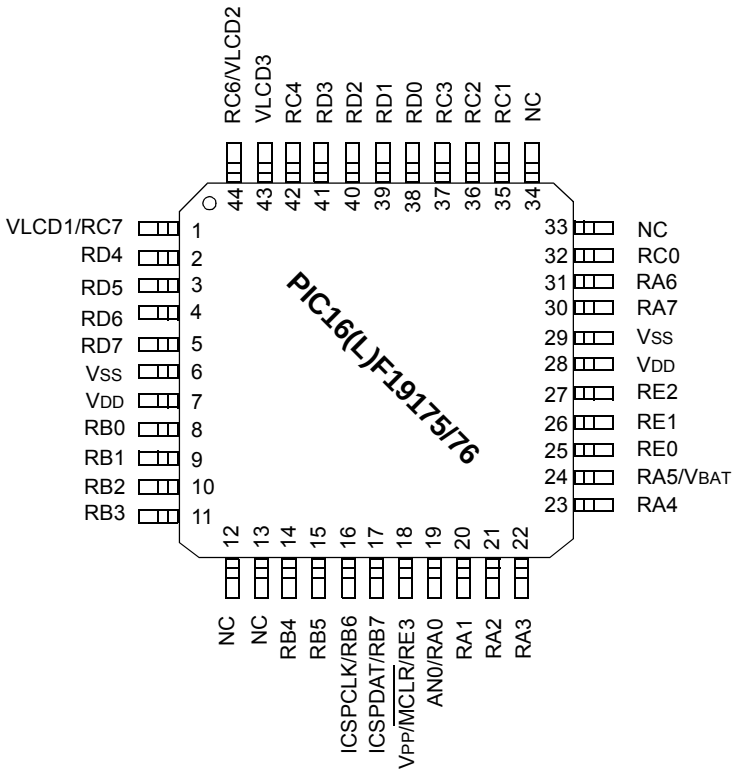
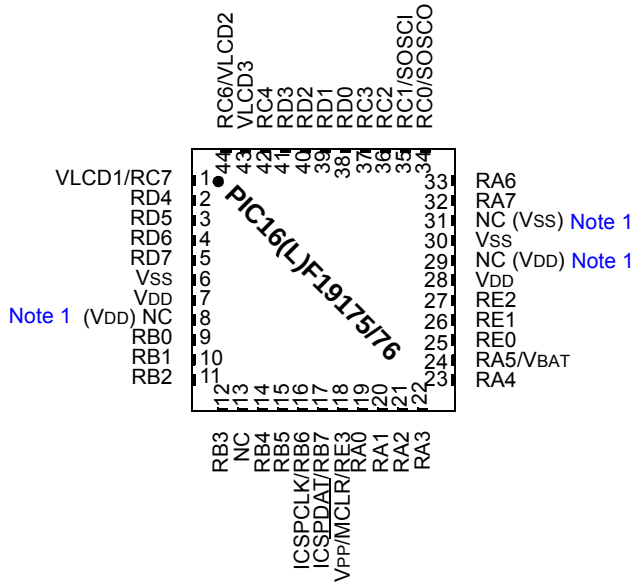


FIGURE 6: 44-PIN QFN (8X8X0.9) PACKAGE DIAGRAM FOR PIC16(L)F19175/76

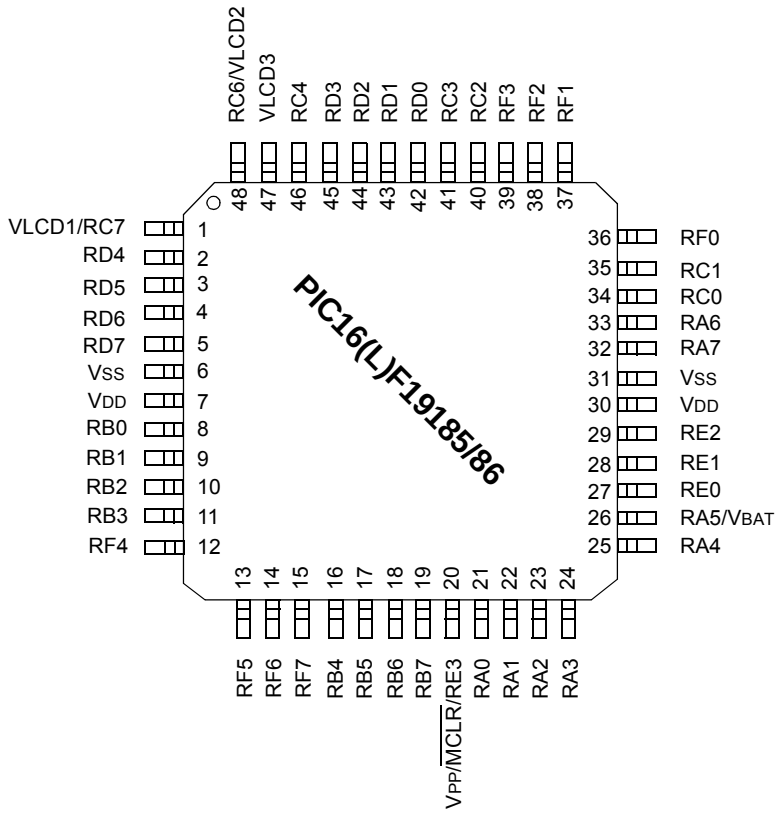
8x8x0.9 QFN-44



Note 1: NC (no bond wire) to reserve the pin for backwards compatibility with previous 44-pin devices.

FIGURE 7: 48-PIN TQFP/UQFN PACKAGE DIAGRAM FOR PIC16(L)F19185/86

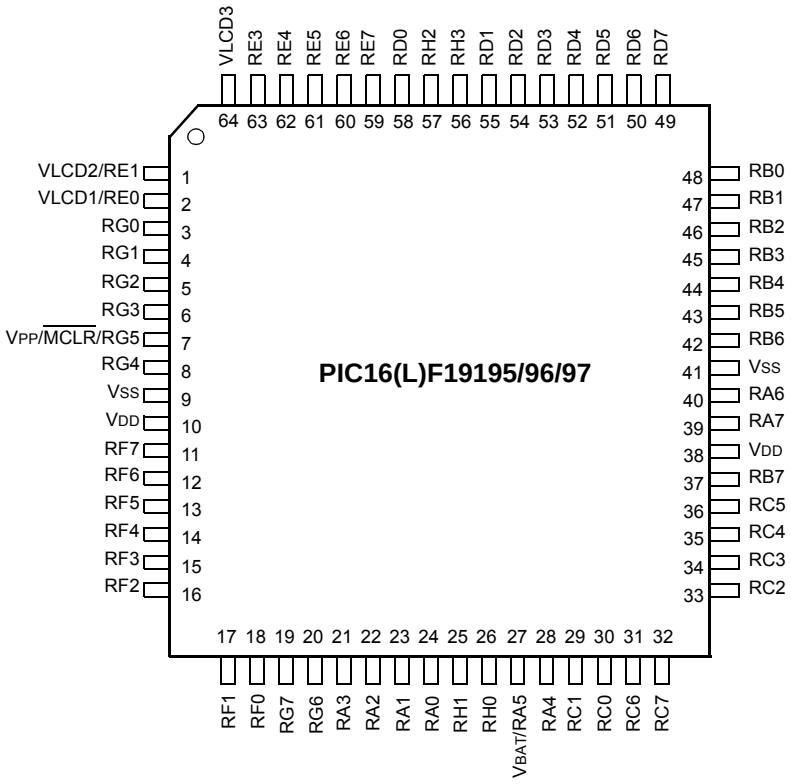
48-Pin TQFP (7x7x1)
48-Pin UQFN (6x6x0.5)



Note: QFN package orientation is the same. No leads are present on the QFN package.

FIGURE 8: 64-PIN TQFP/QFN PACKAGE DIAGRAM FOR PIC16(L)F19195/96/97

64-Pin TQFP (10x10x1)
64-Pin QFN (9x9x0.9)



Note: QFN package orientation is the same. No leads are present on the QFN package.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F19155/56)

I/O(2)	28-Pin SPDIP/SSOP/SOIC	28-Pin UQFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	SEG
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	SEG
RA2	4	1	ANA2	—	C1IN0+ C2IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	SEG
RA3	5	2	ANA3	VREF+	C1IN1+	—	DAC1REF+	—	—	—	—	—	—	—	—	SEG
RA4	6	3	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	SEG COM
RA5	7	4	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	SEG
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	SEG
RB0	21	18	ANB0	—	C2IN1+	ZCD	—	—	—	—	CWG1IN(1)	—	—	—	—	SEG
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG
RB2	23	20	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG COM VLCA
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	SEG COM VLCA
RB4	25	22	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	COM
RB5	26	23	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	SEG COM

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL r SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F19155/56) (CONTINUED)

I/O(2)	28-Pin SPDIP/SSOP/SOIC	28-Pin UQFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RB6	27	24	ANB6	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	CLCIN2(1)	—	SEG
RB7	28	25	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	RX2(1) DT2(1)	CLCIN3(1)	—	SEG
RC0	11	8	—	—	—	—	—	T1CKI(1) SMTWIN1(1)	—	—	—	—	—	—	—	—
RC1	12	9	—	—	—	—	—	SMTSIG1(1) T4IN(1)	CCP2(1)	—	—	—	—	—	—	—
RC2	13	10	ANC2	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	COM SEG
RC3	14	11	ANC3	—	—	—	—	T2IN(1)	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	SEG
RC4	15	12	ANC4	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	SEG
RC6	17	14	ANC6	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	COM SEG VLC
RC7	18	15	ANC7	—	—	—	—	—	—	—	—	—	RX1(1) DT1(1)	—	—	SEG COM VLC
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VLCD3	16	13	—	—	—	—	—	—	—	—	—	—	—	—	—	VLC
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	8 19	5 16	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL r SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	
RA0	2	17	19	19	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	S
RA1	3	18	20	20	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	S
RA2	4	19	21	21	ANA2	—	C1IN0+ C2IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	S
RA3	5	20	22	22	ANA3	VREF+	C1IN1+	—	DAC1REF+	—	—	—	—	—	—	—	—	S
RA4	6	21	23	23	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	S C
RA5	7	22	24	24	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	
RA6	14	29	31	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	S
RA7	13	28	30	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	S
RB0	33	8	8	9	ANB0	—	C2IN1+	ZCD	—	—	—	—	CWG1IN(1)	—	—	—	—	S
RB1	34	9	9	10	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	S
RB2	35	10	10	11	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	S VL
RB3	36	11	11	12	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	S VL
RB4	37	12	14	14	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	C
RB5	38	13	15	15	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	S C
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	CLCIN2(1)	—	S
RB7	40	15	17	17	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	RX2(1) DT2(1)	CLCIN3(1)	—	S

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TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76) (CONTINUED)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	
RC0	15	30	32	34	—	—	—	—	—	T1CKI(1) SMTWIN1(1)	—	—	—	—	—	—	—	
RC1	16	31	35	35	—	—	—	—	—	SMTSIG1(1) T4IN(1)	CCP2(1)	—	—	—	—	—	—	
RC2	17	32	36	36	ANC2	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	C S
RC3	18	33	37	37	ANC3	—	—	—	—	T2IN(1)	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	S
RC4	23	38	42	42	ANC4	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	S
RC6	25	40	44	44	ANC6	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	S V
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	—	—	—	RX1(1) DT1(1)	—	—	S V
RD0	19	34	38	38	AND0	—	—	—	—	—	—	—	—	—	—	—	—	S
RD1	20	35	39	39	AND1	—	—	—	—	—	—	—	—	—	—	—	—	S
RD2	21	36	40	40	AND2	—	—	—	—	—	—	—	—	—	—	—	—	C S
RD3	22	37	41	41	AND3	—	—	—	—	—	—	—	—	—	—	—	—	C S
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	S
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	S
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	S
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	S
RE0	8	23	25	25	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	S
RE1	9	24	26	26	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	C S
RE2	10	25	27	27	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	C S
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	—	—	

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76) (CONTINUED)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	
VLCD3	24	39	43	43	—	—	—	—	—	—	—	—	—	—	—	—	—	V
VDD	11 32	7 26	7 28	7 28	—	—	—	—	—	—	—	—	—	—	—	—	—	
VSS	12 31	6 27	6 29	6 30	—	—	—	—	—	—	—	—	—	—	—	—	—	
OUT(2)	—	—	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 5: 48-PIN ALLOCATION TABLE (PIC16(L)F19185/86)

I/O(2)	48-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RA0	21	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	SEG0
RA1	22	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	SEG1
RA2	23	ANA2	—	C1IN0+ C2IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	SEG2
RA3	24	ANA3	VREF+	C1IN1+	—	DAC1REF+	—	—	—	—	—	—	—	—	SEG3
RA4	25	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	SEG4 COM
RA5	26	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	—
RA6	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	SEG6
RA7	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	SEG7
RB0	8	ANB0	—	C2IN1+	ZCD	—	—	—	—	CWG1IN(1)	—	—	—	—	SEG8
RB1	9	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG9
RB2	10	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG10 VLCAP
RB3	11	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	SEG11 VLCAP
RB4	16	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	COM0
RB5	17	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	SEG12 COM
RB6	18	ANB6	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	CLCIN2(1)	—	SEG13
RB7	19	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	RX2(1) DT2(1)	CLCIN3(1)	—	SEG14

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL
or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 5: 48-PIN ALLOCATION TABLE (PIC16(L)F19185/86) (CONTINUED)

I/O(2)	48-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RC0	34	—	—	—	—	—	T1CKI(1) SMTWIN1(1)	—	—	—	—	—	—	—	—
RC1	35	—	—	—	—	—	SMTSIG1(1) T4IN(1)	CCP2(1)	—	—	—	—	—	—	—
RC2	40	ANC2	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	COM SEG1
RC3	41	ANC3	—	—	—	—	T2IN(1)	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	SEG1
RC4	46	ANC4	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	SEG2
RC6	48	ANC6	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	SEG2 VLCD
RC7	1	ANC7	—	—	—	—	—	—	—	—	—	RX1(1) DT1(1)	—	—	SEG2 VLCD
RD0	42	AND0	—	—	—	—	—	—	—	—	—	—	—	—	SEG2
RD1	43	AND1	—	—	—	—	—	—	—	—	—	—	—	—	SEG2
RD2	44	AND2	—	—	—	—	—	—	—	—	—	—	—	—	COM SEG2
RD3	45	AND3	—	—	—	—	—	—	—	—	—	—	—	—	COM SEG2
RD4	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	SEG2
RD5	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	SEG2
RD6	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	SEG3
RD7	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	SEG3
RE0	27	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	SEG3
RE1	28	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	COM SEG3
RE2	29	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	COM SEG3
RE3	20	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 5: 48-PIN ALLOCATION TABLE (PIC16(L)F19185/86) (CONTINUED)

I/O(2)	48-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RF0	36	ANF0	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RF1	37	ANF1	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RF2	38	ANF2	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RF3	39	ANF3	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RF4	12	ANF4	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RF5	13	ANF5	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RF6	14	ANF6	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RF7	15	ANF7	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
VLCD3	47	—	—	—	—	—	—	—	—	—	—	—	—	—	VLCD
VDD	7 30	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	6 31	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL
or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 6: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/96/97)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RA0	24	ANA0	—	C1IN4- C2IN4-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	SEG33
RA1	23	ANA1	—	—	—	—	T2IN(1)	—	—	—	—	—	CLCIN1(1)	—	SEG18
RA2	22	ANA2	—	C1IN1+ C2IN1+	—	—	—	—	—	—	—	—	—	—	SEG34
RA3	21	ANA3	V_{REF+}	—	—	$DA1_{REF+}$	—	—	—	—	—	—	—	—	SEG35
RA4	28	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	SEG14
RA5	27	—	—	—	—	—	—	—	—	—	—		—	—	—
RA6	40	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	SEG30
RA7	39	ANA7	—	—	—	—	—	—	—	—	—		—	—	SEG37
RB0	48	ANB0	—	—	ZCD	—	—	—	—	—	—	—	—	—	SEG30
RB1	47	ANB1	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)		—	—	SEG8
RB2	46	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG9
RB3	45	ANB3	—	—	—	—	—	—	—	—	—	—	—	—	SEG10
RB4	44	ANB4	—	—	—	—	—	—	—	—	—	—	—	—	SEG11
RB5	43	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	SEG29
RB6	42	ANB6	—	—	—	—	—	—	—	—	—	—	CLCIN2(1)	—	SEG38
RB7	37	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	—	CLCIN3(1)	—	SEG39
RC0	30	—	—	—	—	—	T1CKI(1)	—	—	—	—	—	—	—	—
RC1	29	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RC2	33	—	—	—	—	—	—	—	—	CWG1IN(1)	—	—	—	—	SEG13

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 6: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/96/97) (CONTINUED)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RC3	34	—	—	—	—	—	—	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	SEG17
RC4	35	—	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	SEG16
RC5	36	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG12
RC6	31	—	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	SEG27
RC7	32	—	—	—	—	—	—	—	—	—	—	RX1(1) DT1 (1)	—	—	SEG28
RD0	58	AND0	—	—	—	—	—	—	—	—	—	—	—	—	SEG0
RD1	55	AND1	—	—	—	—	—	—	—	—	—	—	—	—	SEG1
RD2	54	AND2	—	—	—	—	—	—	—	—	—	—	—	—	SEG2
RD3	53	AND3	—	—	—	—	—	—	—	—	—	—	—	—	SEG3
RD4	52	AND4	—	—	—	—	—	—	—	—	—	—	—	—	SEG4
RD5	51	AND5	—	—	—	—	—	—	—	—	—	—	—	—	SEG5
RD6	50	AND6	—	—	—	—	—	—	—	—	—	—	—	—	SEG6
RD7	49	AND7	—	—	—	—	—	—	—	—	—	—	—	—	SEG7
RE0	2	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	VLCD1
RE1	1	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	VLCD2
RE3	63	ANE3	—	—	—	—	—	—	—	—	—	—	—	—	COM0
RE4	62	ANE4	—	—	—	—	T4IN(1)	CCP2(1)	—	—	—	—	—	—	COM1
RE5	61	ANE5	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	COM2
RE6	60	ANE6	—	—	—	—	SMTWIN1(1)	—	—	—	—	—	—	—	COM3
RE7	59	ANE7	—	—	—	—	SMTSIG1(1)	—	—	—	—	—	—	—	SEG31
RF0	18	ANF0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	SEG41

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 6: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/96/97) (CONTINUED)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RF1	17	ANF1	—	—	—	—	—	—	—	—	—	—	—	—	SEG19
RF2	16	ANF2	—	—	—	—	—	—	—	—	—	—	—	—	SEG20
RF3	15	ANF3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	SEG21
RF4	14	ANF4	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	SEG22
RF5	13	ANF5	—	C1IN1- C2IN1-	—	DAC1OUT1	—	—	—	—	—	—	—	—	SEG23
RF6	12	ANF6	—	C1IN0+	—	—	—	—	—	—	—	—	—	—	SEG24
RF7	11	ANF7	—	C1IN3- C2IN3-	—	—	—	—	—	—	SS(1)	—	—	—	SEG25
RG0	3	ANG0	—	—	—	—	—	—	—	—	—	—	—	—	SEG42
RG1	4	ANG1	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	—	—	SEG43
RG2	5	ANG2	—	—	—	—	—	—	—	—	—	RX2(1) DT2(1)	—	—	SEG44
RG3	6	ANG3	—	—	—	—	—	—	—	—	—	—	—	—	SEG45
RG4	8	ANG4	—	—	—	—	—	—	—	—	—	—	—	—	SEG26
RG5	7	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RG6	20	ANG6	—	—	—	—	—	—	—	—	—	—	—	—	COM6
RG7	19	ANG7	—	—	—	—	—	—	—	—	—	—	—	—	SEG15 COM7
RH0	26	—	—	—	—	—	—	—	—	—	—	—	—	—	COM4
RH1	25	ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	COM5
RH2	57	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG32 VLCAP

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 6: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/96/97) (CONTINUED)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD
RH3	56	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG40 VLCAP
VLCD3	64	—	—	—	—	—	—	—	—	—	—	—	—	—	VLCD3
VDD	10	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VDD	38	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	9	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	41	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

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