



# PMN25EN

30 V, 6.2 A N-channel Trench MOSFET

Rev. 1 — 29 August 2011

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Logic level compatible
- Trench MOSFET technology
- Very fast switching

### 1.3 Applications

- Relay driver
- Low-side loadswitch
- High-speed line driver
- Switching circuits

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	6.2	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 6.2\text{ A}; T_j = 25\text{ °C}$	-	20	23	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	<p>SOT457 (TSOP6)</p>	<p>017aaa253</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		



### 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMN25EN	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

### 4. Marking

Table 4. Marking codes

Type number	Marking code
PMN25EN	T8

## 5. Limiting values

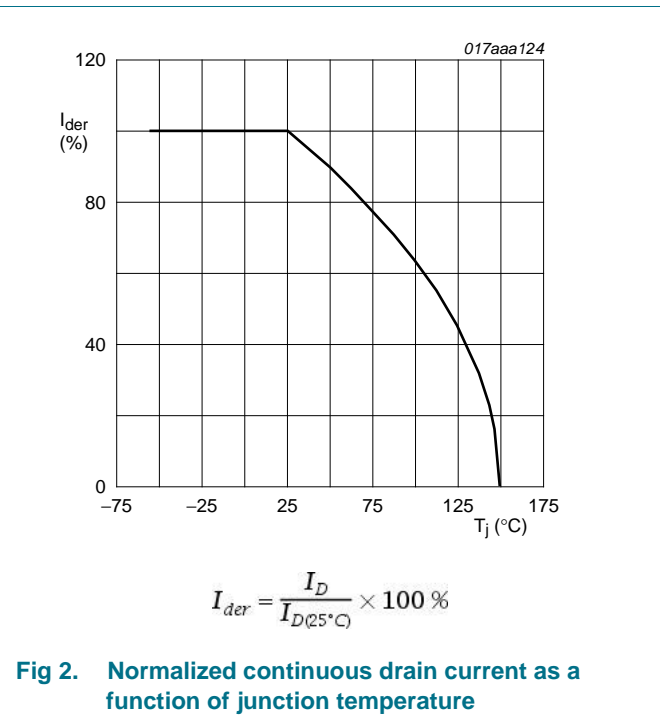
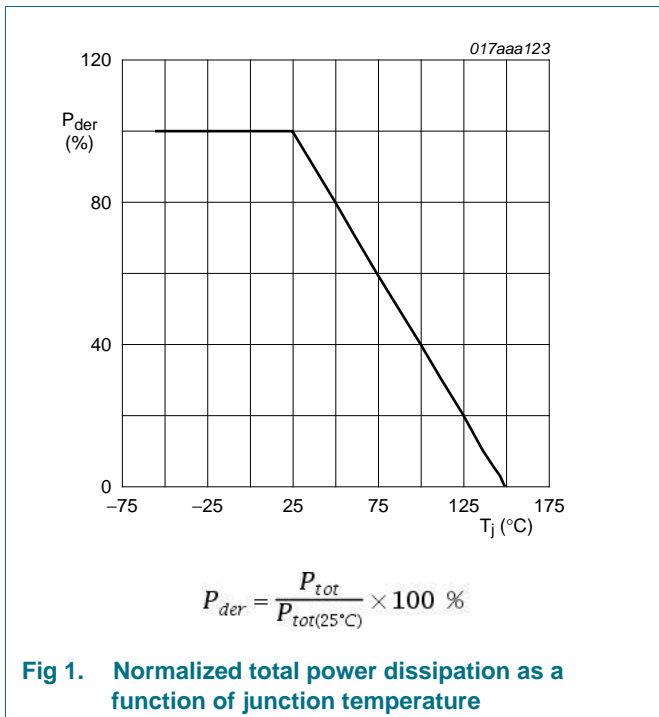
**Table 5. Limiting values**

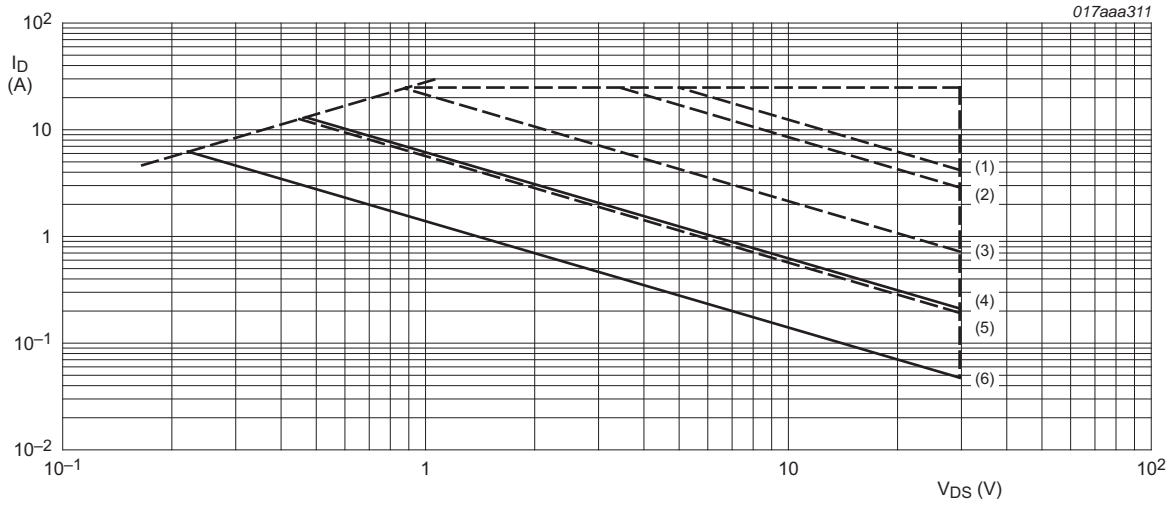
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	30	V	
V <sub>GS</sub>	gate-source voltage		-20	20	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	6.2	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C	[1]	-	3.9	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs	-	25	A	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	540	mW
			[1]	-	1385	mW
		T <sub>sp</sub> = 25 °C		-	6250	mW
T <sub>j</sub>	junction temperature		-55	150	°C	
T <sub>amb</sub>	ambient temperature		-55	150	°C	
T <sub>stg</sub>	storage temperature		-65	150	°C	
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	1.4	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





$I_{DM}$  = single pulse

(1)  $t_p = 100 \mu s$

(2)  $t_p = 1 ms$

(3)  $t_p = 10 ms$

(4) DC;  $T_{sp} = 25 \text{ }^\circ\text{C}$

(5)  $t_p = 100 ms$

(6) DC;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; drain mounting pad  $6 \text{ cm}^2$

**Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

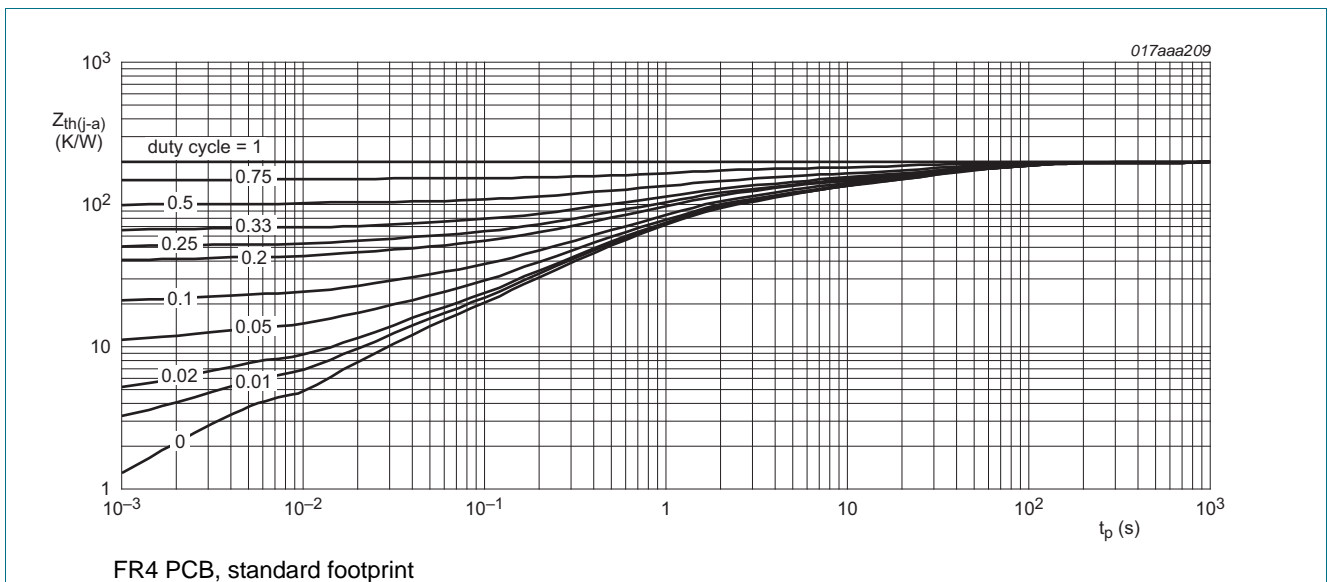
## 6. Thermal characteristics

**Table 6. Thermal characteristics**

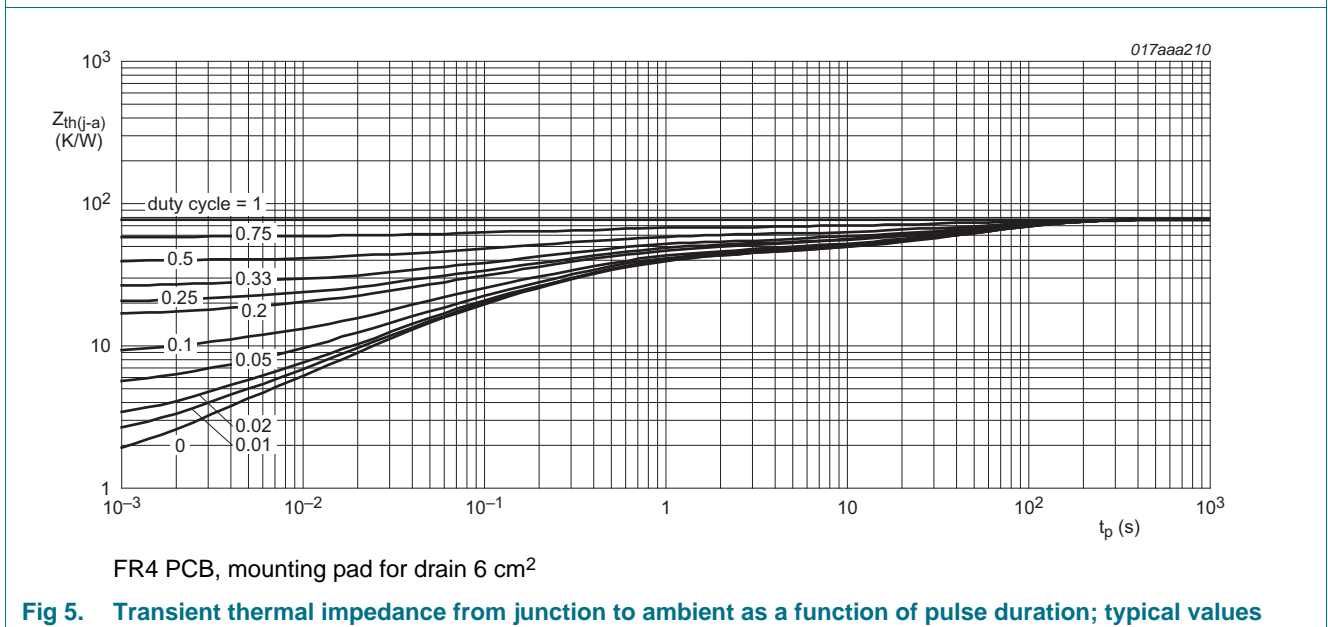
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	200	230	K/W
			[2]	-	78	90	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	15	20	K/W	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

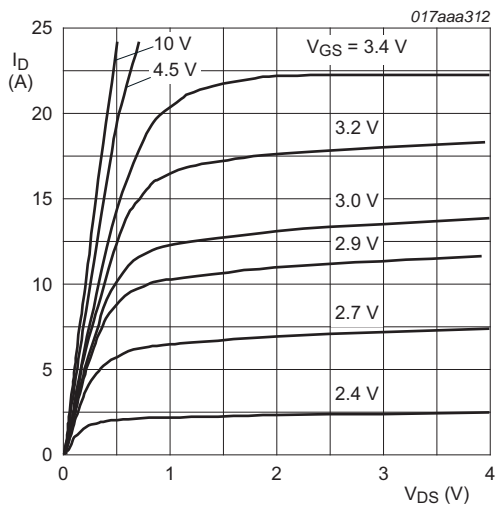


**Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 7. Characteristics

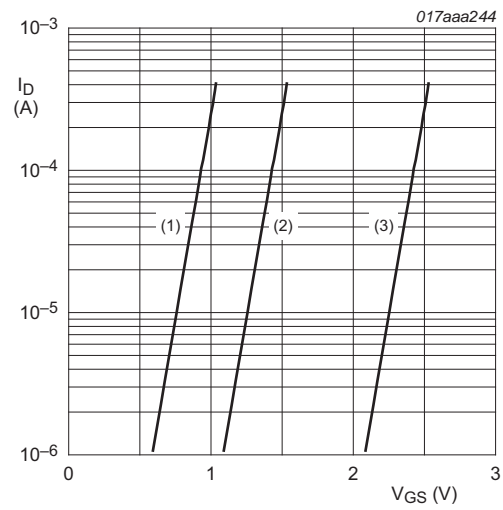
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	1	1.5	2.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	20	23	m $\Omega$
		$V_{GS} = 10 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	31	36	m $\Omega$
		$V_{GS} = 4.5 \text{ V}$ ; $I_D = 5.4 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	24	31	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	18	-	S
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 \text{ V}$ ; $I_D = 6 \text{ A}$ ; $V_{GS} = 10 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	9.6	11	nC
$Q_{GS}$	gate-source charge		-	1.5	-	nC
$Q_{GD}$	gate-drain charge		-	1.5	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 15 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	492	-	pF
$C_{oss}$	output capacitance		-	115	-	pF
$C_{rss}$	reverse transfer capacitance		-	54	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{G(ext)} = 6 \text{ }^\Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; $I_D = 6 \text{ A}$	-	5	-	ns
$t_r$	rise time		-	28	-	ns
$t_{d(off)}$	turn-off delay time		-	94	-	ns
$t_f$	fall time		-	40	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 1.4 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.78	1.2	V



$T_j = 25\text{ °C}$

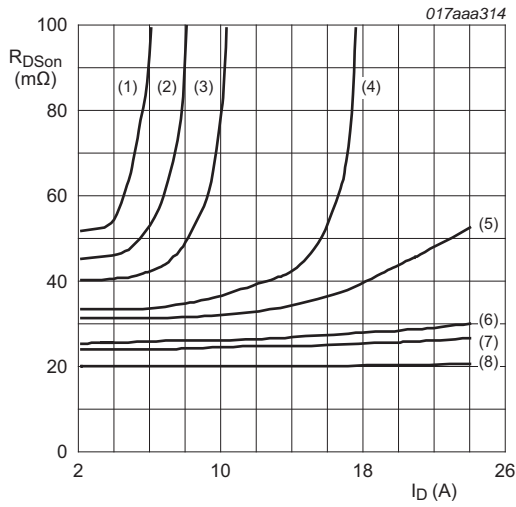
Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

- (1) minimum values
- (2) typical values
- (3) maximum values

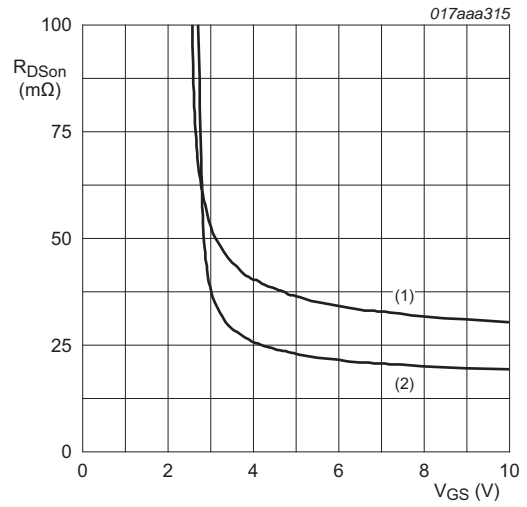
Fig 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^\circ\text{C}$

- (1)  $V_{GS} = 2.7\text{ V}$
- (2)  $V_{GS} = 2.8\text{ V}$
- (3)  $V_{GS} = 2.9\text{ V}$
- (4)  $V_{GS} = 3.2\text{ V}$
- (5)  $V_{GS} = 3.4\text{ V}$
- (6)  $V_{GS} = 4.0\text{ V}$
- (7)  $V_{GS} = 4.5\text{ V}$
- (8)  $V_{GS} = 10\text{ V}$

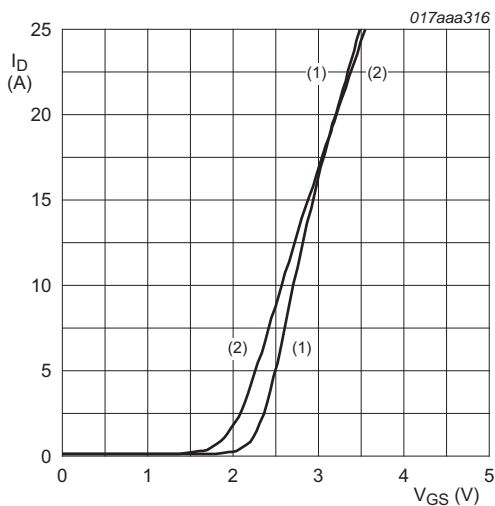
**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**



$I_D = 6.0\text{ A}$

- (1)  $T_j = 150\text{ }^\circ\text{C}$
- (2)  $T_j = 25\text{ }^\circ\text{C}$

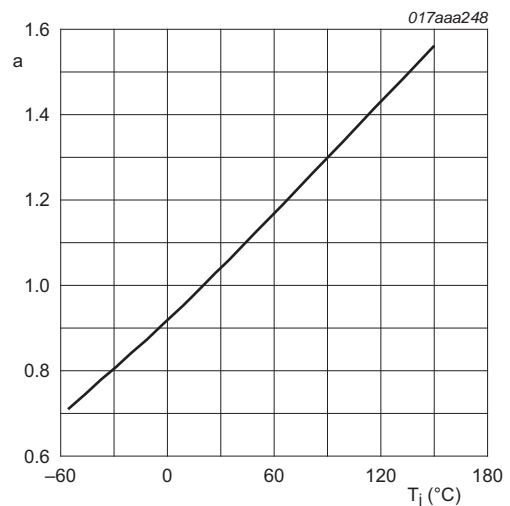
**Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$V_{DS} > I_D \times R_{DS(on)}$

- (1)  $T_j = 25\text{ }^\circ\text{C}$
- (2)  $T_j = 150\text{ }^\circ\text{C}$

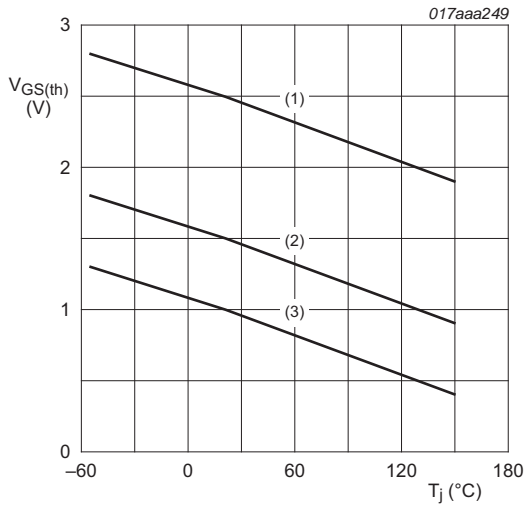
**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

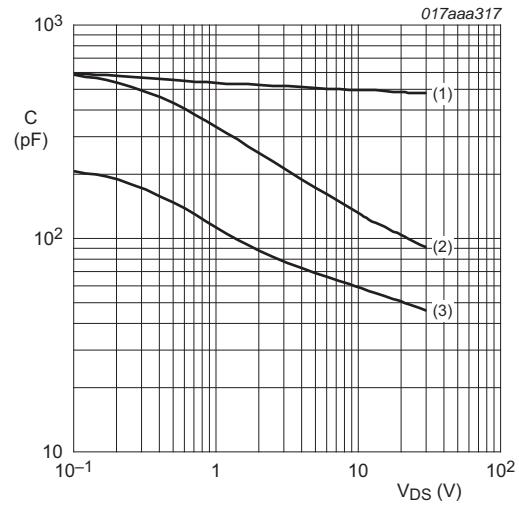
**Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**





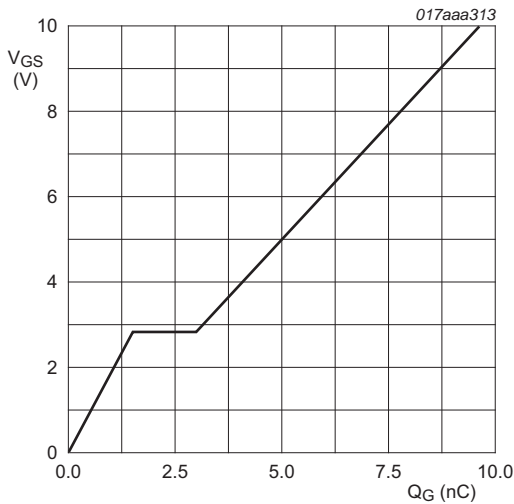
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 6 \text{ A}; V_{DS} = 10 \text{ V}; T_{amb} = 25 \text{ }^{\circ}C$

Fig 14. Gate-source voltage as a function of gate charge; typical values

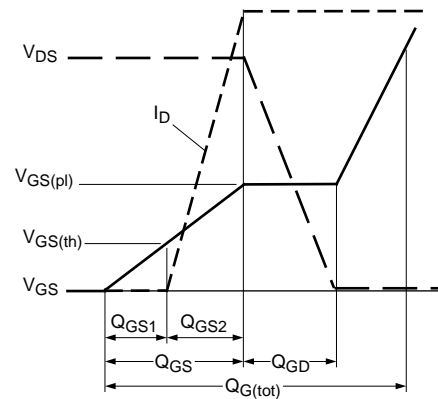
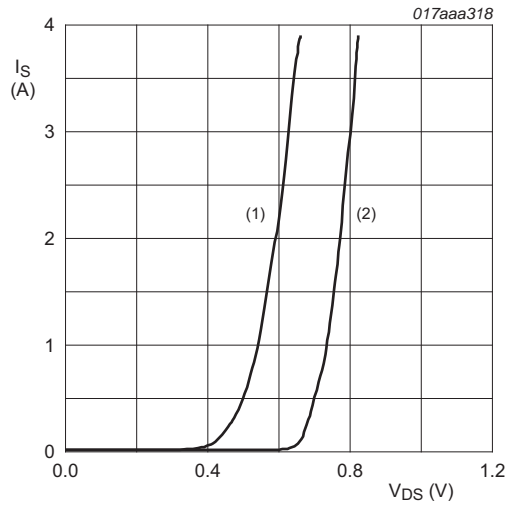


Fig 15. Gate charge waveform definitions



V<sub>GS</sub> = 0 V  
 (1) T<sub>j</sub> = 150 °C  
 (2) T<sub>j</sub> = 25 °C

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

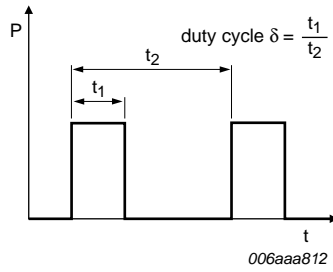


Fig 17. Duty cycle definition

9. Package outline

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

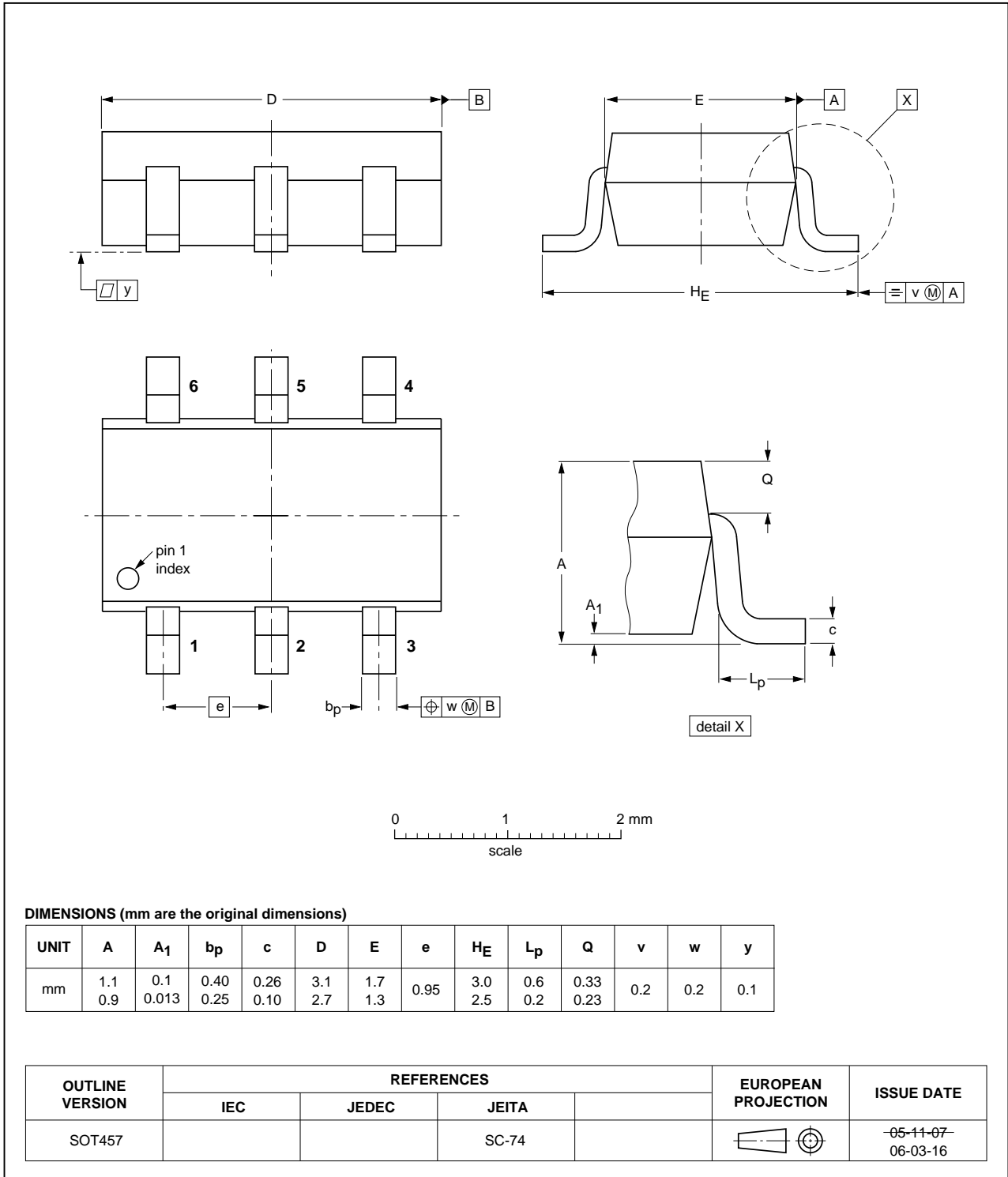


Fig 18. Package outline SOT457 (TSOP6)

10. Soldering

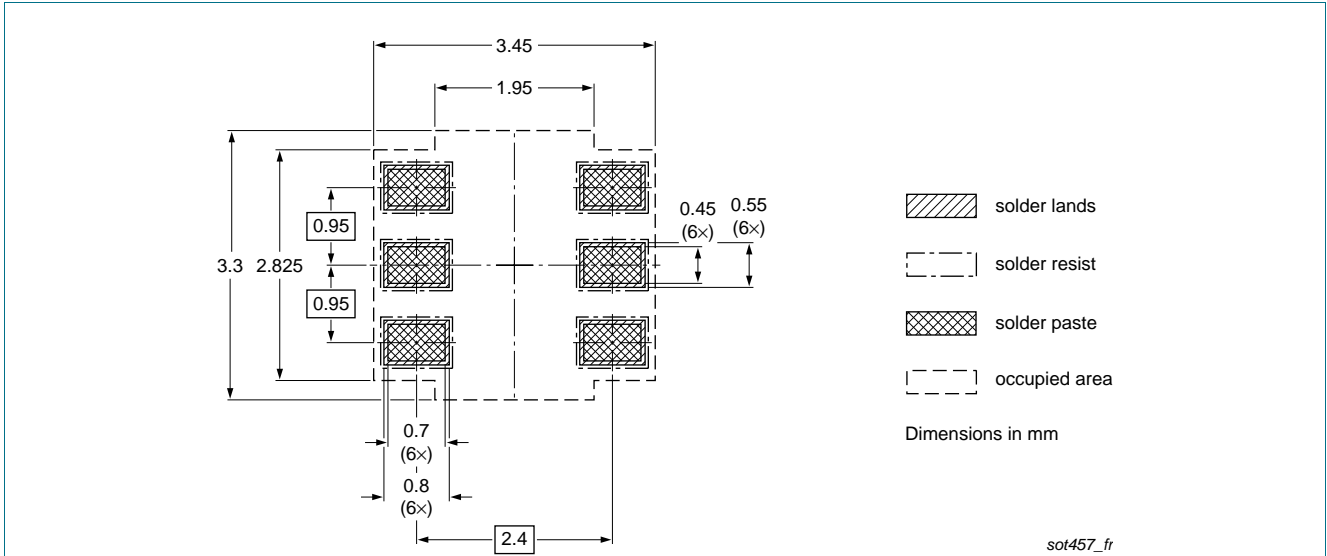


Fig 19. Reflow soldering footprint for SOT457 (TSOP6)

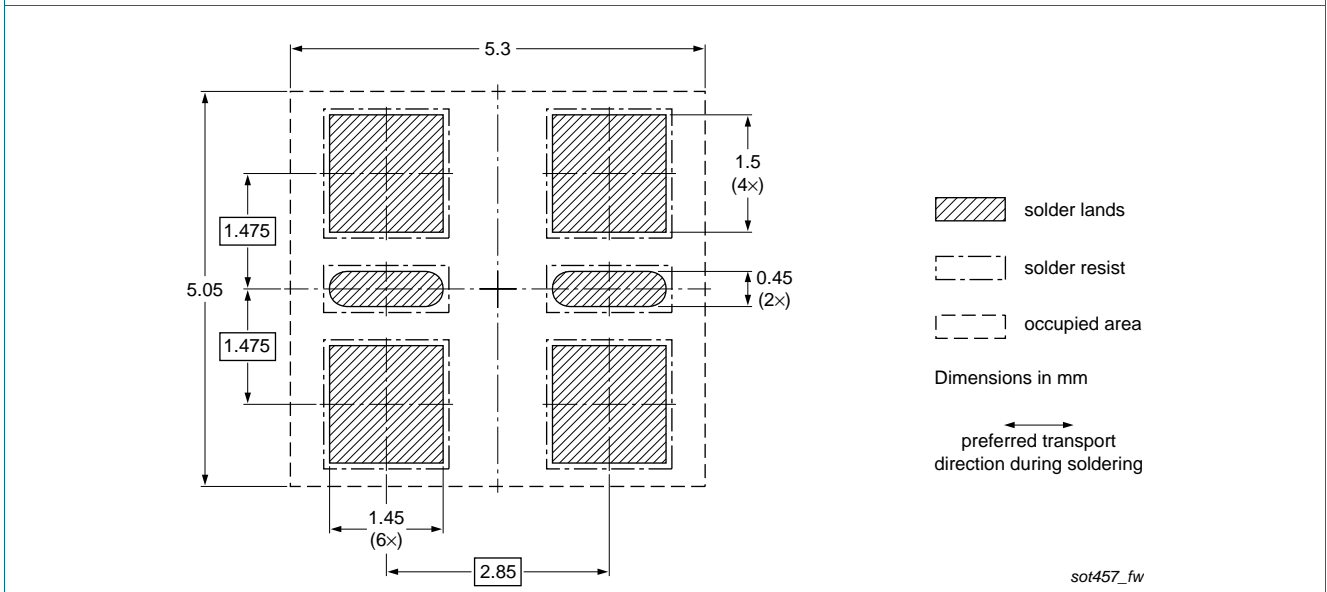


Fig 20. Wave soldering footprint for SOT457 (TSOP6)

## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN25EN v.1	20110829	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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