

# RQJ0201UGDQA

Silicon P Channel MOS FET Power Switching

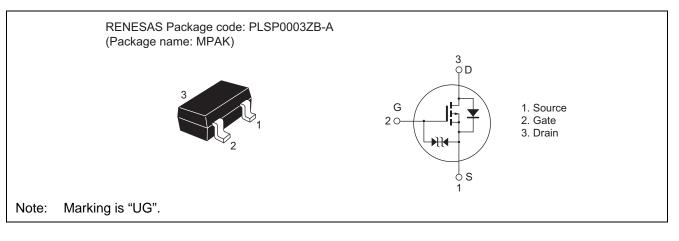
# R07DS0290EJ0500 Rev.5.00

Jan 10, 2014

Datasheet

- Low on-resistance
- $R_{DS(on)} = 53 \text{ m}\Omega \text{ typ} (V_{GS} = -4.5 \text{ V}, I_D = -1.8 \text{ A})$
- Low drive current
- High speed switching
- 2.5 V gate drive

### Outline



#### **Absolute Maximum Ratings**

			$(Ta = 25^{\circ}C)$
ltem	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	-20	V
Gate to source voltage	V <sub>GSS</sub>	+8 / -12	V
Drain current	ID	-3.4	А
Drain peak current	I <sub>D(pulse)</sub> Note1	-10	А
Body - drain diode reverse drain current	I <sub>DR</sub>	-3.4	А
Channel dissipation	Pch <sub>(pulse)</sub> Note2	0.8	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1.  $PW \le 10 \ \mu s$ , duty cycle  $\le 1\%$ 

2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)



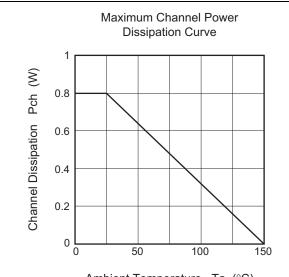
### **Electrical Characteristics**

						$(Ta = 25^{\circ}C)$
Item	Symbol	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	-20			V	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	+8			V	$I_{G} = +100 \ \mu A, V_{DS} = 0$
	V <sub>(BR)GSS</sub>	-12		_	V	$I_G = -100 \ \mu A, \ V_{DS} = 0$
Gate to source leak current	I <sub>GSS</sub>			+10	μA	$V_{GS} = +6 V, V_{DS} = 0$
	I <sub>GSS</sub>	_	_	-10	μA	$V_{GS} = -10 V, V_{DS} = 0$
Drain to source leak current	I <sub>DSS</sub>	_	_	-1	μA	$V_{DS} = -20 V, V_{GS} = 0$
Gate to source cutoff voltage	V <sub>GS(off)</sub>	-0.4		-1.4	V	$V_{DS} = -10 \text{ V}, I_D = -1 \text{ mA}$
Drain to source on state resistance	R <sub>DS(on)</sub>		53	69	mΩ	$I_D = -1.8 \text{ A}, V_{GS} = -4.5 \text{ V}^{\text{Note3}}$
	R <sub>DS(on)</sub>	_	80	112	mΩ	$I_D = -1.8 \text{ A}, V_{GS} = -2.5 \text{ V}^{\text{Note3}}$
Forward transfer admittance	y <sub>fs</sub>	4.5	6.5	_	S	$I_D = -1.8 \text{ A}, V_{DS} = -10 \text{ V}^{\text{Note3}}$
Input capacitance	Ciss		597	_	pF	V <sub>DS</sub> = -10 V
Output capacitance	Coss		149	_	pF	V <sub>GS</sub> = 0 f = 1 MHz
Reverse transfer capacitance	Crss	_	93		pF	
Turn - on delay time	t <sub>d(on)</sub>	_	18		ns	$I_{\rm D} = -1.8 \text{ A}$
Rise time	tr	_	43		ns	$V_{GS} = -4.5 V$ $R_L = 5.5 \Omega$ $Rg = 4.7 \Omega$
Turn - off delay time	t <sub>d(off)</sub>		37	_	ns	
Fall time	t <sub>f</sub>		12	_	ns	
Total gate charge	Qg	_	6.3	—	nC	$V_{DD} = -10 \text{ V}$
Gate to source charge	Qgs	_	1.1	_	nC	$V_{GS} = -4.5 V$ $I_D = -3.4 A$
Gate to drain charge	Qgd	_	2.5	_	nC	
Body - drain diode forward voltage	V <sub>DF</sub>	_	-0.85	-1.1	V	$I_F = -3.4 \text{ A}, V_{GS} = 0^{Note3}$

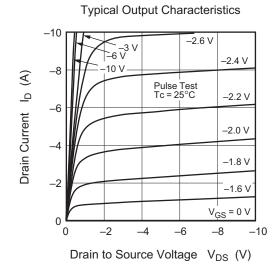
Notes: 3. Pulse test

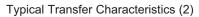


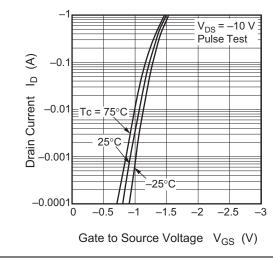
#### **Main Characteristics**



Ambient Temperature Ta (°C) \*When using the glass epoxy board (FR-4:  $40 \times 40 \times 1$  mm)







Maximum Safe Operation Area -100 Operation in this area is limited by R<sub>DS(on)</sub> 100 1 E -10 Drain Current I<sub>D</sub> -0.1 Ta = 25°C

1 Shot Pulse

-0.1

-0.01

-1.5

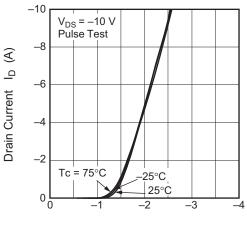
-0.01

Drain to Source Voltage V<sub>DS</sub> (V)

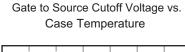
-10

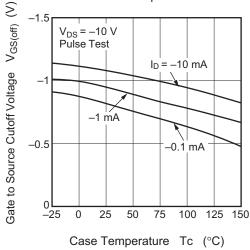
-100

Typical Transfer Characteristics (1)

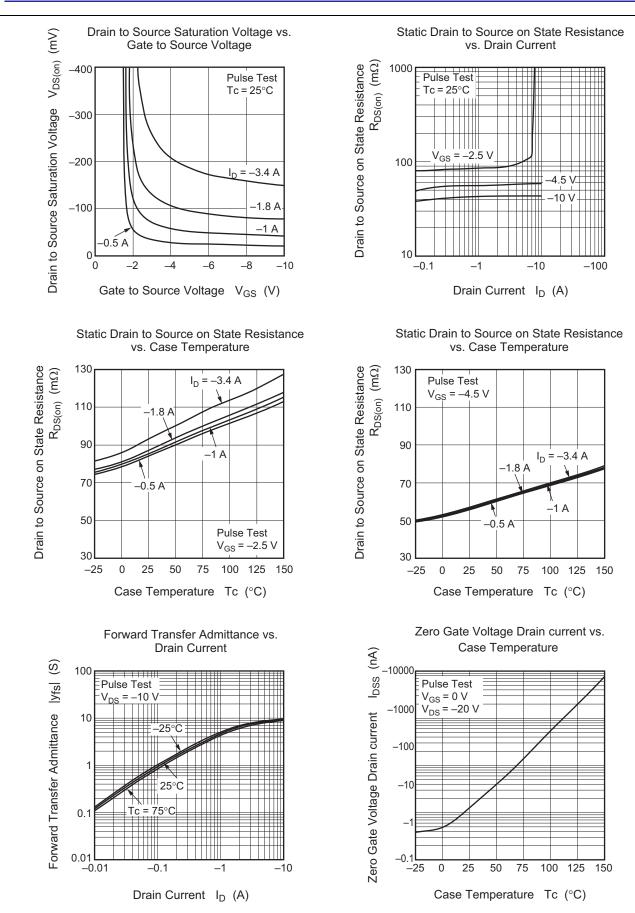


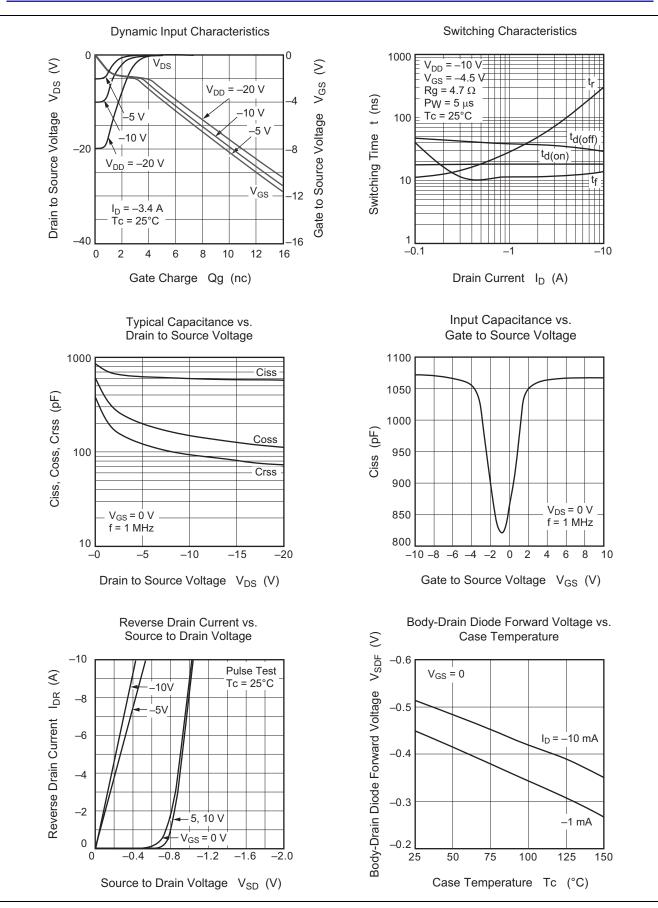
Gate to Source Voltage V<sub>GS</sub> (V)





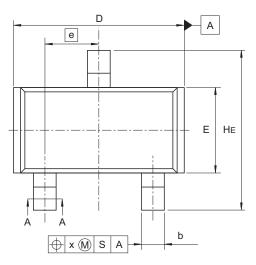


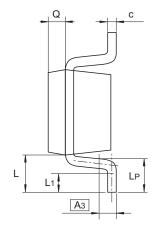


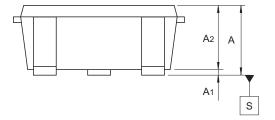


### Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011









A-A Section

Reference	Dimensions in millimeters		
Symbol	Min	Nom	Max
A	1.0		1.3
A <sub>1</sub>	0		0.1
A <sub>2</sub>	1.0	1.1	1.2
A <sub>3</sub>		0.25	
b	0.35	0.4	0.5
С	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
е		0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L <sub>1</sub>	0.15	—	0.55
LP	0.25	—	0.65
Х		—	0.05
Q		0.3	

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## **Ordering Information**

Orderable Part Number	Quantity	Shipping Container
RQJ0201UGDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping



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