

RQK2001HQDQA

Silicon N Channel MOS FET
Power Switching

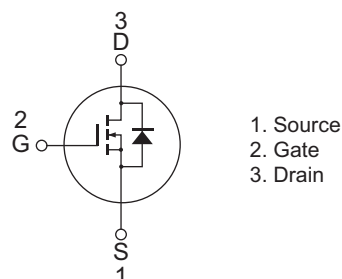
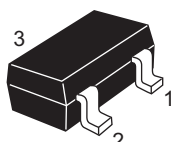
R07DS0311EJ0300
Rev.3.00
Jan 10, 2014

Features

- High drain to source voltage and Low gate drive
 $V_{DSS} : 200\text{ V}$ and $V_{GSS} : \pm 30\text{ V}$
- Low drive current
- High speed switching
- Small traditional package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



Note: Marking is "HQ".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	0.4	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	1.6	A
Body - drain diode reverse drain current	I_{DR}	0.4	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Thermal resistance	$R_{th(ch-a)}$ ^{Note2}	156	$^\circ\text{C} / \text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10\ \mu\text{s}$, Duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

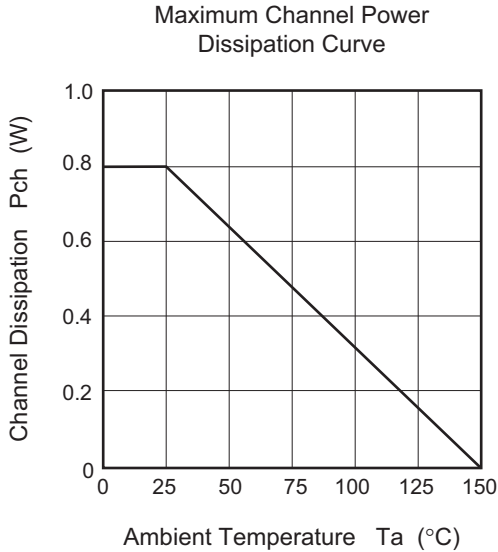
Electrical Characteristics

(Ta = 25°C)

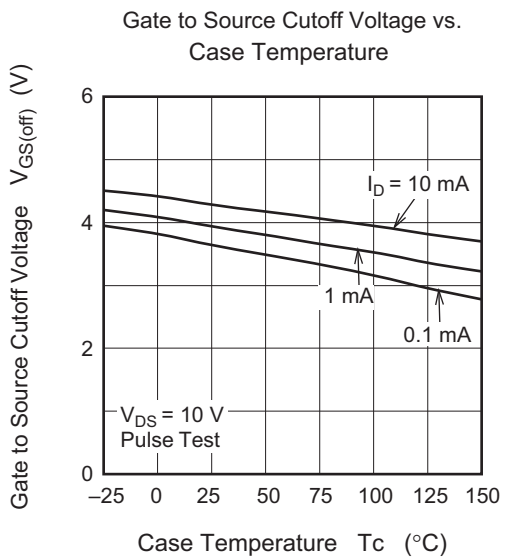
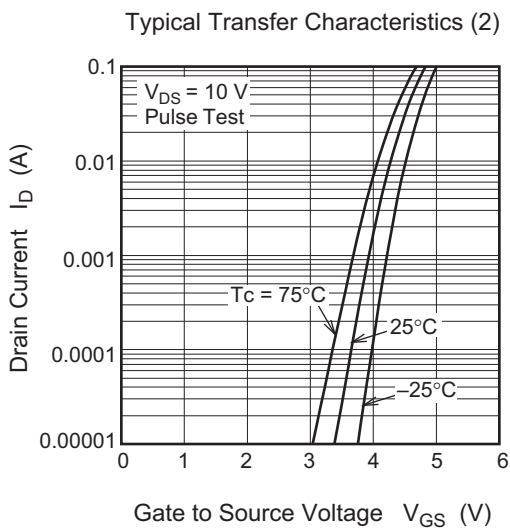
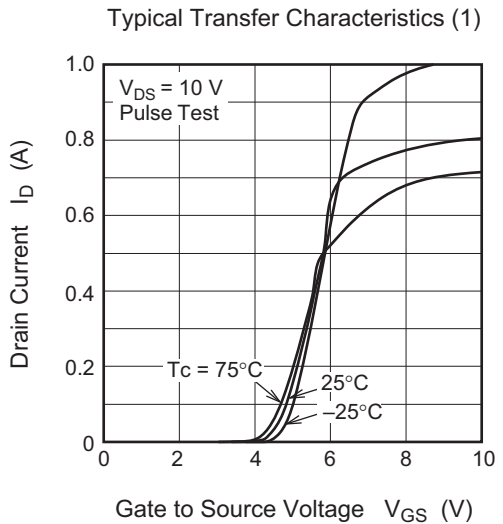
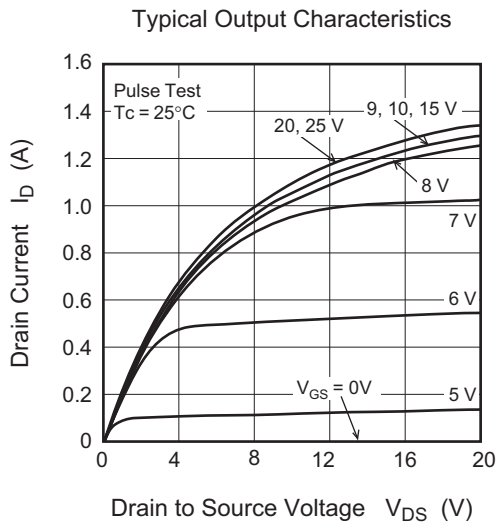
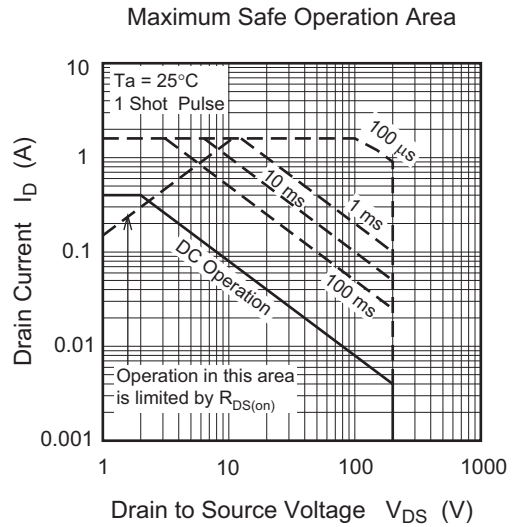
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	+0.1	μA	$V_{GS} = +30 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-0.1	μA	$V_{GS} = -30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	5.0	6.7	Ω	$I_D = 0.15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	0.2	0.3	—	S	$I_D = 0.15 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	30	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	5	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	2	—	pF	$f = 1 \text{ MHz}$
Turn - on delay time	$t_{d(on)}$	—	13	—	ns	$I_D = 0.15 \text{ A}$
Rise time	t_r	—	12	—	ns	$V_{GS} = 10 \text{ V}$
Turn - off delay time	$t_{d(off)}$	—	42	—	ns	$R_L = 667 \Omega$
Fall time	t_f	—	38	—	ns	$R_g = 50 \Omega$
Total gate charge	Q_g	—	1.8	—	nC	$V_{DD} = 100 \text{ V}$
Gate to Source charge	Q_{gs}	—	0.4	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	0.9	—	nC	$I_D = 0.4 \text{ A}$
Body - drain diode forward voltage	V_{DF}	—	0.8	1.2	V	$I_F = 0.4 \text{ A}$, $V_{GS} = 0$ ^{Note3}

Notes: 3. Pulse test

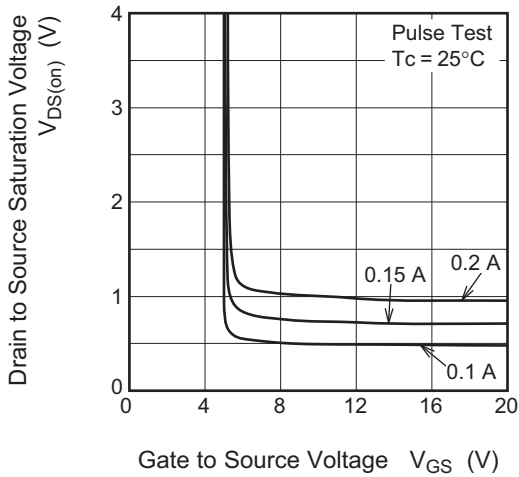
Main Characteristics



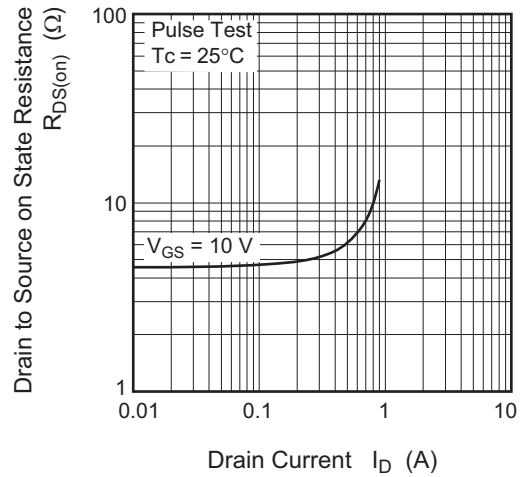
*When using the glass epoxy board (FR-4 40 x 40 x 1 mm)



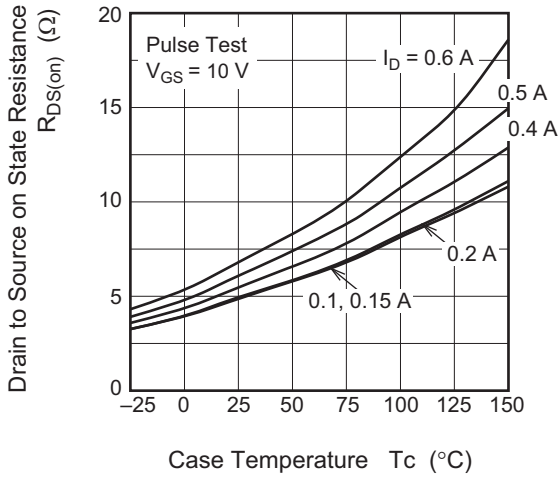
Drain to Source Saturation Voltage vs. Gate to Source Voltage



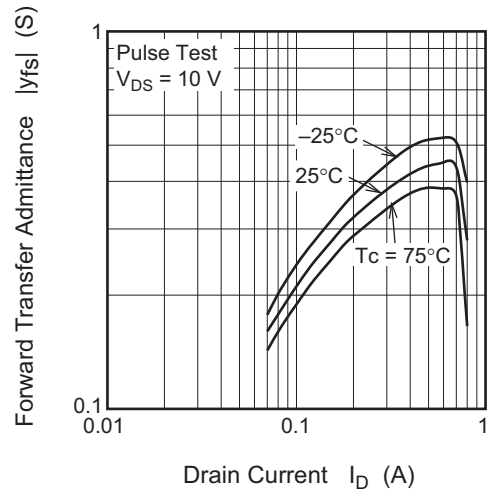
Static Drain to Source on State Resistance vs. Drain Current



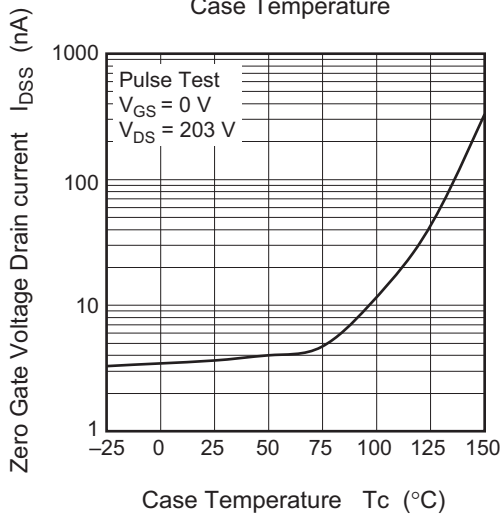
Static Drain to Source on State Resistance vs. Case Temperature (1)



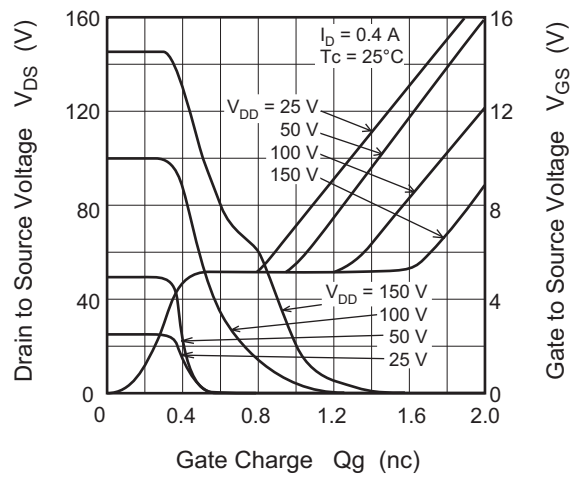
Forward Transfer Admittance vs. Drain Current



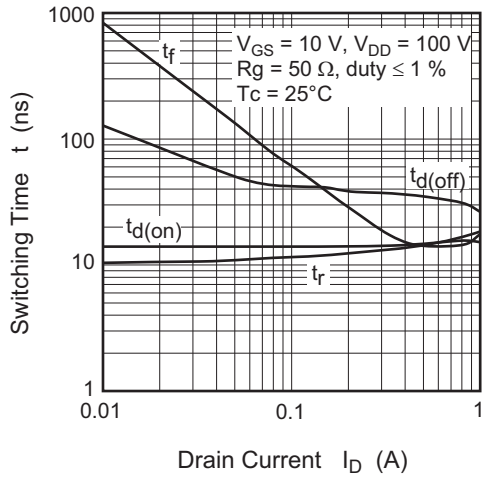
Zero Gate Voltage Drain current vs. Case Temperature



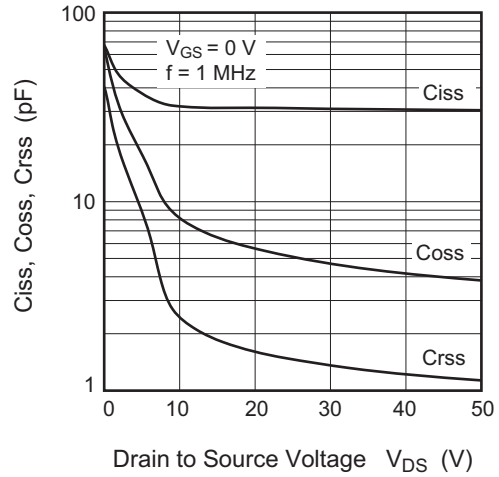
Dynamic Input Characteristics



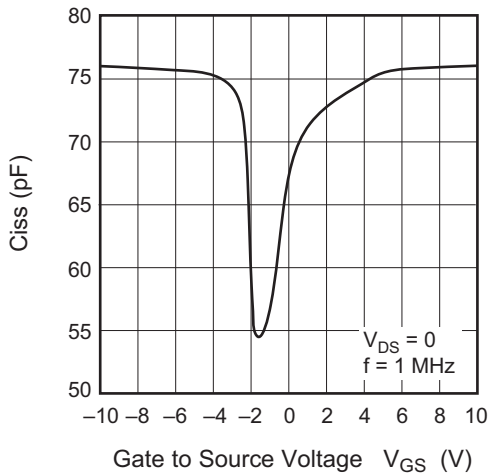
Switching Characteristics



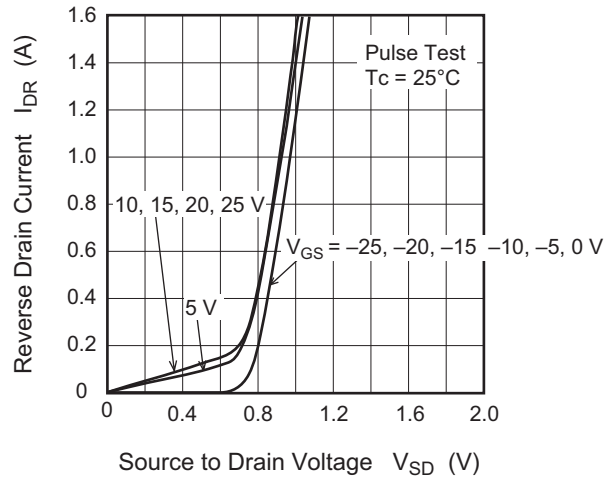
Typical Capacitance vs. Drain to Source Voltage



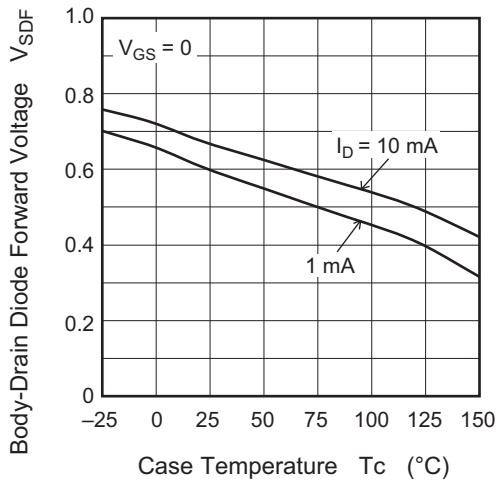
Input Capacitance vs. Gate to Source Voltage

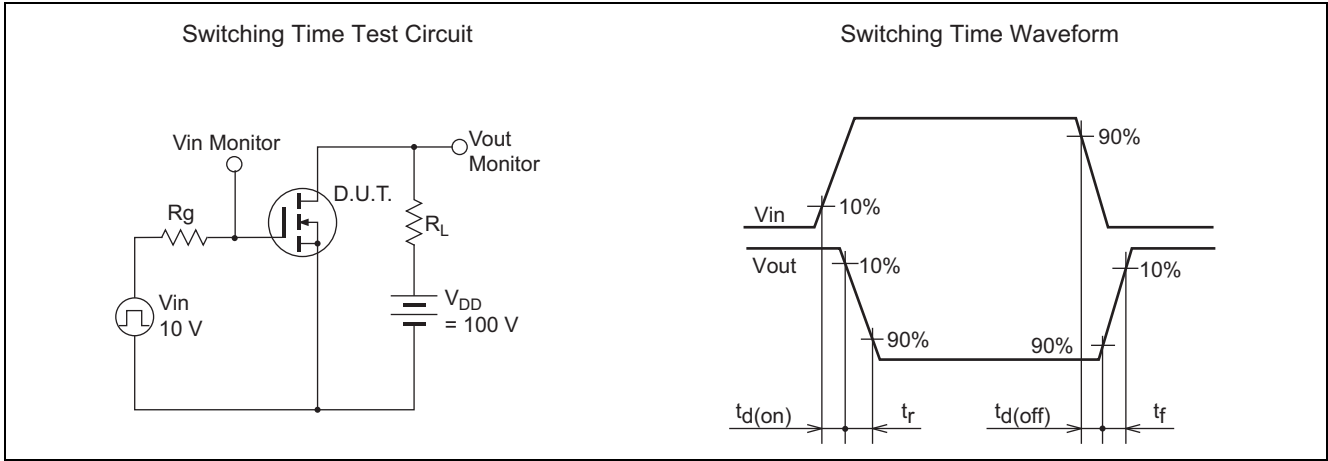


Reverse Drain Current vs. Source to Drain Voltage



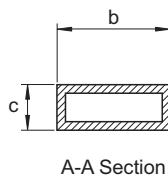
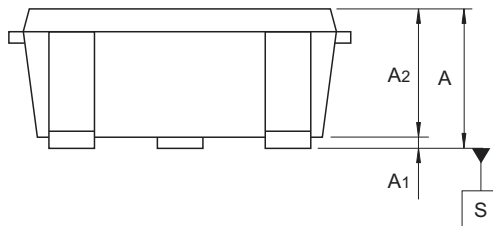
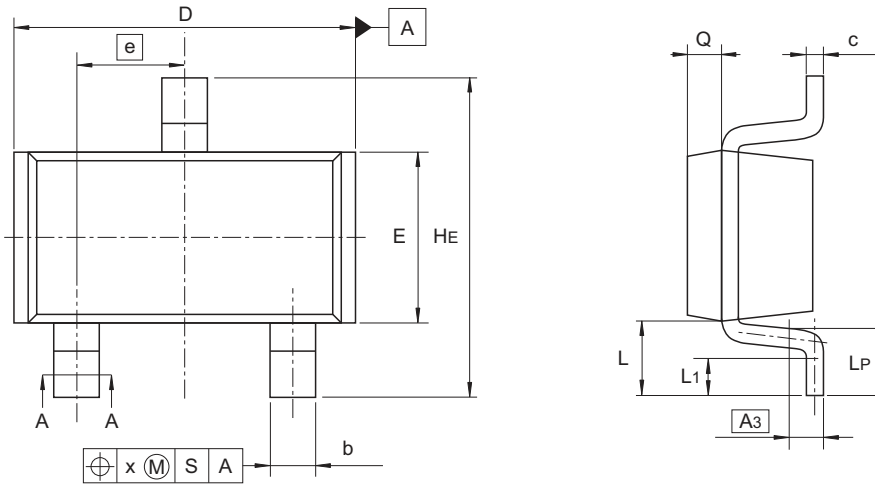
Body-Drain Diode Forward Voltage vs. Case Temperature





Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A1	0	—	0.1
A2	1.0	1.1	1.2
A3	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
e	—	0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L1	0.15	—	0.55
LP	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

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Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQK2001HQDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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