

RQK0606KGDQA

Silicon N Channel MOS FET
Power Switching

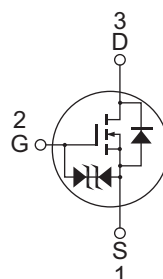
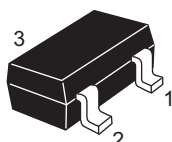
R07DS0310EJ0300
Rev.3.00
Jan 10, 2014

Features

- Low on-resistance
 $R_{DS(on)} = 173 \text{ m}\Omega$ typ.(at $V_{GS} = 4.5 \text{ V}$, $I_D = 0.8 \text{ A}$)
- Low drive current
- High speed switching
- $V_{DSS} \geq 60 \text{ V}$ and capable of 2.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Notes: Marking is "KG".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	± 12	V
Drain current	I_D	1.5	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	6	A
Body - drain diode reverse drain current	I_{DR}	1.5	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$
2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

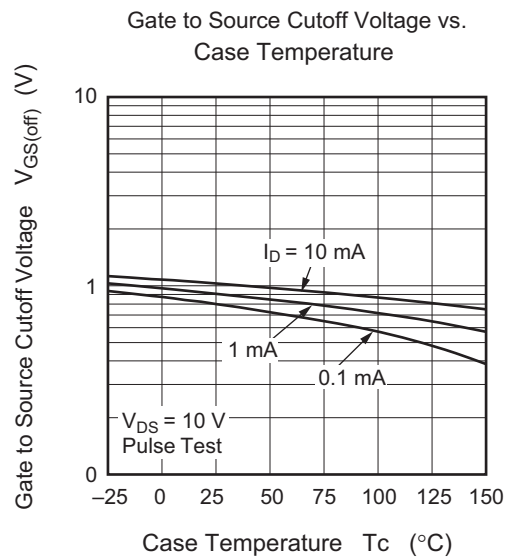
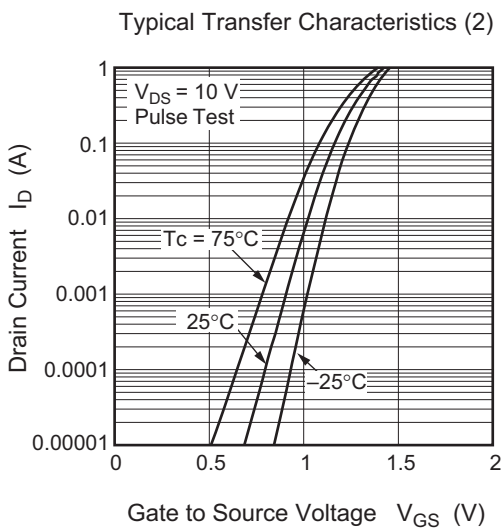
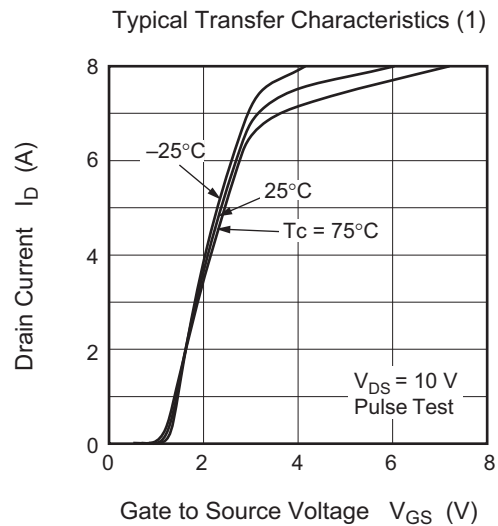
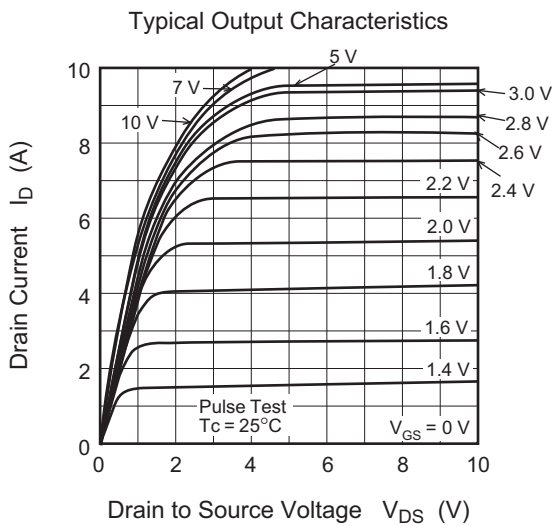
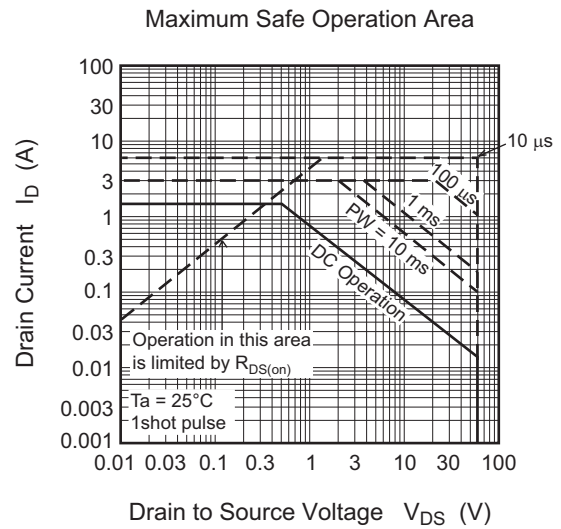
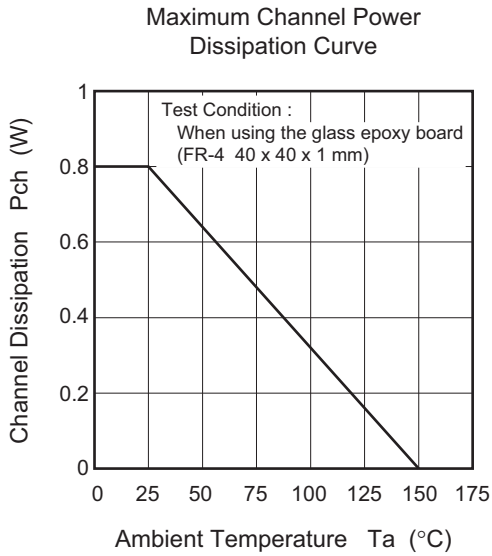
Electrical Characteristics

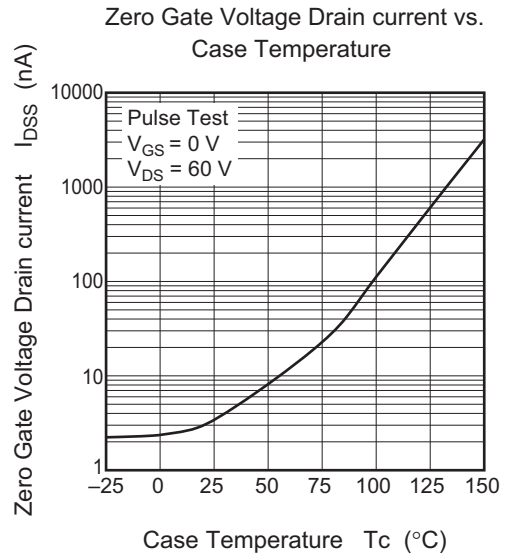
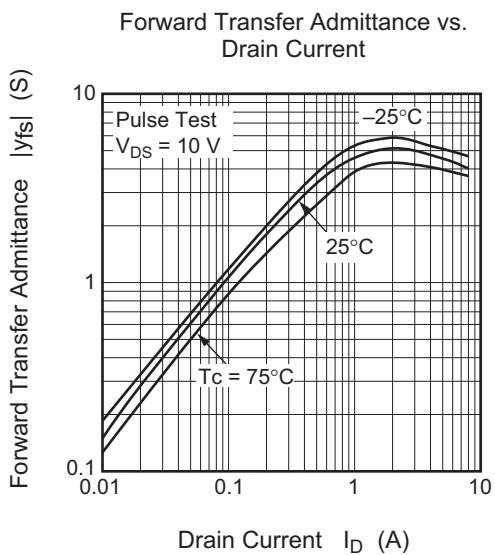
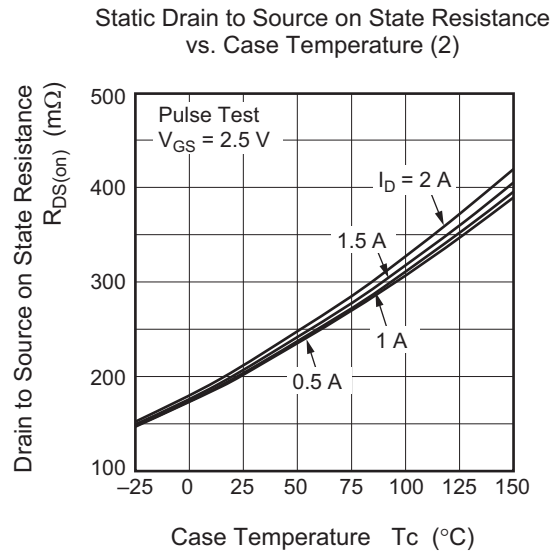
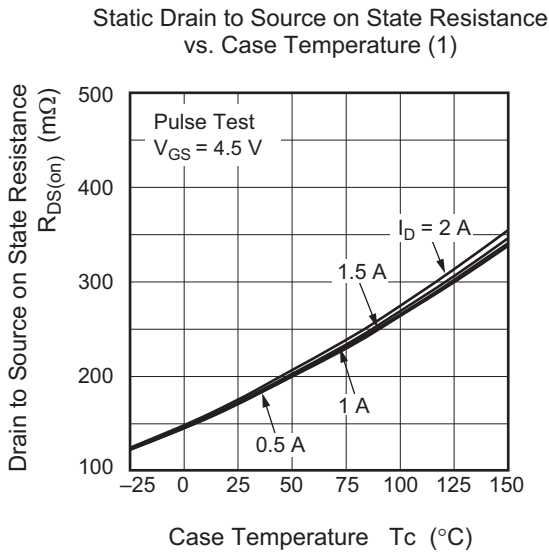
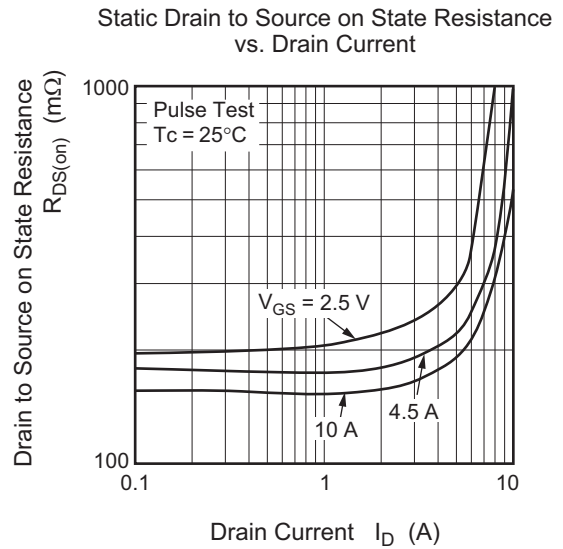
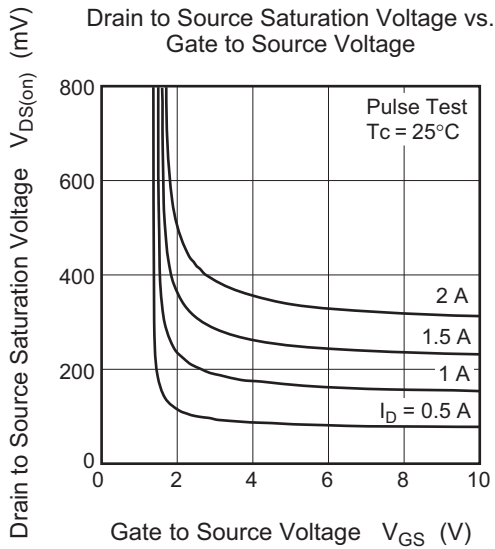
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+12	—	—	V	$I_G = +100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +10 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	1	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	173	225	$\text{m}\Omega$	$I_D = 0.8 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note3}
Drain to source on state resistance	$R_{DS(on)}$	—	207	290	$\text{m}\Omega$	$I_D = 0.8 \text{ A}$, $V_{GS} = 2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	2.3	4	—	S	$I_D = 0.8 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	200	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	25	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	14	—	pF	$f = 1 \text{ MHz}$
Turn - on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = 0.8 \text{ A}$
Rise time	t_r	—	27	—	ns	$V_{GS} = 10 \text{ V}$
Turn - off delay time	$t_{d(off)}$	—	31	—	ns	$R_L = 12.5 \text{ }\Omega$
Fall time	t_f	—	4	—	ns	$R_g = 4.7 \text{ }\Omega$
Total gate charge	Q_g	—	2.2	—	nC	$V_{DD} = 10 \text{ V}$
Gate to Source charge	Q_{gs}	—	0.4	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	0.7	—	nC	$I_D = 1.5 \text{ A}$
Body - drain diode forward voltage	V_{DF}	—	0.8	—	V	$I_F = 1.5 \text{ A}$, $V_{GS} = 0$ ^{Note3}

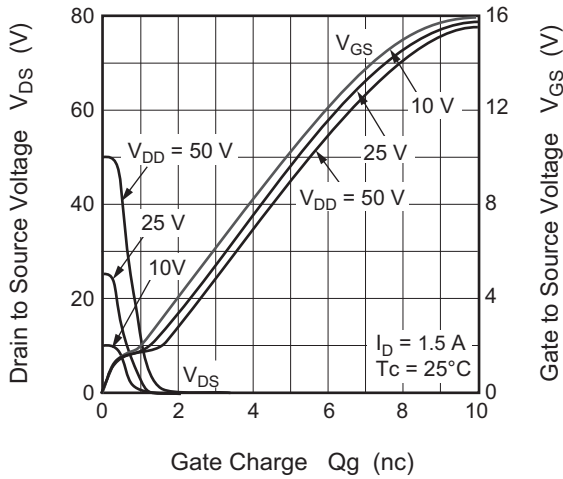
Notes: 3. Pulse test

Main Characteristics

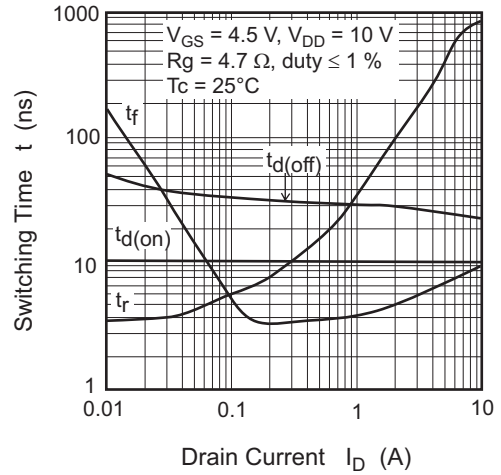




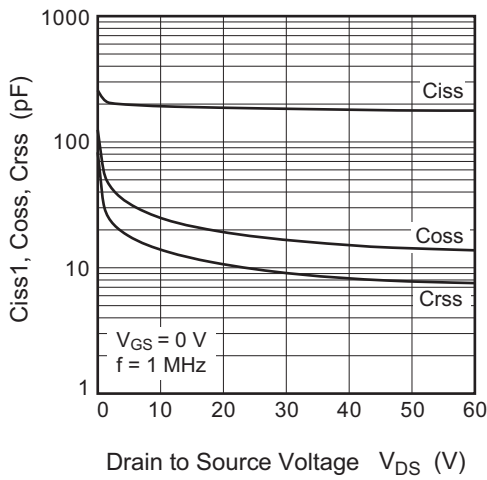
Dynamic Input Characteristics



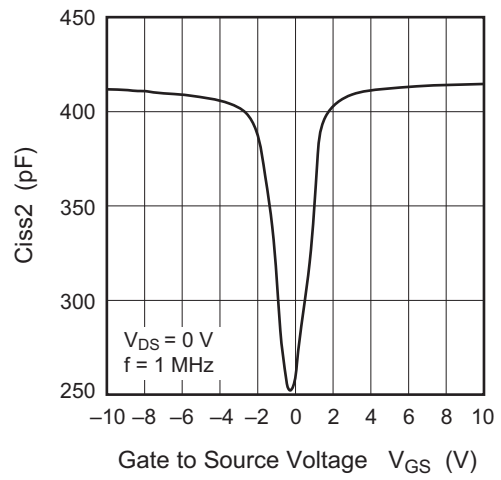
Switching Characteristics



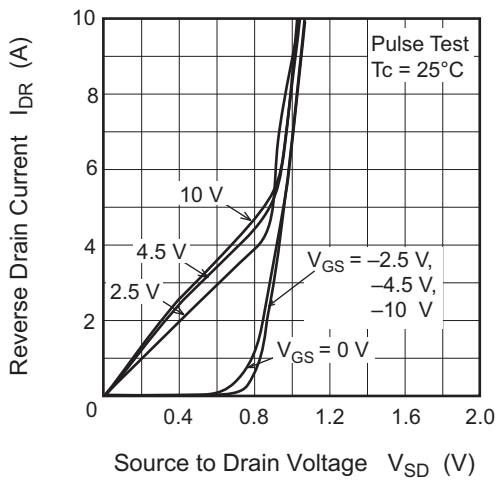
Typical Capacitance vs. Drain to Source Voltage



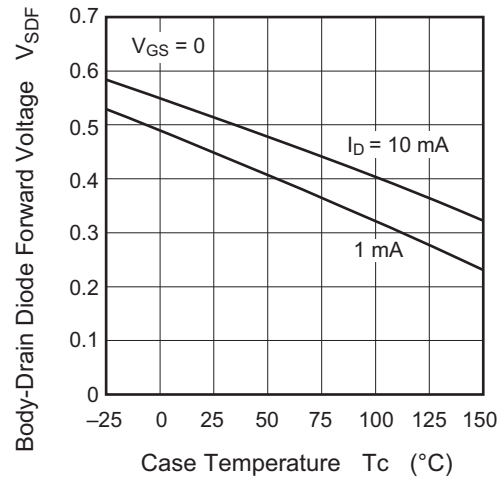
Input Capacitance vs. Gate to Source Voltage

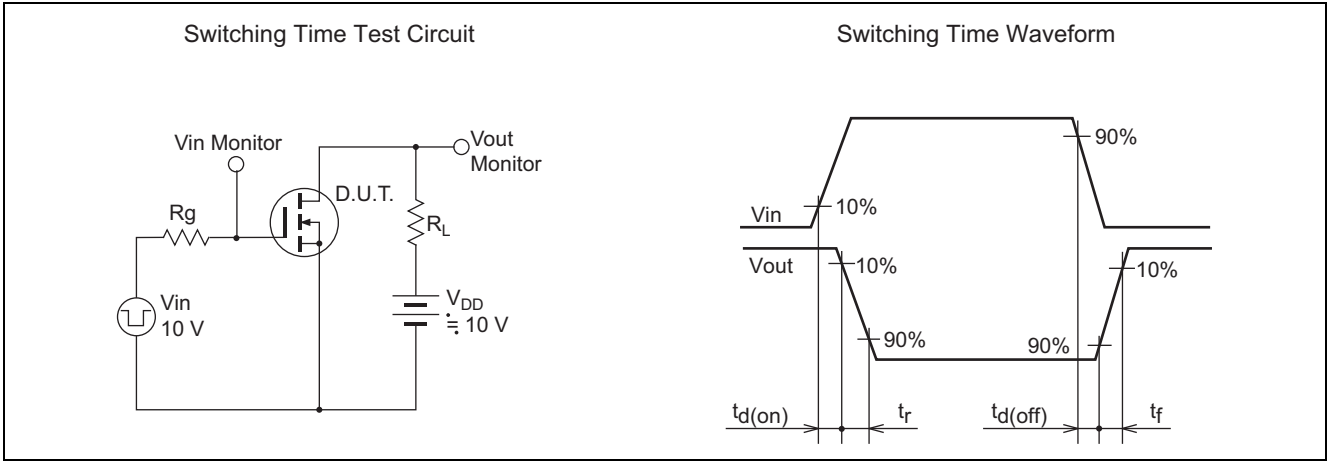


Reverse Drain Current vs. Source to Drain Voltage



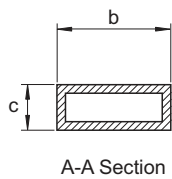
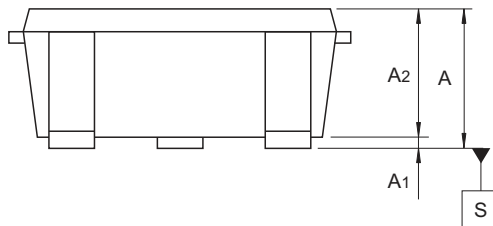
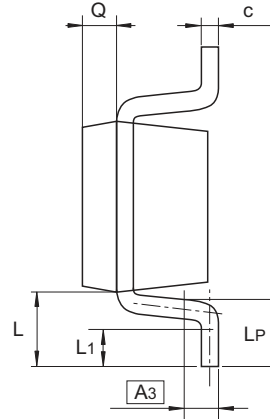
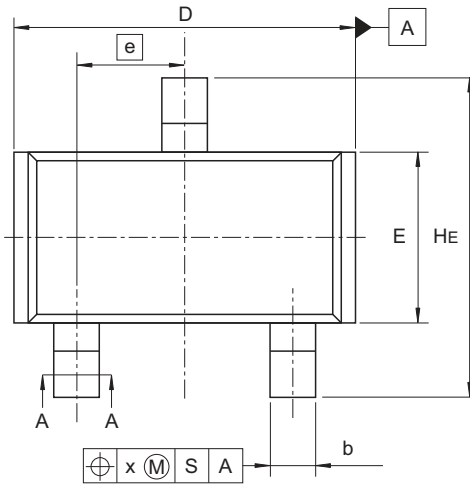
Body-Drain Diode Forward Voltage vs. Case Temperature





Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A1	0	—	0.1
A2	1.0	1.1	1.2
A3	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
e	—	0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L1	0.15	—	0.55
LP	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

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Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQK0606KGDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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Tel: +1-408-586-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 LanGao Rd., Putuo District, Shanghai, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
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Tel: +65-6213-0200, Fax: +65-6213-0300

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Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

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