

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

# SSM3J332R

○Power Management Switch Applications

- 1.8-V drive
- Low ON-resistance:  $R_{DS(ON)} = 144\text{ m}\Omega$  (max) (@ $V_{GS} = -1.8\text{ V}$ )  
 $R_{DS(ON)} = 72.0\text{ m}\Omega$  (max) (@ $V_{GS} = -2.5\text{ V}$ )  
 $R_{DS(ON)} = 50.0\text{ m}\Omega$  (max) (@ $V_{GS} = -4.5\text{ V}$ )  
 $R_{DS(ON)} = 42.0\text{ m}\Omega$  (max) (@ $V_{GS} = -10\text{ V}$ )

**Absolute Maximum Ratings (Ta = 25°C)**

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	$V_{DSS}$	-30	V
Gate-Source voltage	$V_{GSS}$	$\pm 12$	V
Drain current	DC	$I_D$ (Note 1)	-6.0
	Pulse	$I_{DP}$ (Note 1,2)	-24.0
Power dissipation	$P_D$ (Note 3)	$t < 10\text{ s}$	1
			2
Channel temperature	$T_{ch}$	150	°C
Storage temperature range	$T_{stg}$	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

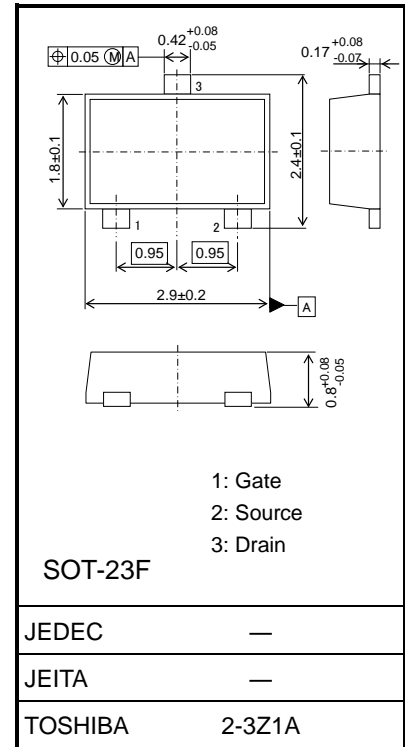
Note 1: The channel temperature should not exceed 150°C during use.

Note 2:  $PW \leq 1\text{ ms}$ , Duty  $\leq 1\%$

Note 3: Mounted on FR4 board.

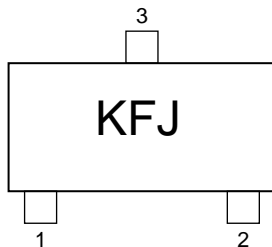
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm<sup>2</sup>)

Unit: mm

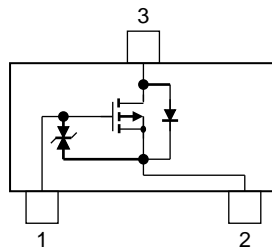


Weight: 11 mg (typ.)

**Marking**



**Equivalent Circuit (Top View)**



Start of commercial production  
2010-08

## Electrical Characteristics (Ta = 25°C)

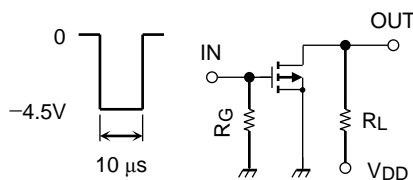
Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit	
Drain-Source breakdown voltage	V (BR) DSS	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 0 V	-30	—	—	V	
	V (BR) DSX	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 8 V (Note 5)	-22	—	—	V	
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V	—	—	-1	μA	
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10 V, V <sub>DS</sub> = 0 V	—	—	±1	μA	
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1 mA	-0.5	—	-1.2	V	
Forward transfer admittance	Y <sub>fs</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -2.5 A (Note 4)	5.7	11.3	—	S	
Drain-source ON-resistance	R <sub>DS</sub> (ON)	I <sub>D</sub> = -5.0 A, V <sub>GS</sub> = -10 V (Note 4)	—	36.0	42.0	mΩ	
		I <sub>D</sub> = -4.0 A, V <sub>GS</sub> = -4.5 V (Note 4)	—	42.5	50.0		
		I <sub>D</sub> = -2.5 A, V <sub>GS</sub> = -2.5 V (Note 4)	—	57.5	72.0		
		I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -1.8 V (Note 4)	—	76.5	144		
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V f = 1 MHz	—	560	—	pF	
Output capacitance	C <sub>oss</sub>		—	80	—		
Reverse transfer capacitance	C <sub>rss</sub>		—	65	—		
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -2.0 A V <sub>GS</sub> = 0 to -4.5 V, R <sub>G</sub> = 10 Ω	—	15	—	ns
	Turn-off time	t <sub>off</sub>		—	75	—	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -6.0 A, V <sub>GS</sub> = -4.5 V	—	8.2	—	nC	
Gate-Source Charge	Q <sub>gs1</sub>		—	1.1	—		
Gate-Drain Charge	Q <sub>gd</sub>		—	2.2	—		
Drain-Source forward voltage	V <sub>D5F</sub>	I <sub>D</sub> = 6.0 A, V <sub>GS</sub> = 0 V (Note 4)	—	0.90	1.2	V	

Note4: Pulse test

Note5: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

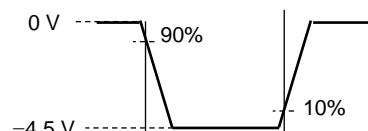
## Switching Time Test Circuit

### (a) Test Circuit

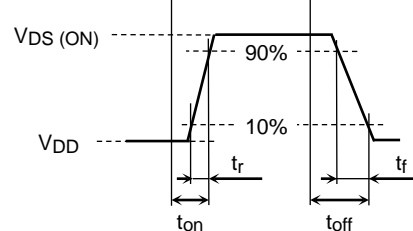


V<sub>DD</sub> = -15 V  
R<sub>G</sub> = 10 Ω  
Duty ≤ 1%  
V<sub>IN</sub>: t<sub>r</sub>, t<sub>f</sub> < 5 ns  
Common Source  
T<sub>a</sub> = 25°C

### (b) V<sub>IN</sub>



### (c) V<sub>OUT</sub>



## Notice on Usage

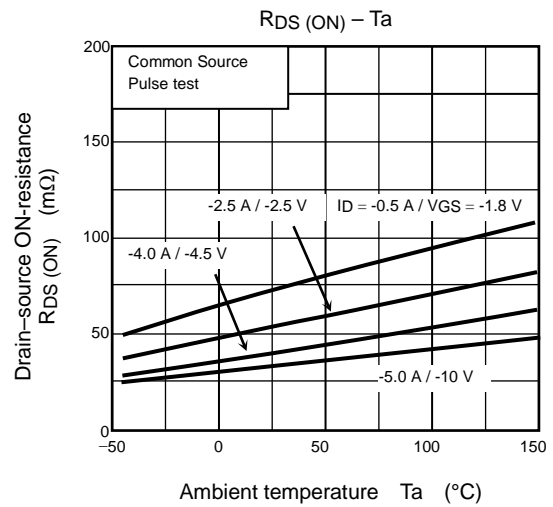
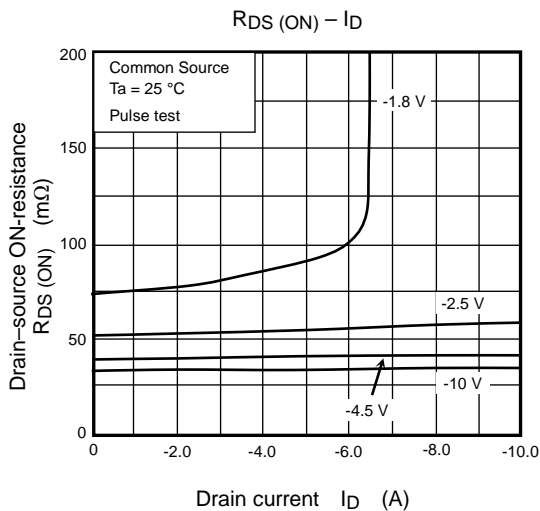
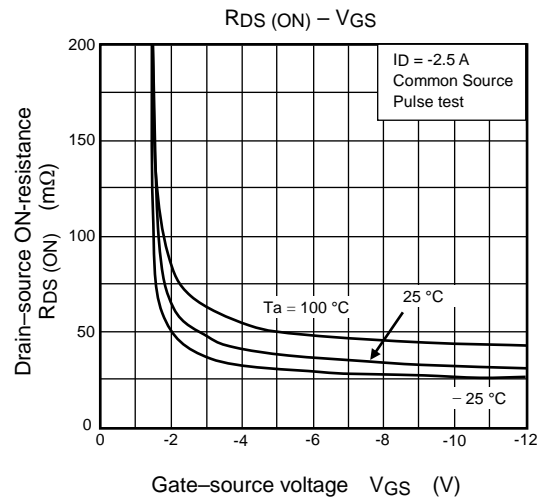
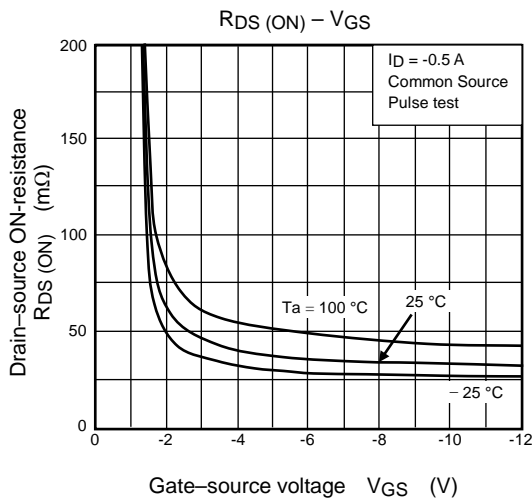
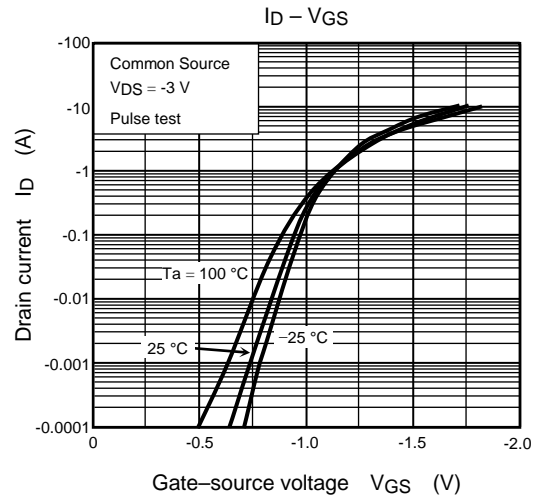
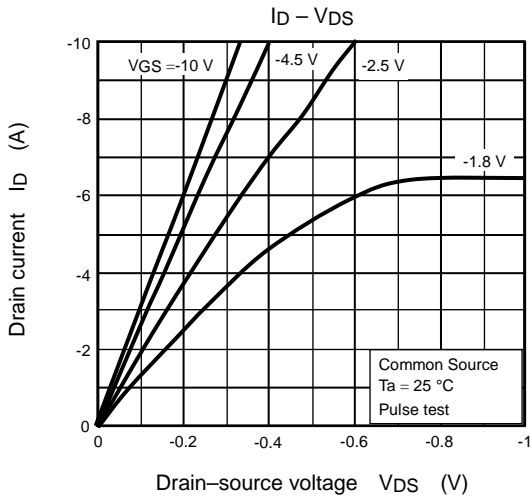
Let V<sub>th</sub> be the voltage applied between gate and source that causes the drain current (I<sub>D</sub>) to be low (-1 mA for the SSM3J332R). Then, for normal switching operation, V<sub>GS(on)</sub> must be higher than V<sub>th</sub>, and V<sub>GS(off)</sub> must be lower than V<sub>th</sub>. This relationship can be expressed as: V<sub>GS(off)</sub> < V<sub>th</sub> < V<sub>GS(on)</sub>.

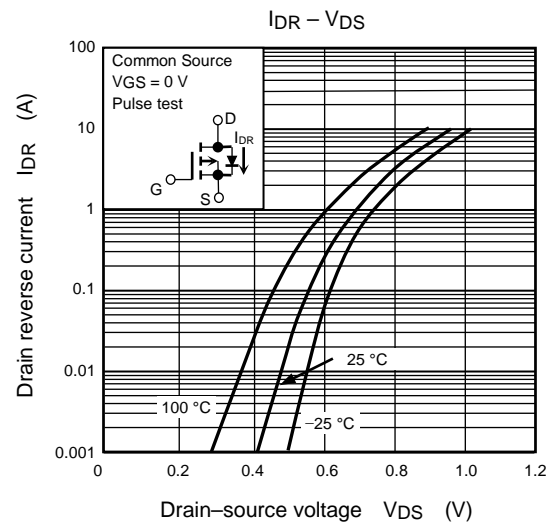
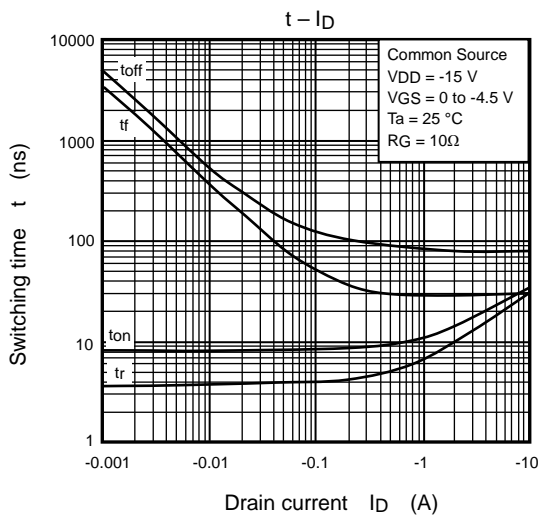
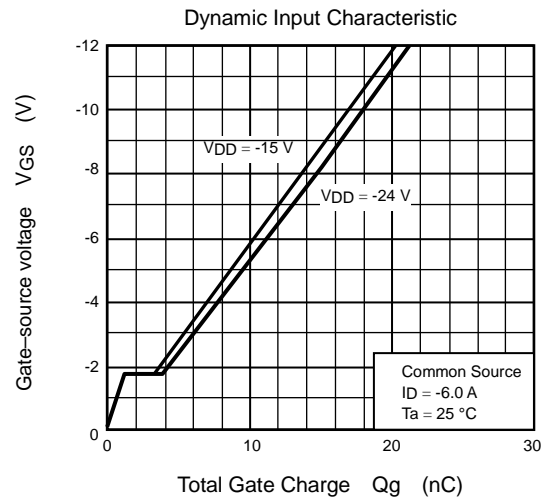
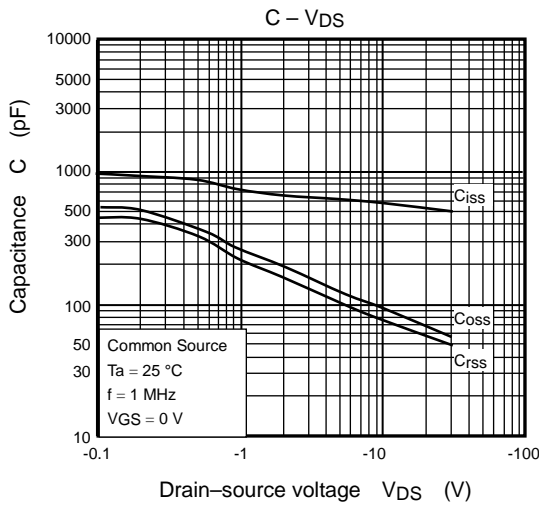
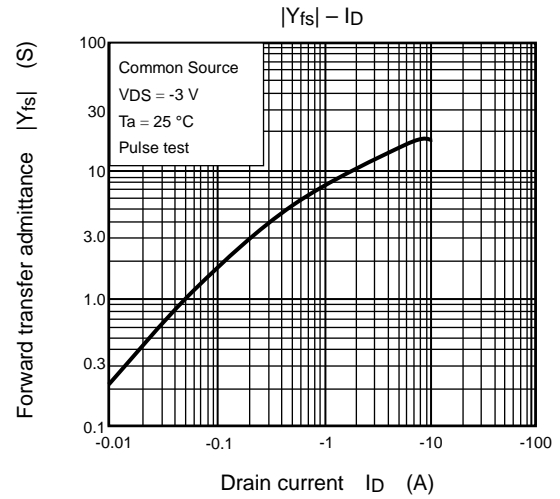
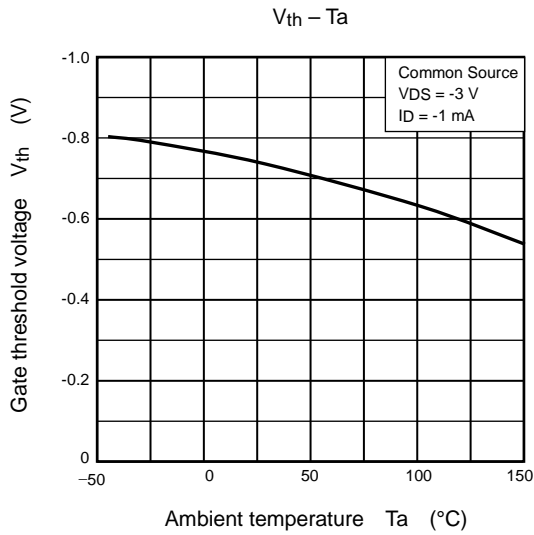
Take this into consideration when using the device.

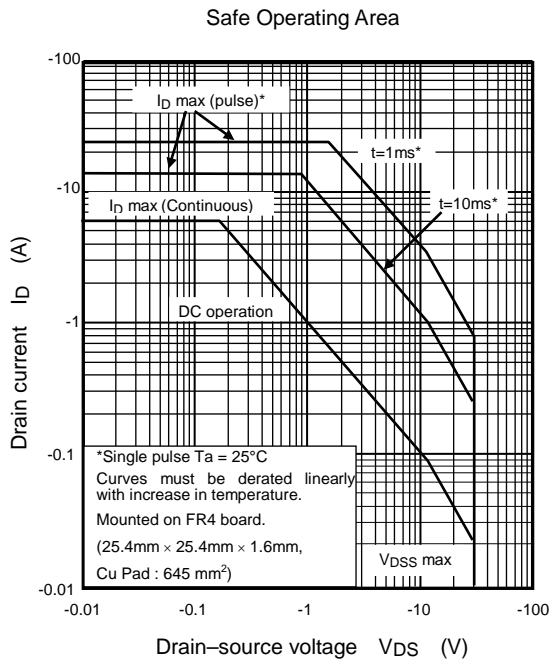
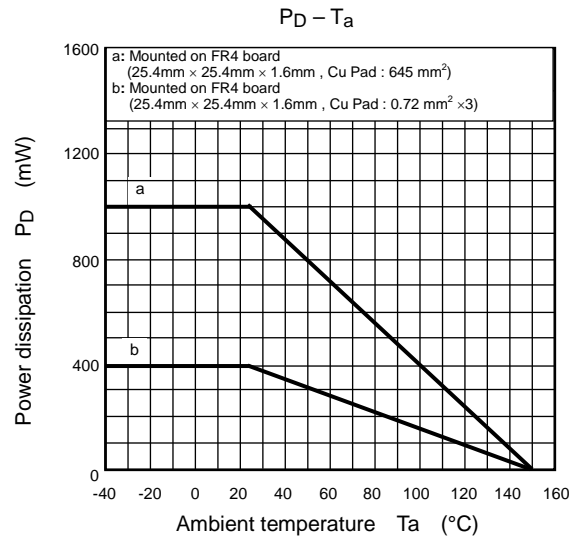
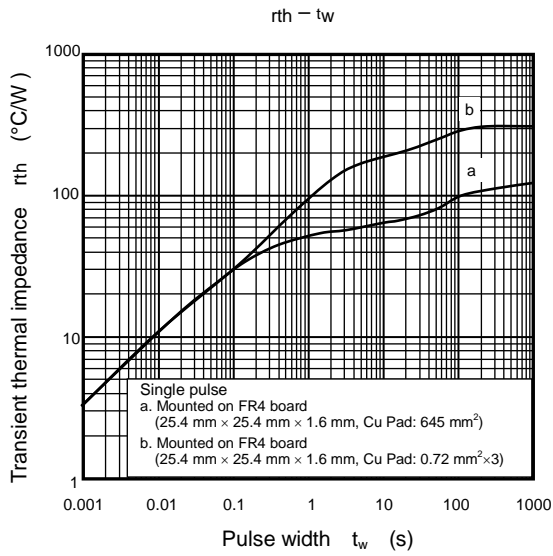
## Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance R<sub>th</sub> (ch-a) and power dissipation P<sub>D</sub> vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration







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