Dual-Channel Synchronous DC/DC Step-Down Controller with 5V/3.3V LDOs

General Description

The RT8230A/B/C/D/E is a dual-channel step-down, controller generating supply voltages for battery-powered systems. It includes two Pulse-Width Modulation (PWM) controllers adjustable from 2V to 5.5V, and two fixed 5V/3.3V linear regulators. Each linear regulator provides up to 100mA output current. The 5V linear regulator supplies power to the PWM drivers. The RT8230A/B/C/D/E includes on-board power-up sequencing, a power-good output, internal soft-start, and soft-discharge output that prevents negative voltage during shutdown.

A constant current ripple PWM control scheme operates without sense resistors and provides 100ns response to load transient. To eliminate noise in audio applications, an ultrasonic mode is included, which maintains the switching frequency above 25kHz. Moreover, the diode-emulation mode maximizes efficiency for light load applications. The RT8230A/B/C/D/E is available in the WQFN-20L 3x3 package.

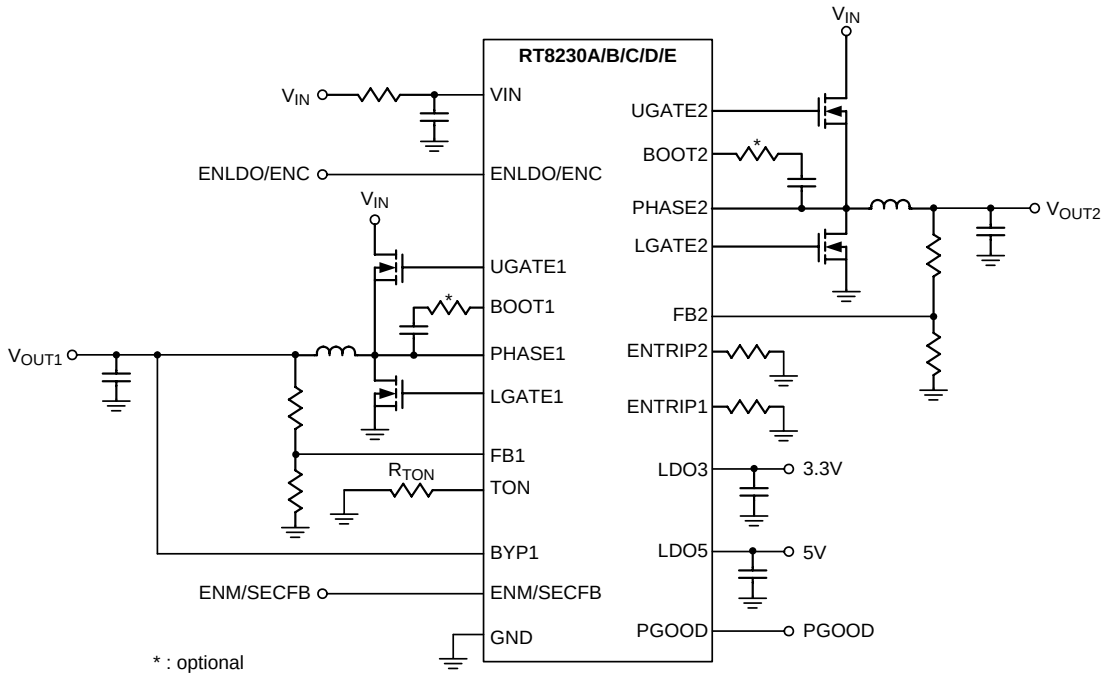
Features

- **Maximum Duty Up to 96%**
- **CCRCOT Control with 100ns Load Step Response**
- **Wide Input Voltage Range : 5V to 25V**
- **Dual Adjustable Outputs from 2V to 5.5V**
- **Fixed 3.3V and 5V LDO Output : 100mA**
- **1% Accuracy on 3.3V LDO Output**
- **Frequency Adjustable Via TON Setting**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing**
- **Adjustable Current Limit Combined with Enable Control**
- **Internal Soft-Start and Soft-Discharge**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook and Sub-Notebook Computers
- 2-Cell, 3-Cell and 4-Cell Li+ Battery-Powered Devices

Simplified Application Circuit



Ordering Information

RT8230A/B/C/D/E□□

- Package Type
  QW : WQFN-20L 3x3 (W-Type)
- Lead Plating System
  G : Green
  (Halogen Free and Pb Free)
- Pin Function With
  A : ENM+ENLDO
  B/D : SECFB+ENLDO
  C/E : SECFB+ENC

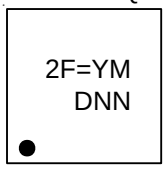
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8230AGQW



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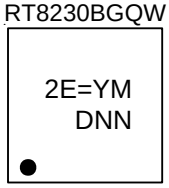
YMDNN : Date Code

RT8230BGQW



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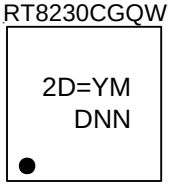

2D= : Product Code
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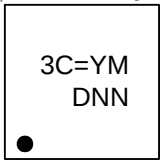
RT8230DGQW



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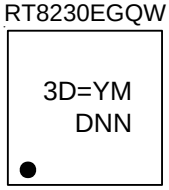

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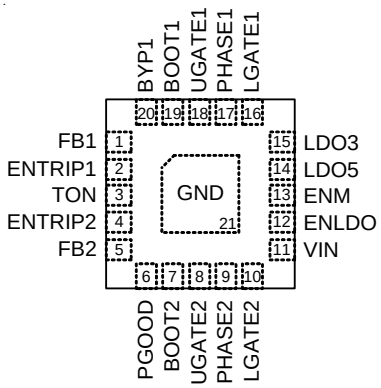
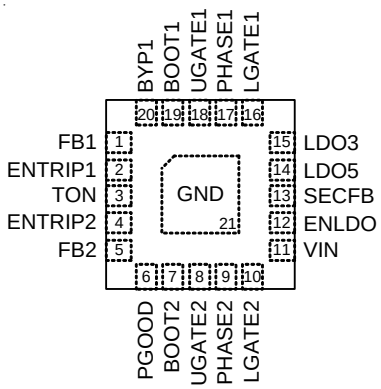
Pin Configurations

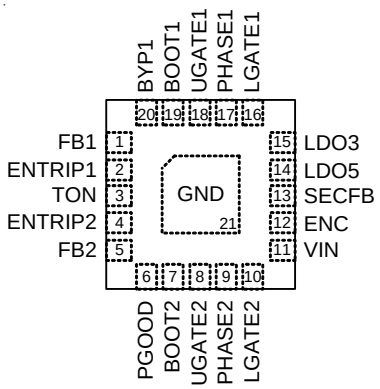
(TOP VIEW)



RT8230A



RT8230B/D



RT8230C/E

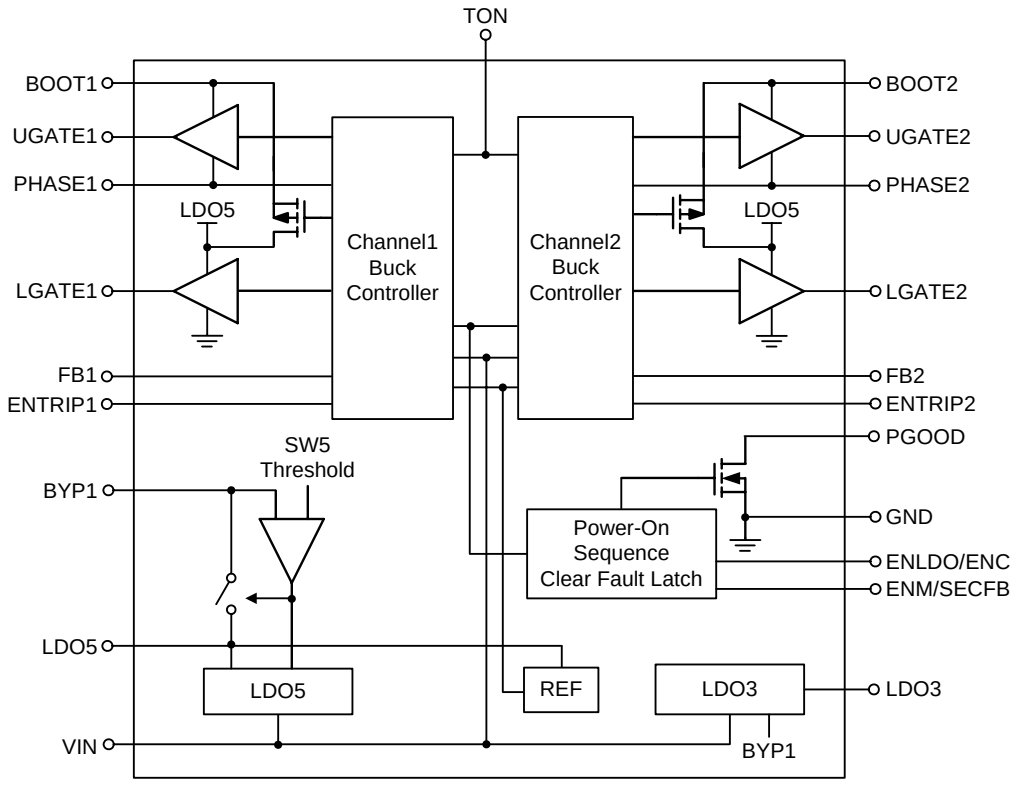
WQFN-20L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB1	Feedback Voltage Input for Channel 1. Connect FB1 to a resistive voltage divider from VOUT1 to GND to adjust output from 2V to 5.5V.
2	ENTRIP1	Enable and Current Limit Setting for Channel 1. There is an internal 5μA current source to the ENTRIP1 pin. Connect a resistor to GND to set the threshold between 0.2V and 3V for channel 1 current limit. The GND – PHASE1 current limit threshold is 1/10th the voltage on the ENTRIP1 pin.
3	TON	Switching Frequency Setting. Connect a resistor to GND to adjust switching frequency.
4	ENTRIP2	Enable and Current Limit Setting for Channel 2. There is an internal 5μA current source to the ENTRIP2 pin. Connect a resistor to GND to set the threshold between 0.2V and 3V for channel 2 current limit. The GND – PHASE2 current limit threshold is 1/10th the voltage on the ENTRIP2 pin.
5	FB2	Feedback Voltage Input for Channel 2. Connect FB2 to a resistive voltage-divider from VOUT2 to GND to adjust output from 2V to 5.5V.
6	PGOOD	Power Good Output for Channel 1 and Channel 2. (Logical AND)
7	BOOT2	Bootstrap Supply for Channel 2 High-Side Gate Driver. Connect to an external capacitor according to the typical application circuits.
8	UGATE2	Gate Drive Output for Channel 2 High-Side MOSFET.
9	PHASE2	Switch Node of Channel 2 MOSFETs. PHASE2 is the return rail for the UGATE2 high-Side gate driver.
10	LGATE2 (RT8230A/B/E)	Gate Drive Output for Channel 2 Low-Side MOSFET.
	LGATE2 (RT8230C/D)	Gate Drive Output for Channel 2 Low-Side MOSFET and Charge Pump CLK. The CLK frequency will become fast to pull up charge pump voltage when the SECFB voltage is low to 2V.
11	VIN	Supply Voltage Input.
12	ENLDO (RT8230A/B/D)	Master Enable Control Input. The LDO5/LDO3 are enabled if it is within logic high level and disable if it is less than the logic low level.
	ENC (RT8230C/E)	Master Enable Control Input. The channels are enabled if it is within logic high level and disable if it is less than the logic low level.
13	ENM (RT8230A)	Mode Selection with Enable Control Input. Pull up to LDO5 (Ultrasonic mode) or LDO3 (DEM) to turn on both switch channels. Short to GND for shutdown.
	SECFB (RT8230B/C/D/E)	Feedback Voltage Input for Charge Pump. The SECFB is used to monitor the optional external 14V charge pump. Connect a resistive voltage divider from 14V charge pump output to GND to detect the output.
14	LDO5	5V Linear Regulator Output. It is also the supply voltage for the low-side MOSFET driver and analog supply control circuits.
15	LDO3	3.3V Linear Regulator Output.
16	LGATE1 (RT8230A/C/D)	Gate Drive Output for Channel 1 Low-Side MOSFET.
	LGATE1 (RT8230B/E)	Gate Drive Output for Channel 1 Low-Side MOSFET and Charge Pump CLK. The CLK frequency will become fast to pull up charge pump voltage when the SECFB voltage is low to 2V.

Pin No.	Pin Name	Pin Function
17	PHASE1	Switch Node of Channel 1 MOSFETs. PHASE1 is the return rail for the UGATE1 high-Side gate driver.
18	UGATE1	Gate Drive Output for Channel 1 High-Side MOSFET.
19	BOOT1	Bootstrap Supply for Channel 1 High-Side Gate Driver. Connect to an external capacitor according to the typical application circuits.
20	BYP1	Switch Over Source Voltage Input for LDO5.
21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

The RT8230A/B/C/D/E includes two constant on-time synchronous step-down controllers and two linear regulators.

Buck Controller

In normal operation, the high-side N-MOSFET is turned on when the output is lower than VREF, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Soft-Start (SS)

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

PGOOD

The power good output is an open-drain architecture. When the two channels soft-start are both finished, the PGOOD open-drain output will be high impedance.

Current Limit

The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the under-voltage protection threshold, inducing IC shutdown.

Over-Voltage Protection (OVP) & Under-Voltage Protection (UVP)

The two channel output voltages are continuously monitored for over-voltage and under-voltage conditions. When the output voltage exceeds OVP threshold (113% of VOUT), UGATE goes low and LGATE is forced high; when it is less than 52% of reference voltage, under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until ENTRIP is reset or LDO5 is re-supplied.

LDO5 and LDO3

When the VIN voltage exceed the POR rising threshold, the LDO5 and LDO3 can be power on by ENLDO.

The linear regulator LDO5 and LDO3 provide 5V and 3.3V regulated output.

Switching Over

The BYP1 is connected to the channel 1 output. After the channel 1 output voltage exceeds the set threshold (4.66V), the output will be bypassed to the LDO5 output to maximize the efficiency.

Absolute Maximum Ratings (Note 1)

- VIN, ENLDO, ENC to GND ---------- –0.3V to 30V
- BOOTx to PHASEx ---------- –0.3V to 6V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - <20ns ---------- –8V to 38V
- UGATEx to PHASEx
  - DC ---------- –0.3V to (LDO5 + 0.3V)
  - <20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to (LDO5 + 0.3V)
  - <20ns ---------- –2.5V to 7.5V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-20L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  - WQFN-20L 3x3, θ_{JA} ---------- 30°C/W
  - WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{ENLDO} = V_{ENC} = 5V, $V_{ENTRIP1}$ = $V_{ENTRIP2}$ = 2V, No load, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Power On Reset	POR_{VIN}	Rising Threshold	--	4.6	5	V
		Falling Threshold	3.2	3.7	--	
VIN Shutdown Supply Current	I_{VIN_SHDN}	V_{ENLDO} = GND	--	10	25	μA
VIN Standby Supply Current	I_{VIN_SBY}	Not Switching, V_{ENLDO} = 5V, V_{ENM} = GND	--	50	80	μA
BYP1 Quiescent Current	I_{Q_nosw}	V_{FBx} = 2.05V	--	150	200	μA
Buck Output and FB Voltage						
FBx Valley Trip Voltage	V_{FBx}	CCM Operation	1.98	2	2.02	V
SECFB Voltage	V_{SECFB}		1.92	2	2.08	V
PHASEx Discharge Current	I_{DCHGx}	V_{PHASEx} = 0.5V	5	8	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Frequency Control						
Switching Frequency	f_{SWx}	V_{IN} = 20V, V_{OUT1} = 5V, R_{TON} = 100k	240	300	360	kHz
		V_{IN} = 20V, V_{OUT2} = 3.33V, R_{TON} = 100k	280	355	430	
Minimum Off-Time	T_{LGATEx}	V_{FBX} = 1.9V	--	275	350	ns
Ultrasonic Mode Frequency	f_{ASM}	V_{ENM} = LDO5	25	33	--	kHz
Soft-Start						
Soft-Start Time	T_{SSX}	From ENTRIP Enable	--	0.8	--	ms
Current Sense						
ENTRIPx Source Current	$I_{ENTRIPx}$	$V_{ENTRIPx}$ = 0.9V	4.5	5	5.5	μA
ENTRIPx Current Temperature Coefficient	$TC_{IENTRIPx}$	In Comparison with 25°C	--	4700	--	ppm/°C
Zero-Current Threshold	V_{ZC}	V_{FBx} = 2.05V, GND – PHASEx	--	1	--	mV
Internal Regulator						
LDO5 Output Voltage	V_{LDO5}	V_{IN} = 12V, No Load	4.9	5	5.1	V
		V_{IN} > 7V, I_{LDO5} < 100mA	4.8	5	5.1	
		V_{IN} > 5.5V, I_{LDO5} < 35mA	4.8	5	5.1	
		V_{IN} > 5V, I_{LDO5} < 20mA	4.5	4.75	5.1	
LDO3 Output Voltage	V_{LDO3}	V_{IN} = 12V, No Load	3.267	3.3	3.333	V
		V_{IN} > 7V, I_{LDO3} < 100mA	3.217	3.3	3.383	
		V_{IN} > 5.5V, I_{LDO3} < 35mA	3.267	3.3	3.333	
		V_{IN} > 5V, I_{LDO3} < 20mA	3.217	3.3	3.383	
LDO5 Output Current	I_{LDO5}	V_{LDO5} = 4.5V, V_{BYP1} = GND, V_{IN} = 7.4V	100	175	--	mA
LDO3 Output Current	I_{LDO3}	V_{LDO3} = 3V, V_{IN} = 7.4V	100	175	--	mA
LDO5 Switchover Threshold to BYP1	V_{SWTH}	Rising Edge At BYP1 Regulation Point	4.4	4.66	4.79	V
LDO5 Switchover Equivalent Resistance	R_{SW}	LDO5 to BYP1, 10mA	--	1.5	3	Ω
UVLO						
LDO5 UVLO Threshold	V_{UVLO5}	Rising Edge	--	4.3	4.5	V
		Falling Edge	3.7	3.9	4.1	
LDO3 UVLO Threshold	V_{UVLO3}	Controllers Off	--	2.5	--	
Power Good						
PGOOD Threshold	V_{PGxTH}	PGOOD Detect, V_{FBx} Rising Edge	87	92.5	96	%
		Hysteresis	--	8	--	
PGOOD Leakage Current		High State, V_{PGOOD} = 5.5V	--	--	1	μA
PGOOD Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
Fault Detection						
OVP Trip Threshold	V_{OVP}	FBx with Respect to Internal Reference	109	113	117	%
OVP Propagation Delay			--	1	--	μs
UVP Trip Threshold	V_{UVP}	UVP Detect, FBx Falling Edge	47	52	57	%
UVP Shutdown Blanking Time	t_{SHDN_UVP}	From ENTRIPx Enable	--	1.6	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}		--	150	--	°C
Thermal Shutdown Hysteresis			--	10	--	°C
Logic Inputs						
ENTRIPx Input Voltage	$V_{ENTRIPx}$	Controller On	0.2	--	3	V
		Controller Off	4.5	--	--	
ENLDO Input Voltage (RT8230A/B/D)	V_{ENLDO}	Shutdown	--	--	0.4	V
		Enable	1	--	--	
		ENLDO Floating, Default Enable	1.6	2.4	3.3	
ENLDO Current (RT8230A/B/D)	I_{ENLDO}	V_{ENLDO} = 0.2V, Source	--	1	5	μA
		V_{ENLDO} = 5V, Sink	--	1	5	
ENC Input Voltage (RT8230C/E)	V_{ENC}	Shutdown	--	--	0.4	V
		Enable	1	--	--	
		ENC Floating, Default Enable	1.6	2.4	3.3	
ENM Input Voltage (RT8230A)	V_{ENM}	Buck Controller Off Level	--	--	0.8	V
		Buck Controller On Level, ASM Operation (only for CH1, CH2 keep on DEM)	1.2	--	1.8	
		Buck Controller On Level, DEM Operation	2.3	--	3.6	
		Buck Controller On Level, ASM Operation	4.5	--	--	
SECFB Input Voltage (RT8230B/C/D/E)	V_{SECFB}	Buck Controller On Level, ASM Operation (RT8230B/E for CH1, RT8230C/D for CH2)	1.2	--	1.8	V
		Buck Controller On Level, DEM Operation	2.3	--	3.6	
		Buck Controller On Level, ASM Operation	4.5	--	--	
Internal Boost Switch						
Internal Boost Switch On-Resistance		LDO5 to BOOTx	--	80	--	Ω
Power MOSFET Drivers						
UGATEx On-Resistance		High State, $V_{BOOTx} - V_{UGATEx}$ = 0.25V, $V_{BOOTx} - V_{PHASEx}$ = 5V	--	3	--	Ω
		Low State, $V_{UGATEx} - V_{PHASEx}$ = 0.25V, $V_{BOOTx} - V_{PHASEx}$ = 5V	--	2	--	
LGATEx On-Resistance		High State, $V_{LDO5} - V_{LGATEx}$ = 0.25V, V_{LDO5} = 5V	--	3	--	Ω
		Low State, V_{LGATEx} – GND = 0.25V	--	1	--	
Dead-Time		LGATEx Rising	--	20	--	ns
		UGATEx Rising	--	30	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

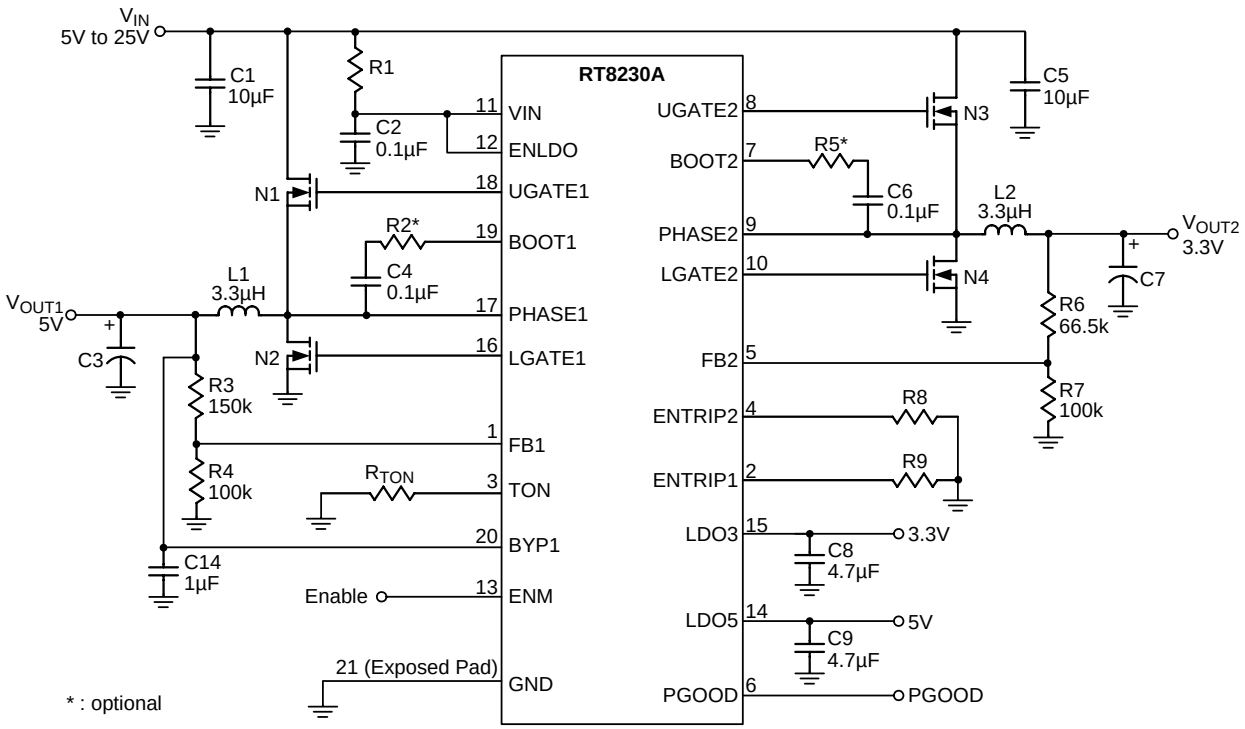
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

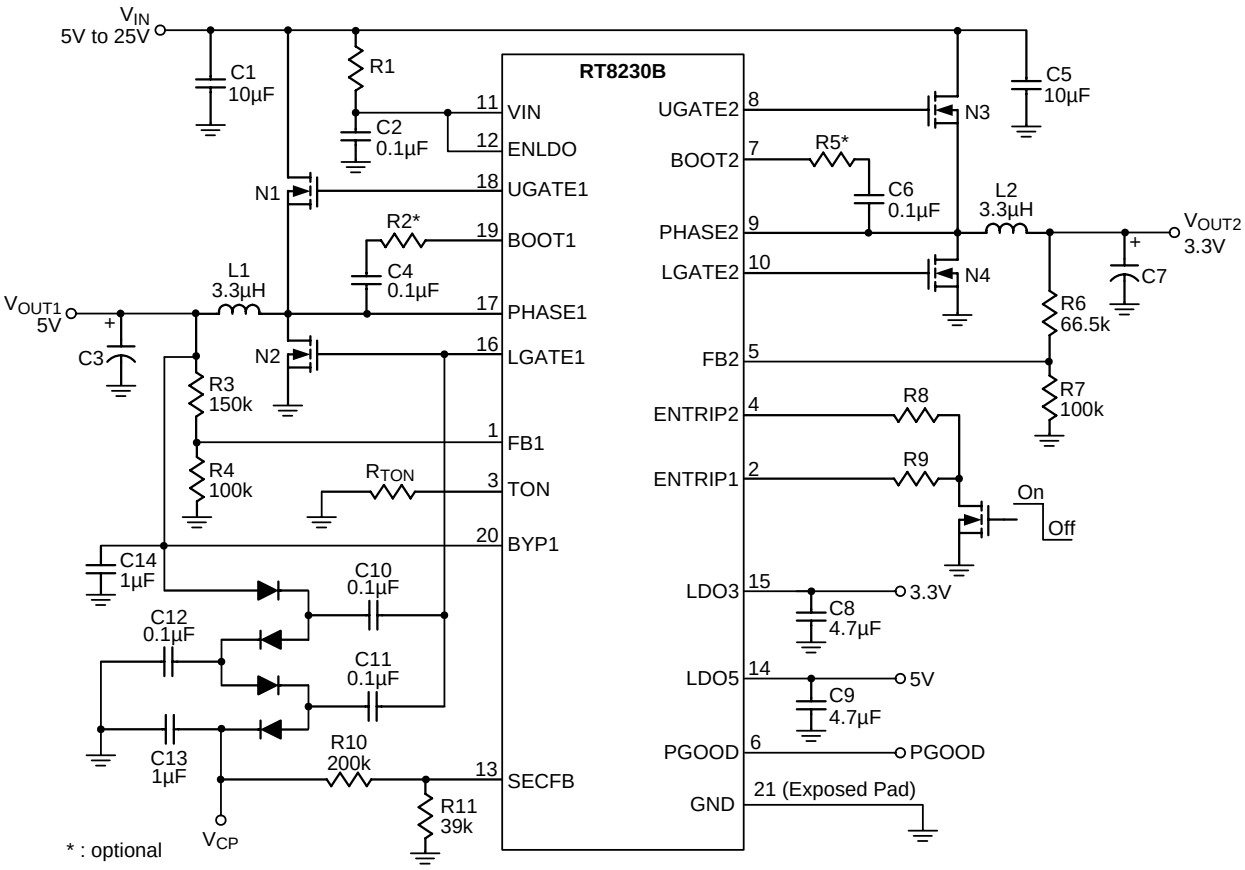
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

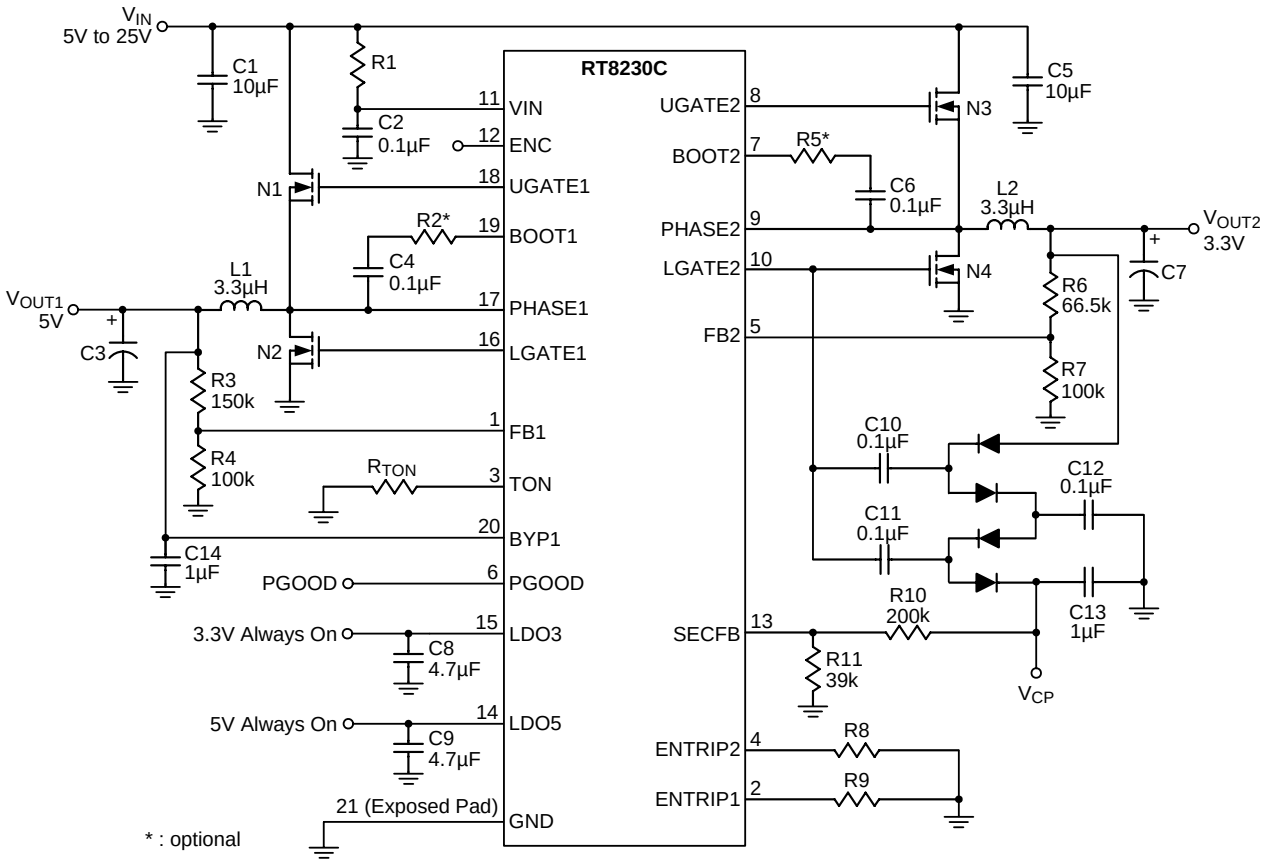
Note 4. The device is not guaranteed to function outside its operating conditions.

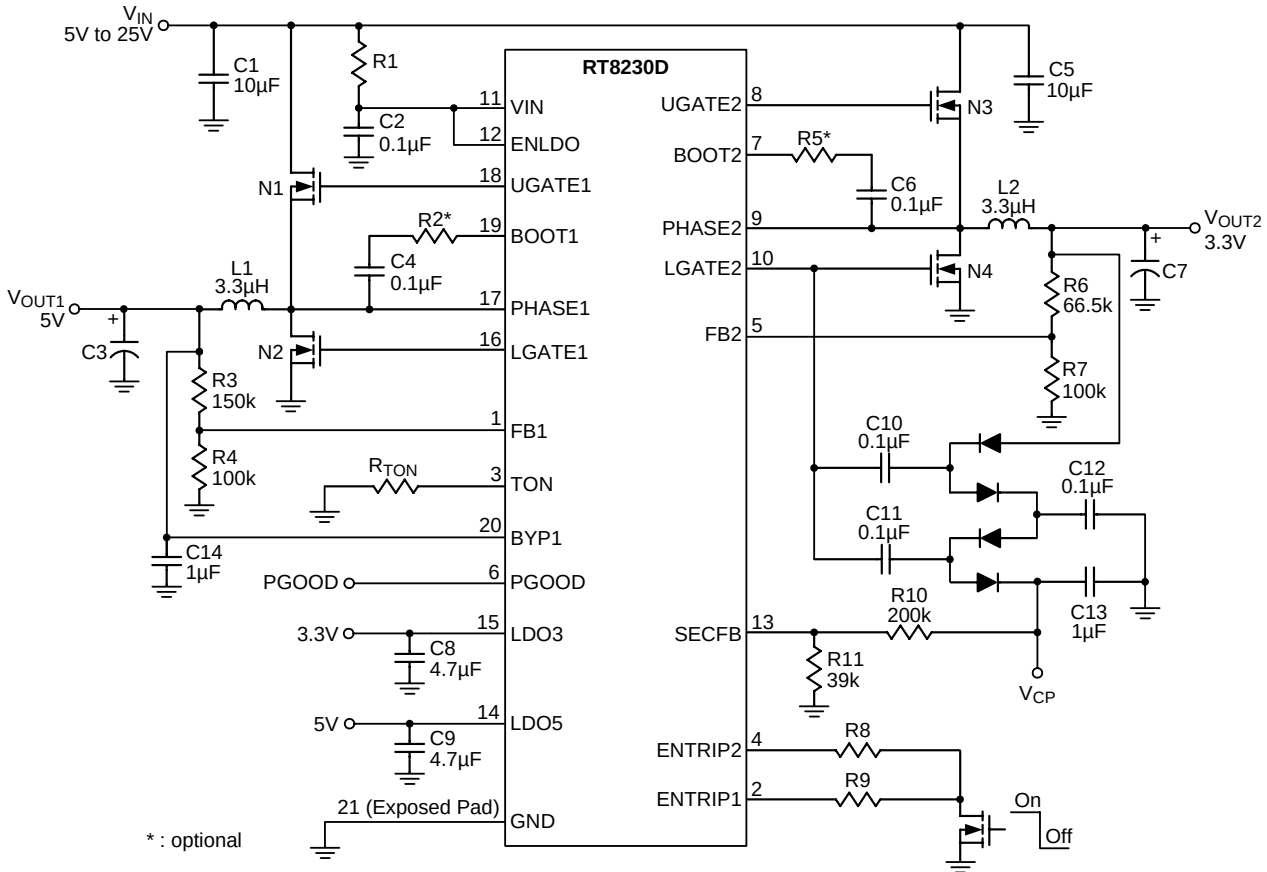
Note 5. Not production tested. Test condition is same with electrical characteristics using application circuit.

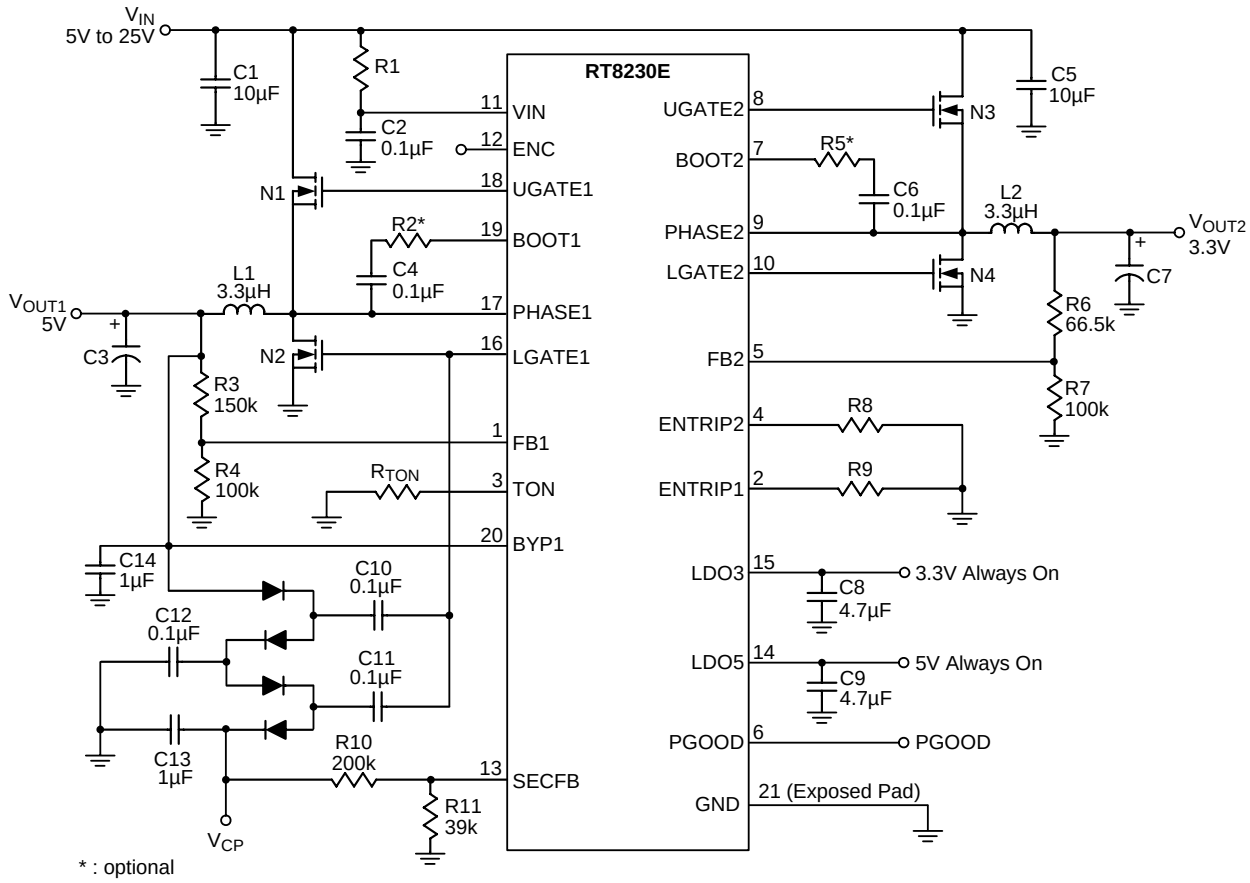
Typical Application Circuit



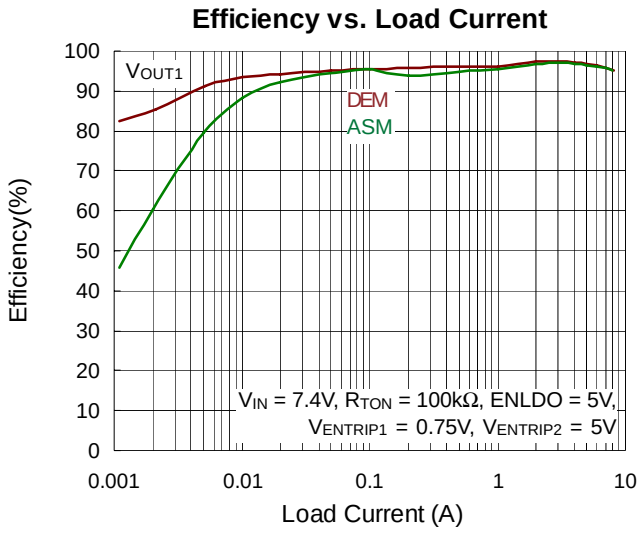


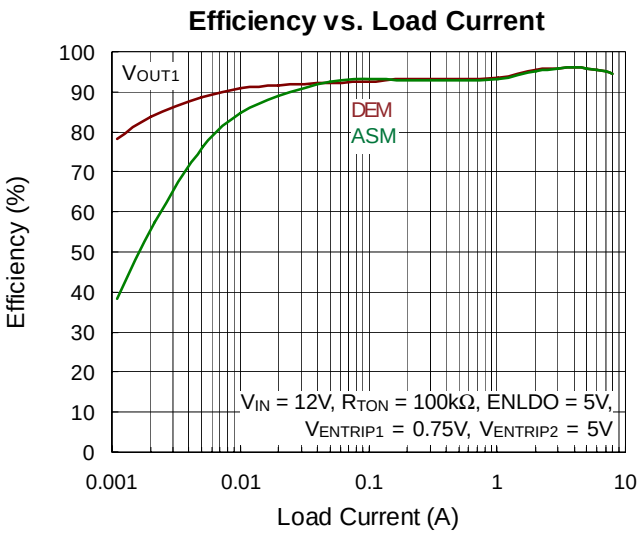


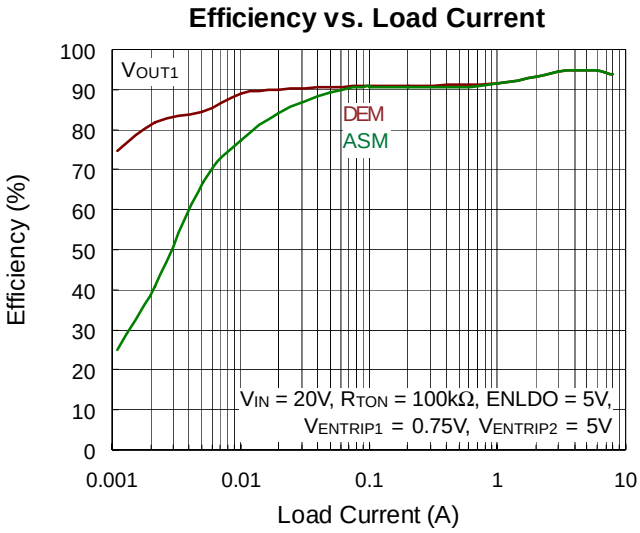


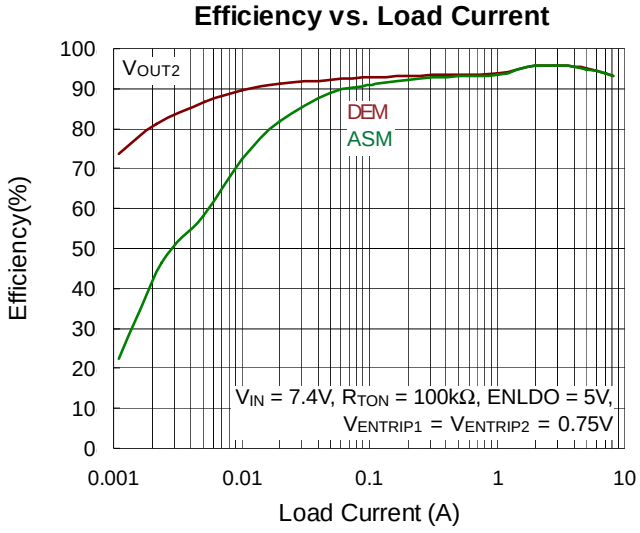


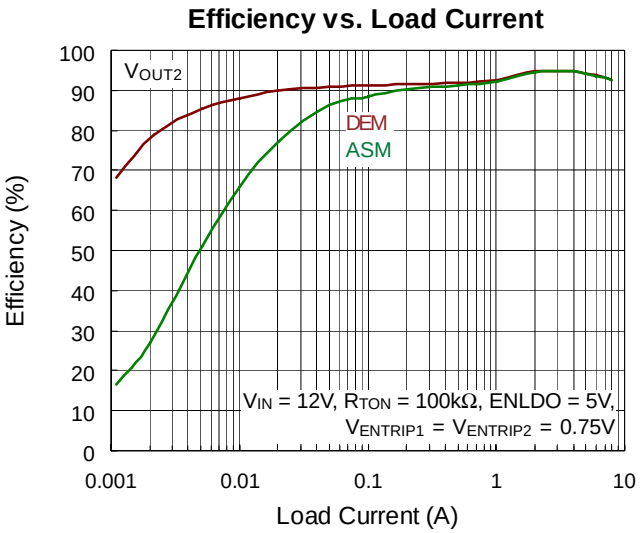
Typical Operating Characteristics

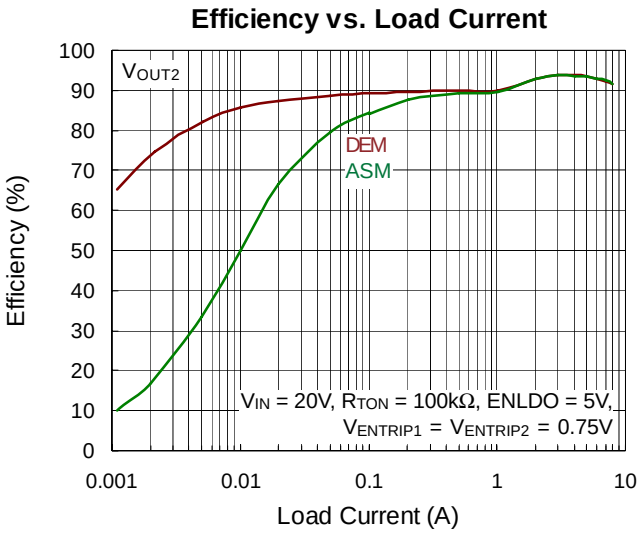




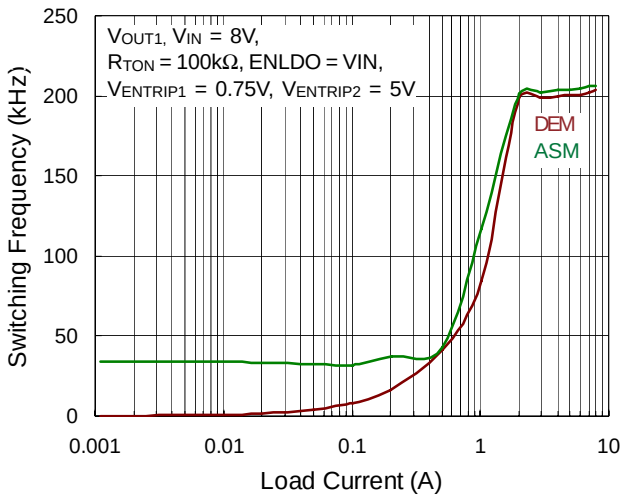




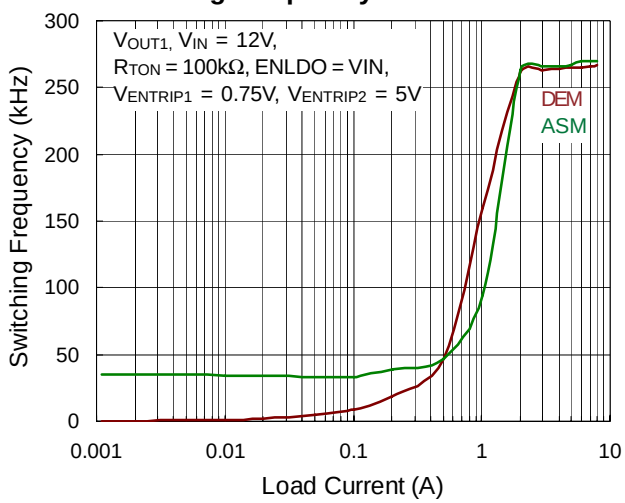




Switching Frequency vs. Load Current



Switching Frequency vs. Load Current



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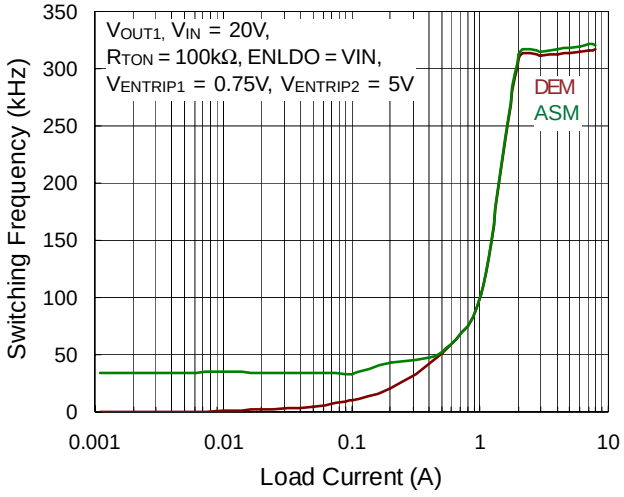

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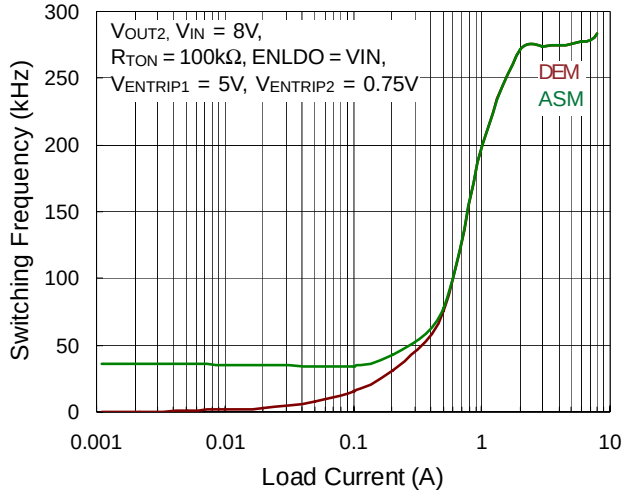

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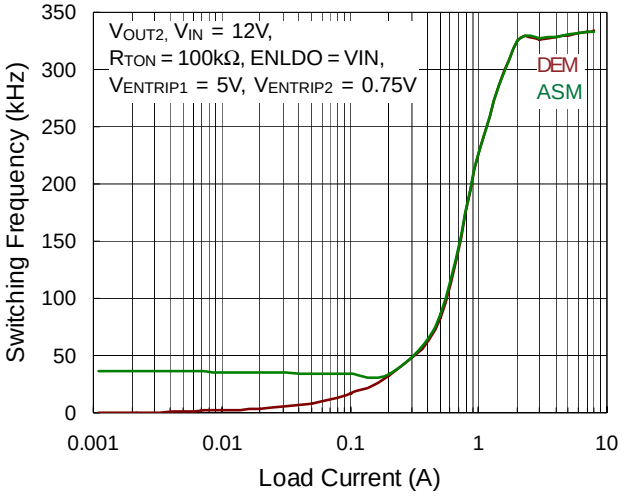

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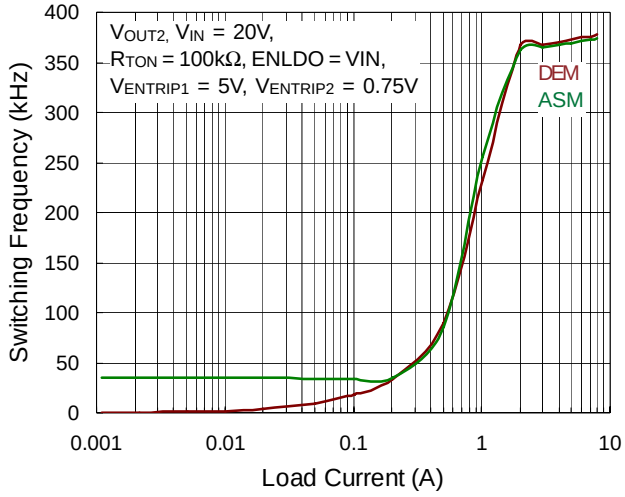
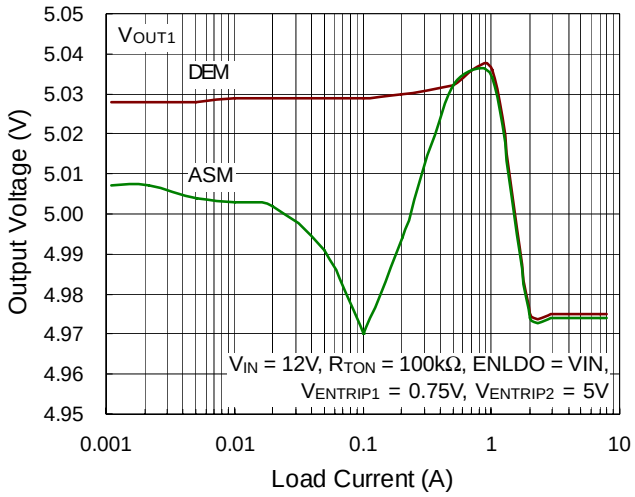
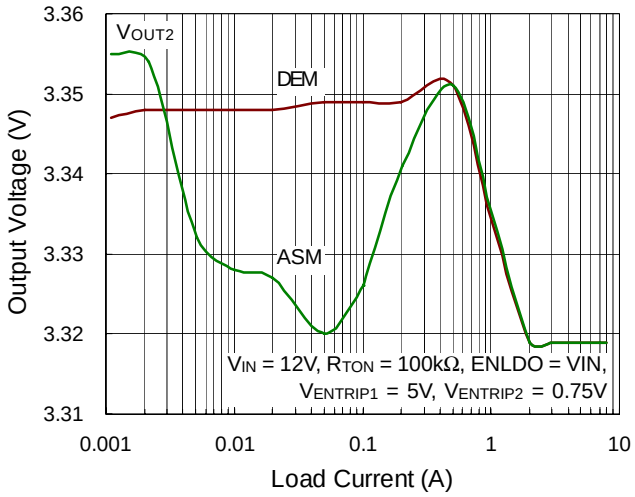


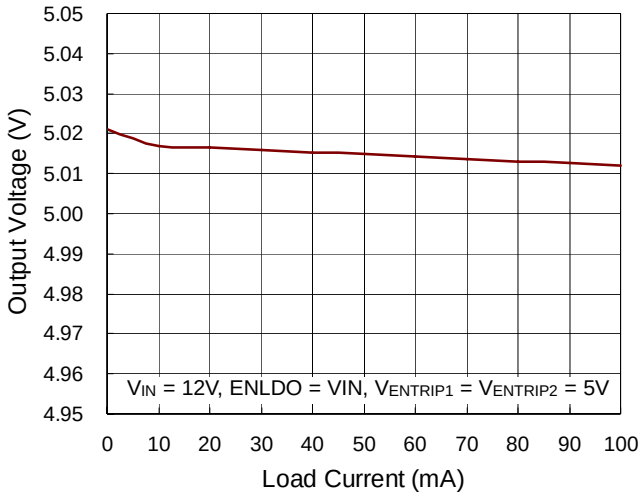
Output Voltage vs. Load Current



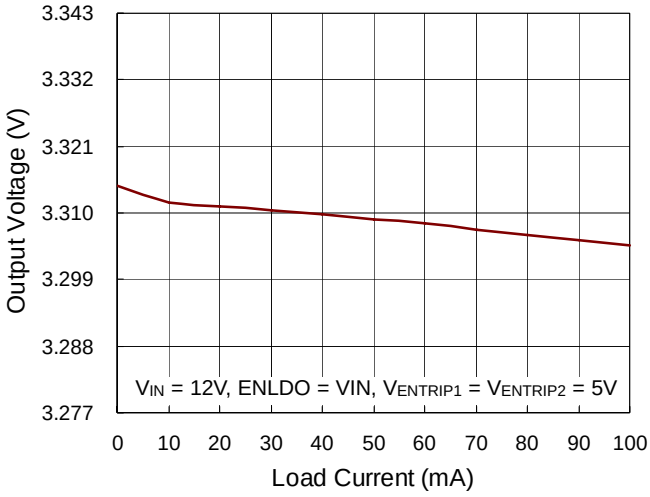
Output Voltage vs. Load Current



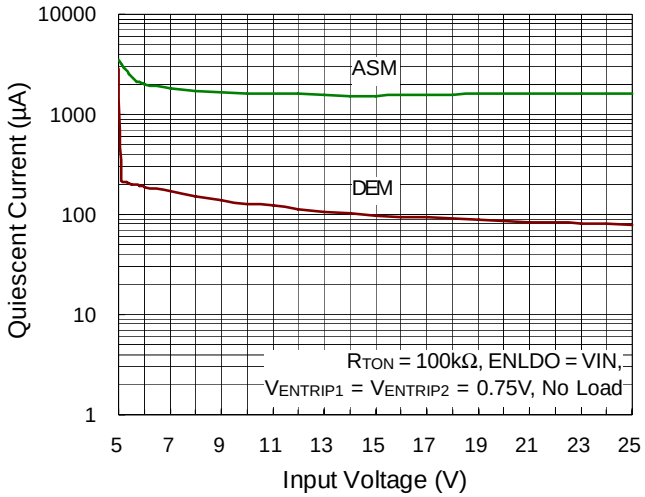
LDO5 Output Voltage vs. Load Current



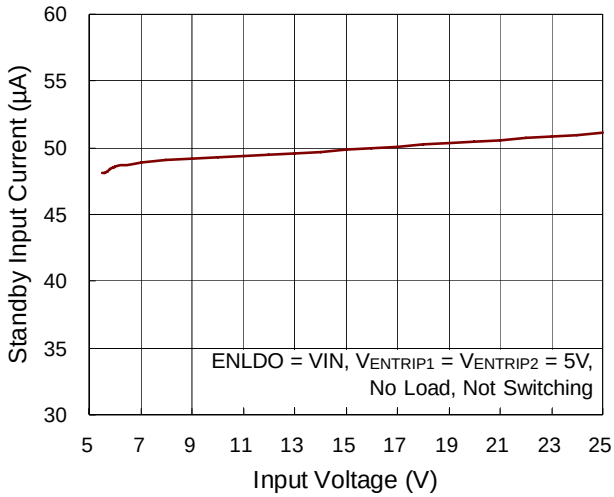
LDO3 Output Voltage vs. Load Current



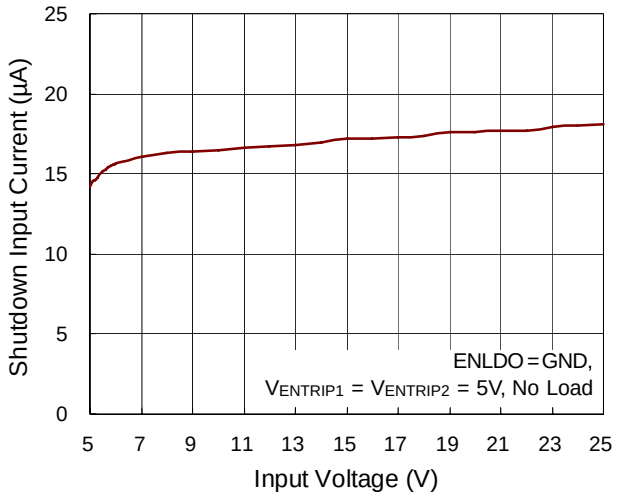
Quiescent Current vs. Input Voltage



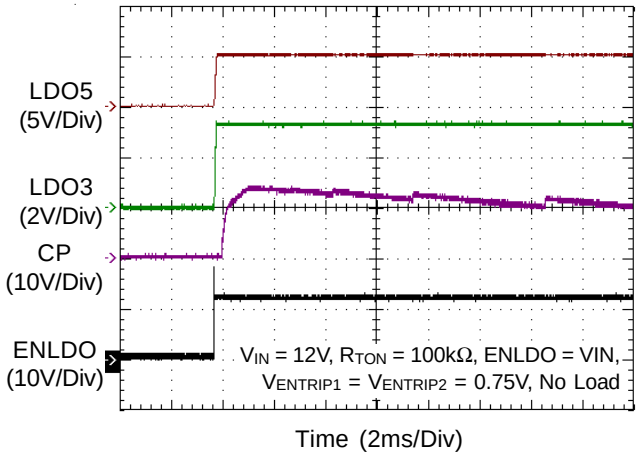
Standby Input Current vs. Input Voltage



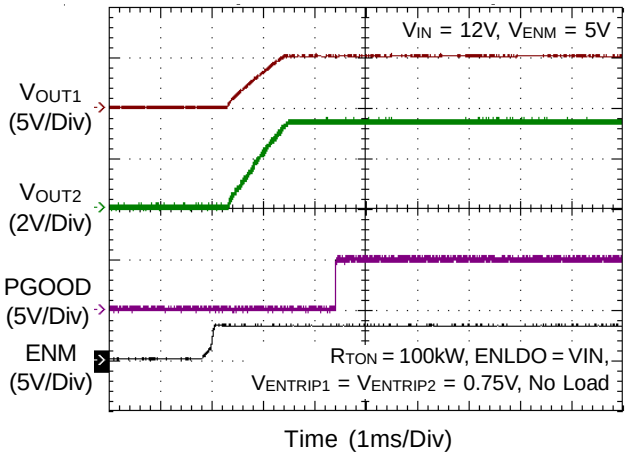
Shutdown Input Current vs. Input Voltage



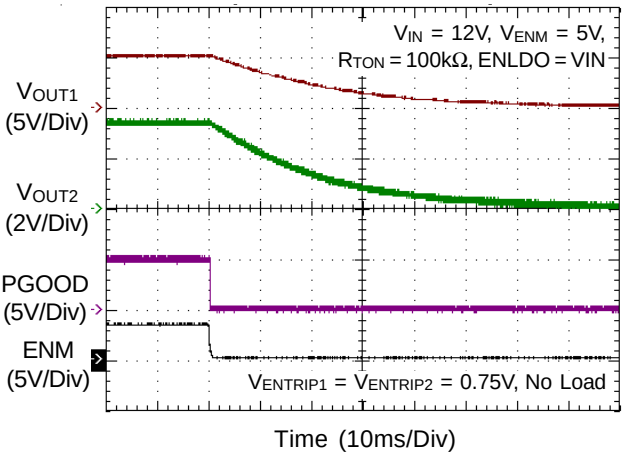
Power On from ENLDO



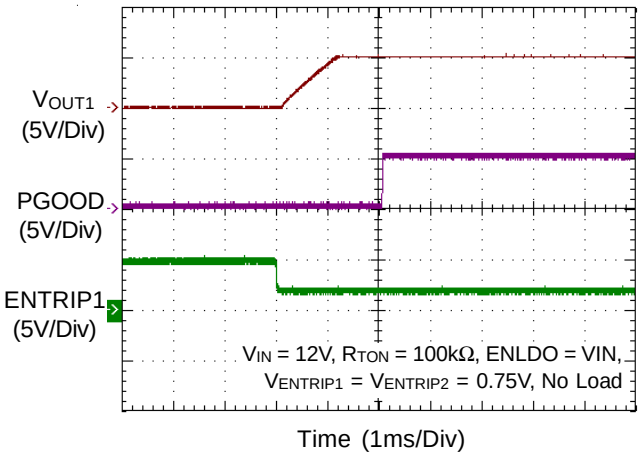
Power On from ENM



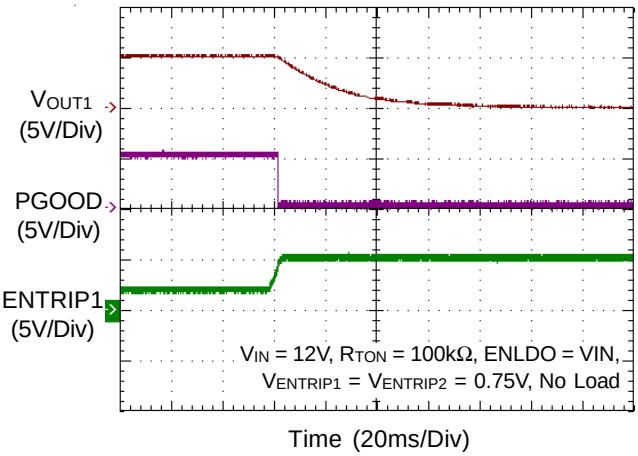
Power Off from ENM



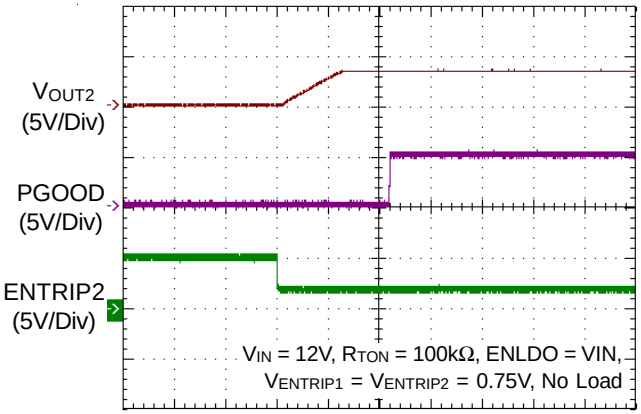
Power On from ENTRIP1



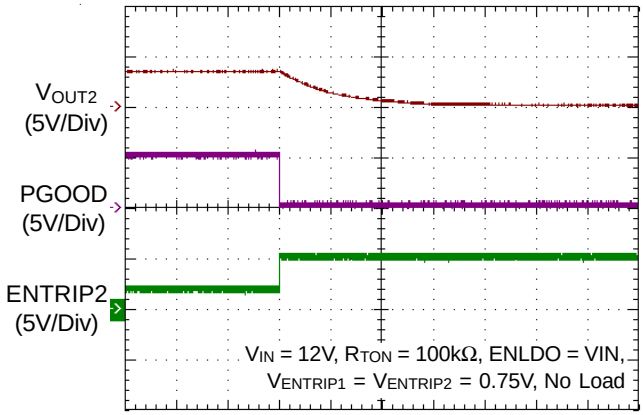
Power Off from ENTRIP1



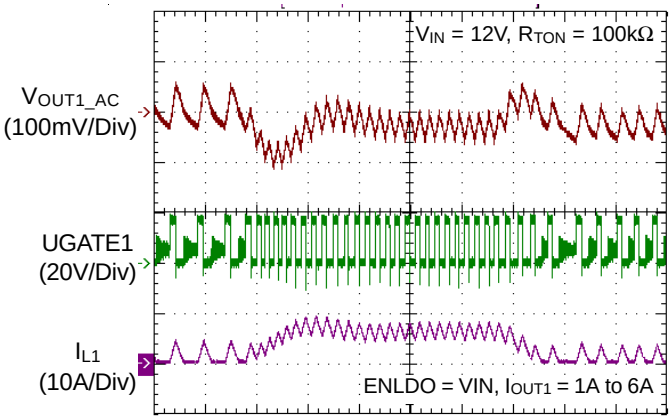
Power On from ENTRIP2



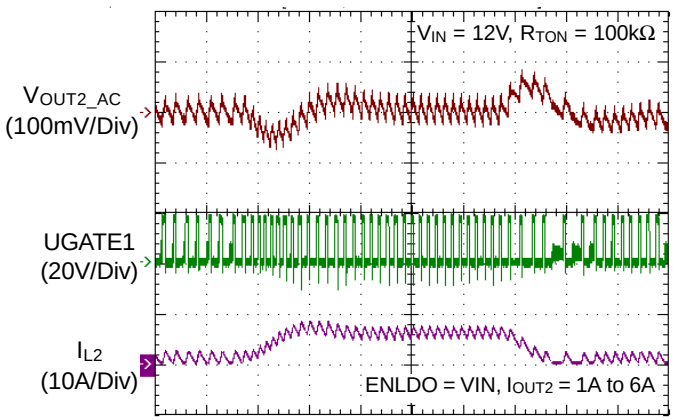
Power Off from ENTRIP2



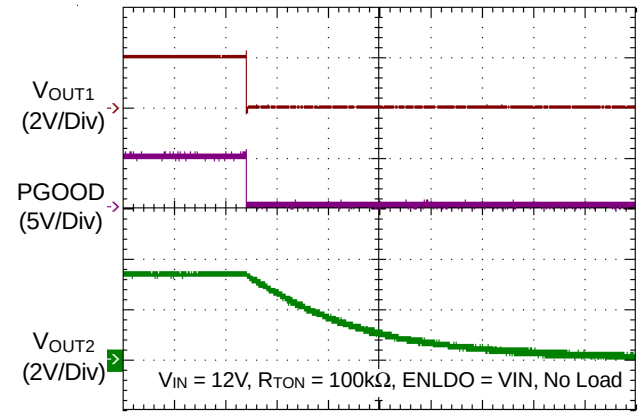
V_{OUT1} DEM-MODE Load Transient Response



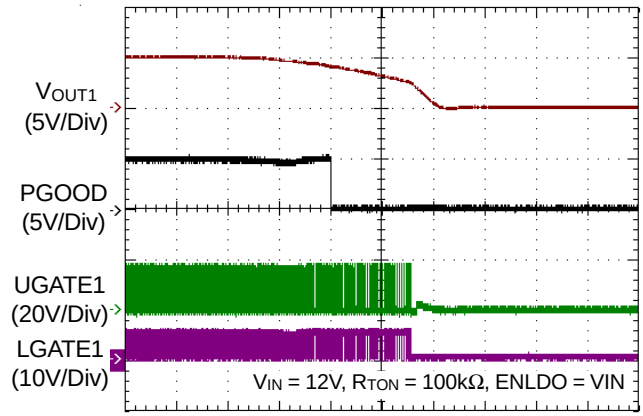
V_{OUT2} DEM-MODE Load Transient Response



OVP



UVP



Application Information

The RT8230A/B/C/D/E is a dual-channel, low quiescent, Mach Response™ DRV™ mode synchronous Buck controller targeted for Ultrabook system power supply solutions. Richtek's Mach Response™ technology provides fast response to load steps. The topology solves the poor load transient response timing problems of fixed frequency current mode PWMs, and avoids the problems caused by widely varying switching frequencies in CCR (constant current ripple) constant on-time and constant off-time PWM schemes. A special adaptive on-time control trades off the performance and efficiency over wide input voltage range. The RT8230A/B/C/D/E includes 5V (LDO5) and 3.3V (LDO3) linear regulators. The LDO5 linear regulator steps down the battery voltage to supply both internal circuitry and gate drivers. The synchronous switch gate drivers are directly powered by LDO5. When V_{OUT1} rises above 4.66V, an automatic circuit disconnects the linear regulator and allows the device to be powered by V_{OUT1} via the BYP1 pin.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so that the output ripple voltage provides the PWM ramp signal. Referring to the RT8230A/B/C/D/E's Function Block Diagram, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one-shot is determined by the converter's input output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (275ns typ.). The on-time one-shot will be triggered if the error comparator is high, the low-side switch current is below the current limit threshold, and the minimum off-time one-shot has timed out.

PWM Frequency and On-time Control

For each specific input voltage range, the Mach Response™ control architecture runs with pseudo constant frequency by feed forwarding the input and output voltage into the on-time one-shot timer. The high-side switch on-time is inversely proportional to the input voltage as measured by V_{IN} and proportional to the output voltage. The inductor ripple current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The frequency of 3V output controller is set higher than the frequency of 5V output controller. This is done to prevent audio frequency "beating" between the two sides, which switch asynchronously for each side. The TON pin is connected to GND through the external resistor R_{TON} to set the switching frequency.

The RT8230A/B/C/D/E adaptively changes the operation frequency according to the input voltage. Higher input voltage usually comes from an external adapter, so the RT8230A/B/C/D/E operates with higher frequency to have better performance. Lower input voltage usually comes from a battery, so the RT8230A/B/C/D/E operates with lower switching frequency for lower switching losses. For a specific input voltage range, the switching cycle period is given by :

For 5V VOUT,

$$\text{Period (sec.)} = \frac{V_{IN} \times (3.23 \times R_{TON} + 3.4 \times 10^4)}{1.36 \times V_{IN} - 5.16} \times 10^{-11}$$

For 3.3V VOUT,

$$\text{Period (sec.)} = \frac{V_{IN} \times (2.94 \times R_{TON} + 3.4 \times 10^4)}{1.36 \times V_{IN} + 1.46 \times 10^{-5} \times R_{TON} - 5.3} \times 10^{-11}$$

where the VIN is in volt, R_{TON} is in ohm.

The on-time guaranteed in the Electrical Characteristics table is influenced by switching delays in the external high-side power MOSFET.

Operation Mode Selection

The RT8230A/B/C/D/E supports two operation modes : diode emulation mode and ultrasonic mode. The operation mode can be set via the ENM pin for the RT8230A or the SECFB pin for the RT8230B/C/D/E.

Table 1. Operation Mode Setting

Part Number	RT8230A	RT8230B/E	RT8230C/D
Pin Name	ENM	SECFB	SECFB
Pin-13 Voltage Range	Mode State		
4.5V to 5V	ASM	ASM	ASM
2.3V to 3.6V	DEM	DEM	DEM
1.2V to 1.8V	CH1 : ASM CH2 : DEM	CH1 : ASM CH2 : DEM	CH1 : DEM CH2 : ASM
Below 0.8V	Shutdown	--	--

Diode Emulation Mode

In diode emulation mode, the RT8230A/B/C/D/E automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 1. and can be calculated as follows :

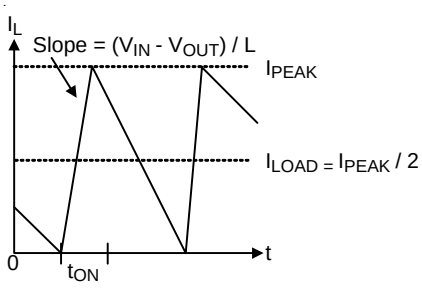


Figure 1. Boundary Condition of CCM/DEM

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

The switching waveforms may appear noisy and asynchronous when light load causes diode emulation operation. This is normal and results in high efficiency. Trade offs in PFM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

In diode emulation mode, the FB voltage will rise to 2.015V (typ.) naturally, because of the design circuit.

Ultrasonic Mode (ASM)

The RT8230A/B/C/D/E activates a unique type of diode emulation mode with a minimum switching frequency of 25kHz, called ultrasonic mode. This mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the low-side switch gate driver signal is "OR"ed with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the controller will turn on UGATE and give it shorter on-time. When the on-time expired, LGATE turns on until the inductor current goes to zero crossing threshold and keep both high-side and low-side MOSFET off to wait for the next trigger. Because shorter on-time causes a smaller pulse of the inductor current, the controller can keep output

voltage and switching frequency simultaneously. The on-time decreasing has a limitation and the output voltage will be lifted up under the slight load condition. The controller will turn on LGATE first to pull down the output voltage. When the output voltage is pulled down to the balance point of the output load current, the controller will proceed the short on-time sequence as the above description.

Linear Regulators (LDOx)

The RT8230A/B/C/D/E includes 5V (LDO5) and 3.3V (LDO3) linear regulators. The regulators can supply up to 100mA for external loads. Bypass LDOx with a minimum 4.7µF ceramic capacitor. When V_{OUT1} is higher than the switch over threshold (4.66V), an internal 1.5Ω P-MOSFET switch connects BYP1 to the LDO5 pin while simultaneously disconnects the internal linear regulator.

Current Limit Setting (ENTRIPx)

The RT8230A/B/C/D/E has cycle-by-cycle current limit control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASEx is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, battery and output voltage.

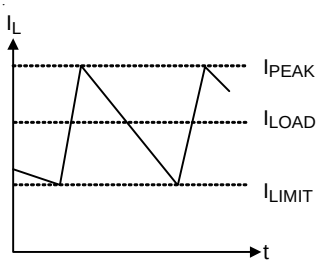


Figure 2. "Valley" Current Limit

The RT8230A/B/C/D/E uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The R_{ILIM} resistor between the ENTRIPx pin and GND sets the current limit threshold. The resistor R_{ILIM} is connected to a current source from ENTRIPx which is 5µA (typ.) at room temperature. The current source has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across the sense resistor or low-side MOSFET equals 1/10 the voltage across the R_{ILIM} resistor, positive current limit will be activated. The high-side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/10 the voltage across the R_{ILIM} resistor.

Choose a current limit resistor according to the following equation :

$$V_{LIMIT} = (R_{LIMIT} \times 5\mu A) / 10 = I_{LIMIT} \times R_{DS(ON)}$$

$$R_{LIMIT} = (I_{LIMIT} \times R_{DS(ON)}) \times 10 / 5\mu A$$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal at PHASEx and GND. Mount or place the IC close to the low-side MOSFET.

Charge Pump (SECFB)

The external 14V charge pump is driven by LGATEx (LGATE1 for RT8230B/E, LGATE2 for RT8230C/D). As shown in Figure 3, when LGATEx is low, C1 will be charged by V_{OUT1} through D1. C1 voltage is equal to V_{OUT1} minus the diode drop. When LGATEx becomes high, C1 transfers the charge to C2 through D2 and charges C2 voltage to V_{LGATEX} plus C1 voltage. As LGATEx transitions low on the next cycle, C3 is charged to C2 voltage minus a diode drop through D3. Finally, C3 charges C4 through D4 when LGATEx switches high. Thus, the total charge pump voltage, V_{CP}, is :

$$V_{CP} = V_{OUT1} + 2 \times V_{LGATEx} - 4 \times V_D$$

where V_{LGATEx} is the peak voltage of the LGATEx driver which is equal to LDO5 and V_D is the forward voltage dropped across the Schottky diode.

The SECFB pin in the RT8230B/C/D/E is used to monitor the charge pump via a resistive voltage divider to generate approximately 14V DC voltage and the clock driver uses V_{OUT1} as its power supply. In the Figure 3 when SECFB drops below its feedback threshold, an ultrasonic pulse will occur to refresh the charge pump driven by LGATEx. If there is an overload on the charge pump in which SECFB can not reach more than its feedback threshold, the

channel x controller will enter ultrasonic mode. Special care should be taken to ensure that enough normal ripple voltage is present on each cycle to prevent charge pump shutdown.

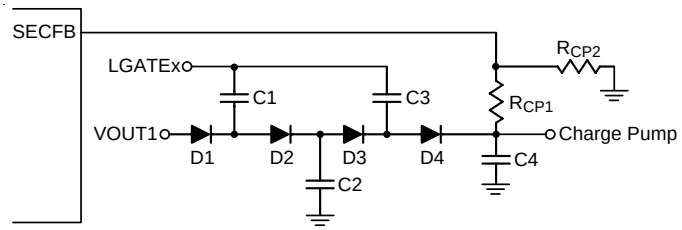


Figure 3. Charge Pump Circuit Connected to SECFB

MOSFET Gate Driver (UGATEx, LGATEx)

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the LDO5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOTx and PHASEx pins. A dead-time to prevent shoot through is internally generated from high-side MOSFET off to low-side MOSFET on and low-side MOSFET off to high-side MOSFET on.

The low-side driver is designed to drive high current low $R_{DS(ON)}$ N-MOSFET(s). The internal pull down transistor that drives LGATEx low is robust, with a 1Ω typical on-resistance. A 5V bias voltage is delivered from the LDO5 supply. The instantaneous drive current is supplied by an input capacitor connected between LDO5 and GND.

For high current applications, some combinations of high and low-side MOSFETs may cause excessive gate drain coupling, which leads to efficiency killing, EMI producing, and shoot through currents. This is often remedied by adding a resistor in series with BOOTx, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time. See Figure 4.

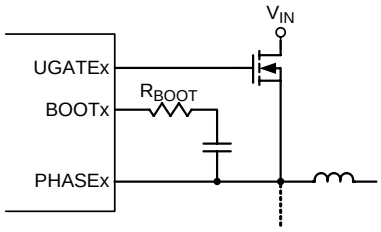


Figure 4. Increasing the UGATEx Rise Time

Soft-Start

The RT8230A/B/C/D/E provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FBx signal. The typical soft-start duration is 0.8ms. A unique PWM duty limit control that prevents output over-voltage during soft-start period is designed specifically for FBx floating.

UVLO Protection

The RT8230A/B/C/D/E has LDO5 under-voltage lock out protection (UVLO). When the LDO5 voltage is lower than 3.9V (typ.) and the LDO3 voltage is lower than 2.5V (typ.), both switch power supplies are shut off. This is a non-latch protection.

Power Good Output (PGOOD)

PGOOD is an open-drain output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when both output voltages are above 90% of the nominal regulation point for RT8230A. For RT8230B/C/D/E, PGOOD is released when both output voltages are above 92.5% of nominal regulation point, and the SECFB threshold is also above 50% of nominal regulation point. The PGOOD signal goes low if either output turns off or is 15.5% below or 13% over its nominal regulation point.

Output Over-Voltage Protection (OVP)

The output voltage can be continuously monitored for over-voltage condition. If the output voltage exceeds 13% of its set voltage threshold, the over-voltage protection is triggered and the LGATEx low-side gate drivers are forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor and pulls the output voltage downward. In addition, the BYP1 pin also has the OVP function.

When detect BYP1 Voltage over 6V, RT8230A/B/C/D/E will active OVP function immediately.

The RT8230A/B/C/D/E is latched once OVP is triggered and can only be released by either toggling ENLDO, ENTRIPx or cycling VIN. There is a 1μs delay built into the over-voltage protection circuit to prevent false transition.

Note that latching LGATEx high will cause the output voltage to dip slightly negative due to previously stored energy in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over-voltage condition is caused by a shorted in high-side switch, turning the low-side MOSFET on 100% will create an electrical shorted circuit between the battery and GND to blow the fuse and disconnecting the battery from the output.

Output Under-Voltage Protection (UVP)

The output voltage can be continuously monitored for under-voltage condition. If the output is less than 52% (typ.) of its set voltage threshold, the under-voltage protection will be triggered and then both UGATEx and LGATEx gate drivers will be forced low. The UVP is ignored for at least 3ms (typ.) after a start-up or a rising edge on ENTRIPx. Toggle ENTRIPx or cycle VIN to reset the UVP fault latch and restart the controller.

Thermal Protection

The RT8230A/B/C/D/E features thermal shutdown to prevent damage from excessive heat dissipation. Thermal shutdown occurs when the die temperature exceeds 150°C. All internal circuitries are turned off during thermal shutdown. The RT8230A/B/C/D/E triggers thermal shutdown if LDOx is not supplied from V_{OUTx}, while input voltage on VIN and drawing current from LDOx are too high. Nevertheless, even if LDOx is supplied from V_{OUTx}, overloading LDOx can cause large power dissipation on automatic switches, which may still result in thermal shutdown.

Discharge Mode (Soft Discharge)

When ENTRIPx is high and a transition to standby or shutdown mode occurs, or the output under-voltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

Shutdown Mode

SMPS1, SMPS2, LDO3 and LDO5 all have independent enabling control. Drive ENLDO (RT8230A/B/D), ENC (RT8230C/E), ENTRIP1 and ENTRIP2 below the precise input falling edge trip level to place the device in its low power shutdown state. The RT8230A/B/C/D/E consumes only 10μA of input current while in shutdown. When shutdown mode is activated, the reference turns off. The 0.4V falling edge threshold on ENLDO/ENC can be used to detect a specific analog voltage level and to shutdown the device. Once in shutdown, the 1V rising edge threshold activates, providing sufficient hysteresis for most applications.

Power-Up Sequencing and On/Off Controls (ENTRIPx, ENM)

ENTRIP1 and ENTRIP2 control the power-up sequencing of the two channels of the Buck converter. When the RT8230A/B/C/D/E is applied in the single-channel mode, ENTRIPx disables the respective output when ENTRIPx voltage rises above 4.5V. Furthermore, when the RT8230A is applied in the dual-channel mode, the outputs are enabled when ENM connects to LDO3 for DEM operation.

Table 2. Operation Mode Truth Table

Mode	Condition	Comment
LDO Over Current Limit	LDOx < UVLO threshold	Transitions to discharge mode after VIN POR LDO5 and LDO3 remain active.
Run	ENLDO/ENC = high, V_{OUT1} or V_{OUT2} are enabled	Normal Operation.
Over-Voltage Protection	Either output >113% of the nominal level.	LGATEx is forced high. LDO3 and LDO5 are active. Exit by VIN POR or by toggling ENLDO/ENC, ENTRIPx, and ENM.
Under-Voltage Protection	Either output < 52% of the nominal level after 3ms time-out expires and output is enabled	Both UGATEx and LGATEx are forced low and enter discharge mode. LDO3 and LDO5 are active. Exit by VIN POR or by toggling ENLDO/ENC, ENTRIPx, and ENM.
Discharge	Either output is still high in standby mode or shutdown mode	During discharge mode, there is one path to discharge the output capacitors' residual charge to GND via an internal switch.
Standby	ENTRIPx > startup threshold or ENM < startup threshold, ENLDO/ENC = high.	LDO3 and LDO5 are active.
Shutdown	ENLDO/ENC = low	All circuitries are off. LDO3 and LDO5 are kept active for RT8230C/E only.
Thermal Shutdown	T_J > 150°C	All circuitries are off. Exit by VIN POR or by toggling ENLDO/ENC, ENTRIPx, and ENM.

Table 3. Power-Up Sequencing (RT8230A)

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	SMPS1	SMPS2
Low	Low	X	X	Off	Off	Off	Off
">1V" => High	Low	X	X	On	On	Off	Off
">1V" => High	">2.3V" => High	Off	Off	On	On	Off	Off
">1V" => High	">2.3V" => High	Off	On	On	On	Off	On
">1V" => High	">2.3V" => High	On	On	On	On	On	On
">1V" => High	">2.3V" => High	On	Off	On	On	On	Off

Output Voltage Setting (FBx)

Connect a resistive voltage divider at the FBx pin between V_{OUTx} and GND to adjust the output voltage between 2V and 5.5V (Figure 5). Choose R2 to be approximately 10kΩ, and solve for R1 using the equation below :

$$V_{OUT} = V_{FBx} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FBx} is 2V (typ.).

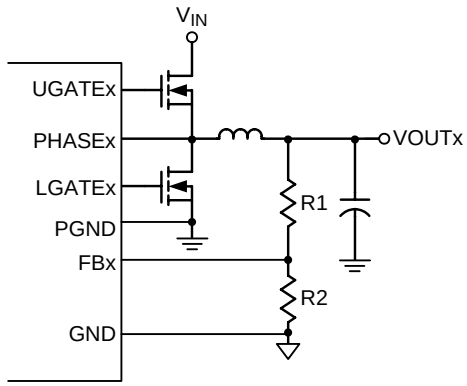


Figure 5. Setting V_{OUTx} with a resistive voltage divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUTx})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current, I_{PEAK} :

$I_{PEAK} = I_{LOAD(MAX)} + [\ (LIR / 2) \times I_{LOAD(MAX)}\ ]$

The calculation above shall serve as a general reference. To further improve transient response, the output inductance can be further reduced. Of course, besides the inductor, the output capacitor should also be considered when improving transient response.

Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from the equations below :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \times \left[V_{IN} \times t_{ON} - V_{OUTx}(t_{ON} + t_{OFF(MIN)})\right]}$$

$$V_{SOAR} = \frac{(\Delta I_{LOAD})^2 \times L}{2 \times C_{OUT} \times V_{OUTx}}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f}\right)$$

where V_{SAG} and V_{SOAR} are the allowable amount of undershoot and overshoot voltage during load transient, V_{p-p} is the output ripple voltage, and $t_{OFF(MIN)}$ is the minimum off-time.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-20L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

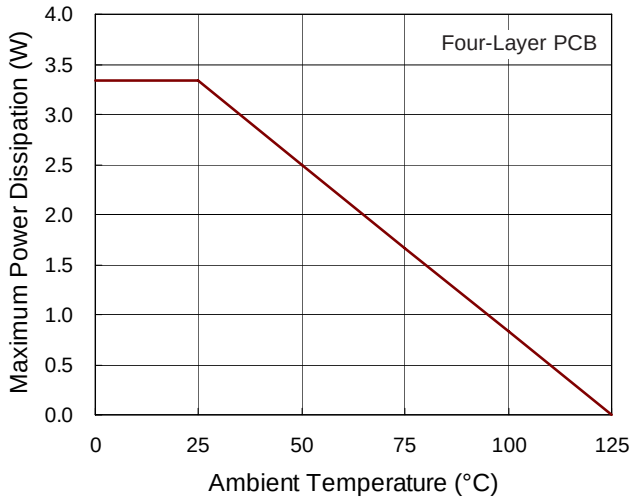


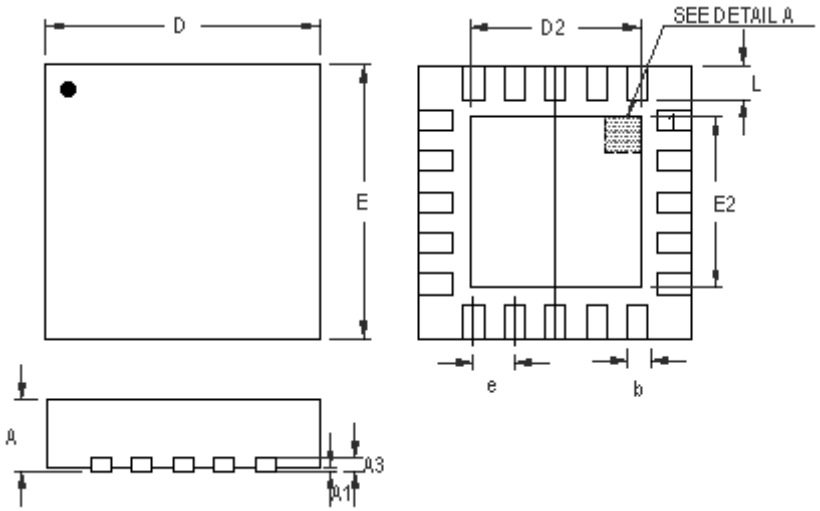
Figure 6. Derating Curve of Maximum Power Dissipation

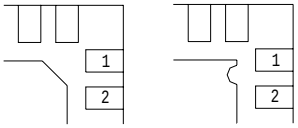
Layout Considerations

Layout is very important in high frequency switching converter design. Improper PCB layout can radiate excessive noise and contribute to the converter's instability. Certain points must be considered before starting a layout with the RT8230A/B/C/D/E.

- Place the filter capacitor close to the IC, within 12mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25 mils) or wider trace.
- All sensitive analog traces and components such as FBx, ENTRIPx, PGOOD, and TON should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Place ground terminal of VIN capacitor(s), V_{OUTx} capacitor(s), and Source of low-side MOSFETs as close to each other as possible. The PCB trace of PHASEx node, which connects to Source of high-side MOSFET, Drain of low-side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

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