

# TK3P50D

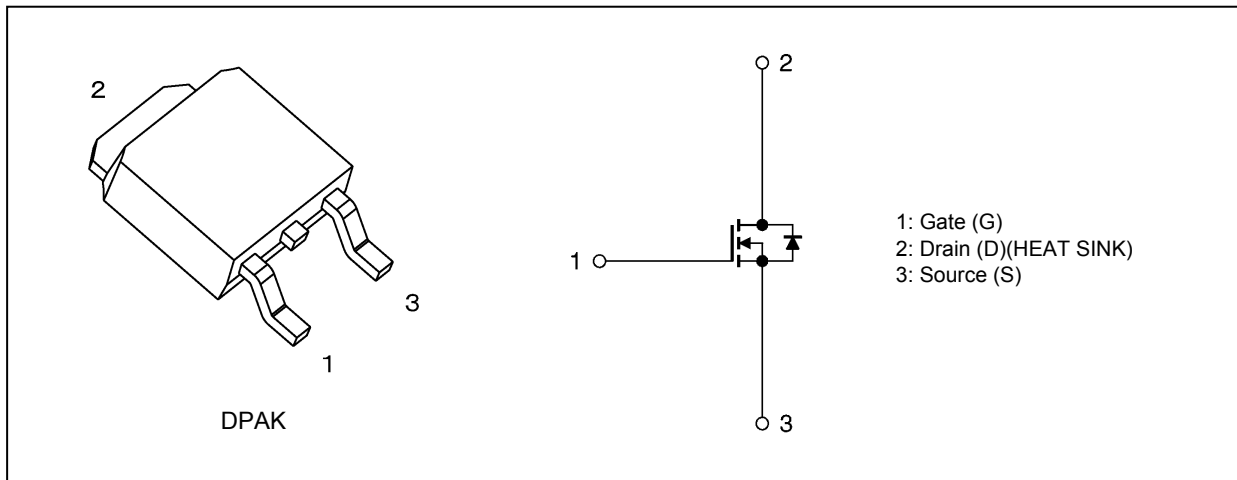
## 1. Applications

- Switching Voltage Regulators

## 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 2.3 \Omega$  (typ.)
- (2) High forward transfer admittance:  $|Y_{fs}| = 1.0 S$  (typ.)
- (3) Low leakage current:  $I_{DSS} = 10 \mu A$  (max) ( $V_{DS} = 500 V$ )
- (4) Enhancement mode:  $V_{th} = 2.4$  to  $4.4 V$  ( $V_{DS} = 10 V, I_D = 1 mA$ )

## 3. Packaging and Internal Circuit



## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ C$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	500	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	
Drain current (DC)	(Note 1) $I_D$	3	A
Drain current (pulsed)	(Note 1) $I_{DP}$	6	
Power dissipation	( $T_c = 25^\circ C$ ) $P_D$	60	W
Single-pulse avalanche energy	(Note 2) $E_{AS}$	81	mJ
Avalanche current	$I_{AR}$	3	A
Repetitive avalanche energy	(Note 3) $E_{AR}$	6	mJ
Channel temperature	$T_{ch}$	150	$^\circ C$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2010-10

## 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	2.08	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	125	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:  $V_{DD} = 90\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 15.3\text{ mH}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = 3\text{ A}$

Note 3: Repetitive rating; pulse width limited by maximum channel temperature

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

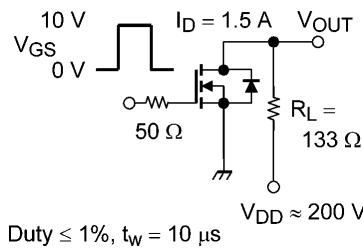
**6. Electrical Characteristics**

**6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	500	—	—	V
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.4	—	4.4	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$	—	2.3	3.0	$\Omega$
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 1.5\text{ A}$	0.3	1	—	S

**6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	280	—	$\mu\text{F}$
Reverse transfer capacitance	$C_{rss}$		—	1.5	—	
Output capacitance	$C_{oss}$		—	30	—	
Switching time (rise time)	$t_r$	See Figure 6.2.1.	—	20	—	ns
Switching time (turn-on time)	$t_{on}$		—	50	—	
Switching time (fall time)	$t_f$		—	10	—	
Switching time (turn-off time)	$t_{off}$		—	80	—	



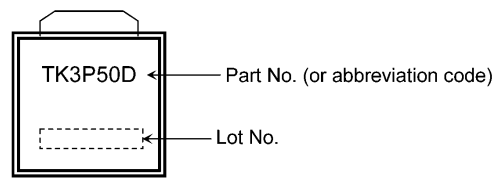
**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

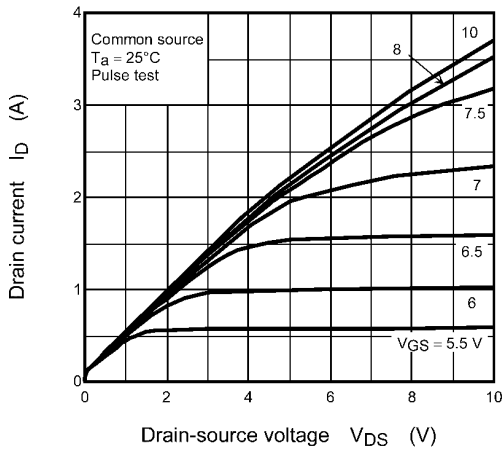
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 3\text{ A}$	—	7	—	nC
Gate-source charge	$Q_{gs}$		—	4	—	
Gate-drain charge	$Q_{gd}$		—	3	—	

**6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

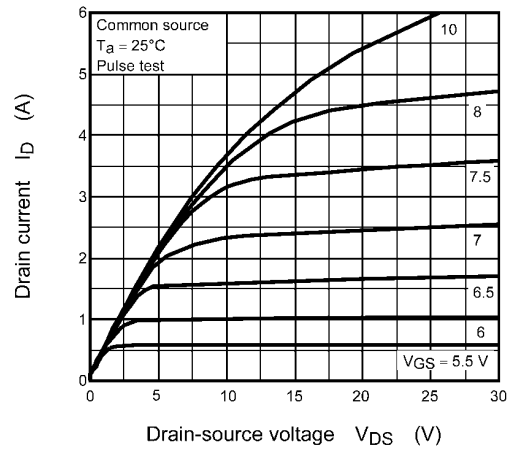
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (DC) (Note 1)	$I_{DR}$	—	—	—	3	A
Reverse drain current (pulsed) (Note 1)	$I_{DRP}$	—	—	—	6	
Diode forward voltage	$V_{DSF}$	$I_{DR1} = 3\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 3\text{ A}, V_{GS} = 0\text{ V}$ $-di_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	770	—	ns
Reverse recovery charge	$Q_{rr}$		—	2.5	—	$\mu\text{C}$

**7. Marking****Fig. 7.1 Marking**

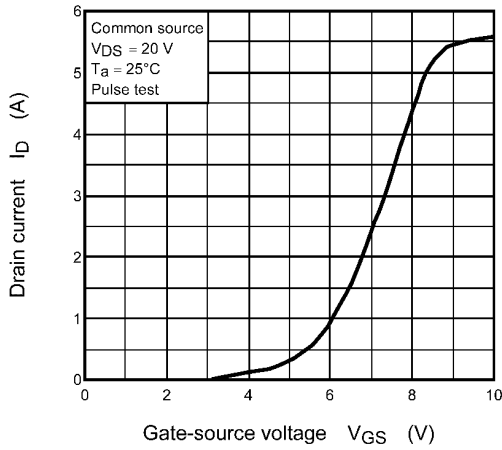
**8. Characteristics Curves (Note)**



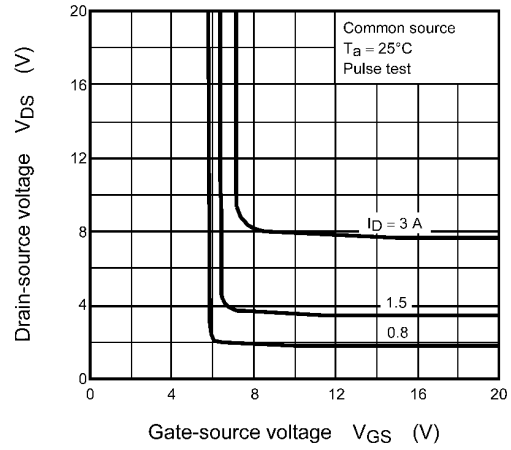
**Fig. 8.1  $I_D - V_{DS}$**



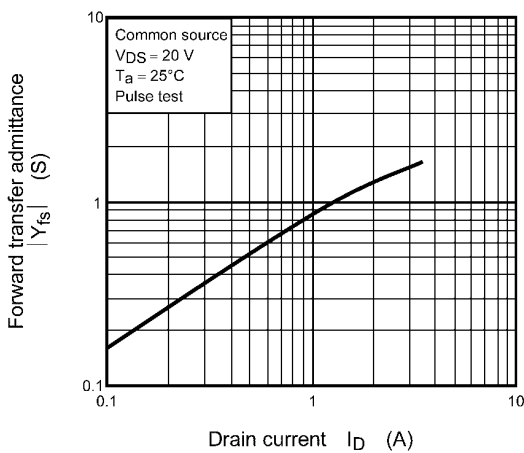
**Fig. 8.2  $I_D - V_{DS}$**



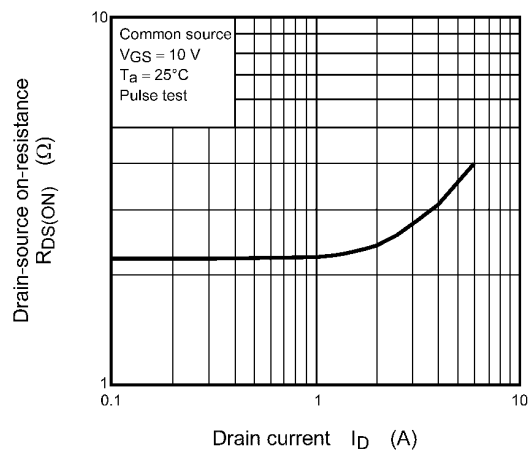
**Fig. 8.3  $I_D - V_{GS}$**



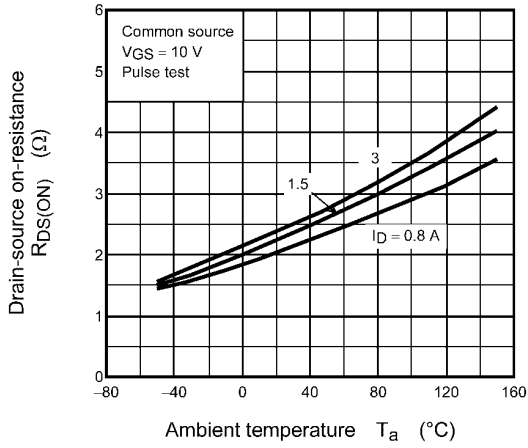
**Fig. 8.4  $V_{DS} - V_{GS}$**



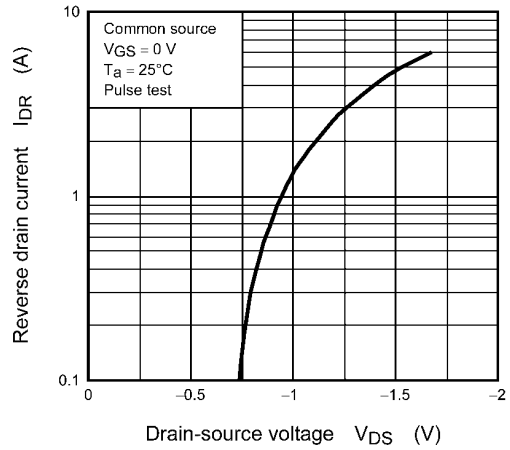
**Fig. 8.5  $|Y_{fs}| - I_D$**



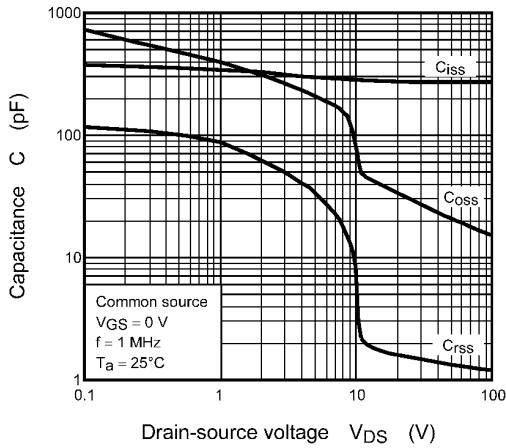
**Fig. 8.6  $R_{DS(ON)} - I_D$**



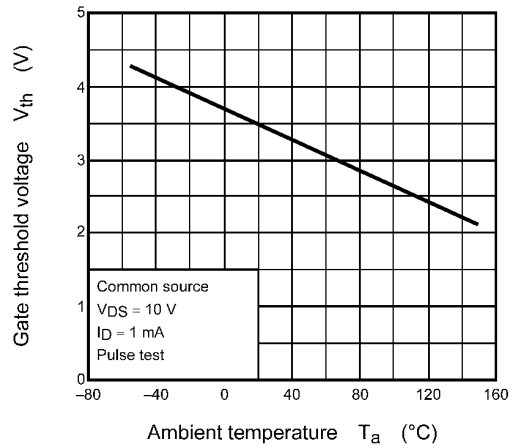
**Fig. 8.7  $R_{DS(ON)} - T_a$**



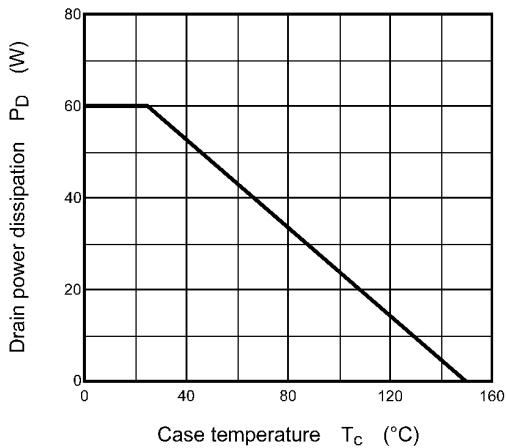
**Fig. 8.8  $I_{DR} - V_{DS}$**



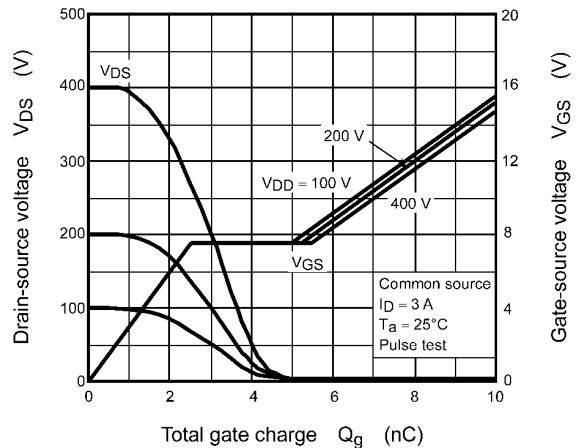
**Fig. 8.9  $C - V_{DS}$**



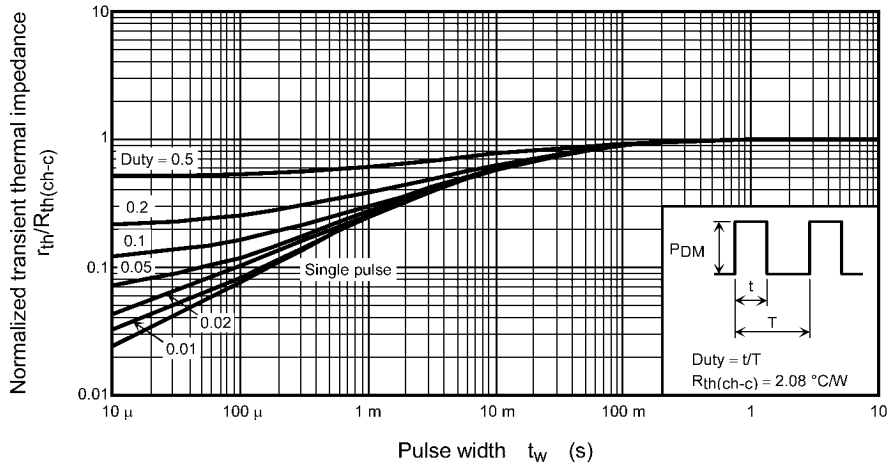
**Fig. 8.10  $V_{th} - T_a$**



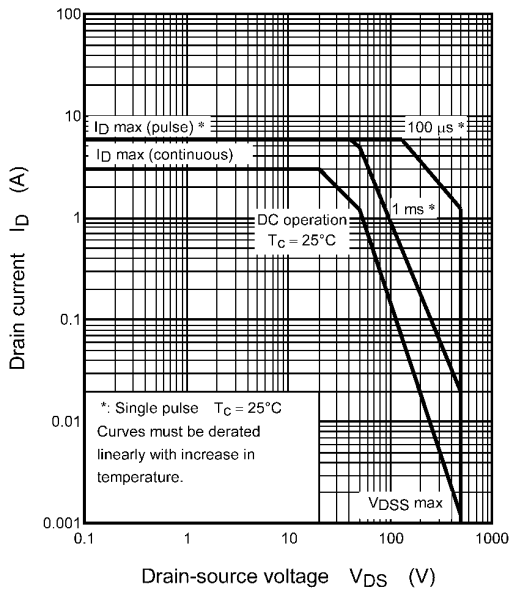
**Fig. 8.11  $P_D - T_c$   
(Guaranteed Maximum)**



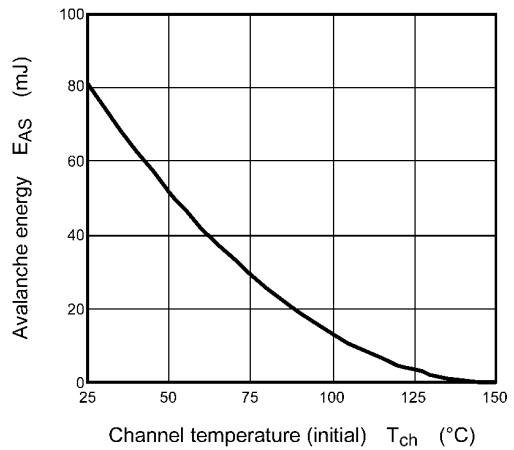
**Fig. 8.12 Dynamic Input/Output Characteristics**



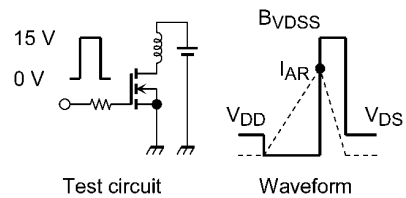
**Fig. 8.13**  $r_{th}/R_{th(ch-c)} - t_w$   
(Guaranteed Maximum)



**Fig. 8.14** Safe Operating Area  
(Guaranteed Maximum)



**Fig. 8.15**  $E_{AS} - T_{ch}$   
(Guaranteed Maximum)



$R_G = 25 \Omega$   
 $V_{DD} = 90 \text{ V}, L = 15.3 \text{ mH}$

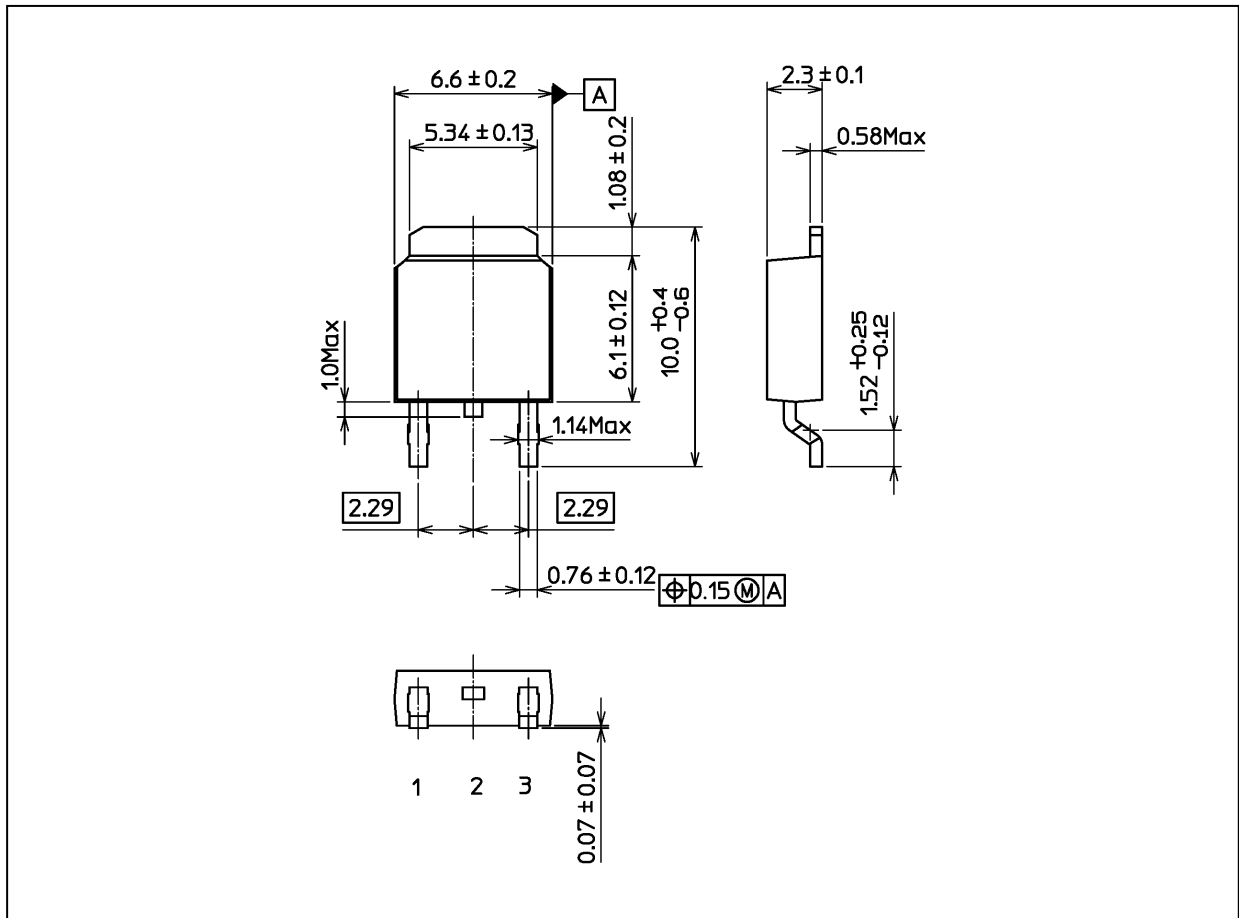
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

**Fig. 8.16** Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

Package Name(s)
TOSHIBA: 2-7K1S
Nickname: DPAK



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