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User's Manual

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H8/36109 Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer
H8 Family / H8/300H Tiny Series

H8/36109F HD64F36109
HD64F36109G

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are in their open states, intermediate levels are induced by noise in the vicinity, a through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughou chip and a low level is input on the reset pin. During the period where the states a undefined, the register settings and the output state of each pin are also undefined your system so that it does not malfunction because of processing while it is in th undefined state. For those products which have a reset function, reset the LSI imr after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test reg may have been be allocated to these addresses. Do not access these registers; the operation is not guaranteed if they are accessed.

- CPU and System-Control Modules
- On-Chip Peripheral Modules

The configuration of the functional description of each module differs according to t
module. However, the generic style includes the following items:

i) Feature
ii) Input/Output Pin
iii) Register Description
iv) Operation
v) Usage Note

When designing an application system that includes this LSI, take notes into account. Ea
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7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier ve
This does not include all of the revised contents. For details, see the actual locations in t
manual.

11. Index

Objective: This manual was written to explain the hardware functions and electrical characteristics of the H8/36109 Group to the target users.
Refer to the H8/300H Series Software Manual for a detailed description o instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
  Read the manual according to the contents. This manual can be roughly categorized in on the CPU, system control functions, peripheral functions, and electrical characterist
- In order to understand the details of the CPU's functions
  Read the H8/300H Series Software Manual.
- In order to understand the details of a register when its name is known
  Read the index that is the final part of the manual to find the page number of the entry register. The addresses, bits, and initial values of the registers are summarized in secti List of Registers.

Example:	Register name:	The following notation is used for cases when the sa similar function, e.g. serial communication interface implemented on more than one channel: XXX_N (XXX is the register name and N is the cha number)
	Bit order:	The MSB is on the left and the LSB is on the right.
	Number notation:	Binary is B'xxxx, hexadecimal is H'xxxx, and decim xxxx.
	Signal notation:	An overbar is added to a low-active signal: $\overline{xxxx}$

by the E7 or E8. If address breaks are set as being used by the E7 or E8, the address control registers must not be accessed.

6. When the E7 or E8 is used, $\overline{\text{NMI}}$ is an input/output pin (open-drain in output mode), P87 are input pins, and P86 is an output pin.
7. Use channel 1 of the SCI3 (P21/RXD, P22/TXD) in on-board programming mode by mode.

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H8/36109 Group manuals:

Document Title	Docume
H8/36109 Group Hardware Manual	This mar
H8/300H Series Software Manual	REJ09B0

User's manuals for development tools:

Document Title	Docume
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual	REJ10B
H8S, H8/300 Series Simulator/Debugger User's Manual	REJ10B
H8S, H8/300 Series High-Performance Embedded Workshop 3, Tutorial	REJ10B
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RTC (can be used as a free running counter)

Timer B1 (8-bit timer)

Timer V (8-bit timer)

Timer RC (16-bit timer)

Timer RD (16-bit timer)

14-bit PWM

Watchdog timer

SCI3 (Asynchronous or clock synchronous serial communication interface)

I^2C bus interface 2 (conforms to the I^2C bus interface format that is advocated by Phi Electronics)

10-bit A/D converter

POR/LVD (Power-on reset and low-voltage detection circuit) (optional)

- On-chip memory

Product Classification		Model: Standard Version	Model: On-Chip Power-On Reset and Low-Voltage Detection Circuit Version	ROM	RAM	Re
Flash memory version (F-ZTAT™ version)	H8/36109F	HD64F36109	HD64F36109G	128 kbytes	5 kbytes	

Note: F-ZTAT™ is a trademark of Renesas Technology Corp.

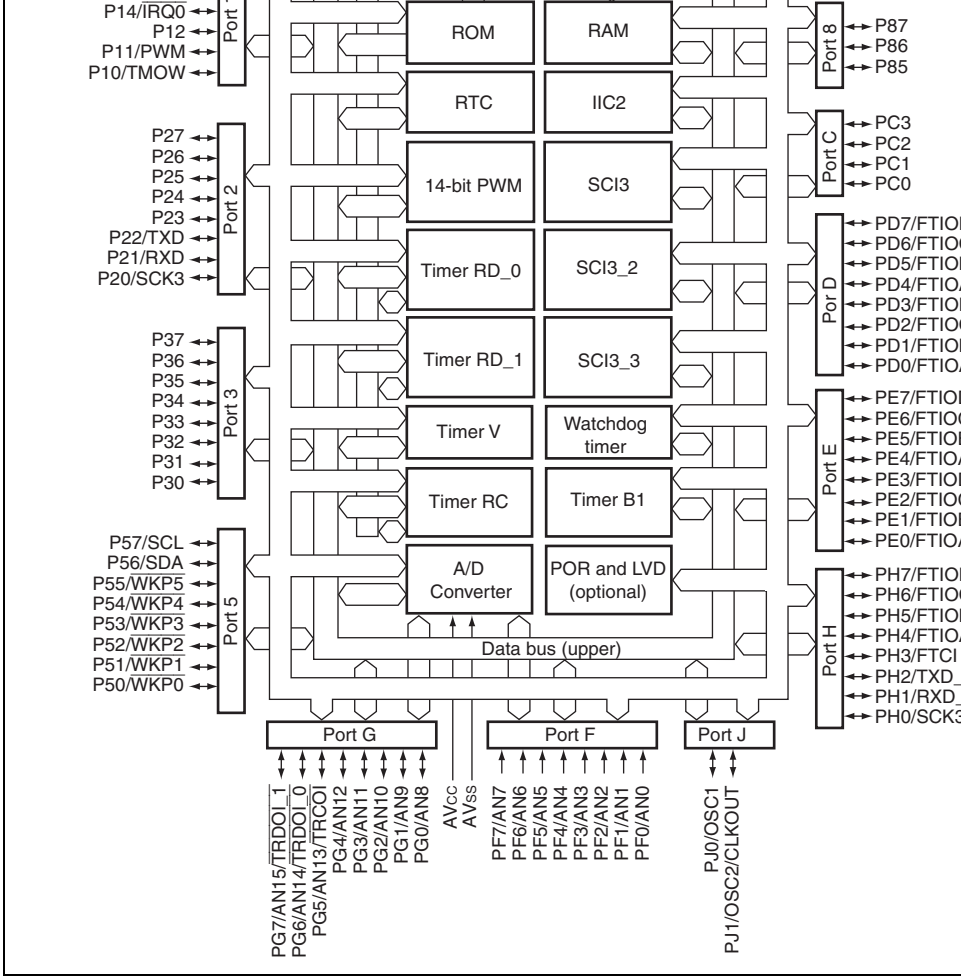


Figure 1.1 Internal Block Diagram

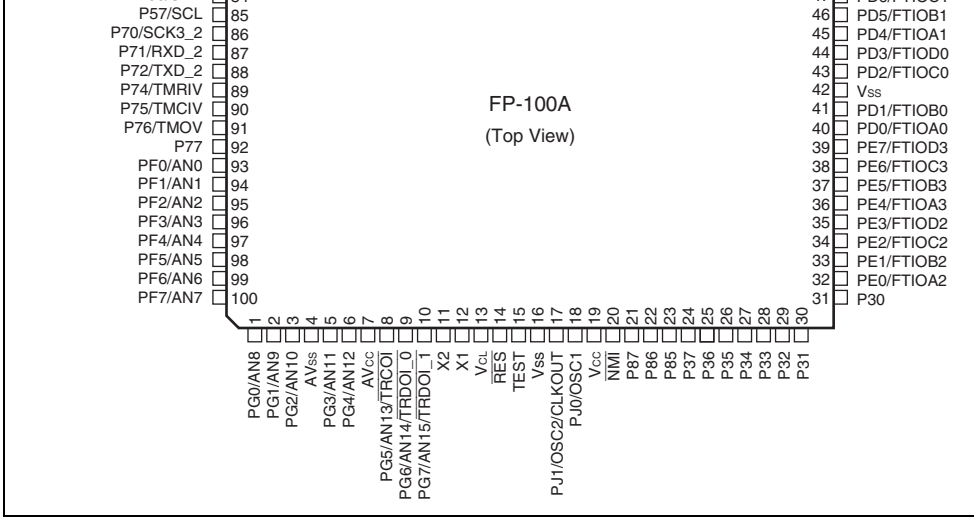


Figure 1.2 Pin Assignments (FP-100A)

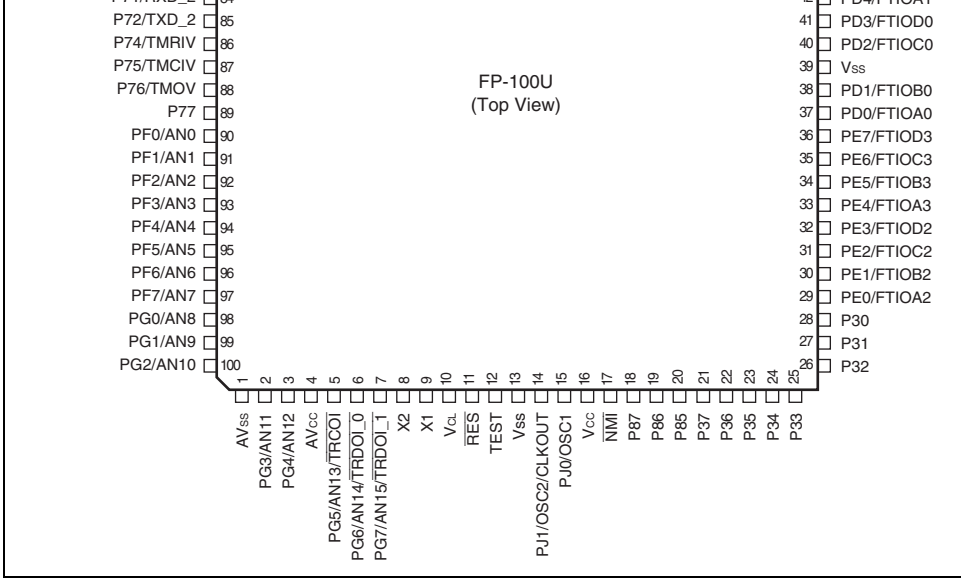


Figure 1.3 Pin Assignments (FP-100U)

	AVcc	7	4	Input	Analog power supply pin for the A converter. When the A/D convert used, connect this pin to the syst power supply.
	AVss	4	1	Input	Analog ground pin for the A/D co Connect this pin to the system po supply (0 V).
	VCL	13	10	Input	Internal step-down power supply Connect a capacitor of around 0. between this pin and the Vss pin stabilization.
Clock pins	OSC1	18	15	Input	These pins connect with crystal o ceramic resonator for the system can be used to input an external When using the on-chip oscillato system clock can be output from pin. See section 5, Clock Pulse Gene for a typical connection.
	OSC2/ CLKOUT	17	14	Output	
	X1	12	9	Input	These pins connect with a 32.76 crystal resonator for the subclock section 5, Clock Pulse Generator typical connection.
	X2	11	8	Output	
System control	$\overline{\text{RES}}$	14	11	Input	Reset pin. The pull-up resistor (ty kΩ) is incorporated. When driven chip is reset.
	TEST	15	12	Input	Test pin. Connect this pin to Vss

Timer V	TMOV	91	88	Output	This is an output pin for wavefo generated by the output compa
	TMCIV	90	87	Input	External event input pin.
	TMRIV	89	86	Input	Counter reset input pin.
	TRGV	73	70	Input	Count start trigger input pin.
Timer RC	FTCI	56	53	Input	External event input pin.
	FTIOA to FTIOD	49 to 52	46 to 49	I/O	Output compare output/input ca input/PWM output pin.
	TRGC	49	46	Input	External trigger input pin.
	$\overline{\text{TRCOI}}$	8	5	Input	Input pin for the timer output enable/disable signal.
Timer RD_0	FTIOA0	40	37	I/O	Output compare output/input ca input/external clock input pin.
	FTIOB0	41	38	I/O	Output compare output/input ca input/PWM output pin.
	FTIOC0	43	40	I/O	Output compare output/input ca input/PWM synchronous output reset or in complementary PWM
	FTIOD0	44	41	I/O	Output compare output/input ca input/PWM output pin.
	FTIOA1	45	42	I/O	Output compare output/input ca input/PWM output pin (at a rese complementary PWM mode).
	FTIOB1 to FTIOD1	46 to 48	43 to 45	I/O	Output compare output/input ca input/PWM output pin.
	$\overline{\text{TRDOI\_0}}$	9	6	Input	Input pin for the timer output enable/disable signal.

	FTIOA3	36	33	I/O	Output compare output/input cap input/PWM output pin (at a reset complementary PWM mode)
	FTIOB3 to FTIOD3	37 to 39	34 to 36	I/O	Output compare output/input cap input/PWM output pin
	$\overline{\text{TRDOI\_1}}$	10	7	Input	Input pin for the timer output enable/disable signal.
I^2C bus interface 2 (IIC2)	SDA	84	81	I/O	IIC data I/O pin. Can directly driv by NMOS open-drain output. Wh this pin, external pull-up resistor required.
	SCL	85	82	I/O	IIC clock I/O pin. Can directly dri by NMOS open-drain output. Wh this pin, external pull-up resistor required.
Serial communication interface 3 (SCI3)	TXD, TXD_2, TXD_3	59, 88, 55	56, 85, 52	Output	Transmit data output pin
	RXD, RXD_2, RXD_3	58, 87, 54	55, 84, 51	Input	Receive data input pin
	SCK3, SCK3_2, SCK3_3	57, 86, 53	54, 83, 50	I/O	Clock I/O pin

P17 to P14, P12 to P10	73 to 71, 69, 68, 66, 65	70 to 68, 66, 65, 63, 62	I/O	7-bit I/O port
P27 to P20	64 to 57	61 to 54	I/O	8-bit I/O port
P37 to P30	24 to 31	21 to 28	I/O	8-bit I/O port
P57 to P50	85, 84, 79 to 74	82, 81, 76 to 71	I/O	8-bit I/O port
P77 to P74, P72 to P70	92 to 89, 88 to 86	89 to 86, 85 to 83	I/O	7-bit I/O port
P87 to P85	21 to 23	18 to 20	I/O	3-bit I/O port
PC3 to PC0	83 to 80	80 to 77	I/O	4-bit I/O port
PD7 to PD0	48 to 43, 41, 40	45 to 40, 38, 37	I/O	8-bit I/O port
PE7 to PE0	39 to 32	36 to 29	I/O	8-bit I/O port
PG7 to PG0	10 to 8, 6, 5, 3 to 1	7 to 5, 3, 2, 100 to 98	I/O	8-bit I/O port
PH7 to PH0	52 to 49, 56 to 53	49 to 46, 53 to 50	I/O	8-bit I/O port
PJ1, PJ0	17, 18	14, 15	I/O	2-bit I/O port

- General-register architecture

  Sixteen 16-bit general registers also usable as sixteen 8-bit registers and eight 16-bit or eight 32-bit registers
- 62 basic instructions

  8/16/32-bit data transfer and arithmetic and logic instructions

  Multiply and divide instructions

  Powerful bit-manipulation instructions
- Eight addressing modes

  Register direct [Rn]

  Register indirect [@ERn]

  Register indirect with displacement [@(d:16,ERn) or @(d:24,ERn)]

  Register indirect with post-increment or pre-decrement [@ERn+ or @–ERn]

  Absolute address [@aa:8, @aa:16, @aa:24]

  Immediate [#xx:8, #xx:16, or #xx:32]

  Program-counter relative [@(d:8,PC) or @(d:16,PC)]

  Memory indirect [@@aa:8]
- 16-Mbyte address space
- High-speed operation

  All frequently-used instructions execute in two to four states

  8/16/32-bit register-register add/subtract: 2 state

  8 × 8-bit register-register multiply: 14 states

  16 ÷ 8-bit register-register divide: 14 states

  16 × 16-bit register-register multiply: 22 states

  32 ÷ 16-bit register-register divide: 22 states

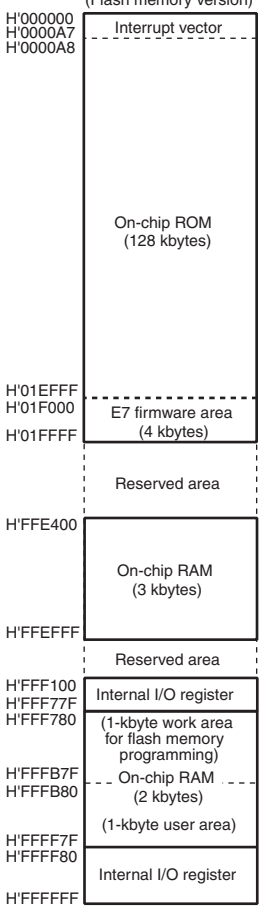


Figure 2.1 Memory Map

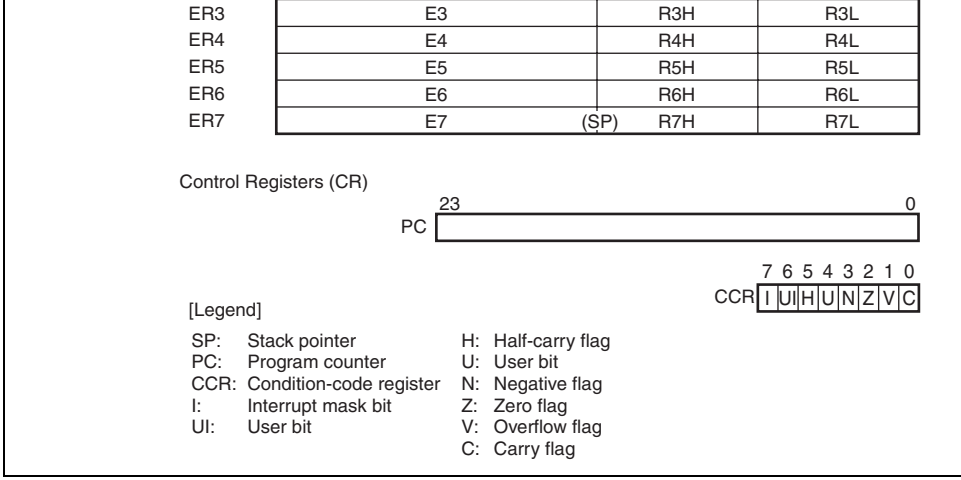


Figure 2.2 CPU Registers

The R registers divide into 8-bit registers designated by the letters RH (R0H to R7H) and
to R7L). These registers are functionally equivalent, providing a maximum of sixteen 8-b
registers.

The usage of each register can be selected independently.

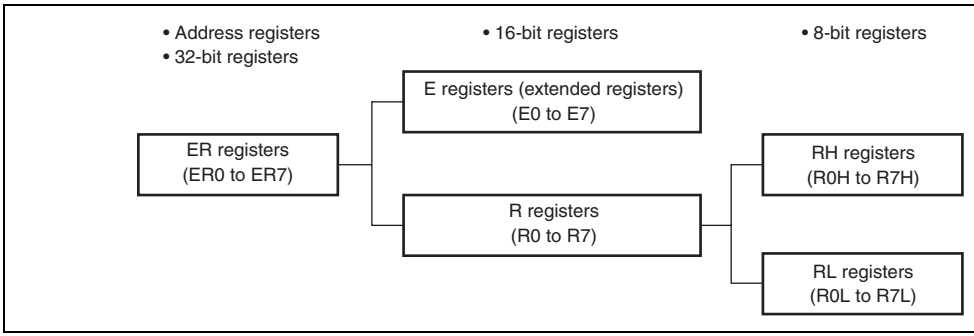


Figure 2.3 Usage of General Registers

General register ER7 has the function of stack pointer (SP) in addition to its general-regis
function, and is used implicitly in exception handling and subroutine calls. Figure 2.4 sho
relationship between the stack pointer and the stack area.

Figure 2.4 Relationship between Stack Pointer and Stack Area

2.2.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. Th
of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (
instruction is fetched, the least significant PC bit is regarded as 0). The PC is initialized
start address is loaded by the vector address generated during reset exception-handling s

2.2.3 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask
half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. The I bit is initi
by reset exception-handling sequence, but other bits are not initialized.

Some instructions leave flag bits unchanged. Operations can be performed on the CCR b
LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as
conditions for conditional branch (Bcc) instructions.

For the action of each instruction on the flag bits, see appendix A.1, Instruction List.

				or NEG.B instruction is executed, this flag is se there is a carry or borrow at bit 3, and cleared t otherwise. When the ADD.W, SUB.W, CMP.W NEG.W instruction is executed, the H flag is se there is a carry or borrow at bit 11, and clearec otherwise. When the ADD.L, SUB.L, CMP.L, o instruction is executed, the H flag is set to 1 if t carry or borrow at bit 27, and cleared to 0 othe
4	U	Undefined	R/W	User Bit Can be written and read by software using the STC, ANDC, ORC, and XORC instructions.
3	N	Undefined	R/W	Negative Flag Stores the value of the most significant bit of da sign bit.
2	Z	Undefined	R/W	Zero Flag Set to 1 to indicate zero data, and cleared to 0 indicate non-zero data.
1	V	Undefined	R/W	Overflow Flag Set to 1 when an arithmetic overflow occurs, a cleared to 0 at other times.
0	C	Undefined	R/W	Carry Flag Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by: • Add instructions, to indicate a carry • Subtract instructions, to indicate a borrow • Shift and rotate instructions, to indicate a ca The carry flag is also used as a bit accumulato manipulation instructions.

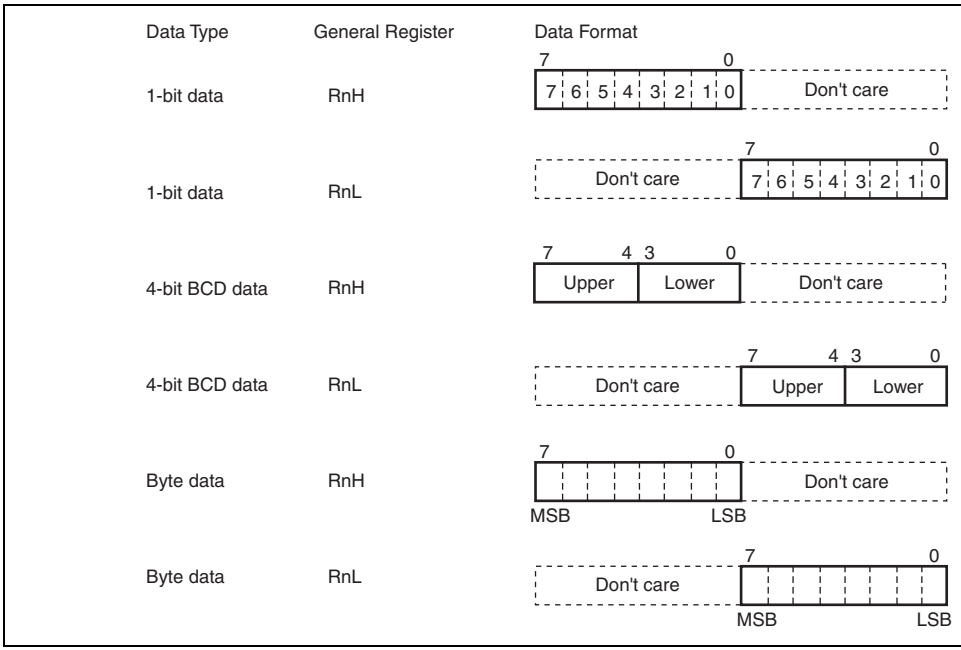


Figure 2.5 General Register Data Formats (1)

[Legend]

ERn: General register ER
En: General register E
Rn: General register R
RnH: General register RH
RnL: General register RL
MSB: Most significant bit
LSB: Least significant bit

Figure 2.5 General Register Data Formats (2)

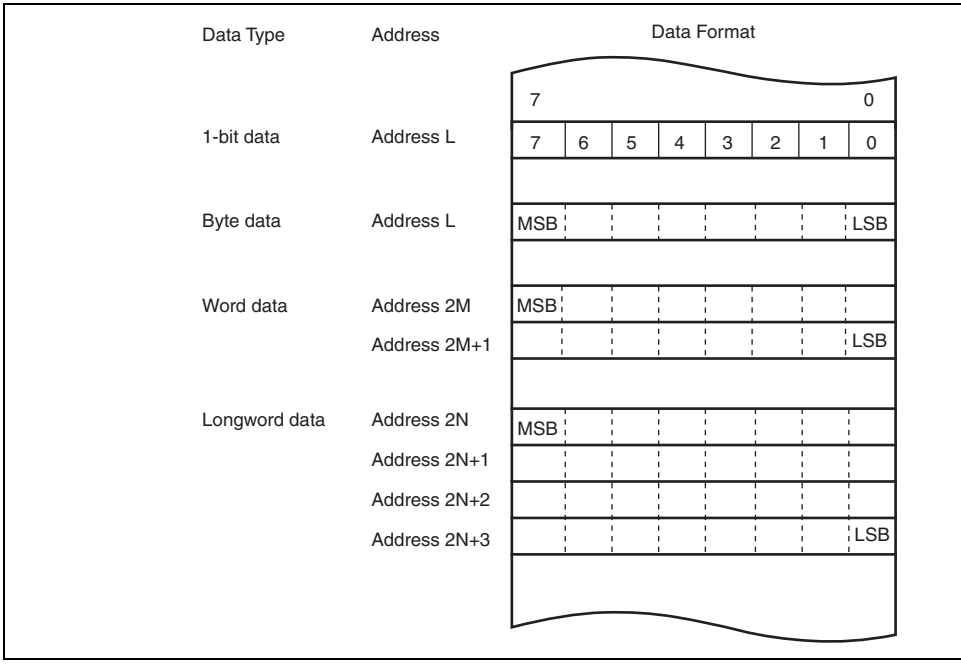


Figure 2.6 Memory Data Formats

Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register or address register)
(EAd)	Destination operand
(EAs)	Source operand
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical XOR
→	Move
~	NOT (logical complement)
:3/:8/:16/:24	3-, 8-, 16-, or 24-bit length

Note: * General registers include 8-bit registers (R0H to R7H, R0L to R7L), 16-bit regis
to R7, E0 to E7), and 32-bit registers/address register (ER0 to ER7).

		Pops a general register from the stack. POP.W Rn is identical MOV.W @SP+, Rn. POP.L ERn is identical to MOV.L @SP+,
PUSH	W/L	Rn → @–SP Pushes a general register onto the stack. PUSH.W Rn is identi MOV.W Rn, @–SP. PUSH.L ERn is identical to MOV.L ERn, @

[Legend]

B: Byte

W: Word

L: Longword

Note: * Refers to the operand size.

DEC		Increments or decrements a general register by 1 or 2. (Byte op can be incremented or decremented by 1 only.)
ADDS SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit
DAA DAS	B	Rd (decimal adjust) → Rd Decimal-adjusts an addition or subtraction result in a general re referring to the CCR to produce 4-bit BCD data.
MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general register 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
DIVXU	B/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: eith bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 16-bit quotient and 16-bit remainder.

[Legend]

B: Byte

W: Word

L: Longword

Note: * Refers to the operand size.

		Takes the two's complement (arithmetic complement) of data i general register.
EXTU	W/L	Rd (zero extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the bits of a 32-bit register to longword size, by padding with zeros left.
EXTS	W/L	Rd (sign extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the bits of a 32-bit register to longword size, by extending the sign

[Legend]

B: Byte

W: Word

L: Longword

Note: * Refers to the operand size.

		another general register or immediate data.
NOT	B/W/L	~ (Rd) → (Rd) Takes the one's complement (logical complement) of general re contents.

[Legend]

B: Byte

W: Word

L: Longword

Note: * Refers to the operand size.

Table 2.5 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B/W/L	Rd (shift) → Rd Performs an arithmetic shift on general register contents.
SHLL SHLR	B/W/L	Rd (shift) → Rd Performs a logical shift on general register contents.
ROTL ROTR	B/W/L	Rd (rotate) → Rd Rotates general register contents.
ROTXL ROTXR	B/W/L	Rd (rotate) → Rd Rotates general register contents through the carry flag.

[Legend]

B: Byte

W: Word

L: Longword

Note: * Refers to the operand size.

BNOT	B	~ (<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in a general register or memory operand number is specified by 3-bit immediate data or the lower three general register.
BTST	B	~ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory operand a or clears the Z flag accordingly. The bit number is specified by immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C ANDs the carry flag with a specified bit in a general register or operand and stores the result in the carry flag.
BIAND	B	C ∧ ~ (<bit-No.> of <EAd>) → C ANDs the carry flag with the inverse of a specified bit in a gene register or memory operand and stores the result in the carry fl The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the carry flag with a specified bit in a general register or m operand and stores the result in the carry flag.
BIOR	B	C ∨ ~ (<bit-No.> of <EAd>) → C ORs the carry flag with the inverse of a specified bit in a gener or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

[Legend]

B: Byte

Note: * Refers to the operand size.

		carry flag.
BILD	B	~ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or m operand to the carry flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general regis memory operand.
BIST	B	~ C → (<bit-No.> of <EAd>) Transfers the inverse of the carry flag value to a specified bit in general register or memory operand. The bit number is specified by 3-bit immediate data.

[Legend]

B: Byte

Note: * Refers to the operand size.

BCC(BHS)	Carry clear (high or same)	C = 0
BCS(BLO)	Carry set (low)	C = 1
BNE	Not equal	Z = 0
BEQ	Equal	Z = 1
BVC	Overflow clear	V = 0
BVS	Overflow set	V = 1
BPL	Plus	N = 0
BMI	Minus	N = 1
BGE	Greater or equal	N ⊕ V = 0
BLT	Less than	N ⊕ V = 1
BGT	Greater than	Z∨(N ⊕ V) = 0
BLE	Less or equal	Z∨(N ⊕ V) = 1

JMP	—	Branches unconditionally to a specified address.
BSR	—	Branches to a subroutine at a specified address.
JSR	—	Branches to a subroutine at a specified address.
RTS	—	Returns from a subroutine

Note: * Bcc is the general name for conditional branch instructions.

		by word access.
ANDC	B	CCR ∧ #IMM → CCR Logically ANDs the CCR with immediate data.
ORC	B	CCR ∨ #IMM → CCR Logically ORs the CCR with immediate data.
XORC	B	CCR ⊕ #IMM → CCR Logically XORs the CCR with immediate data.
NOP	—	PC + 2 → PC Only increments the program counter.

[Legend]

B: Byte

W: Word

Note: * Refers to the operand size.

else next;

Transfers a data block. Starting from the address set in ER5, tr
data for the number of bytes set in R4L or R4 to the address lo
in ER6.

Execution of the next instruction begins as soon as the transfe
completed.

on the operand. The operation field always includes the first four bits of the instruction. S
instructions have two operation fields.

(2) Register Field

Specifies a general register. Address registers are specified by 3 bits, and data registers by
4 bits. Some instructions have two register fields. Some have no register field.

(3) Effective Address Extension

8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement. A 24-
address or displacement is treated as a 32-bit data in which the upper 8 bits are 0 (H'00).

(4) Condition Field

Specifies the branching condition of Bcc instructions.

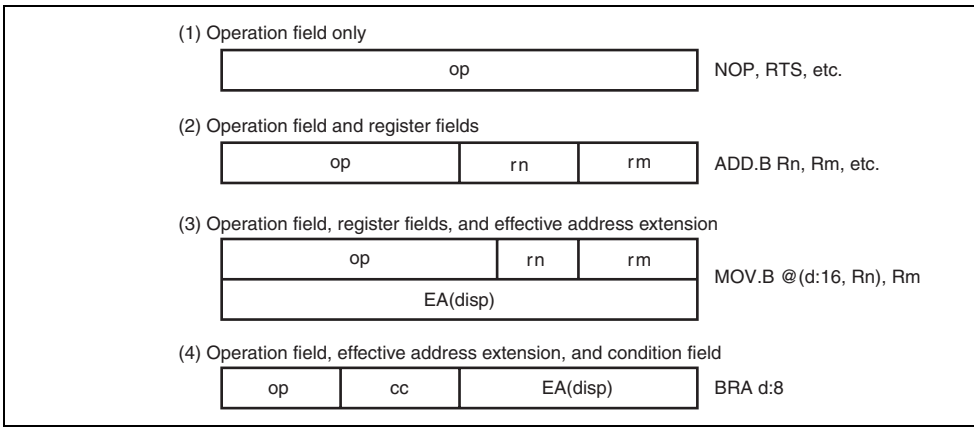


Figure 2.7 Instruction Formats

Bit-manipulation instructions use register direct, register indirect, or the absolute addres
(@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST ins
or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.10 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:24,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

(1) Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register contain
operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and
can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

(2) Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn), the lower 2
which contain the address of the operand on memory.

added to the address register contents (32 bits) and the sum is stored in the address reg
The value added is 1 for byte access, 2 for word access, or 4 for longword access. For
or longword access, the register value should be even.

- Register indirect with pre-decrement—@-ERn

  The value 1, 2, or 4 is subtracted from an address register (ERn) specified by the regis
  in the instruction code, and the lower 24 bits of the result is the address of a memory
  The result is also stored in the address register. The value subtracted is 1 for byte acce
  word access, or 4 for longword access. For the word or longword access, the register
  should be even.

(5) Absolute Address—@aa:8, @aa:16, @aa:24

The instruction code contains the absolute address of a memory operand. The absolute ad
may be 8 bits long (@aa:8), 16 bits long (@aa:16), 24 bits long (@aa:24)

For an 8-bit absolute address, the upper 16 bits are all assumed to be 1 (H'FFFF). For a 1
absolute address the upper 8 bits are a sign extension. A 24-bit absolute address can acces
entire address space.

The access ranges of absolute addresses for the group of this LSI are those shown in table

Table 2.11 Absolute Address Access Ranges

Absolute Address	Access Range
8 bits (@aa:8)	H'FFFF00 to H'FFFFFF
16 bits (@aa:16)	H'000000 to H'007FFF
	H'FF8000 to H'FFFFFF
24 bits (@aa:24)	H'000000 to H'FFFFFF

This mode is used in the BSR instruction. An 8-bit or 16-bit displacement contained in t
instruction is sign-extended and added to the 24-bit PC contents to generate a branch ad
PC value to which the displacement is added is the address of the first byte of the next in
so the possible branching range is –126 to +128 bytes (–63 to +64 words) or –32766 to +
bytes (–16383 to +16384 words) from the branch instruction. The resulting value should
even number.

(8) Memory Indirect—@@aa:8

This mode can be used by the JMP and JSR instructions. The instruction code contains a
absolute address specifying a memory operand. This memory operand contains a branch
The memory operand is accessed by longword access. The first byte of the memory oper
ignored, generating a 24-bit branch address. Figure 2.8 shows how to specify branch add
memory indirect mode.

The upper bits of the absolute address are all assumed to be 0, so the address range is 0 t
(H'0000 to H'00FF). Note that the first part of the address range is also the exception vec

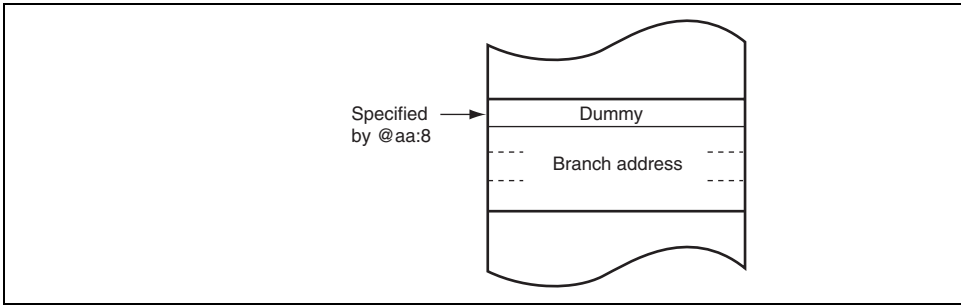
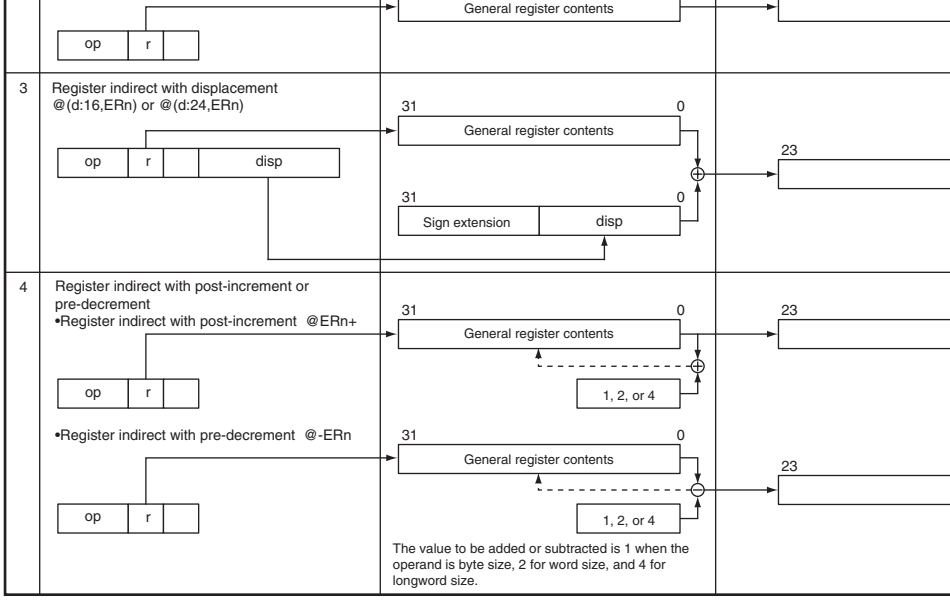
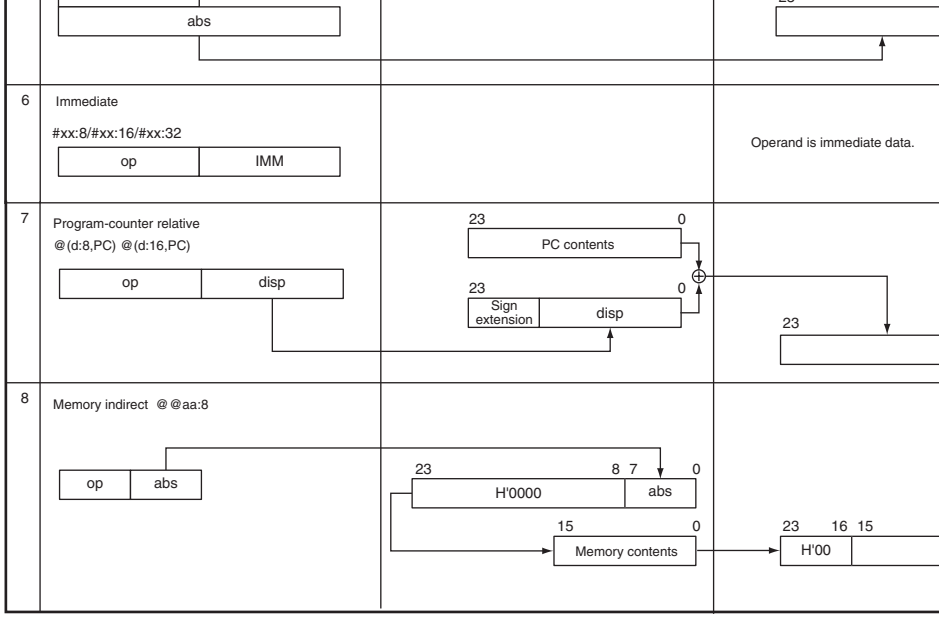


Figure 2.8 Branch Address Specification in Memory Indirect Mode


General register contents
op
r
3
Register indirect with displacement
@(d:16,ERn) or @(d:24,ERn)
31
0
General register contents
op
r
disp
23
31
0
Sign extension
disp
4
Register indirect with post-increment or
pre-decrement
•Register indirect with post-increment @ERn+
31
0
General register contents
23
op
r
1, 2, or 4
•Register indirect with pre-decrement @-ERn
31
0
General register contents
23
op
r
1, 2, or 4
The value to be added or subtracted is 1 when the operand is byte size, 2 for word size, and 4 for longword size.



[Legend]
r, rm,rn : Register field
op : Operation field
disp : Displacement
IMM : Immediate data
abs : Absolute address

in byte or word size. Figure 2.9 shows the on-chip memory access cycle.

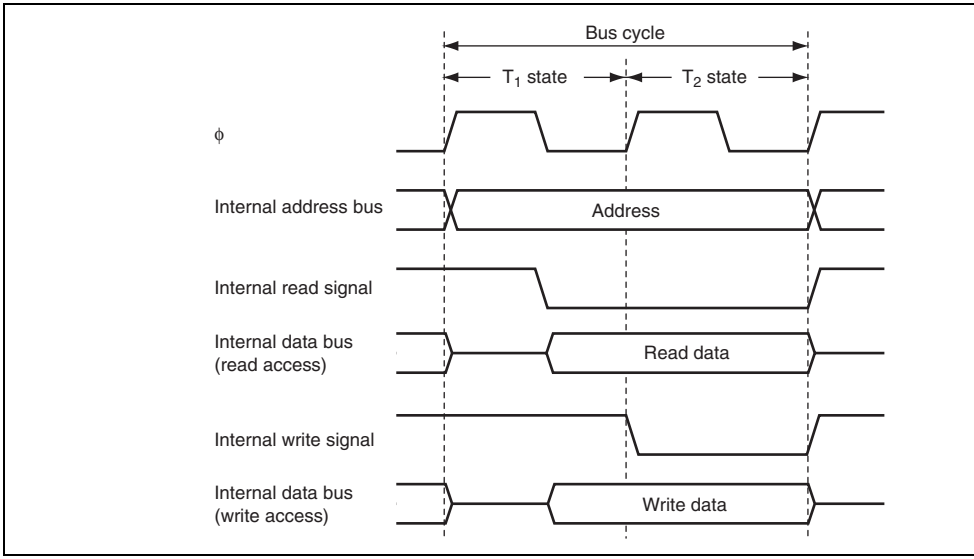


Figure 2.9 On-Chip Memory Access Cycle

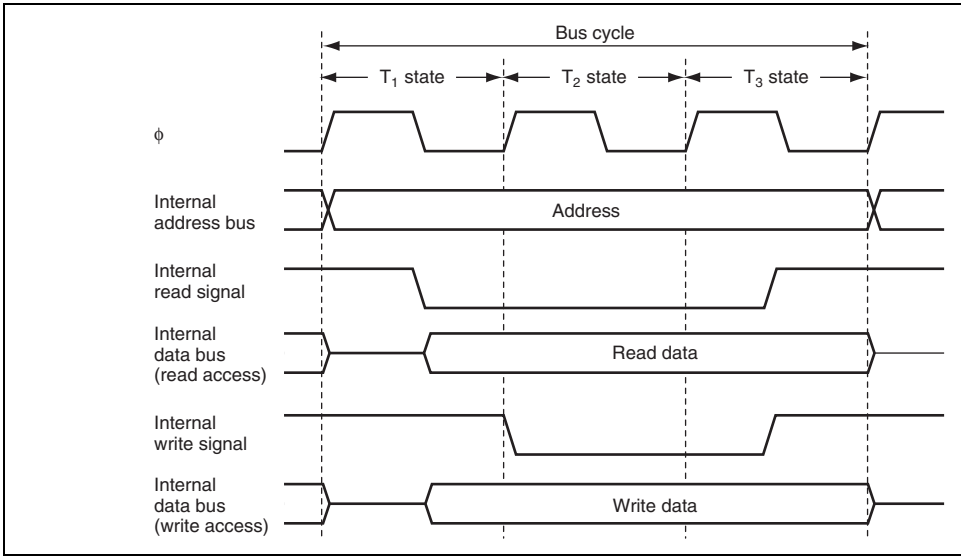


Figure 2.10 On-Chip Peripheral Module Access Cycle (3-State Access)

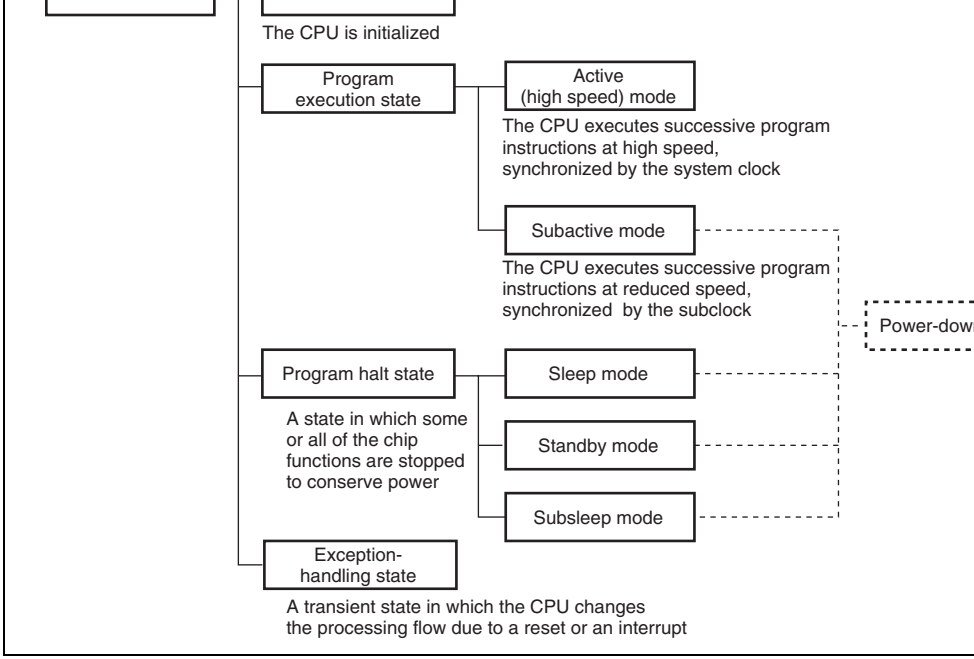


Figure 2.11 CPU Operation States

Figure 2.12 State Transitions

2.8 Usage Notes

2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and
I/O registers areas available to the user. When data is transferred from CPU to empty ar
transferred data will be lost. This action may also cause the CPU to malfunction. When
transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by
R4L, which starts from the address indicated by ER5, to the address indicated by ER6. S
R4L and ER6 so that the end address of the destination address (value of ER6 + R4 or E
does not exceed H'FFFFFF (the value of ER6 must not change from H'FFFFFF to H'000
during execution).

2.8.3 Bit Manipulation Instruction

The BSET, BCLR, BNOT, BST, and BIST instructions read data from the specified add
byte units, manipulate the data of the target bit, and write data to the same address again
units. Special care is required when using these instructions in cases where two registers
assigned to the same address, or when a bit is directly manipulated for a port or a registe
containing a write-only bit, because this may rewrite data of a bit other than the bit to be
manipulated.

2. The CPU sets or resets the bit to be manipulated with the bit-manipulation instruction
3. The written data is written again in byte units to the timer load register.

The timer is counting, so the value read is not necessarily the same as the value in the tim
register. As a result, bits other than the intended bit in the timer counter may be modified
modified value may be written to the timer load register.

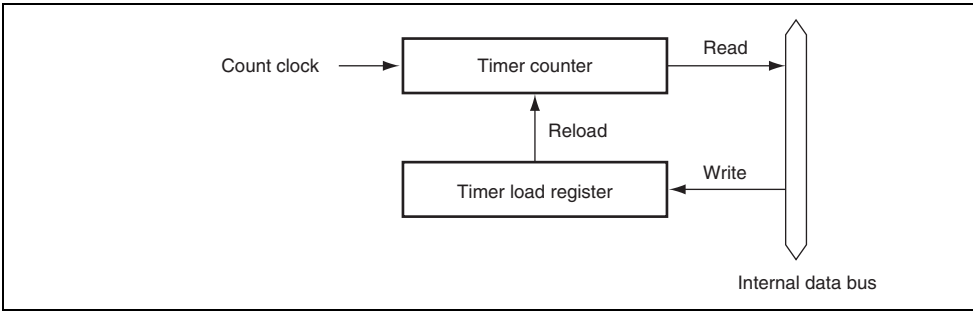


Figure 2.13 Example of Timer Configuration with Two Registers Allocated to Same Address

PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0

- BSET instruction executed instruction

```
BSET    #0,     @PDR5
```

The BSET instruction is executed for port 5.

- After executing BSET instruction

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**
Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	0	1	0	0	0	0	0

- Description on operation

1. When the BSET instruction is executed, first the CPU reads port 5.
   Since P57 and P56 are input pins, the CPU reads the pin states (low-level and high-l input).
   P55 to P50 are output pins, so the CPU reads the value in PDR5. In this example PD value of H'80, but the value read by the CPU is H'40.
2. Next, the CPU sets bit 0 of the read data to 1, changing the PDR5 data to H'41.
3. Finally, the CPU writes H'41 to PDR5, completing execution of BSET instruction.

Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0
RAM0	1	0	0	0	0	0	0

- BSET instruction executed

```
BSET    #0,    @RAM0
```

The BSET instruction is executed designating the
work area (RAM0).

- After executing BSET instruction

```
MOV.B   @RAM0, R0L
MOV.B   R0L,   @PDR5
```

The work area (RAM0) value is written to PDR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**
Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0
RAM0	1	0	0	0	0	0	0

Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0

- BCLR instruction executed

```
BCLR    #0,     @PCR5
```

The BCLR instruction is executed for PCR5.

- After executing BCLR instruction

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**
Input/output	Output	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	1	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0

- Description on operation

1. When the BCLR instruction is executed, first the CPU reads PCR5. Since PCR5 is a register, the CPU reads a value of H'FF, even though the PCR5 value is actually H'3
2. Next, the CPU clears bit 0 in the read data to 0, changing the data to H'FE.
3. Finally, H'FE is written to PCR5 and BCLR instruction execution ends.

Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1

- BCLR instruction executed

```
BCLR    #0,     @RAM0
```

The BCLR instructions executed for the PCR5 wo
(RAM0).

- After executing BCLR instruction

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PCR5
```

The work area (RAM0) value is written to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**
Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1

Exception handling starts when a trap instruction (TRAPA) is executed. A vector ad
corresponding to a vector number from 0 to 3 which are specified in the instruction c
generated. Exception handling can be executed at all times in the program execution
regardless of the setting of the I bit in CCR.

- Interrupts

  External interrupts other than the NMI and internal interrupts other than the address
  masked by the I bit in CCR, and kept pending while the I bit is set to 1. Exception ha
  starts when the current instruction or exception handling ends, if an interrupt is requ

- Priority level

  The priority levels of interrupt sources other than the NMI and address break can be
  each module by the interrupt control register (ICR).

3.1 Exception Sources and Vector Address

Table 3.1 shows the vector addresses and priority of each exception handling. When mo
one interrupt is requested, handling is performed from the interrupt with the highest prio
priority level can be set for an interrupt source to which a bit in ICR is assigned. When p
level 1 (priority is given) is set for an interrupt source other than the NMI and address br
execution of the exception handling for the interrupt request has priority that for an inter
request whose source is set to priority level 0.

	Trap instruction #2	10	H'000028 to H'00002B	—
	Trap instruction #3	11	H'00002C to H'00002F	—
Address break	Break conditions satisfied	12	H'000030 to H'000033	—
CPU	Direct transition by executing the SLEEP instruction	13	H'000034 to H'000037	ICRA7
External interrupt pin	IRQ0 Low-voltage detection interrupt*	14	H'000038 to H'00003B	ICRA6
	IRQ1	15	H'00003C to H'00003F	ICRA5
	IRQ2	16	H'000040 to H'000043	ICRA4
	IRQ3	17	H'000044 to H'000047	ICRA3
	WKP	18	H'000048 to H'00004B	ICRA2
RTC	Overflow	19	H'00004C to H'00004F	ICRA1
—	Reserved for system use	20, 21	H'000050 to H'000053	—
Timer V	Compare match A Compare match B Overflow	22	H'000058 to H'00005B	ICRB6
SCI3	Receive data full Transmit data empty Transmit end Receive error	23	H'00005C to H'00005F	ICRB5
IIC2	Transmit data empty Transmit end Receive data full Arbitration lost/overrun error NACK detection Stop condition detected	24	H'000060 to H'000063	ICRB4

SCI3_3	Receive data full Transmit data empty Transmit end Receive error	34	H'000088 to H'00008B	ICRC2
Timer RC	Input capture A/compare match A Input capture B/compare match B Input capture C/compare match C Input capture D/compare match D Overflow	35	H'00008C to H'00008F	ICRC1
A/D converter	A/D conversion end	36	H'000090 to H'000093	ICRC0
Timer RD_0	Compare match/input capture A0 to D0 Overflow	37	H'000094 to H'000097	ICRD7
Timer RD_1	Compare match/input capture A1 to D1 Overflow	38	H'000098 to H'00009B	ICRD6
Timer RD_2	Compare match/input capture A2 to D2 Overflow	39	H'00009C to H'00009F	ICRD5
Timer RD_3	Compare match/input capture A3 to D3 Overflow	40	H'0000A0 to H'0000A3	ICRD4
Clock switching	When the system clock sources are switched from the external-input signal to the internal-generated signal	41	H'0000A4 to H'0000A7	ICRD3

Note: * A low-voltage detection interrupt is available only in the product with an on-ch
on reset and low-voltage detection circuit.

- Wakeup interrupt flag register (IWPR)
- Interrupt control registers A to D (ICRA to ICRD)

3.2.1 Interrupt Edge Select Register 1 (IEGR1)

IEGR1 selects the direction of an edge that generates interrupt requests of pins $\overline{\text{NMI}}$ and $\overline{\text{IRQ0}}$.

Bit	Bit Name	Initial Value	R/W	Description
7	NMIEG	0	R/W	NMI Edge Select 0: Falling edge of $\overline{\text{NMI}}$ pin input is detected 1: Rising edge of $\overline{\text{NMI}}$ pin input is detected
6 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	IEG3	0	R/W	IRQ3 Edge Select 0: Falling edge of $\overline{\text{IRQ3}}$ pin input is detected 1: Rising edge of $\overline{\text{IRQ3}}$ pin input is detected
2	IEG2	0	R/W	IRQ2 Edge Select 0: Falling edge of $\overline{\text{IRQ2}}$ pin input is detected 1: Rising edge of $\overline{\text{IRQ2}}$ pin input is detected
1	IEG1	0	R/W	IRQ1 Edge Select 0: Falling edge of $\overline{\text{IRQ1}}$ pin input is detected 1: Rising edge of $\overline{\text{IRQ1}}$ pin input is detected
0	IEG0	0	R/W	IRQ0 Edge Select 0: Falling edge of $\overline{\text{IRQ0}}$ pin input is detected 1: Rising edge of $\overline{\text{IRQ0}}$ pin input is detected

				1: Rising edge of $\overline{\text{WKP5}}$($\overline{\text{ADTRG}}$) pin input is
4	WPEG4	0	R/W	WKP4 Edge Select 0: Falling edge of $\overline{\text{WKP4}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP4}}$ pin input is detected
3	WPEG3	0	R/W	WKP3 Edge Select 0: Falling edge of $\overline{\text{WKP3}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP3}}$ pin input is detected
2	WPEG2	0	R/W	WKP2 Edge Select 0: Falling edge of $\overline{\text{WKP2}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP2}}$ pin input is detected
1	WPEG1	0	R/W	WKP1Edge Select 0: Falling edge of $\overline{\text{WKP1}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP1}}$ pin input is detected
0	WPEG0	0	R/W	WKP0 Edge Select 0: Falling edge of $\overline{\text{WKP0}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP0}}$ pin input is detected

				enabled.
5	IENWP	0	R/W	Wakeup Interrupt Enable This bit is an enable bit for signals $\overline{\text{WKP5}}$ to $\overline{\text{W}}$ When this bit is set to 1, an interrupt request is
4	—	1	—	Reserved This bit is always read as 1.
3	IEN3	0	R/W	IRQ3 Interrupt Enable When this bit is set to 1, an interrupt request of $\overline{\text{IRQ3}}$ signal is enabled.
2	IEN2	0	R/W	IRQ2 Interrupt Enable When this bit is set to 1, an interrupt request of $\overline{\text{IRQ2}}$ signal is enabled.
1	IEN1	0	R/W	IRQ1 Interrupt Enable When this bit is set to 1, an interrupt request of $\overline{\text{IRQ1}}$ signal is enabled.
0	IEN0	0	R/W	IRQ0 Interrupt Enable When this bit is set to 1, an interrupt request of $\overline{\text{IRQ0}}$ signal is enabled.

A bit in an interrupt enable register to disable the interrupt or a bit in an interrupt flag reg
be cleared while the interrupt is masked (I = 1). If the execution of clearing the above bi
interrupt request occurs at the same time while I = 0, the exception handling for the interr
executed after the bit has been cleared.

4 to 0	—	All 1	—	Reserved These bits are always read as 1.

A bit in an interrupt enable register to disable the interrupt or a bit in an interrupt flag re be cleared while the interrupt is masked (I = 1). If the execution of clearing the above b interrupt request occurs at the same time while I = 0, the exception handling for the inte executed after the bit has been cleared.

3.2.5 Interrupt Flag Register 1 (IRR1)

IRR1 is a status flag register for a direct transition interrupt, an RTC interrupt, and $\overline{\text{IRQ}}$ interrupts.

Bit	Bit Name	Initial Value	R/W	Description
7	IRRDT	0	R/W	Direct Transition Interrupt Request Flag [Setting condition] When a direct transition is made by executing SLEEP instruction while the DTON bit in SYS to 1. [Clearing condition] When writing 0

				[Setting condition] When the $\overline{\text{IRQ3}}$ pin is specified as an interrupt the specified edge is detected. [Clearing condition] When writing 0
2	IRRI2	0	R/W	IRQ2 Interrupt Request Flag [Setting condition] When the $\overline{\text{IRQ2}}$ pin is specified as an interrupt the specified edge is detected. [Clearing condition] When writing 0
1	IRRI1	0	R/W	IRQ1 Interrupt Request Flag [Setting condition] When the $\overline{\text{IRQ1}}$ pin is specified as an interrupt the specified edge is detected. [Clearing condition] When writing 0
0	IRRI0	0	R/W	IRQ0 Interrupt Request Flag [Setting condition] When the $\overline{\text{IRQ0}}$ pin is specified as an interrupt the specified edge is detected. [Clearing condition] When writing 0

				When the timer BT counter overflows
				[Clearing condition]
				When writing 0
4 to 0	—	All 1	—	Reserved
				These bits are always read as 1.

3.2.7 Wakeup Interrupt Flag Register (IWPR)

IWPR is a status flag register for $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$ interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved
				These bits are always read as 1.
5	IWPF5	0	R/W	WKP5 Interrupt Request Flag
				[Setting condition]
				When the $\overline{\text{WKP5}}$ pin is specified as an interru and the specified edge is detected
				[Clearing condition]
				When writing 0
4	IWPF4	0	R/W	WKP4 Interrupt Request Flag
				[Setting condition]
				When $\overline{\text{WKP4}}$ pin is specified as an interrupt ir the specified edge is detected
				[Clearing condition]
				When writing 0

				and the specified edge is detected. [Clearing condition] When writing 0
1	IWPF1	0	R/W	WKP1 Interrupt Request Flag [Setting condition] When the $\overline{\text{WKP1}}$ pin is specified as an interrup and the specified as an edge is detected [Clearing condition] When writing 0.
0	IWPF0	0	R/W	WKP0 Interrupt Request Flag [Setting condition] When the $\overline{\text{WKP0}}$ pin is specified as an interrup and the specified edge is detected [Clearing condition] When writing 0

priority level 1 (priority)

n = A to D

Note: * The initial values of the reserved bits are also all 0.

Table 3.2 Interrupt request and ICR

		Registers			
Bit	**Bit Name**	**ICRA**	**ICRB**	**ICRC**	**ICRD**
7	ICRn7	Direct transition	—	Timer B1	Time
6	ICRn6	IRQ0, Low-voltage detection	Timer V	—	Time
5	ICRn5	IRQ1	SCI3	—	Time
4	ICRn4	IRQ2	IIC2	SCI3_2	Time
3	ICRn3	IRQ3	—	—	Clock switc
2	ICRn2	WKP	—	SCI3_3	—
1	ICRn1	RTC	—	Timer RC	—
0	ICRn0	—	—	A/D converter	—

n = A to D

—: Reserved. These bits are always read as 0.

Low-Voltage Detection Circuits (Optional).

The reset exception handling sequence is as follows:

1. Set the I bit in the condition code register (CCR) to 1.
2. The CPU generates the vector address for the reset exception handling (from H'00000 H'000003), the data in the address is sent to the program counter (PC) as the start add program execution starts from the address.

3.4 Interrupt Exception Handling

3.4.1 External Interrupts

As the external interrupts, there are the NMI, IRQ3 to IRQ0, and WKP5 to WKP0 interru

- NMI Interrupt

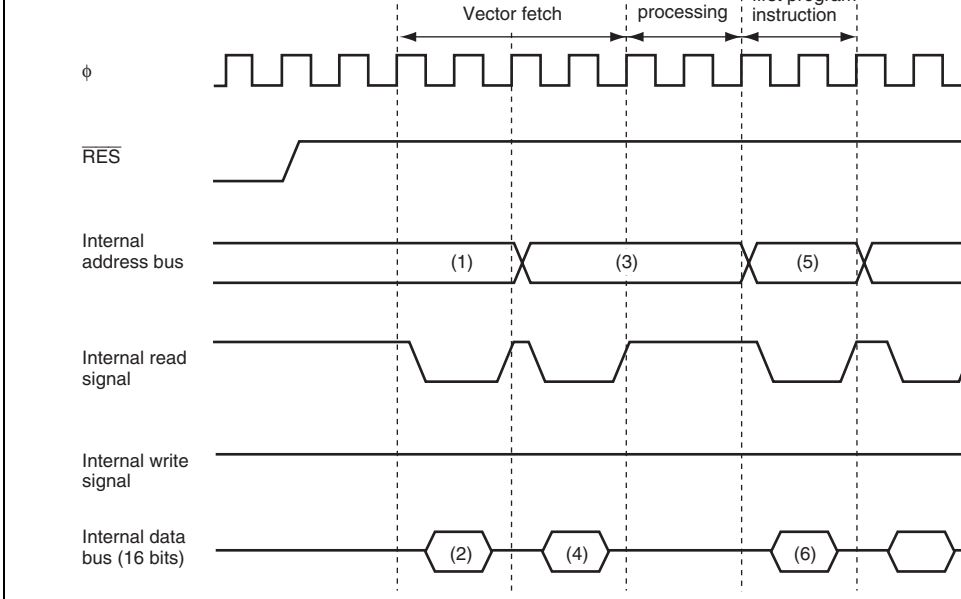
  An NMI interrupt is generated when the edge of the $\overline{\text{NMI}}$ signal is input. The detectin selected from rising or falling, depending on the setting of the NMIEG bit in IEGR1.

  Since the NMI interrupt is given the highest priority level, it can always be accepted r of the setting of the I bit in CCR.

- IRQ3 to IRQ0 Interrupts

  IRQ3 to IRQ0 interrupts are generated when the edges of the $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ signals ar These four interrupts are given different vector addresses, and the detecting edge of ea can be selected from rising or falling, depending on the settings of bits IEG3 to IEG0 IEGR1.

  When the $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ pins are specified as an interrupt input by PMR1 and the spe edge is input, the corresponding bit in IRR1 is set to 1, requesting the interrupt to the These interrupts can be masked by setting bits IEN3 to IEN0 in IENR1.



(1), (3) Address of reset vector: (1) = H'000000, (3) = H'000002
(2), (4) Start address (contents of reset vector)
(5) Start address
(6) First instruction of program

Figure 3.1 Reset Sequence

3.4.3 Interrupt Handling Sequence

Interrupts are controlled by an interrupt controller.

Interrupt operation is described below.

1. If an NMI or an interrupt with its enable bit set to 1 is generated, an interrupt request s sent to the interrupt controller.
2. When multiple interrupt requests are generated, the interrupt controller requests the in handling with the highest priority level which has been set in ICR to the CPU. Other i requests are held pending. When the priority levels are the same, the interrupt controll an interrupt request according to the default priority levels shown in table 3.1.
3. The CPU accepts the NMI and address break regardless of the setting of the I bit. Oth interrupt requests are accepted, if the I bit is cleared to 0 in CCR; if the I bit is set to 1 interrupt request is held pending.
4. If the CPU accepts the interrupt after execution of the current instruction is completed interrupt exception handling will begin. First, both PC and CCR are pushed onto the s stack status at this time is shown in figure 3.3. The PC value pushed onto the stack is address of the first instruction to be executed upon return from interrupt handling.
5. Then, the I bit in CCR is set to 1, masking further interrupts excluding the NMI and a break. Upon return from interrupt handling, the values of I bit and other bits in CCR v restored and returned to the values prior to the start of interrupt exception handling.
6. Next, the CPU generates the vector address corresponding to the accepted interrupt, a transfers the address to PC as a start address of the interrupt handler. Then a program executing from the address indicated in PC.

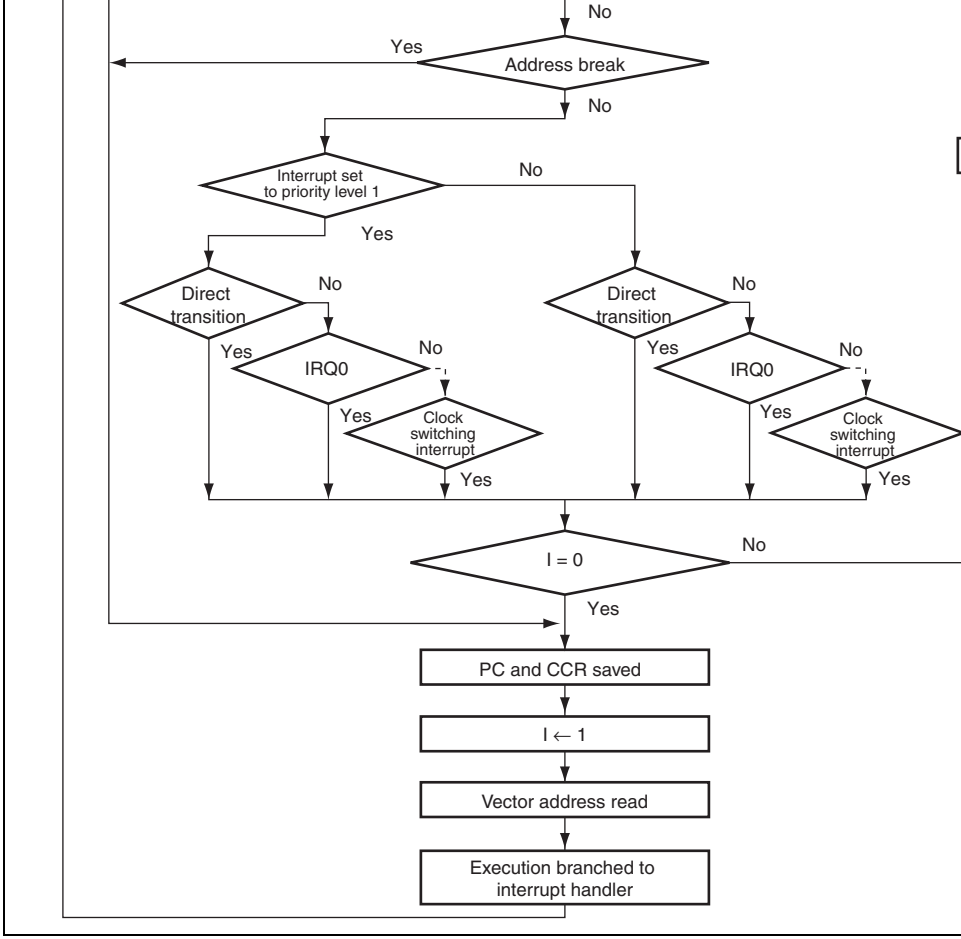


Figure 3.2 Interrupt Acceptance Flowchart

[Legend]
PCE: Bits 23 to 16 of program counter (PC)
PCH: Bits 15 to 8 of program counter (PC)
PCL: Bits 7 to 0 of program counter (PC)
CCR: Condition code register
SP: Stack pointer

Notes: 1. PC shows the address of the first instruction to be executed upon return from the interrupt handling routine.
2. Register contents must always be saved and restored by word length, starting from an even-numbered address.

Figure 3.3 Stack Status after Exception Handling

Figure 3.4 Interrupt Sequence

Saving of PC and CCR to stack	4
Vector fetch	4
Instruction fetch	4
Internal processing	4

Notes: 1. For internal interrupts, the number of states is 1.
2. Not including EEPMOV instruction.

3.5.2 Notes on Stack Area Use

When word data is accessed, the least significant bit of the address is regarded as 0. Acc
stack always takes place in words, so the stack pointer (SP: ER7) should never indicate
address. Use PUSH Rn (MOV.W Rn, @–SP) or POP Rn (MOV.W @SP+, Rn) to save
register values.

3.5.3 Notes on Rewriting Port Mode Registers

When a port mode register is rewritten to switch the functions of external interrupt pins,
$\overline{\text{IRQ0}}$, and $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$, the interrupt request flag may be set to 1.

When switching pin functions, mask the interrupt before setting the bit in the port mode
After accessing the port mode register, execute at least one instruction (e.g., NOP), then
interrupt request flag from 1 to 0.

Figure 3.5 shows a port mode register setting and interrupt request flag clearing procedu

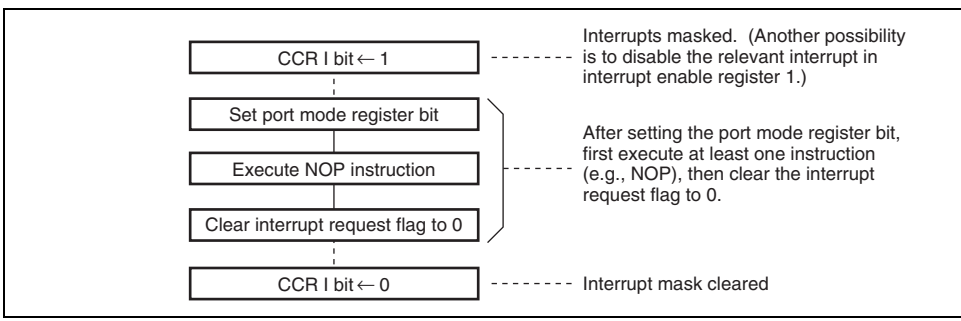
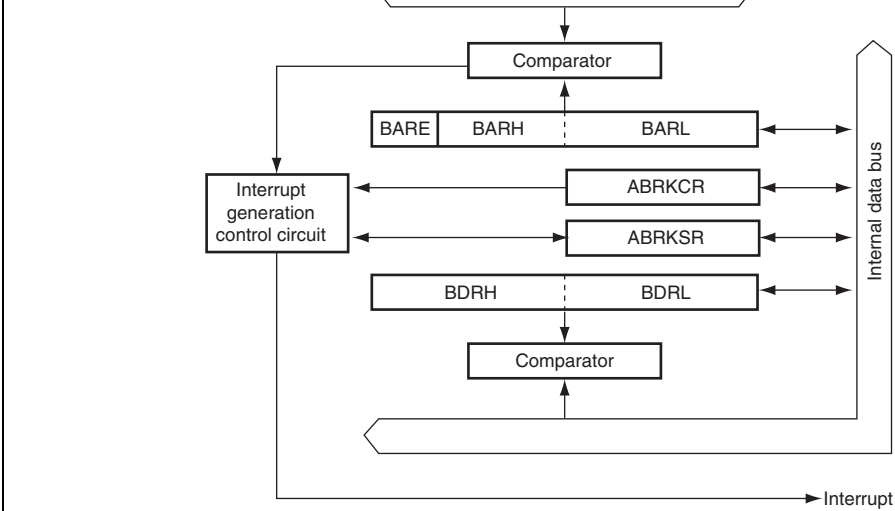


Figure 3.5 Port Mode Register Setting and Interrupt Request Flag Clearing Pr



[Legend]
BARE, BARH, BARL: Break address register
BDRH, BDRL: Break data register
ABRKCR: Address break control register
ABRKSR: Address break status register

Figure 4.1 Block Diagram of Address Break

ABRKCR sets address break conditions.

Bit	Bit Name	Initial Value	R/W	Description
7	RTINTE	1	R/W	RTE Interrupt Enable When this bit is 0, the interrupt immediately aft executing RTE is masked and then one instruc be executed. When this bit is 1, the interrupt is masked.
6	CSEL1	0	R/W	Condition Select 1 and 0 These bits set address break conditions. 00: Instruction execution cycle 01: CPU data read cycle 10: CPU data write cycle 11: CPU data read/write cycle
5	CSEL0	0	R/W	
4	ACMP2	0	R/W	Address Compare 2 to 0 These bits set the comparison condition betwe address set in BAR and the internal address bu 000: Compares 24-bit addresses 001: Compares upper 20-bit addresses 010: Compares upper 16-bit addresses 011: Compares upper 12-bit addresses 1xx: Reserved
3	ACMP1	0	R/W	
2	ACMP0	0	R/W	

[Legend]
x: Don't care.

When an address break is set in the data read cycle or data write cycle, the data bus used depend on the combination of the byte/word access and address. Table 4.1 shows the ac data bus used. When an I/O register space with an 8-bit data bus width is accessed in wo byte access is generated twice. For details on data widths of each register, see section 22 Register Addresses (Address Order).

Table 4.1 Access and Data Bus Used

	Word Access		Byte Access	
	Even Address	**Odd Address**	**Even Address**	**Odd A**
ROM space	Upper 8 bits	Lower 8 bits	Upper 8 bits	Upper
RAM space	Upper 8 bits	Lower 8 bits	Upper 8 bits	Upper
I/O register with 8-bit data bus width	Upper 8 bits	Upper 8 bits	Upper 8 bits	Upper
I/O register with 16-bit data bus width	Upper 8 bits	Lower 8 bits	—	—

				When 0 is written after ABIF=1 is read
6	ABIE	0	R/W	Address Break Interrupt Enable When this bit is 1, an address break interrupt r is enabled.
5 to 0	—	All 1	—	Reserved These bits are always read as 1.

4.1.3 Break Address Registers E, H, L (BARE, BARH, BARL)

BAR (BARE, BARH, BARL) is a 24-bit readable/writable register that sets the address f generating an address break interrupt. The initial value of this register is H'FFFFFF. Whe the address break condition to the instruction execution cycle, set the first byte address of instruction.

4.1.4 Break Data Registers H, L (BDRH, BDRL)

BDR (BDRH, BDRL) is a 16-bit readable/writable register that sets the data for generatin address break interrupt. BDRH is compared with the upper 8-bit data bus. BDRL is comp the lower 8-bit data bus. When memory or registers are accessed by byte, the upper 8-bit is used for even and odd addresses in the data transmission. Therefore, comparison data n set in BDRH for byte access. For word access, the data bus used depends on the address. section 4.1.1, Address Break Control Register (ABRKCR), for details. The initial value o register is undefined.

When the address break is specified in instruction execution cycle

Register setting
- ABRKCR = H'80
- BAR = H'025A

Program

```
  0258  NOP
* 025A  NOP
  025C  MOV.W @H'025A,R0
  0260  NOP
  0262  NOP
   :     :
```

Underline indicates the address to be stacked.

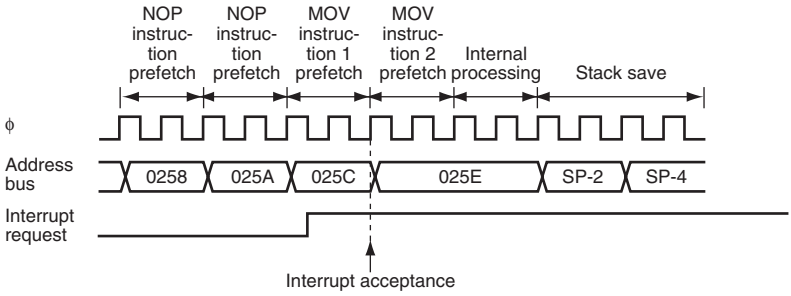


Figure 4.2 Address Break Interrupt Operation Example (1)

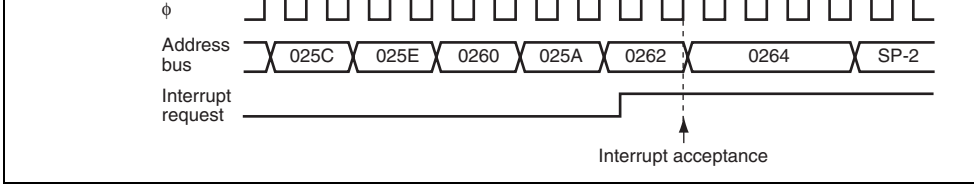


Figure 4.2 Address Break Interrupt Operation Example (2)

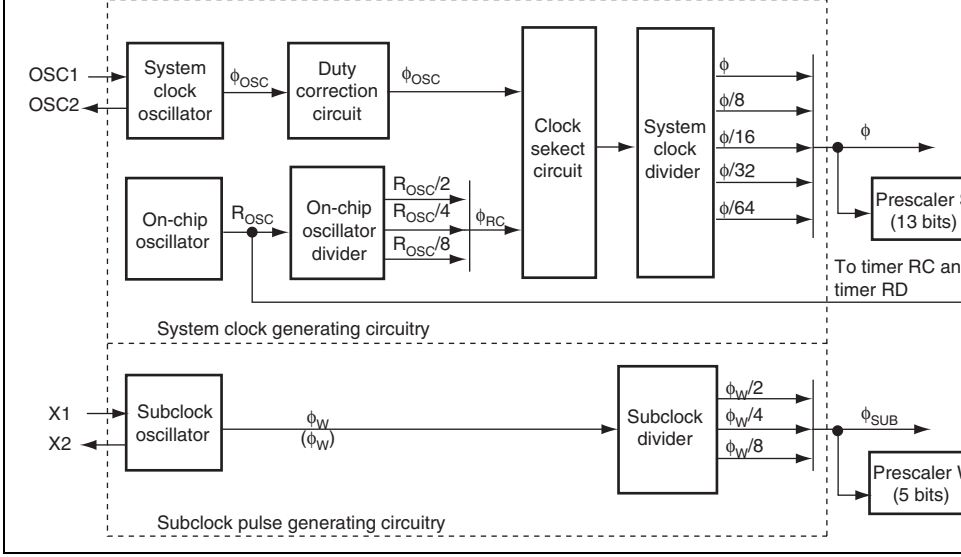


Figure 5.1 Block Diagram of Clock Pulse Generators

The system clock (ϕ) and subclock (ϕ_{SUB}) are basic clocks on which the CPU and on-chip peripheral modules operate. The system clock is divided by a value from 2 to 8192 in pr and the subclock is divided by a value from 8 to 128 in prescaler W. These divided clock supplied to respective on-chip peripheral modules. The on-chip oscillator can generate s clock ϕ_{RC}, which is produced by dividing R_{OSC} by 2, 4, or 8, and the ϕ_{40M} clock supplied to and timer RD.

- Frequency trimming

  The initial frequency of the on-chip oscillator is within the range shown above, so use need to trim the frequency. If needed, users can adjust the on-chip oscillator frequency range by rewriting the trimming registers.
- Interrupt can be requested to the CPU when the system clock is changed from the exte clock to the on-chip oscillator clock.

5.2 Register Descriptions

Clock oscillators are controlled by the following registers.

- RC control register (RCCR)
- RC trimming data protect register (RCTRMDPR)
- RC trimming data register (RCTRMDR)
- Clock control/status register (CKCSR)

				The system clock is generated by dividing this c this clock is supplied to timer RC or timer RD (ϕ 0: 32MHz 1: 40MHz
5	VCLSEL	0	R/W	Power Supply Select for On-Chip Oscillator 0: Selects VBGR 1: Selects VCL When VCL is selected, the accuracy of the on-c oscillator frequency cannot be guaranteed.
4 to 2	—	All 0	—	Reserved These bits are always read as 0.
1	RCPSC1	1	R/W	Division Ratio Select for On-Chip Oscillator
0	RCPSC0	0	R/W	These bits select the operating clock frequency mode or sleep mode when the on-chip oscillato The division ratio for dividing R_{osc} changes righ rewriting this bit. These bits can only be written to when the CKS CKCSR is 0. 0X: $R_{osc}/2$ 10: $R_{osc}/4$ 11: $R_{osc}/8$

[Legend]

X: Don't care

6	PRWE	0	R/W	Protect Information Write Enable Bits 5 and 4 can be written to when this bit is set [Setting condition] • When writing 0 to the WRI bit and writing 1 to PRWE bit [Clearing conditions] • Reset • When writing 0 to the WRI bit and writing 0 to PRWE bit
5	LOCKDW	0	R/W	Trimming Data Register Lock Down The RC trimming data register (RCTRMDR) can written to when this bit is set to 1. Once this bit is this register cannot be written to until a reset is in if 0 is written to this bit. [Setting condition] • When writing 0 to the WRI bit and writing 1 to TRMDRWE bit while the PRWE bit is 1. [Clearing condition] • Reset

				• When writing 0 to the WRI bit and writing 0 TRMDRWE bit while the PRWE bit is 1.
3 to 0	—	All 1	—	Reserved These bits are always read as 1.

5.2.3 RC Trimming Data Register (RCTRMDR)

RCTRMDR stores the trimming data of the on-chip oscillator frequency.

Bit	Bit Name	Initial Value	R/W	Description
7	TRMD7	(0)*	R/W	Trimming Data
6	TRMD6	(0)*	R/W	The trimming data is loaded to this register righ
5	TRMD5	(0)*	R/W	reset. The read data from these bits is always u
4	TRMD4	(0)*	R/W	The on-chip oscillator frequency can be trimme
3	TRMD3	(0)*	R/W	rewriting these bits. The frequency of the on-ch
2	TRMD2	(0)*	R/W	oscillator changes right after rewriting these bit bits are initialized to H'00.
1	TRMD1	(0)*	R/W	Changes in frequency are shown below (bit 7 is
0	TRMD0	(0)*	R/W	bit): (Min.) H'80 ← H'FF ← H'00 →H'01 → H'7F (Ma

Note: * These values are initialized while loading the trimming data.

				0 1 Hi-Z OSC1 (external cloc
				1 1 OSC2 OSC1
5	—	0	—	Reserved This bit is always read as 0.
4	OSCSEL	0	R/W	LSI Operating Clock Select This bit selects the system clock of this LSI. 0: Selects the on-chip oscillator clock as the syst 1: Selects the external clock as the system clock [Setting condition] • When writing 1 while the CKSWIF bit is 0* [Clearing condition] • When writing 0 Note: * When the on-chip oscillator is in the st state (the RCTSP bit in RCCR is set to not write 1 to this bit. When this bit is w 1, the on-chip oscillator should be in o
3	CKSWIE	0	R/W	Clock Switch Interrupt Enable Setting this bit to 1 enables the clock switch inter request.
2	CKSWIF	0	R/W	Clock Switch Interrupt Request Flag [Setting condition] • When the external clock is switched to the on oscillator clock [Clearing condition] • When writing 0 after reading 1

5.3.1 State Transition of System Clock

The system clock of this LSI is generated from the on-chip oscillator clock after a reset. clock sources can be switched from the on-chip oscillator clock to the external clock and versa by the user software.

Figure 5.2 shows the state transition of the system clock.

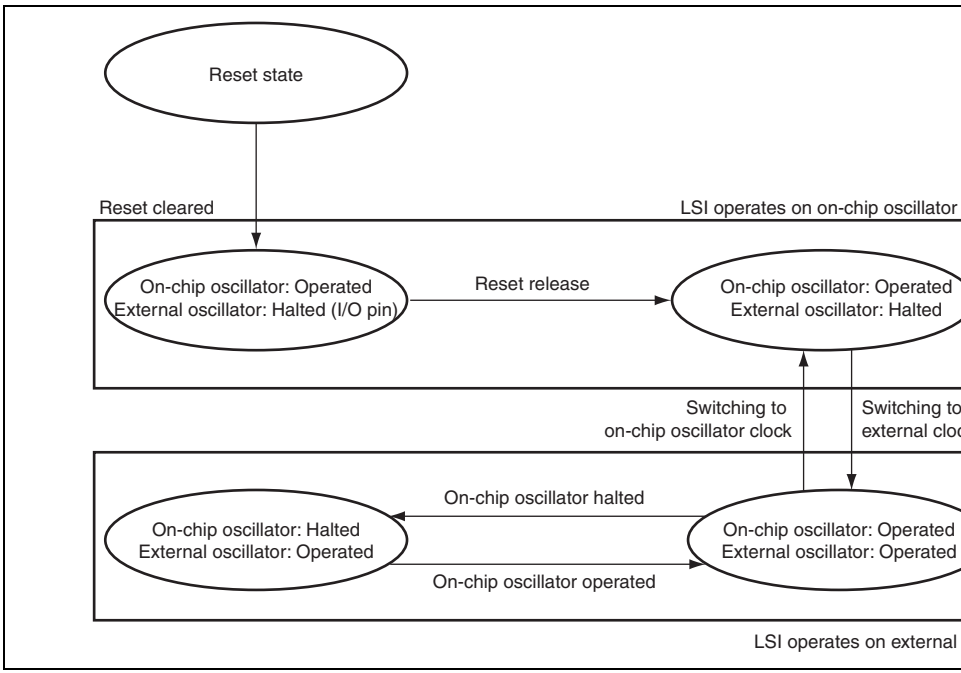
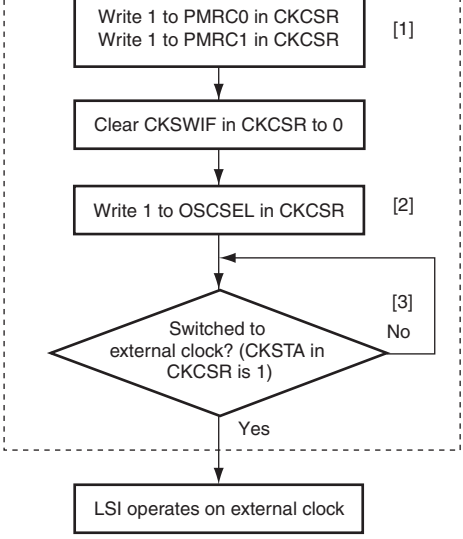


Figure 5.2 State Transition of System Clock



[2] After writing 1 to the OSCSEL bit, this LSI wait
oscillation of the external oscillator settles. The
correspondence between Nwait, which is the n
wait cycles for oscillation settling, and Nstby, w
the number of wait cycles for oscillation settling
returning from standby mode, is as follows:
Nstby ≤ Nwait ≤ 2 × Nstby
Nstby is set by bits STS2 to STS0 in SYSCR1
STS3 in SYSCR3. For details, see section 6.1.
Control Register 1 (SYSCR1), and section 6.1.
System Control Register 3 (SYSCR3).

[3] While waiting for external oscillation settling, th
not halted but continues to operate on the on-c
oscillator clock. Read the CKSTA bit in CKCSR
ensure whether or not clocks are switched.

Figure 5.3 Flowchart of Clock Switching (From On-Chip Oscillator Clock to External Clock)

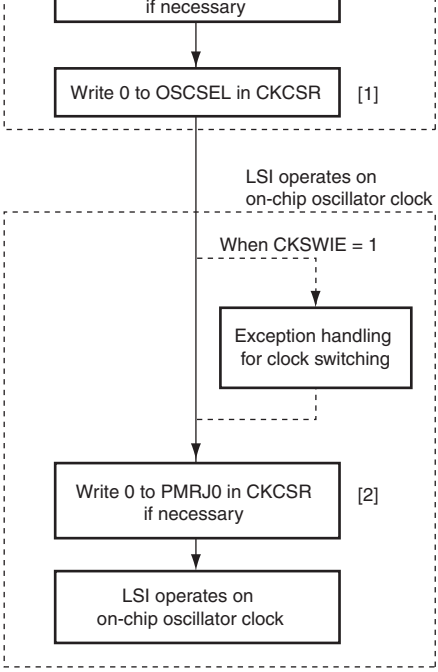
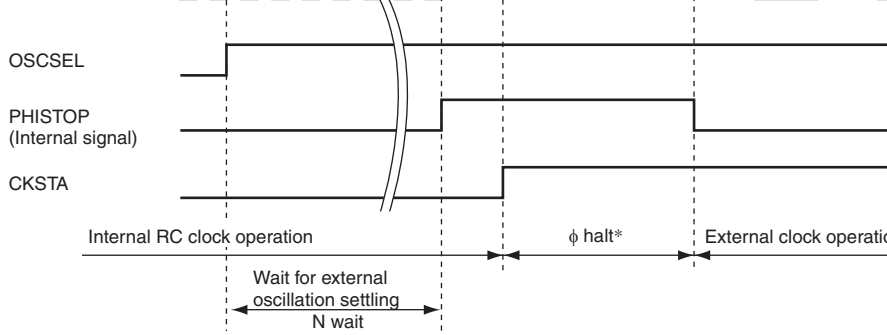


Figure 5.4 Flowchart of Clock Switching (From External Clock to On-Chip Oscillator Clock)

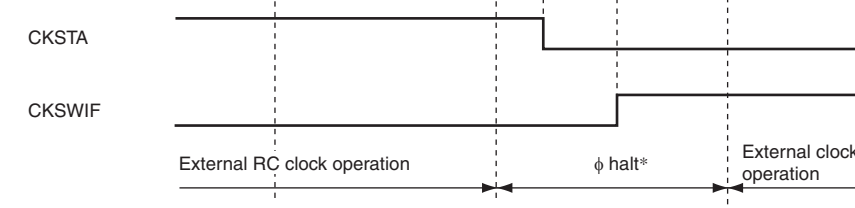


[Legend]

ϕ_{OSC}:	External clock
ϕ_{RC}:	Internal RC clock
ϕ:	System clock
OSCSEL:	Bit 4 in CKCSR
PHISTOP:	System clock stop control signal
CKSTA:	Bit 0 in CKCSR

Note: * The ϕ halt duration is the duration from the timing when the ϕ clock stops to the first rising edge of the ϕ_{OSC} clock after seven clock cycles of the ϕ_{RC} clock have elapsed.

Figure 5.5 Timing Chart of Switching from On-Chip Oscillator Clock to Externa

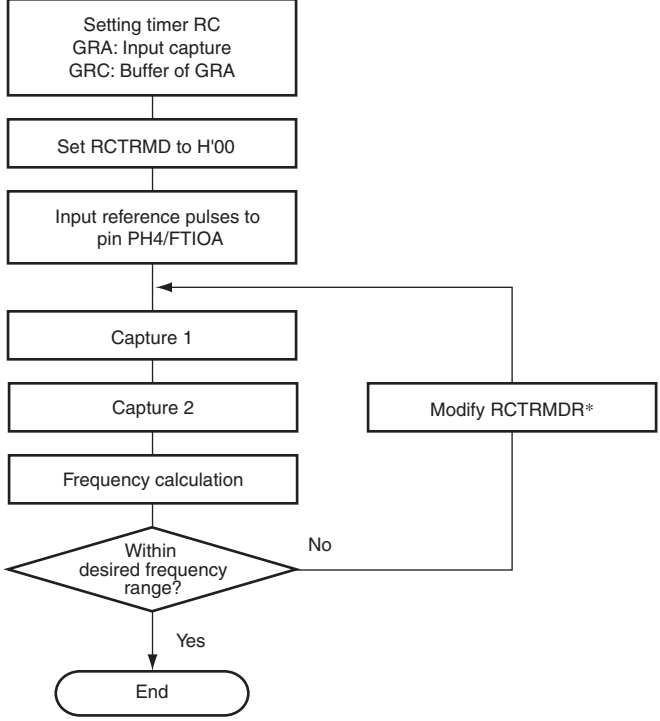


[Legend]

ϕ_{OSC}:	External clock
ϕ_{RC}:	Internal RC clock
φ:	System clock
OSCSEL:	Bit 4 in CKCSR
PHISTOP:	System clock stop control signal
CKSTA:	Bit 0 in CKCSR
CKSWIF:	Bit 2 in CKCSR

Note: * The φ halt duration is the duration from the timing when the φ clock stops to the seventh rising edge of the ϕ_{RC} clock.

Figure 5.6 Timing Chart to Switch from External Clock to On-Chip Oscillator



Note: * Comparing the difference between the measured frequency and the desired frequency, individual bits of RCTRMDR are decided from the MSB bit by bit.

Figure 5.7 Example of Trimming Flow for On-Chip Oscillator Frequency

Figure 5.8 Timing Chart of Trimming of On-Chip Oscillator Frequency

The on-chip oscillator frequency is obtained by the expression below. Since the input-c input is sampled at the rate of ϕ_{RC}, the calculated result includes a sampling error of ±1 ϕ cycle.

$$\phi RC = \frac{(M + \alpha) - M}{t_A} \text{ (MHz)}$$

ϕRC: Frequency of divided on-chip oscillator clock (MHz)
t_A: Cycle of reference clock (µs)
M: Timer RC counter value

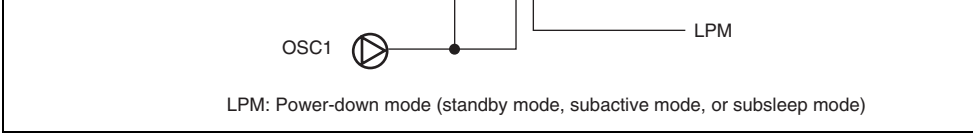


Figure 5.9 Block Diagram of External Oscillator

5.5.1 Connecting Crystal Resonator

Figure 5.10 shows an example of connecting a crystal resonator. An AT-cut parallel-reso crystal resonator should be used. Figure 5.11 shows the equivalent circuit of a crystal reso resonator having the characteristics given in table 5.1 should be used.

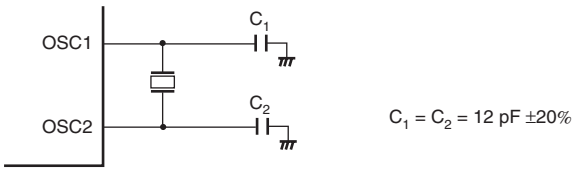


Figure 5.10 Example of Connection to Crystal Resonator

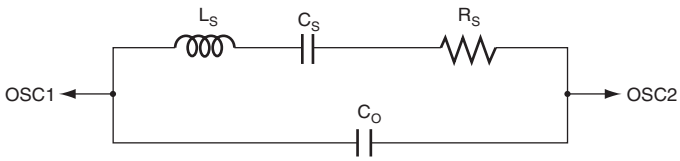
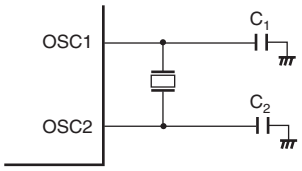


Figure 5.11 Equivalent Circuit of Crystal Resonator



C_1 = 30 pF ±10%
C_2 = 30 pF ±10%
Capacitances are reference values.

Figure 5.12 Example of Connection to Ceramic Resonator

5.5.3 External Clock Input Method

To use the external clock, input the external clock on pin OSC1 and leave pin OSC2 ope
5.13 shows an example of connection. The duty cycle of the external clock signal must l
55%.

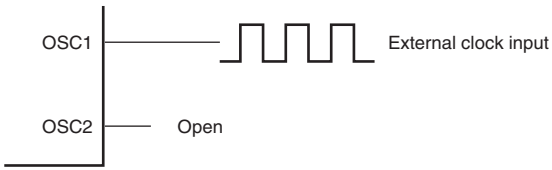


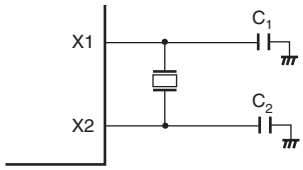
Figure 5.13 Example of External Clock Input

Note: Resistance is a reference value.

Figure 5.14 Block Diagram of Subclock Generator

5.6.1 Connecting 32.768-kHz Crystal Resonator

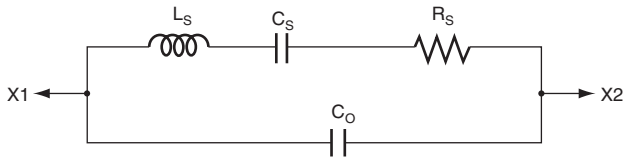
Clock pulses can be supplied to the subclock divider by connecting a 32.768-kHz crystal resonator, as shown in figure 5.15. Figure 5.16 shows the equivalent circuit of the 32.768 crystal resonator.



$C_1 = C_2 = 15$ pF (typ.)

Capacitances are reference values.

Figure 5.15 Typical Connection to 32.768-kHz Crystal Resonator



$C_O = 1.5$ pF (typ.)
$R_S = 14$ kΩ (typ.)
fW = 32.768 kHz
Note: Parameters are reference values.

Figure 5.16 Equivalent Circuit of 32.768-kHz Crystal Resonator

Figure 5.17 Pin Connection when not Using Subclock

5.7 Prescaler

5.7.1 Prescaler S

Prescaler S is a 13-bit counter using the system clock (ϕ) as its input clock. The outputs, divided clocks, are used as internal clocks by the on-chip peripheral modules. Prescaler initialized to H'0000 by a reset, and starts counting on exit from the reset state. In standb and subsleep mode, the system clock pulse generator stops. Prescaler S also stops and is to H'0000. It cannot be read from or written to by the CPU.

The outputs from prescaler S is shared by the on-chip peripheral modules. The division be set separately for each on-chip peripheral module. In active mode and sleep mode, th input to prescaler S is a system clock with the division ratio specified by bits MA2 to M SYSCR2.

5.7.2 Prescaler W

Prescaler W is a 5-bit counter using a 32.768 kHz signal divided by 4 (ϕ_w/4) as its input divided output is used for clock time base operation of timer A. Prescaler W is initialize by a reset, and starts counting on exit from the reset state. Even in standby mode, subact or subsleep mode, prescaler W continues functioning so long as clock signals are suppli X_1 and X_2.

5.8.2 Notes on Board Design

When using a crystal resonator (ceramic resonator), place the resonator and its load capac
close as possible to pins OSC1 and OSC2. Other signal lines should be routed away from
oscillator circuit to prevent induction from interfering with correct oscillation (see figure

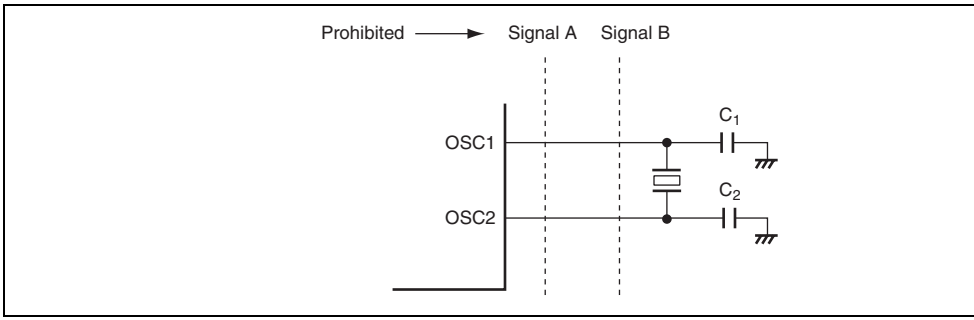


Figure 5.18 Example of Incorrect Board Design

frequency can be selected from among ϕ, ϕ/8, ϕ/16, ϕ/32, and ϕ/64.

- Subactive mode

  The CPU and all on-chip peripheral modules operate on the subclock. The subclock can be selected from ϕw/2, ϕw/4, or ϕw/8.

- Sleep mode

  The CPU halts. On-chip peripheral modules operate on the system clock.

- Subsleep mode

  The CPU halts. On-chip peripheral modules operate on the subclock.

- Standby mode

  The CPU and all on-chip peripheral modules halt. When the clock time-base functio selected, the RTC operates.

- Module standby function

  Independent of the above modes, power consumption can be reduced by halting indi chip peripheral modules that are not in use.

- Module standby control register 4 (MSTCR4)
- Serial Mode Control Register (SMCR)

6.1.1 System Control Register 1 (SYSCR1)

SYSCR1, SYSCR2, and SYSCR3 control the power-down modes.

Bit	Bit Name	Initial Value	R/W	Description
7	SSBY	0	R/W	Software Standby This bit selects the mode to transit after the ex of the SLEEP instruction. 0: Enters sleep mode or subsleep mode. 1: Enters standby mode. For details, see table 6.2.

on-chip oscillator is used as the system clock
after the transition. The relationship between
setting and the number of cycles is shown in t
A clock used for counting the number of cycle
divided regardless of the setting in bits MA2 t
SYSCR2. When the system clock source afte
transition is the external oscillator or on-chip o
the ϕ_{OSC} or ϕRC clock is used for counting, res

These bits also specify the waiting time until t
external oscillator settles when system clock s
are switched from the on-chip oscillator to the
clock by user software. The relationship of wa
times between the above transition and clock
is shown below. The number of cycles for ext
oscillator settling should be specified so that t
value multiplied by the external oscillator freq
6.5 ms or more. In this case, a clock used for
the number of cycles is the ϕ_{RC} clock divided b
setting in bits MA2 to MA0 in SYSCR2.

Nstby $\leq$ Nwait $\leq 2 \times$ Nstby

Nwait: The number of waiting cycles for exter
oscillator settling

Nstby: The number of waiting cycles when re
from a standby mode

				1: Sampling rate is $\phi_{OSC}/4$ or $\phi_{RC}/4$
2 to 0	—	All 0	—	Reserved These bits are always read as 0.

Table 6.1 Operating Frequency and Waiting Time

Bit Name				Cycle Count for Waiting Time	Operating Frequency						
STS3	STS2	STS1	STS0		20 MHz	16 MHz	10 MHz	8 MHz	4 MHz	2 MHz	1 MHz
x	0	0	0	8,192 cycles	0.4	0.5	0.8	1.0	2.0	4.1	8.1
x	0	0	1	16,384 cycles	0.8	1.0	1.6	2.0	4.1	8.2	16.4
x	0	1	0	32,768 cycles	1.6	2.0	3.3	4.1	8.2	16.4	32.8
x	0	1	1	65,536 cycles	3.3	4.1	6.6	8.2	16.4	32.8	65.5
x	1	0	0	131,072 cycles	6.6	8.2	13.1	16.4	32.8	65.5	131.1
1	1	0	1	1,024 cycles	0.05	0.06	0.10	0.13	0.26	0.51	1.02
1	1	1	0	128 cycles	0.00	0.00	0.01	0.02	0.03	0.06	0.13
1	1	1	1	16 cycles	0.00	0.00	0.00	0.00	0.00	0.00	0.02
0	1	0	1	4,096 cycles	0.20	0.25	0.40	0.51	1.02	2.05	4.01
0	1	1	0	2,048 cycles	0.10	0.13	0.20	0.26	0.51	1.02	2.05
0	1	1	1	512 cycles	0.02	0.03	0.05	0.06	0.13	0.26	0.51

[Legend]

x: Don't care

Note: Time unit is ms.

				of a SLEEP instruction, as well as bit SSBY o SYSCR1. For details, see table 6.2.
4	MA2	0	R/W	Active Mode Clock Select 2 to 0
3	MA1	0	R/W	These bits select the operating clock frequenc
2	MA0	0	R/W	active and sleep modes. The operating clock changes to the set frequency after the SLEEP instruction is executed. When the on-chip osc selected as the system clock source, the on-c oscillator output is further divided. 0xx: ϕ_{OSC} or ϕ_{RC} 100: $\phi_{OSC}/8$ or $\phi_{RC}/8$ 101: $\phi_{OSC}/16$ or $\phi_{RC}/16$ 110: $\phi_{OSC}/32$ or $\phi_{RC}/32$ 111: $\phi_{OSC}/64$ or $\phi_{RC}/64$
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	These bits select the operating clock frequenc subactive and subsleep modes. The operating frequency changes to the set frequency after SLEEP instruction is executed. 00: $\phi_W/8$ 01: $\phi_W/4$ 1x: $\phi_W/2$

[Legend]

x: Don't care.

6 to 0	—	All 1	—	Reserved These bits are always read as 0.

6.1.4 Module Standby Control Register 1 (MSTCR1)

MSTCR1 allows the on-chip peripheral modules to enter a standby state in module units.

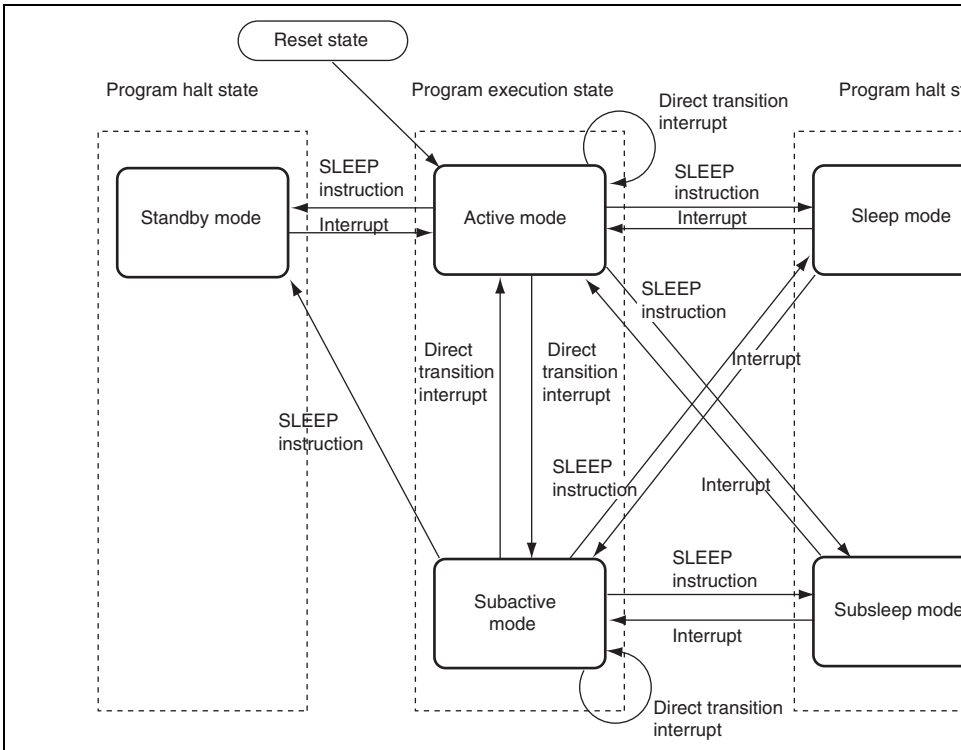
Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	MSTIIC	0	R/W	IIC2 Module Standby IIC2 enters the standby mode when this bit is
5	MSTS3	0	R/W	SCI3 Module Standby SCI3 enters the standby mode when this bit is
4	—	0	—	Reserved This bit is always read as 0.
3	MSTWD	0	R/W	Watchdog Timer Module Standby Watchdog timer enters the standby mode whe is set to 1. When the on-chip oscillator is selec the watchdog timer clock, the watchdog timer regardless of the setting of this bit
2	—	0	—	Reserved This bit is always read as 0.

MSTCR2 allows the on-chip peripheral modules to enter a standby state in module units

Bit	Bit Name	Initial Value	R/W	Description
7	MSTS3_2	0	R/W	SCI3_2 Module Standby SCI3_2 enters the standby mode when this b 1
6	—	0	—	Reserved
5	—	0	—	These bits are always read as 0.
4	MSTTB1	0	R/W	Timer B1 Module Standby Timer B1 enters the standby mode when this to 1
3 to 1	—	All 0	—	Reserved These bits are always read as 0.
0	MSTPWM	0	R/W	PWM Module Standby PWM enters the standby mode when this bit

				A/D converter enters the standby mode when set to 1
5	MSTTRD0	0	R/W	Timer RD_0 Module Standby Timer RD_0 enters the standby mode when th set to 1
4	MSTTRD1	0	R/W	Timer RD_1 Module Standby Timer RD_1 enters the standby mode when th set to 1
3 to 0	—	All 0	—	Reserved These bits are always read as 0.

by an interrupt. Table 6.3 shows the internal states of the LSI in each mode.



Notes: 1. To make a transition to another mode by an interrupt, make sure interrupt handling is after the in is accepted.
2. Details on the mode transition conditions are given in table 6.2.

Figure 6.1 Mode Transition Diagram

1	X	0*	0	Active mode (direct transition)	—
	X	X	1	Subactive mode (direct transition)	—

[Legend]

X: Don't care.

Note: * When a state transition is performed while SMSEL is 1, timer V, SCI3, SCI3_2 and the A/D converter are reset, and all registers are set to their initial values. these functions after entering active mode, reset the registers.

External interrupts	IRQ3 to IRQ0	Functioning	Functioning	Functioning	Functioning	Fun
	WKP5 to WKP0	Functioning	Functioning	Functioning	Functioning	Fun
Peripheral functions	RTC	Functioning	Functioning	Functioning if the timekeeping time-b function is selected, and retained if n		
	Timer V	Functioning	Functioning	Reset	Reset	Res
	Watchdog timer	Functioning	Functioning	Retained (functioning if the internal c selected as a count clock*)		
	SCI3, SCI3_2, SCI3_3	Functioning	Functioning	Reset	Reset	Res
	IIC2	Functioning	Functioning	Retained*	Retained	Ret
	Timer B1	Functioning	Functioning	Retained*	Retained	Ret
	Timer RD	Functioning	Functioning	Retained (the counter is incremented by a subclock if the internal clock ϕ is selected as a count clock*)		Ret
	Timer RC	Functioning	Functioning			Ret
	14-bit PWM	Functioning	Functioning	Retained*	Retained	Ret
	A/D converter	Functioning	Functioning	Reset	Reset	Res

Note: * Registers can be read or written in subactive mode.

6.2.2 Standby Mode

In standby mode, the system clock oscillator stops, so the CPU and on-chip peripheral mo stop functioning. However, as long as the rated voltage is supplied, the contents of CPU r on-chip RAM, and some on-chip peripheral module registers are retained. On-chip RAM will be retained as long as the voltage set by the RAM data retention voltage is provided. ports go to the high-impedance state.

The standby mode is cleared by an interrupt. When an interrupt is requested, the system c oscillator starts. After the time set in bits STS2 to STS0 in SYSCR1 and bit STS3 in SYS elapsed, the standby mode is lifted and the interrupt exception handling starts. The standb is not lifted if the I bit in CCR is set to 1 or the requested interrupt is disabled in the interr enable register.

When the $\overline{\text{RES}}$ signal goes low, the on-chip oscillator starts oscillation. Since clock signa supplied to the entire chip as soon as the on-chip oscillator starts oscillation, the $\overline{\text{RES}}$ sign be kept low over a given time. After the given time, the CPU starts the reset exception ha when the $\overline{\text{RES}}$ signal is driven high.

according to the LSON bit in SYSCR2 is 0. After the time set in bits STS2 to STS0 in S and bit STS3 in SYSCR has elapsed, a transition is made to active mode.

When the $\overline{\text{RES}}$ signal goes low, the on-chip oscillator starts oscillation. Since clock sign supplied to the entire chip as soon as the on-chip oscillator starts oscillation, the $\overline{\text{RES}}$ sig be kept low over a given time. After the given time, the CPU starts the reset exception h when the $\overline{\text{RES}}$ signal is driven high.

6.2.4 Subactive Mode

The operating frequency in subactive mode is selected from $\phi_w/2$, $\phi_w/4$, and $\phi_w/8$ by the SA0 bits in SYSCR2. After the SLEEP instruction is executed, the operating frequency the frequency which is set before the execution.

When the SLEEP instruction is executed in subactive mode, a transition to sleep mode, mode, standby mode, active mode, or subactive mode is made, depending on the combi SYSCR1 and SYSCR2.

When the $\overline{\text{RES}}$ signal goes low, the on-chip oscillator starts oscillation. Since clock sign supplied to the entire chip as soon as the on-chip oscillator starts oscillation, the $\overline{\text{RES}}$ sig be kept low over a given time. After the given time, the CPU starts the reset exception h when the $\overline{\text{RES}}$ signal is driven high.

6.3 Operating Frequency in Active Mode

This LSI operates in active mode at the frequency specified by bits MA2, MA1, and MA SYSCR2. The operating frequency changes to the set frequency after the SLEEP instruc execution.

by means of an interrupt.

6.4.1 Direct Transition from Active Mode to Subactive Mode

The time from the start of the SLEEP instruction execution to the end of the interrupt exc
handling (the direct transition time) is calculated by equation (1).

Direct transition time = {(number of SLEEP instruction execution cycles) + (number of i
clock cycles)}× (tcyc before transition) + (number of interrupt exception handling cycles)
(tsubcyc after transition) …. (1)

Example 1: Case when the CPU operating clock changes from ϕ_{osc} to $\phi_w/8$

$$\text{Direct transition time} = (2 + 1) \times t_{OSC} + 16 \times 8\ t_W = 3\ t_{OSC} + 128\ t_W$$

Example 2: Case when the system clock source is Rosc/4 and the division ratio is 16; the
operating clock changes from $\phi/16$ to $\phi_w/2$

$$\text{Direct transition time} = (2 + 1) \times 4\ t_{ROSC} \times 16 + 16 \times 2\ t_w = 192\ t_{ROSC} + 32\ t_w$$

[Legend]

t_{OSC}: OSC clock cycle time
t_{ROSC}: Period of oscillation of the on-chip oscillator
t_W: Watch clock cycle time
t_{cyc}: System clock (ϕ) cycle time
t_{subcyc}: Subclock (ϕ_{SUB}) cycle time

$$\text{Direct transition time} = (2 + 1) \times 8\ t_w + (32768 + 16) \times t_{OSC} = 24\ t_w + 32784\ t_{OSC}$$

Example 2: Case when the CPU operating clock changes from $\phi_w/4$ to Rosc/2, and a wai
of 4096 cycles is set

$$\text{Direct transition time} = (2 + 1) \times 4\ t_w + (4096 + 16) \times t_{ROSC} = 12\ t_w + 8224\ t_{OSC}$$

[Legend]

t_{OSC}:	OSC clock cycle time
t_{ROSC}:	Period of oscillation of the on-chip oscillator
t_W:	Watch clock cycle time
tcyc:	System clock (ϕ) cycle time
tsubcyc:	Subclock (ϕ_{SUB}) cycle time

6.5 Module Standby Function

The module-standby function can be set to any peripheral module. In the module standb
clock supply to modules stops to enter the power-down mode. Setting a bit in MSTCR1,
MSTCR2, MSTCR4, or SMCR that corresponds to each module to 1 enables each on-ch
peripheral module to enter the module standby state and the module standby state is can
clearing the bit to 0.

— The flash memory can be reprogrammed up to 1,000 times.

- On-board programming
  — On-board programming/erasing can be done in boot mode, in which the boot pro into the chip is started to erase or program of the entire flash memory. In normal programming mode, individual blocks can be erased or programmed.
- Programmer mode
  — Flash memory can be programmed/erased in programmer mode using a PROM programmer, as well as in on-board programming mode.
- Automatic bit rate adjustment
  — For data transfer in boot mode, this LSI's bit rate can be automatically adjusted to the transfer bit rate of the host.
- Programming/erasing protection
  — Sets software protection against flash memory programming/erasing.
- Power-down mode
  — Operation of the power supply circuit can be partly halted in subactive mode. As flash memory can be read with low power consumption.

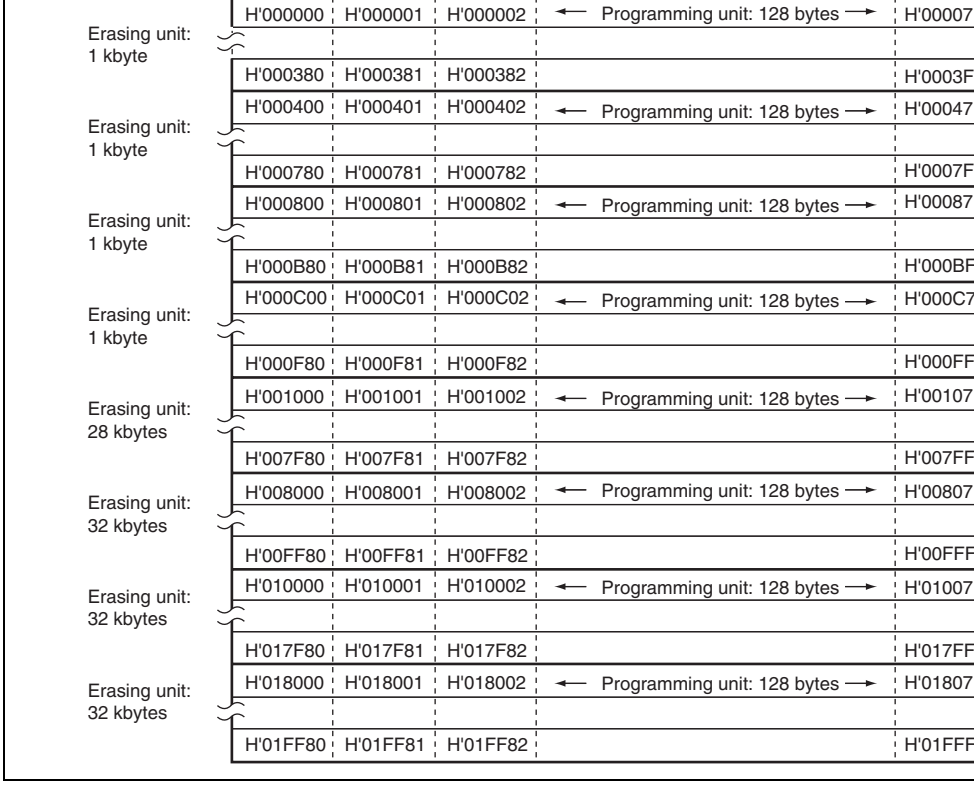


Figure 7.1 Block Configuration of Flash Memory

7.2.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is a register that makes the flash memory change to programming mode, prog
mode, erasing mode, or erase-verify mode. For details on register setting, refer to sectio
Flash Memory Programming/Erasing.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	SWE	0	R/W	Software Write Enable When this bit is set to 1, flash memory programming/erasing is enabled. When this b cleared to 0, other FLMCR1 register bits and bits cannot be set.
5	ESU	0	R/W	Erasure Setup When this bit is set to 1, the flash memory cha the erasure setup state. When it is cleared to erasure setup state is cancelled. Set this bit t setting the E bit to 1 in FLMCR1.
4	PSU	0	R/W	Program Setup When this bit is set to 1, the flash memory cha the program setup state. When it is cleared to program setup state is cancelled. Set this bit before setting the P bit in FLMCR1.
3	EV	0	R/W	Erase-Verify When this bit is set to 1, the flash memory cha erase-verify mode. When it is cleared to 0, era mode is cancelled.

				When this bit is set to 1 while SWE=1 and PSU flash memory changes to programming mode. is cleared to 0, programming mode is cancelle

7.2.2 Flash Memory Control Register 2 (FLMCR2)

FLMCR2 is a register that displays the state of flash memory programming/erasing. FLM read-only register, and should not be written to.

Bit	Bit Name	Initial Value	R/W	Description
7	FLER	0	R	Flash Memory Error Indicates that an error has occurred during an operation on flash memory (programming or er When FLER is set to 1, flash memory goes to t protection state. See section 7.5.3, Error Protection, for details.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

				H'017FFF will be erased.
5	EB5	0	R/W	When this bit is set to 1, 32 kbytes of H'00800 H'00FFFF will be erased.
4	EB4	0	R/W	When this bit is set to 1, 28 kbytes of H'00100 H'007FFF will be erased.
3	EB3	0	R/W	When this bit is set to 1, 1 kbyte of H'000C00 H'000FFF will be erased.
2	EB2	0	R/W	When this bit is set to 1, 1 kbyte of H'000800 H'000BFF will be erased.
1	EB1	0	R/W	When this bit is set to 1, 1 kbyte of H'000400 H'0007FF will be erased.
0	EB0	0	R/W	When this bit is set to 1, 1 kbyte of H'000000 H'0003FF will be erased.

				When this bit is 0 and a transition is made to su mode, the flash memory enters the power-dow When this bit is 1, the flash memory remains in normal mode even after a transition is made to subactive mode.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

7.2.5 Flash Memory Enable Register (FENR)

Bit 7 (FLSHE) in FENR enables or disables the CPU access to the flash memory control FLMCR1, FLMCR2, EBR1, and FLPWCR.

Bit	Bit Name	Initial Value	R/W	Description
7	FLSHE	0	R/W	Flash Memory Control Register Enable Flash memory control registers can be accesse this bit is set to 1. Flash memory control registe cannot be accessed when this bit is set to 0.
6	—	0	R/W	Reserved This bit can be read from or written to, but shou set to 1.
5 to 0	—	All 0	—	Reserved These bits are always read as 0.

via SCI3. After erasing the entire flash memory, the programming control program is ex
This can be used for programming initial values in the on-board state or for a forcible re
programming/erasing can no longer be done in user programming mode. In user progra
mode, individual blocks can be erased and programmed by branching to the user
programming/erasure control program prepared by the user.

Table 7.1 Setting Programming Modes

TEST	$\overline{\text{NMI}}$	P85	PC0	PC1	PC2	LSI State after Reset End
0	1	X	X	X	X	User Mode
0	0	1	X	X	X	Boot Mode
1	X	X	0	0	0	Programmer Mode

[Legend]
X : Don't care.

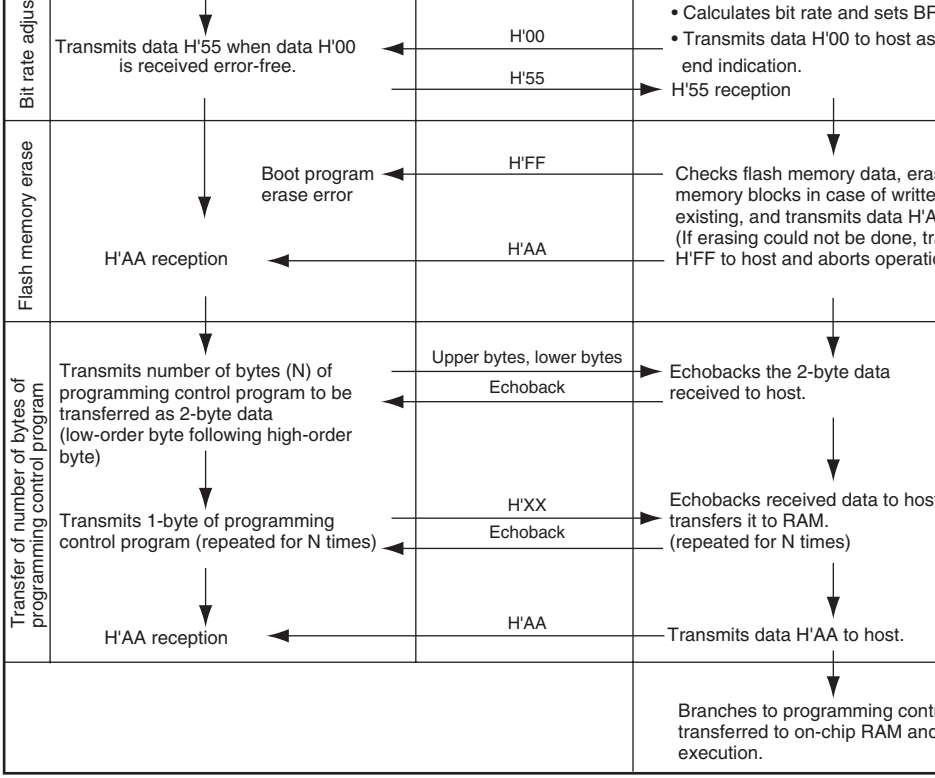
7.3.1 Boot Mode

Table 7.2 shows the boot mode operations between reset end and branching to the progr
control program.

1. When boot mode is used, the flash memory programming control program must be p
   the host beforehand. Prepare a programming control program in accordance with the
   description in section 7.4, Flash Memory Programming/Erasing.
2. SCI3 should be set to asynchronous mode, and the transfer format as follows: 8-bit d
   bit, and no parity.

the bit rates of the host and the chip. To operate the SCI properly, set the host's transfe
and system clock frequency of this LSI within the ranges listed in table 7.3.

5. In boot mode, a part of the on-chip RAM area is used by the boot program. The area I
to H'FFFEEF is the area to which the programming control program is transferred fro
host. The boot program area cannot be used until the execution state in boot mode swi
the programming control program.
6. Before branching to the programming control program, the chip terminates transfer op
by SCI3 (by clearing the RE and TE bits in SCR to 0), however the adjusted bit rate v
remains set in BRR. Therefore, the programming control program can still use it for tr
program data or verify data with the host. The TxD pin is high (PCR22 = 1, P22 = 1).
contents of the CPU general registers are undefined immediately after branching to th
programming control program. These registers must be initialized at the beginning of
programming control program, as the stack pointer (SP), in particular, is used implicit
subroutine calls, etc.
7. Boot mode can be cleared by a reset. End the reset after driving the reset pin low, wai
least 20 states, and then setting the TEST pin and $\overline{\text{NMI}}$ pin. Boot mode is also cleared
WDT overflow occurs.
8. Do not change the TEST pin and $\overline{\text{NMI}}$ pin input levels in boot mode.


Bit rate adjus
Transmits data H'55 when data H'00 is received error-free.
H'00
H'55
• Calculates bit rate and sets BF
• Transmits data H'00 to host as end indication.
H'55 reception
Flash memory erase
Boot program erase error
H'FF
Checks flash memory data, era memory blocks in case of writte existing, and transmits data H'A (If erasing could not be done, tr H'FF to host and aborts operati
H'AA reception
H'AA
Transfer of number of bytes of programming control program
Transmits number of bytes (N) of programming control program to be transferred as 2-byte data (low-order byte following high-order byte)
Upper bytes, lower bytes
Echoback
Echobacks the 2-byte data received to host.
Transmits 1-byte of programming control program (repeated for N times)
H'XX
Echoback
Echobacks received data to host transfers it to RAM. (repeated for N times)
H'AA reception
H'AA
Transmits data H'AA to host.
Branches to programming cont transferred to on-chip RAM and execution.

On-board programming/erasing of an individual flash memory block can also be perform
programming mode by branching to a user programming/erasure control program. The us
set branching conditions and provide on-board means of supplying programming data. Th
memory must contain the user programming/erasure control program or a program that pr
the user programming/erasure control program from external memory. As the flash memo
cannot be read during programming/erasing, transfer the user programming/erasure contr
program to on-chip RAM, as in boot mode. Figure 7.2 shows a sample procedure for
programming/erasing in user programming mode. Prepare a user programming/erasure co
program in accordance with the description in section 7.4, Flash Memory Programming/E

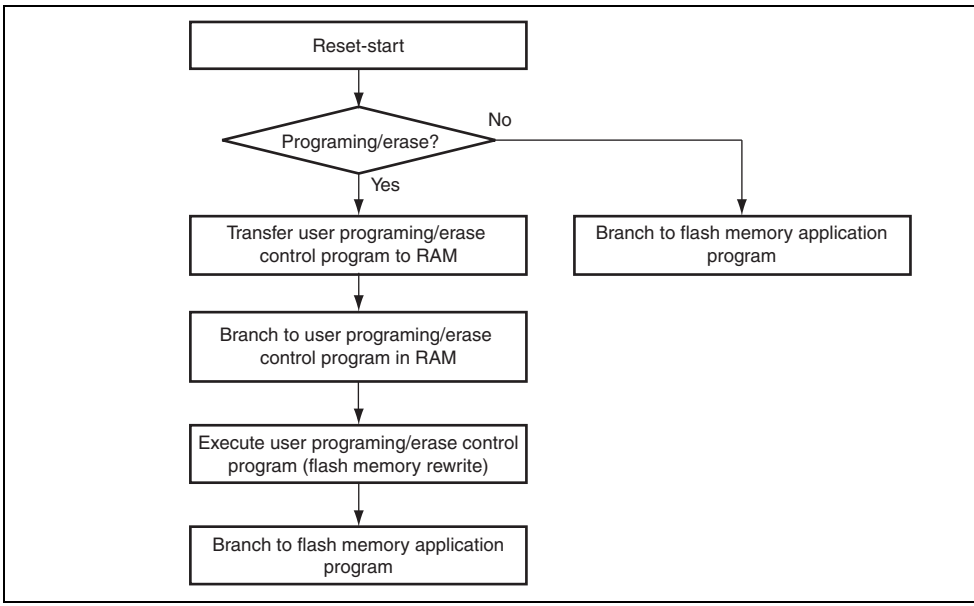
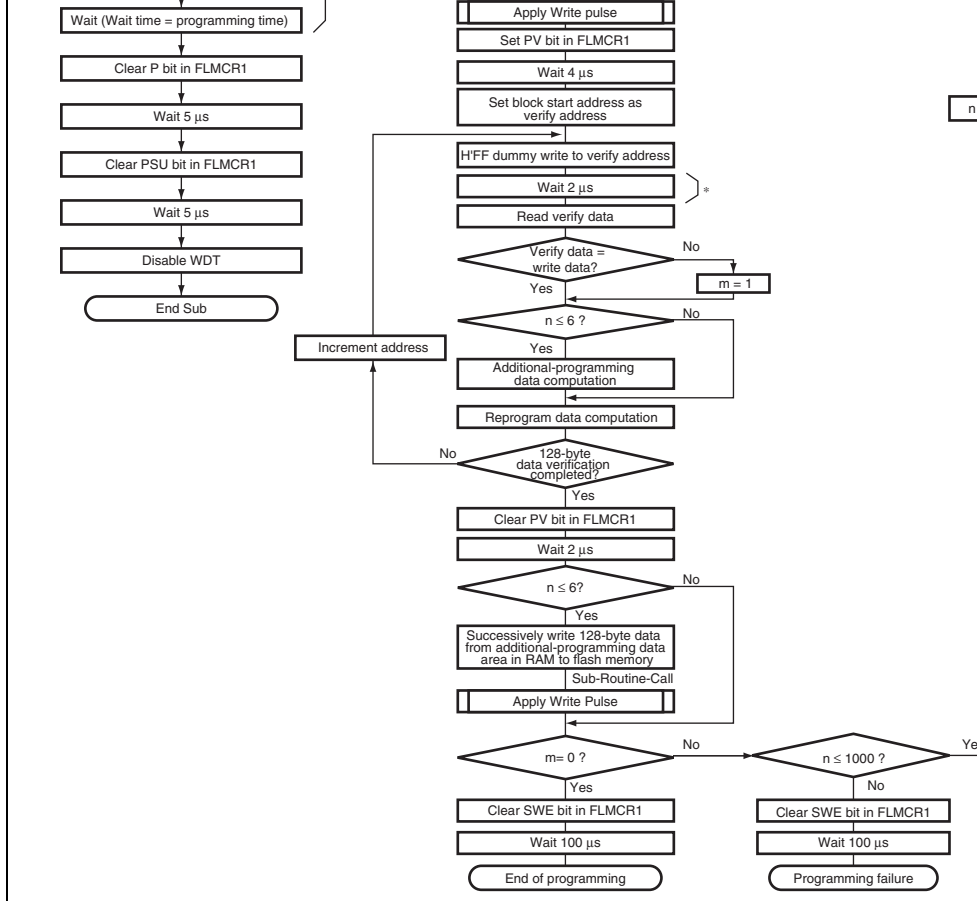


Figure 7.2 Programming/Erasing Flowchart Example in User Programming M

7.4.1 Programming/Program-Verify

When writing data or programs to the flash memory, the programming/program-verify f
shown in figure 7.3 should be followed. Performing programming operations according
flowchart will enable data or programs to be written to the flash memory without subjec
chip to voltage stress or sacrificing program data reliability.

1. Programming must be done to an empty address. Do not reprogram an address to wh
programming has already been performed.
2. Programming should be carried out 128 bytes at a time. A 128-byte data transfer mu
performed even if writing fewer than 128 bytes. In this case, H'FF data must be writt
extra addresses.
3. Prepare the following data storage areas in RAM: A 128-byte programming data are
byte reprogramming data area, and a 128-byte additional-programming data area. Pe
reprogramming data computation according to table 7.4, and additional programmin
computation according to table 7.5.
4. Consecutively transfer 128 bytes of data in byte units from the reprogramming data a
additional-programming data area to the flash memory. The program address and 12
data are latched in the flash memory. The lower 8 bits of the start address in the flash
destination area must be H'00 or H'80.
5. The time during which the P bit is set to 1 is the programming time. Table 7.6 shows
allowable programming times.
6. The watchdog timer (WDT) is set to prevent overprogramming due to program runa
An overflow cycle of approximately 6.6 ms is allowed.
7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose
bits are B'00. Verify data can be read in words or in longwords from the address to
dummy write was performed.



Note: * The RTS instruction must not be used during the following 1. and 2. periods.
1. A period between 128-byte data programming to flash memory and the P bit clearing
2. A period between dummy writing of H'FF to a verify address and verify data reading

Figure 7.3 Programming/Program-Verify Flowchart

Reprogramming Data	Verify Data	Additional-Program Data	Comments
0	0	0	Additional-program
0	1	1	No additional progra
1	0	1	No additional progra
1	1	1	No additional progra

Table 7.6 Programming Time

n (Number of Writes)	Programming Time	In Additional Programming	Comments
1 to 6	30	10	
7 to 1,000	200	—	

Note: Time shown in μs.

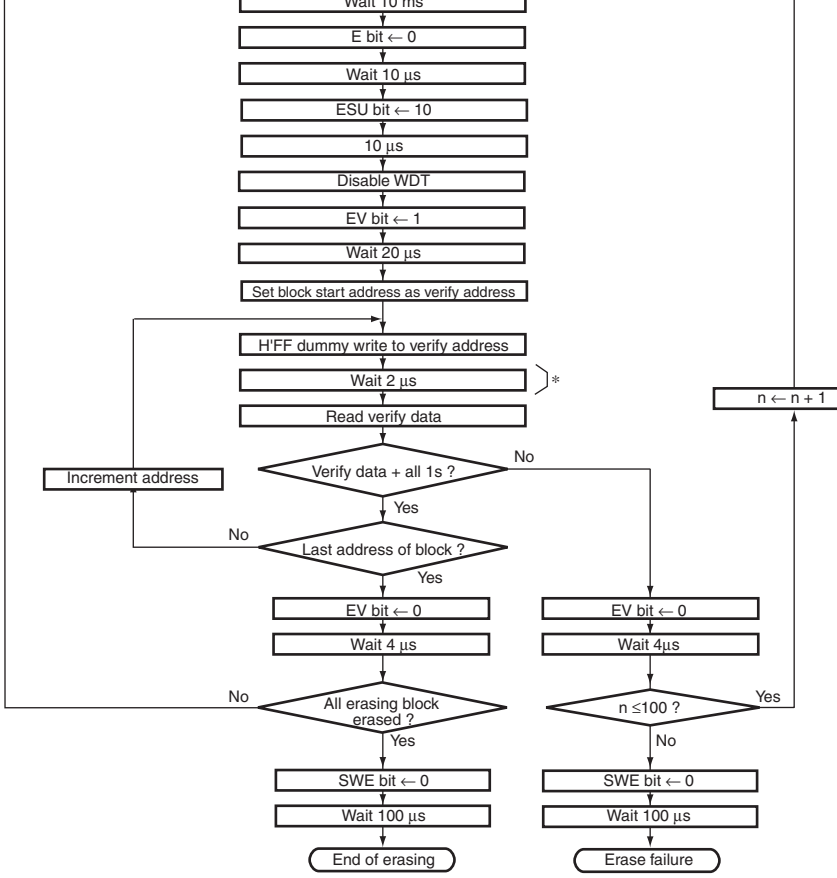
overflow cycle of approximately 19.8 ms is allowed.

5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lo bits are B'00. Verify data can be read in longwords from the address to which a dumm was performed.
6. If the read data is not erased successfully, set erasing mode again, and repeat the erase verify sequence as before. The maximum number of repetitions of the erase/erase-ver sequence is 100.

7.4.3 Interrupt Handling when Programming/Erasing Flash Memory

All interrupts, including the NMI interrupt, are disabled while flash memory is being prog or erased, or while the boot program is executing, for the following three reasons:

1. Interrupt during programming/erasing may cause a violation of the programming or e algorithm, with the result that normal operation cannot be assured.
2. If interrupt exception handling starts before the vector address is written or during programming/erasing, a correct vector cannot be fetched and the CPU malfunctions.
3. If an interrupt occurs during boot program execution, normal boot mode sequence can carried out.



Note: * The RTS instruction must not be used during a period between dummy writing of H'FF to a verify address and verify da

Figure 7.4 Erasure/Erase-Verify Flowchart

and erase block register 1 (EBR1) are initialized. In a reset via the RES pin, the reset state
entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the
a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC
Characteristics section.

7.5.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memor
by clearing the SWE bit in FLMCR1. When software protection is in effect, setting the P
in FLMCR1 does not cause a transition to programming mode or erasing mode. By settin
erase block register 1 (EBR1), erase protection can be set for individual blocks. When EB
to H'00, erase protection is set for all blocks.

7.5.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory
programming/erasing, or operation is not performed in accordance with the programming
algorithm, and the programming/erasing operation is forcibly aborted. Aborting the
programming/erasing operation prevents damage to the flash memory due to overprogram
overerasing.

When the following errors are detected during programming/erasing of flash memory, the
bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/eras
  (including vector read and instruction fetch)
- Immediately after exception handling excluding a reset during programming/erasing
- When a SLEEP instruction is executed during programming/erasing

7.7 Power-Down States for Flash Memory

In user mode, the flash memory will operate in either of the following states:

- Normal operating mode
  The flash memory can be read and written to at high speed.
- Power-down operating mode
  The power supply circuit of flash memory can be partly halted. As a result, flash me
  be read with low power consumption.
- Standby mode
  All flash memory circuits are halted.

Table 7.7 shows the correspondence between the operating modes of this LSI and the fla
memory. In subactive mode, the flash memory can be set to operate in power-down mod
PDWND bit in FLPWCR. When the flash memory returns to its normal operating state f
power-down mode or standby mode, a period to stabilize operation of the power supply
that were stopped is needed. When the flash memory returns to its normal operating stat
STS2 to STS0 in SYSCR1 and bit STS3 in SYSCR3 must be set so that the waiting time
or more, even when the external clock is being used.

For functions in each port, see appendix B.1, I/O Port Block Diagrams. For the executio
manipulation instructions to the port control register and port data register, see section 2
Manipulation Instruction.

9.1 Port 1

Port 1 is a general I/O port also functioning as IRQ interrupt input pins, an RTC output p
bit PWM output pin, a timer B1 input pin, and a timer V input pin. Figure 9.1 shows its
configuration.

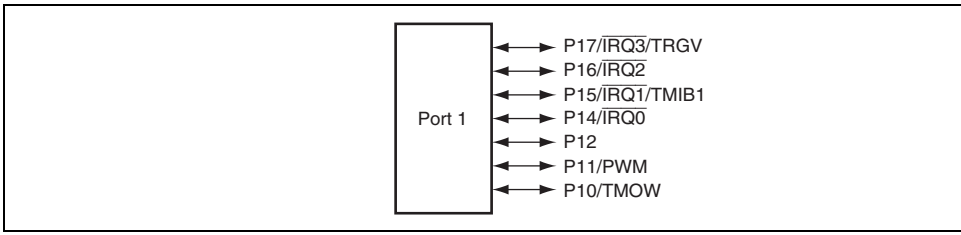


Figure 9.1 Port 1 Pin Configuration

Port 1 has the following registers.

- Port mode register 1 (PMR1)
- Port control register 1 (PCR1)
- Port data register 1 (PDR1)
- Port pull-up control register 1 (PUCR1)

				0: General I/O port 1: $\overline{\text{IRQ2}}$ input pin
5	IRQ1	0	R/W	Selects the function of pin P15/$\overline{\text{IRQ1}}$/TMIB1. 0: General I/O port 1: $\overline{\text{IRQ1}}$/TMIB1 input pin
4	IRQ0	0	R/W	Selects the function of pin P14/$\overline{\text{IRQ0}}$. 0: General I/O port 1: $\overline{\text{IRQ0}}$ input pin
3	TXD2	0	R/W	Selects the function of pin P72/TXD_2. 0: General I/O port 1: TXD_2 output pin
2	PWM	0	R/W	Selects the function of pin P11/PWM. 0: General I/O port 1: PWM output pin
1	TXD	0	R/W	Selects the function of pin P22/TXD. 0: General I/O port 1: TXD output pin
0	TMOW	0	R/W	Selects the function of pin P10/TMOW. 0: General I/O port 1: TMOW output pin

3	—	—	—
2	PCR12	0	W
1	PCR11	0	W
0	PCR10	0	W

9.1.3 Port Data Register 1 (PDR1)

PDR1 is a general I/O port data register of port 1.

Bit	Bit Name	Initial Value	R/W	Description
7	P17	0	R/W	PDR1 stores output data for port 1 pins.
6	P16	0	R/W	If PDR1 is read while PCR1 bits are set to 1, t
5	P15	0	R/W	stored in PDR1 are read. If PDR1 is read whil
4	P14	0	R/W	bits are cleared to 0, the pin states are read r of the value stored in PDR1.
3	—	1	—	Bit 3 is a reserved bit. This bit is always read
2	P12	0	R/W	
1	P11	0	R/W	
0	P10	0	R/W	

3	—	1	—
2	PUCR12	0	R/W
1	PUCR11	0	R/W
0	PUCR10	0	R/W

9.1.5 Pin Functions

The correspondence between the register specification and the port functions is shown be

- P17/$\overline{\text{IRQ3}}$/TRGV pin

Register	PMR1	PCR1	
Bit Name	**IRQ3**	**PCR17**	**Pin Function**
Setting value	0	0	P17 input pin
		1	P17 output pin
	1	X	$\overline{\text{IRQ3}}$ input/TRGV input pin

[Legend] X: Don't care.

Register	PMR1	PCR1	
Bit Name	**IRQ1**	**PCR15**	**Pin Function**
Setting value	0	0	P15 input pin
		1	P15 output pin
	1	X	$\overline{\text{IRQ1}}$ input/TMIB1 input pin

[Legend] X: Don't care.

- P14/$\overline{\text{IRQ0}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ0**	**PCR14**	**Pin Function**
Setting value	0	0	P14 input pin
		1	P14 output pin
	1	X	$\overline{\text{IRQ0}}$ input pin

[Legend] X: Don't care.

- P12 pin

Register	PCR1	
Bit Name	**PCR12**	**Pin Function**
Setting value	0	P12 input pin
	1	P12 output pin

Register	PMR1	PCR1	
Bit Name	**TMOW**	**PCR10**	**Pin Function**
Setting value	0	0	P10 input pin
		1	P10 output pin
	1	X	TMOW output pin

[Legend] X: Don't care.

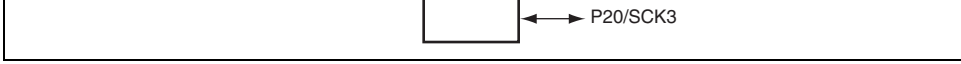


Figure 9.2 Port 2 Pin Configuration

Port 2 has the following registers.

- Port control register 2 (PCR2)
- Port data register 2 (PDR2)
- Port mode register 3 (PMR3)

9.2.1 Port Control Register 2 (PCR2)

PCR2 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 2

Bit	Bit Name	Initial Value	R/W	Description
7	PCR27	0	W	When each of the port 2 pins P24 to P20 func
6	PCR26	0	W	general I/O port, setting a PCR2 bit to 1 make
5	PCR25	0	W	corresponding pin an output port, while clearin
4	PCR24	0	W	to 0 makes the pin an input port.
3	PCR23	0	W	
2	PCR22	0	W	
1	PCR21	0	W	
0	PCR20	0	W	

3	P23	0	R/W	
2	P22	0	R/W	
1	P21	0	R/W	
0	P20	0	R/W	

9.2.3 Port Mode Register 3 (PMR3)

PMR3 selects the CMOS output or NMOS open-drain output for port 2.

Bit	Bit Name	Initial Value	R/W	Description
7	POF27	0	R/W	When the bit is set to 1, the corresponding pin
6	POF26	0	R/W	by PMOS and it functions as the NMOS open-
5	POF25	0	R/W	output. When cleared to 0, the pin functions as CMOS output.
4	POF24	0	R/W	
3	POF23	0	R/W	
2 to 0	—	All 1	—	Reserved These bits are always read as 1.

- P26 pin

Register	PCR2	
Bit Name	**PCR26**	**Pin Function**
Setting Value	0	P26 input pin
	1	P26 output pin

- P25 pin

Register	PCR2	
Bit Name	**PCR25**	**Pin Function**
Setting Value	0	P25 input pin
	1	P25 output pin

- P24 pin

Register	PCR2	
Bit Name	**PCR24**	**Pin Function**
Setting Value	0	P24 input pin
	1	P24 output pin

Bit Name	TXD	PCR22	Pin Function
Setting Value	0	0	P22 input pin
		1	P22 output pin
	1	X	TXD output pin

[Legend] X: Don't care.

- P21/RXD pin

Register	SCR3	PCR2	
Bit Name	RE	PCR21	Pin Function
Setting Value	0	0	P21 input pin
		1	P21 output pin
	1	X	RXD input pin

[Legend] X: Don't care.

- P20/SCK3 pin

Register	SCR3		SMR	PCR2	
Bit Name	CKE1	CKE0	COM	PCR20	Pin Function
Setting Value	0	0	0	0	P20 input pin
				1	P20 output pin
	0	0	1	X	SCK3 output pin
	0	1	X	X	SCK3 output pin
	1	X	X	X	SCK3 input pin

[Legend] X: Don't care.

Figure 9.3 Port 3 Pin Configuration

Port 3 has the following registers.

- Port control register 3 (PCR3)
- Port data register 3 (PDR3)

9.3.1 Port Control Register 3 (PCR3)

PCR3 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 3

Bit	Bit Name	Initial Value	R/W	Description
7	PCR37	0	W	Setting a PCR3 bit to 1 makes the correspond
6	PCR36	0	W	an output port, while clearing the bit to 0 mak
5	PCR35	0	W	an input port.
4	PCR34	0	W	
3	PCR33	0	W	
2	PCR32	0	W	
1	PCR31	0	W	
0	PCR30	0	W	

3	P33	0	R/W
2	P32	0	R/W
1	P31	0	R/W
0	P30	0	R/W

9.3.3 Pin Functions

The correspondence between the register specification and the port functions is shown be

- P37 pin

Register	PCR3	
Bit Name	**PCR37**	**Pin Function**
Setting Value	0	P37 input pin
	1	P37 output pin

- P36 pin

Register	PCR3	
Bit Name	**PCR36**	**Pin Function**
Setting Value	0	P36 input pin
	1	P36 output pin

Bit Name	PCR34	Pin Function
Setting Value	0	P34 input pin
	1	P34 output pin

- P33 pin

Register	PCR3	
Bit Name	PCR33	Pin Function
Setting Value	0	P33 input pin
	1	P33 output pin

- P32 pin

Register	PCR3	
Bit Name	PCR32	Pin Function
Setting Value	0	P32 input pin
	1	P32 output pin

- P31 pin

Register	PCR3	
Bit Name	PCR31	Pin Function
Setting Value	0	P31 input pin
	1	P31 output pin

input pin. Each pin of port 5 is shown in figure 9.4. The register setting of the I^2C bus inte
priority for functions of the pins P57/SCL and P56/SDA. Since the output buffer for pins
P57 has the NMOS push-pull structure, it differs from an output buffer with the CMOS st
in the high-level output characteristics (see section 23, Electrical Characteristics).

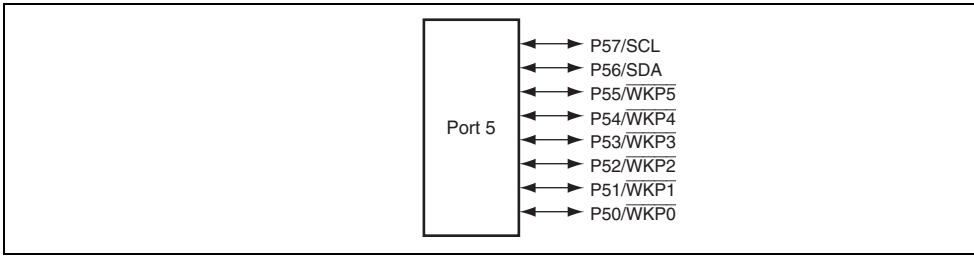


Figure 9.4 Port 5 Pin Configuration

Port 5 has the following registers.

- Port mode register 5 (PMR5)
- Port control register 5 (PCR5)
- Port data register 5 (PDR5)
- Port pull-up control register 5 (PUCR5)

				0: General I/O port 1: $\overline{\text{WKP5}}$ input pin
4	WKP4	0	R/W	Selects the function of pin P54/$\overline{\text{WKP4}}$. 0: General I/O port 1: $\overline{\text{WKP4}}$ input pin
3	WKP3	0	R/W	Selects the function of pin P53/$\overline{\text{WKP3}}$. 0: General I/O port 1: $\overline{\text{WKP3}}$ input pin
2	WKP2	0	R/W	Selects the function of pin P52/$\overline{\text{WKP2}}$. 0: General I/O port 1: $\overline{\text{WKP2}}$ input pin
1	WKP1	0	R/W	Selects the function of pin P51/$\overline{\text{WKP1}}$. 0: General I/O port 1: $\overline{\text{WKP1}}$ input pin
0	WKP0	0	R/W	Selects the function of pin P50/$\overline{\text{WKP0}}$. 0: General I/O port 1: $\overline{\text{WKP0}}$ input pin

3	PCR53	0	W
2	PCR52	0	W
1	PCR51	0	W
0	PCR50	0	W

9.4.3 Port Data Register 5 (PDR5)

PDR5 is a general I/O port data register of port 5.

Bit	Bit Name	Initial Value	R/W	Description
7	P57	0	R/W	PDR5 stores output data for port 5 pins.
6	P56	0	R/W	If PDR5 is read while PCR5 bits are set to 1, th
5	P55	0	R/W	stored in PDR5 are read. If PDR5 is read while
4	P54	0	R/W	bits are cleared to 0, the pin states are read re
3	P53	0	R/W	of the value stored in PDR5.
2	P52	0	R/W	
1	P51	0	R/W	
0	P50	0	R/W	

3	PUCR53	0	R/W	state when these bits are cleared to 0.
2	PUCR52	0	R/W	
1	PUCR51	0	R/W	
0	PUCR50	0	R/W	

9.4.5 Pin Functions

The correspondence between the register specification and the port functions is shown b

- P57/SCL pin

Register	ICCR1	PCR5	
Bit Name	**ICE**	**PCR57**	**Pin Function**
Setting Value	0	0	P57 input pin
		1	P57 output pin
	1	X	SCL I/O pin

[Legend] X: Don't care.

SCL performs the NMOS open-drain output, that enables a direct bus drive.

- P55/$\overline{\text{WKP5}}$ pin

Register	PMR5	PCR5	
Bit Name	**WKP5**	**PCR55**	**Pin Function**
Setting Value	0	0	P55 input pin
		1	P55 output pin
	1	X	$\overline{\text{WKP5}}$ input pin

[Legend] X: Don't care.

- P54/$\overline{\text{WKP4}}$ pin

Register	PMR5	PCR5	
Bit Name	**WKP4**	**PCR54**	**Pin Function**
Setting Value	0	0	P54 input pin
		1	P54 output pin
	1	X	$\overline{\text{WKP4}}$ input pin

[Legend] X: Don't care.

Register	PMR5	PCR5	
Bit Name	**WKP2**	**PCR52**	**Pin Function**
Setting Value	0	0	P52 input pin
		1	P52 output pin
	1	X	$\overline{\text{WKP2}}$ input pin

[Legend] X: Don't care.

- P51/$\overline{\text{WKP1}}$ pin

Register	PMR5	PCR5	
Bit Name	**WKP1**	**PCR51**	**Pin Function**
Setting Value	0	0	P51 input pin
		1	P51 output pin
	1	X	$\overline{\text{WKP1}}$ input pin

[Legend] X: Don't care.

- P50/$\overline{\text{WKP0}}$ pin

Register	PMR5	PCR5	
Bit Name	**WKP0**	**PCR50**	**Pin Function**
Setting Value	0	0	P50 input pin
		1	P50 output pin
	1	X	$\overline{\text{WKP0}}$ input pin

[Legend] X: Don't care.

Figure 9.5 Port 7 Pin Configuration

Port 7 has the following registers.

- Port control register 7 (PCR7)
- Port data register 7 (PDR7)

9.5.1 Port Control Register 7 (PCR7)

PCR7 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR77	0	W	When each of the port 7 pins P77 to P74 and P
6	PCR76	0	W	P70 functions as a general I/O port, setting a P
5	PCR75	0	W	to 1 makes the corresponding pin an output po
4	PCR74	0	W	clearing the bit to 0 makes the pin an input por
3	—	—	—	Bit 3 is a reserved bit.
2	PCR72	0	W	
1	PCR71	0	W	
0	PCR70	0	W	

3	—	1	—	Bit 3 is a reserved bit. This bit is always read
2	P72	0	R/W	
1	P71	0	R/W	
0	P70	0	R/W	

9.5.3 Pin Functions

The correspondence between the register specification and the port functions is shown b

- P77 pin

Register	PCR7	
Bit Name	**PCR77**	**Pin Function**
Setting Value	0	P77 input pin
	1	P77 output pin

- P76/TMOV pin

Register	TCSRV	PCR7	
Bit Name	**OS3 to OS0**	**PCR76**	**Pin Function**
Setting Value	0000	0	P76 input pin
		1	P76 output pin
	Other than above	X	TMOV output pin

[Legend] X: Don't care.

Bit Name	PCR74	Pin Function
Setting Value	0	P74 input/TMRIV input pin
	1	P74 output/TMRIV input pin

- P72/TXD_2 pin

Register	PMR1	PCR7	
Bit Name	**TXD2**	**PCR72**	**Pin Function**
Setting Value	0	0	P72 input pin
		1	P72 output pin
	1	X	TXD_2 output pin

[Legend] X: Don't care.

- P71/RXD_2 pin

Register	SCR3_2	PCR7	
Bit Name	**RE**	**PCR71**	**Pin Function**
Setting Value	0	0	P71 input pin
		1	P71 output pin
	1	X	RXD_2 input pin

[Legend] X: Don't care.

9.6 Port 8

Port 8 is a general I/O port. Each pin of port 8 is shown in figure 9.6.

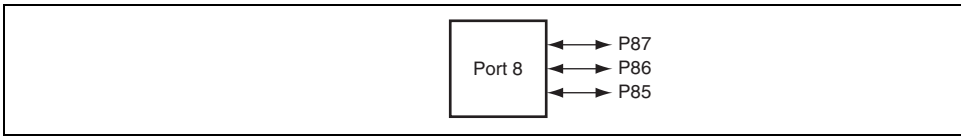


Figure 9.6 Port 8 Pin Configuration

Port 8 has the following registers.

- Port control register 8 (PCR8)
- Port data register 8 (PDR8)

9.6.1 Port Control Register 8 (PCR8)

PCR8 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 8

Bit	Bit Name	Initial Value	R/W	Description
7	PCR87	0	W	When each of the port 8 pins P87 to P80 func
6	PCR86	0	W	general I/O port, setting a PCR8 bit to 1 make
5	PCR85	0	W	corresponding pin an output port, while clearin to 0 makes the pin an input port.
4 to 0	—	—	—	Reserved

4 to 0	—	All 1	—	Reserved These bits are always read as 1.

9.6.3 Pin Functions

The correspondence between the register specification and the port functions is shown be

- P87 pin

Register	PCR8	
Bit Name	**PCR87**	**Pin Function**
Setting Value	0	P87 input pin
	1	P87 output pin

- P86 pin

Register	PCR8	
Bit Name	**PCR86**	**Pin Function**
Setting Value	0	P86 input pin
	1	P86 output pin

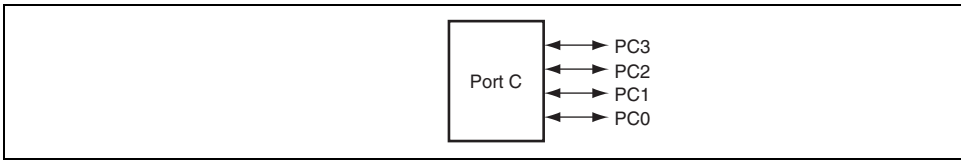


Figure 9.7 Port C Pin Configuration

Port C has the following registers.

- Port control register C (PCRC)
- Port data register C (PDRC)

9.7.1 Port Control Register C (PCRC)

PCRC selects inputs/outputs in bit units for pins to be used as general I/O ports of port C

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	—	—	Reserved
3	PCRC3	0	W	Setting a PCR9 bit to 1 makes the correspond
2	PCRC2	0	W	an output port, while clearing the bit to 0 mak
1	PCRC1	0	W	an input port.
0	PCRC0	0	W	

1	PC1	0	R/W	values stored in PDRC are read. If PDRC is re PCRC bits are cleared to 0, the pin states are r
0	PC0	0	R/W	regardless of the value stored in PDRC.

9.7.3 Pin Functions

The correspondence between the register specification and the port functions is shown be

- PC3 pin

Register	PCRC	
Bit Name	**PCRC3**	**Pin Function**
Setting Value	0	PC3 input pin
	1	PC3 output pin

- PC2 pin

Register	PCRC	
Bit Name	**PCRC2**	**Pin Function**
Setting Value	0	PC2 input pin
	1	PC2 output pin

Bit Name	PCRC0	Pin Function
Setting Value	0	PC0 input pin
	1	PC0 output pin

9.8 Port D

Port D is a general I/O port also functioning as timer RD_0 I/O pins. Each pin of port D
in figure 9.8. The setting for the timer RD_0 function has priority over those for other fu

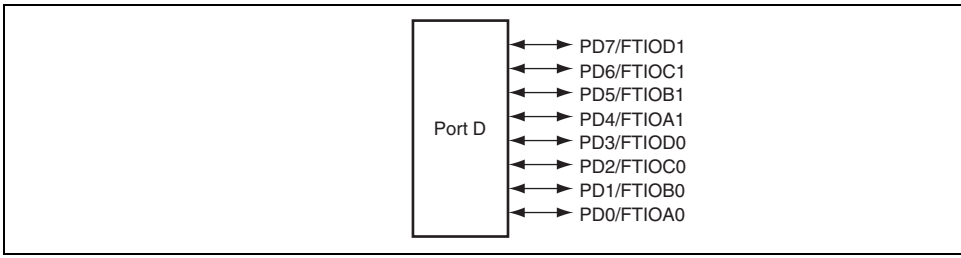


Figure 9.8 Port D Pin Configuration

Port D has the following registers.

- Port control register D (PCRD)
- Port data register D (PDRD)

3	PCRD3	0	W	
2	PCRD2	0	W	
1	PCRD1	0	W	
0	PCRD0	0	W	

9.8.2 Port Data Register D (PDRD)

PDRD is a general I/O port data register of port D.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7	0	R/W	PDRD stores output data for port D pins.
6	PD6	0	R/W	If PDRD is read while PCRD bits are set to 1, t
5	PD5	0	R/W	values stored in PDRD are read. If PDRD is re
4	PD4	0	R/W	PCRD bits are cleared to 0, the pin states are r
3	PD3	0	R/W	regardless of the value stored in PDRD.
2	PD2	0	R/W	
1	PD1	0	R/W	
0	PD0	0	R/W	

Value							input pin
						1	PD7 outp
	0	00	0	X	XXXX	0	PD7 inpu input pin
						1	PD7 outp
			1	1	XXXX	X	FTIOD1
				0	0XXX	0	PD7 inpu input pin
						1	PD7 outp
					101X or 1001	X	FTIOD1
					11XX or 1000	0	PD7 inpu input pin
						1	PD7 outp
		Other than 00	X	X	XXXX	X	FTIOD1

[Legend] X: Don't care.

					input pin
				1	PD6 output
	1	1	XXXX	X	FTIOC1 ou
		0	0XXX	0	PD6 input/F input pin
				1	PD6 output
			101X or 1001	X	FTIOC1 ou
			11XX or 1000	0	PD6 input/F input pin
				1	PD6 output
Other than 00	X	X	XXXX	X	FTIOC1 ou

[Legend] X: Don't care.

				1	PD5 outp
		1	1	XXX	X	FTIOB1
			0	01X or 001	X	FTIOB1
				1XX or 000	0	PD5 inpu input pin
					1	PD5 outp
	Other than 00	X	X	XXX	X	FTIOB1

[Legend] X: Don't care.

			1	PD4 outpu
	1	01X or 001	X	FTIOA1 o
		1XX or 000	0	PD4 input input pin
			1	PD4 outpu
Other than 00	X	XXX	X	FTIOA1 o

[Legend] X: Don't care.

				1	PD3 outp
	1	1	XXXX	X	FTIOD0
		0	0XXX	0	PD3 inpu input pin
				1	PD3 outp
			101X or 1001	X	FTIOD0
			11XX or 1000	0	PD3 inpu input pin
				1	PD3 outp
	Other than 00	X	X	XXXX	X	FTIOD0

[Legend] X: Don't care.

					input/FTI input pin
				1	PD2 outp
		1	1	XXXX	X	FTIOC0 pin
			0	0XXX	0	PD2 input/FTI input pin
					1	PD2 outp
				101X or 1001	X	FTIOC0 pin
				11XX or 1000	0	PD2 input/FTI input pin
					1	PD2 outp
	Other than 00	X	X	XXXX	X	FTIOC0 pin

[Legend] X: Don't care.

			001		
			1XX or 000	0	PD1 inpu input pin
				1	PD1 outp
Other than 00	X	X	XXX	X	FTIOB0 c

[Legend] X: Don't care.

0	00	0	XXX	X	FTIOA0 outp
		1	01X or 001	X	FTIOA0 outp
			1XX or 000	0	PD0 input/F input pin
				1	PD0 output p
	Other than 00	X	XXX	0	PD0 input/F input pin
				1	PD0 output p

[Legend] X: Don't care.

9.9 Port E

Port E is a general I/O port also functioning as timer RD_1 I/O pins. Each pin of port E is in figure 9.9. The setting of the timer RD_1 function has priority over those for other func

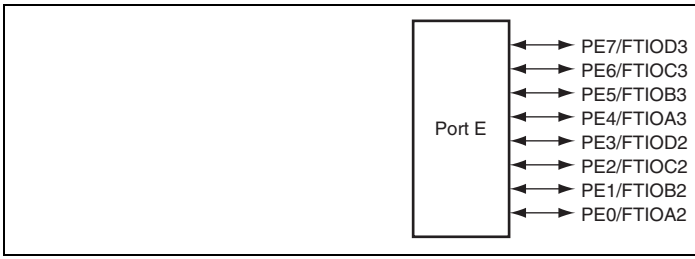


Figure 9.9 Port E Pin Configuration

7	PCRE7	0	W	When each of the port E pins functions as a g
6	PCRE6	0	W	port, setting a PCRE bit to 1 makes the corres
5	PCRE5	0	W	pin an output port, while clearing the bit to 0 m
4	PCRE4	0	W	pin an input port.
3	PCRE3	0	W	
2	PCRE2	0	W	
1	PCRE1	0	W	
0	PCRE0	0	W	

9.9.2 Port Data Register E (PDRE)

PDRE is a general I/O port data register of port E.

Bit	Bit Name	Initial Value	R/W	Description
7	PE7	0	R/W	PDRE stores output data for port E pins.
6	PE6	0	R/W	If PDRE is read while PCRE bits are set to 1,
5	PE5	0	R/W	values stored in PDRE are read. If PDRE is re
4	PE4	0	R/W	PCRE bits are cleared to 0, the pin states are
3	PE3	0	R/W	regardless of the value stored in PDRE.
2	PE2	0	R/W	
1	PE1	0	R/W	
0	PE0	0	R/W	

Value						input pin
					1	PE7 output
	0	00	0	X	XXXX	0	PE7 input/F input pin
						1	PE7 output
			1	1	XXXX	X	FTIOD3 ou
				0	0XXX	0	PE7 input/F input pin
						1	PE7 output
					101X or 1001	X	FTIOD3 ou
					11XX or 1000	0	PE7 input/F input pin
						1	PE7 output
		Other than 00	X	X	XXXX	X	FTIOD3 ou

[Legend] X: Don't care.

					pin
				1	PE6 output pin
		1	1	XXXX	X	FTIOC3 output p
			0	0XXX	0	PE6 input/FTIOC pin
					1	PE6 output pin
				101X or 1001	X	FTIOC3 output p
				11XX or 1000	0	PE6 input/FTIOC pin
					1	PE6 output pin
	Other than 00	X	X	XXXX	X	FTIOC3 output p

[Legend] X: Don't care.

					pin
				1	PE5 output pin
	1	1	XXX	X	FTIOB3 output pi
		0	01X or 001	X	FTIOB3 output pi
			1XX or 000	0	PE5 input/FTIOB3 pin
				1	PE5 output pin
Other than 00	X	X	XXX	X	FTIOB3 output pi

[Legend] X: Don't care.

			1	PE4 output pin
	1	01X or 001	X	FTIOA3 output p
		1XX or 000	0	PE4 input/FTIOA pin
			1	PE4 output pin
Other than 00	X	XXX	X	FTIOA3 output p

[Legend] X: Don't care.

					pin
				1	PE3 output pin
	1	1	XXXX	X	FTIOD2 output pi
		0	0XXX	0	PE3 input/FTIOD2 pin
				1	PE3 output pin
			101X or 1001	X	FTIOD2 output pi
			11XX or 1000	0	PE3 input/FTIOD2 pin
				1	PE3 output pin
Other than 00	X	X	XXXX	X	FTIOD2 output pi

[Legend] X: Don't care.

					pin
				1	PE2 output pin
		1	1	XXXX	X	FTIOC2 output p
			0	0XXX	0	PE2 input/FTIOC pin
					1	PE2 output pin
				101X or 1001	X	FTIOC2 output p
				11XX or 1000	0	PE2 input/FTIOC pin
					1	PE2 output pin
	Other than 00	X	X	XXXX	X	FTIOC2 output p

[Legend] X: Don't care.

	1	1	XXX	X	FTIOB2 output pi
		0	01X or 001	X	FTIOB2 output pi
			1XX or 000	0	PE1 input/FTIOB2 pin
				1	PE1 output pin
	Other than 00	X	X	XXX	X	FTIOB2 output pi

[Legend] X: Don't care.

					pin
				1	PE0 output pin
0	00	0	XXX	X	FTIOA2 output p
		1	01X or 001	X	FTIOA2 output p
			1XX or 000	0	PE0 input/FTIOA pin
				1	PE0 output pin
	Other than 00	X	XXX	0	FTIOA2 output p

[Legend] X: Don't care.

Figure 9.10 Port F Pin Configuration

Port F has the following registers.

- Port data register F (PDRF)
- Port mode register F (PMRF)

9.10.1 Port Data Register F (PDRF)

PDRF is a general input port data register of port F.

Bit	Bit Name	Initial Value	R/W	Description
7	PF7	—	R	If PDRF is read, the pin states are read.
6	PF6	—	R	However, if a port F pin is specified as an anal
5	PF5	—	R	channel by ADCSR in the A/D converter, the b
4	PF4	—	R	as 0.
3	PF3	—	R	
2	PF2	—	R	
1	PF1	—	R	
0	PF0	—	R	

9.10.3 Pin Functions

The correspondence between the register specification and the port functions is shown b

- PF7/AN7 pin

Register	ADCR	ADCSR				
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**Pin Function**
Setting Value	0	X	1	1	1	AN7 input pin
	Other than above					PF7 input pin

[Legend] X: Don't care.

- PF6/AN6 pin

Register	ADCR	ADCSR				
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**Pin Function**
Setting Value	0	0	1	1	0	AN6 input pin
		1	1	1	X	
	Other than above					PF6 input pin

[Legend] X: Don't care.

- PF4/AN4 pin

Register	ADCR	ADCSR				
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**Pin Function**
Setting Value	0	0	1	0	0	AN4 input pin
		1	1	X	X	
	Other than above					PF4 input pin

[Legend] X: Don't care.

- PF3/AN3 pin

Register	ADCR	ADCSR				
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**Pin Function**
Setting Value	0	X	0	1	1	AN3 input pin
	Other than above					PF3 input pin

[Legend] X: Don't care.

- PF2/AN2 pin

Register	ADCR	ADCSR				
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**Pin Function**
Setting Value	0	0	0	1	0	AN2 input pin
		1	0	1	X	
	Other than above					PF2 input pin

[Legend] X: Don't care.

- PF0/AN0 pin

Register	PMRF	ADCR	ADCSR				
Bit Name	PF0	CH3	SCAN	CH2	CH1	CH0	Pin Functio
Setting Value	0	0	0	0	0	0	AN0 input pi
			1	0	X	X	
			Other than above				PF0 input pi

[Legend] X: Don't care.

9.11 Port G

Port G is a general input port also functioning as A/D converter analog input pins, timer pins, and timer RD input pins. Each pin of port G is shown in figure 9.11.

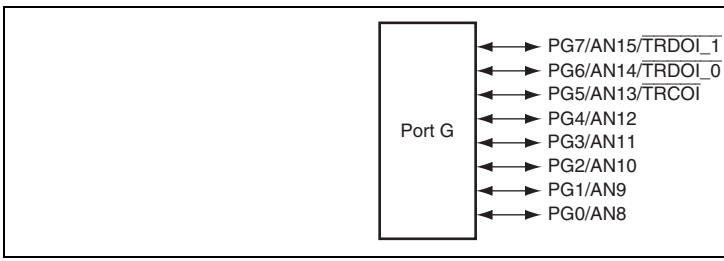


Figure 9.11 Port G Pin Configuration

Bit	Bit Name	Value	R/W	Description
7	PCRG7	0	W	When each of the port G pins functions as a ge I/O port, setting a PCRG bit to 1 makes the corresponding pin an output port, while clearin to 0 makes the pin an input port.
6	PCRG6	0	W	
5	PCRG5	0	W	
4	PCRG4	0	W	
3	PCRG3	0	W	
2	PCRG2	0	W	
1	PCRG1	0	W	
0	PCRG0	0	W	

9.11.2 Port Data Register G (PDRG)

PDRG is a general I/O port data register of port G.

Bit	Bit Name	Initial Value	R/W	Description
7	PG7	0	R/W	PDRG stores output data for port G pins.
6	PG6	0	R/W	If PDRG is read while PCRG bits are set to 1, t values stored in PDRG are read. If PDRG is re PCRG bits are cleared to 0, the pin states are regardless of the value stored in PDRG. Howe port G pin is specified as an analog input chan ADCSR or ADCR in the A/D converter, the bit as 0 even when the PGRG bit is cleared.
5	PG5	0	R/W	
4	PG4	0	R/W	
3	PG3	1	R/W	
2	PG2	0	R/W	
1	PG1	0	R/W	
0	PG0	0	R/W	

				0: General I/O port 1: AN14/$\overline{\text{TRDOI\_0}}$ input pin
5	PMRG5	0	R/W	This bit selects the function of pin PG5/AN13/$\overline{\text{T}}$ 0: General I/O port 1: AN14/$\overline{\text{TRCOI}}$ input pin
4	—	1	—	Reserved This bit is always read as 1.
3	PMRG3	0	R/W	These bits select the trigger source of the A/D
2	PMRG2	0	R/W	00: A/D converter is activated by the $\overline{\text{ADTRG}}$ s 01: A/D converter is activated by timer RD_0 10: A/D converter is activated by timer RD_1 11: Reserved
1	PMRG1	0	R/W	Selects the edge of the $\overline{\text{ADTRG}}$ signal. 0: Falling edge 1: Rising edge
0	PMRG0	0	R/W	This bit selects the function of pin PH0/SCK3_ 0: General I/O port 1: $\overline{\text{ADTRG}}$ input pin

						0	0	PG7 input pin
							1	PG7 output pin

[Legend] X: Don't care.

- PG6/AN14/$\overline{\text{TRDOI\_0}}$ pin

Register	**ADCR**	**ADCSR**				**PMRG**	**PCRG**	
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**PMRG6**	**PCRG6**	**Pin Function**
Setting Value	1	X	1	1	0	X	X	AN14 input pin
	1	1	1	1	1	X	X	
	Other than above					1	X	$\overline{\text{TRDOI\_0}}$ input
						0	0	PG6 input pin
							1	PG6 output pin

[Legend] X: Don't care.

[Legend] X: Don't care.

- PG4/AN12 pin

Register	ADCR		ADCSR			PCRG	
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**PCRG4**	**Pin Function**
Setting Value	1	X	1	0	0	X	AN12 input pi
	1	1	1	X	X	X	
	Other than above					0	PG4 input pin
						1	PG4 output pi

[Legend] X: Don't care.

- PG3/AN11 pin

Register	ADCR		ADCSR			PCRG	
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**PCRG3**	**Pin Function**
Setting Value	1	X	0	1	1	X	AN11 input pi
	Other than above					0	PG3 input pin
						1	PG3 output pi

[Legend] X: Don't care.

- PG1/AN9 pin

Register	ADCR		ADCSR			PCRG	
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**PCRG1**	**Pin Function**
Setting Value	1	X	0	0	1	X	AN9 input pin
	1	1	0	1	0	X	
	1	1	0	1	1	X	
	Other than above					0	PG1 input pin
						1	PG1 output pin

[Legend] X: Don't care.

- PG0/AN8 pin

Register	ADCR		ADCSR			PCRG	
Bit Name	**CH3**	**SCAN**	**CH2**	**CH1**	**CH0**	**PCRG0**	**Pin Function**
Setting Value	1	X	0	0	0	X	AN8 input pin
	1	1	0	X	X	X	
	Other than above					0	PG0 input pin
						1	PG0 output pin

[Legend] X: Don't care.

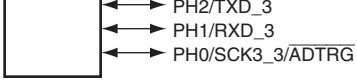


Figure 9.12 Port H Pin Configuration

Port H has the following registers.

- Port control register H (PCRH)
- Port data register H (PDRH)

9.12.1 Port Control Register H (PCRH)

PCRH selects inputs/outputs in bit units for pins to be used as general I/O ports of port H

Bit	Bit Name	Initial Value	R/W	Description
7	PCRH7	0	W	When each of the port H pins PH7 to PH0 fun
6	PCRH6	0	W	a general I/O port, setting a PCRH bit to 1 ma
5	PCRH5	0	W	corresponding pin an output port, while clearin
4	PCRH4	0	W	to 0 makes the pin an input port.
3	PCRH3	0	W	
2	PCRH2	0	W	
1	PCRH1	0	W	
0	PCRH0	0	W	

3	PH3	0	R/W
2	PH2	0	R/W
1	PH1	0	R/W
0	PH0	0	R/W

9.12.3 Pin Functions

The correspondence between the register specification and the port functions is shown be

- PH7/FTIOD pin

Register	TRCOER	TRCMR		TRCIOR1			PCRH	
Bit Name	ED	PWM2	PWMD	IOD2	IOD1	IOD0	PCRH7	Pin Function
Setting Value	1	X	X	X	X	X	0	PH7 input/FTIOD i
							1	PH7 output pin
	0	0	X	X	X	X	0	PH7 input/FTIOD i
							1	PH7 output pin
		1	1	X	X	X	X	FTIOD (PWM) outp
			0	0	1	X	X	FTIOD output pin
					0	1	X	FTIOD output pin
						0	0	PH7 input/FTIOD i
							1	PH7 output pin
				1	X	X	0	PH7 input/FTIOD i
							1	PH7 output pin

[Legend] X: Don't care.

				0	1	X	FTIOC output pin
					0	0	PH6 input/FTIOC
						1	PH6 output pin
				1	X	X	0	PH6 input/FTIOC
							1	PH6 output pin

[Legend] X: Don't care.

- PH5/FTIOB pin

Register	TRCOER	TRCMR		TRCIOR0			PCRH	
Bit Name	**EB**	**PWM2**	**PWMB**	**IOB2**	**IOB1**	**IOB0**	**PCRH5**	**Pin Function**
Setting Value	1	X	X	X	X	X	0	PH5 input/FTIOB
							1	PH5 output
	0	0	X	X	X	X	X	FTIOB (PWM2) o
		1	1	X	X	X	X	FTIOB (PWM) ou
			0	0	1	X	X	FTIOB output pin
					0	1	X	FTIOB output pin
						0	0	PH5 input/FTIOB
							1	PH5 output
				1	X	X	0	PH5 input/FTIOB
							1	PH5 output

[Legend] X: Don't care.

	1	0	1	X	X	FTIOA output pin
			0	1	X	FTIOA output pin
				0	0	PH4 input/FTIOA in /TRGC input pin
					1	PH4 output pin
		1	X	X	0	PH4 input/FTIOA in /TRGC input pin
					1	PH4 output pin

[Legend] X: Don't care.

- PH3/FTCI pin

Register	**PCRH**	
Bit Name	**PCRH3**	**Pin Function**
Setting Value	0	PH3 input/FTCI input pin
	1	PH3 output/FTCI input pin

[Legend] X: Don't care.

Register	SCR3_3	PCRH	
Bit Name	**RE**	**PCRH1**	**Pin Function**
Setting Value	0	0	PH1 input pin
		1	PH1 output pin
	1	X	RXD_3 input pin

[Legend] X: Don't care.

- PH0/SCK3_3/$\overline{\text{ADTRG}}$ pin

Register	SCR3_3		SMR3_3	PMRG	PCRH	
Bit Name	**CKE1**	**CKE0**	**COM**	**PMRG0**	**PCRH0**	**Pin Function**
Setting Value	0	0	0	0	0	PH0 input pin
					1	PH0 output pin
				1	X	$\overline{\text{ADTRG}}$ input pin
	0	0	1	X	X	SCK3_3 output pin
	0	1	X	X	X	SCK3_3 output pin
	1	X	X	X	X	SCK3_3 input pin

[Legend] X: Don't care.

Figure 9.13 Port J Pin Configuration

Port J has the following registers.

- Port control register J (PCRJ)
- Port data register J (PDRJ)

9.13.1 Port Control Register J (PCRJ)

PCRJ selects inputs/outputs in bit units for pins to be used as general I/O ports of port J.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	—	—	Reserved
1	PCRJ1	0	W	When each of the port J pins PJ1 to PJ0 functi
0	PCRJ0	0	W	general I/O port, setting a PCRJ bit to 1 makes corresponding pin an output port, while clearin to 0 makes the pin an input port.

of the value stored in PDRJ.

9.13.3 Pin Functions

The correspondence between the register specification and the port functions is shown b

- PJ1/OSC2/CLKOUT pin

Register	CKCSR		PCRJ	
Bit Name	**PMRJ1**	**PMRJ0**	**PCRJ1**	**Pin Function**
Setting Value	0	X	0	PJ1 input pin
			1	PJ1 output pin
	1	0	X	CLKOUT output pin
		1	X	OSC2 output pin

[Legend] X: Don't care.

- PJ0/OSC1 pin

Register	CKCSR	PCRJ	
Bit Name	**PMRJ0**	**PCRJ0**	**Pin Function**
Setting Value	0	0	PJ0 input pin
		1	PJ0 output pin
	1	X	OSC1 input pin

[Legend] X: Don't care.

- Readable/writable counter of seconds, minutes, hours, and day-of-week with BCD c
- Periodic (seconds, minutes, hours, days, and weeks) interrupts
- 8-bit free running counter
- Selection of clock source

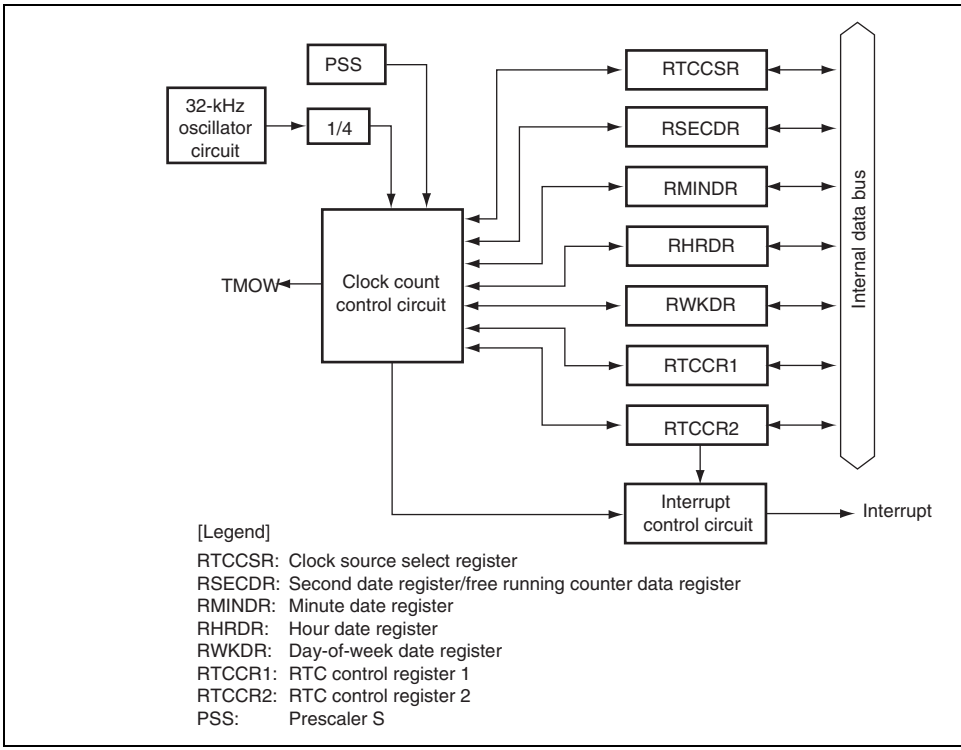


Figure 10.1 Block Diagram of RTC

The RTC has the following registers.

- Second data register/free running counter data register (RSECDR)
- Minute data register (RMINDR)
- Hour data register (RHRDR)
- Day-of-week data register (RWKDR)
- RTC control register 1 (RTCCR1)
- RTC control register 2 (RTCCR2)
- Clock source select register (RTCCSR)

10.3.1 Second Data Register/Free Running Counter Data Register (RSECDR)

RSECDR counts the BCD-coded second value. The setting range is decimal 00 to 59. It i
read register used as a counter, when it operates as a free running counter. For more infor
on reading seconds, minutes, hours, and day-of-week, see section 10.4.3, Data Reading P

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—	R	RTC Busy This bit is set to 1 when the RTC is updating (c the values of second, minute, hour, and day-of data registers. When this bit is 0, the values of minute, hour, and day-of-week data registers n adopted.

10.3.2 Minute Data Register (RMINDR)

RMINDR counts the BCD-coded minute value on the carry generated once per minute b
RSECDR counting. The setting range is decimal 00 to 59.

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—	R	RTC Busy This bit is set to 1 when the RTC is updating (the values of second, minute, hour, and day-o data registers. When this bit is 0, the values o minute, hour, and day-of-week data registers adopted.
6	MN12	—	R/W	Counting Ten's Position of Minutes
5	MN11	—	R/W	Counts on 0 to 5 for 60-minute counting.
4	MN10	—	R/W	
3	MN03	—	R/W	Counting One's Position of Minutes
2	MN02	—	R/W	Counts on 0 to 9 once per minute. When a ca generated, 1 is added to the ten's position.
1	MN01	—	R/W	
0	MN00	—	R/W	

				data registers. When this bit is 0, the values of minute, hour, and day-of-week data registers n adopted.
6	—	0	—	Reserved This bit is always read as 0.
5	HR11	—	R/W	Counting Ten's Position of Hours
4	HR10	—	R/W	Counts on 0 to 2 for ten's position of hours.
3	HR03	—	R/W	Counting One's Position of Hours
2	HR02	—	R/W	Counts on 0 to 9 once per hour. When a carry generated, 1 is added to the ten's position.
1	HR01	—	R/W	
0	HR00	—	R/W	

				minute, hour, and day-of-week data registers adopted.
6	—	0	—	Reserved
5	—	0	—	These bits are always read as 0.
4	—	0	—	
3	—	0	—	
2	WK2	—	R/W	Day-of-Week Counting
1	WK1	—	R/W	Day-of-week is indicated with a binary code
0	WK0	—	R/W	000: Sunday
				001: Monday
				010: Tuesday
				011: Wednesday
				100: Thursday
				101: Friday
				110: Saturday
				111: Reserved (setting prohibited)

				0: RTC operates in 12-hour mode. RHRDR cou to 11.
				1: RTC operates in 24-hour mode. RHRDR cou to 23.
5	PM	—	R/W	a.m./p.m.
				0: Indicates a.m. when RTC is in the 12-hour m
				1: Indicates p.m. when RTC is in the 12-hour m
4	RST	0	R/W	Reset
				0: Normal operation
				1: Resets registers and control circuits except and this bit. Clear this bit to 0 after having be 1.
3	INT	—	R/W	Interrupt Generation Timing
				0: Generates a second, minute, hour, or day-o periodic interrupt during RTC busy period.
				1: Generates a second, minute, hour, or day-o periodic interrupt immediately after completi busy period.
2 to 0	—	All 0	—	Reserved
				These bits are always read as 0.

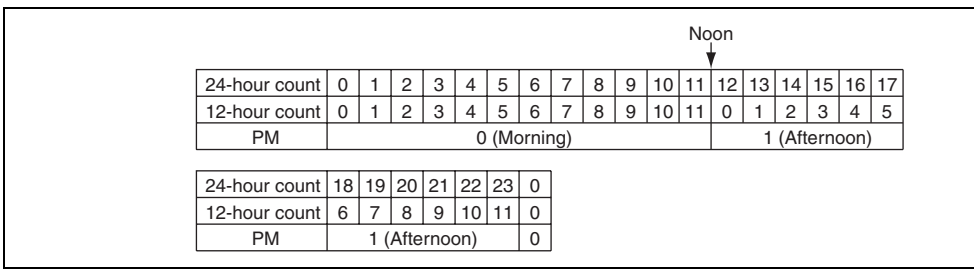


Figure 10.2 Definition of Time Expression

6	—	0		These bits are always read as 0.
5	FOIE	—	R/W	Free Running Counter Overflow Interrupt Ena 0: Disables an overflow interrupt 1: Enables an overflow interrupt
4	WKIE	—	R/W	Week Periodic Interrupt Enable 0: Disables a week periodic interrupt 1: Enables a week periodic interrupt
3	DYIE	—	R/W	Day Periodic Interrupt Enable 0: Disables a day periodic interrupt 1: Enables a day periodic interrupt
2	HRIE	—	R/W	Hour Periodic Interrupt Enable 0: Disables an hour periodic interrupt 1: Enables an hour periodic interrupt
1	MNIE	—	R/W	Minute Periodic Interrupt Enable 0: Disables a minute periodic interrupt 1: Enables a minute periodic interrupt
0	SEIE	—	R/W	Second Periodic Interrupt Enable 0: Disables a second periodic interrupt 1: Enables a second periodic interrupt

7	—	0	—	Reserved This bit is always read as 0.
6	RCS6	0	R/W	Clock Output Selection
5	RCS5	0	R/W	Selects a clock output from the TMOW pin whe TMOW in PMR1 to 1. 00: φ/4 01: φ/8 10: φ/16 11: φ/32
4	—	0	—	Reserved This bit is always read as 0.
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: φ/8····· Free running counter opera
1	RCS1	0	R/W	0001: φ/32····· Free running counter oper
0	RCS0	0	R/W	0010: φ/128····· Free running counter oper 0011: φ/256····· Free running counter oper 0100: φ/512····· Free running counter oper 0101: φ/2048····· Free running counter oper 0110: φ/4096····· Free running counter oper 0111: φ/8192····· Free running counter oper 1XXX: 32.768 kHz···RTC operation

[Legend]

X: Don't care

Figure 10.3 shows the procedure for the initial setting of the RTC. To set the RTC again follow this procedure.

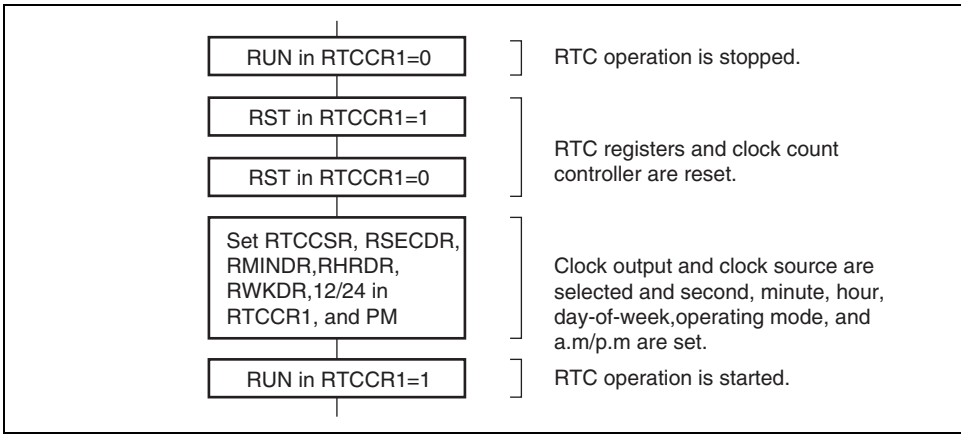


Figure 10.3 Initial Setting Procedure

bit is set to 1, the registers are updated, and the BSY bit is cleared to 0.

2. Making use of interrupts, read from the second, minute, hour, and day-of week registe the IRRTA flag in IRR1 is set to 1 and the BSY bit is confirmed to be 0.
3. Read from the second, minute, hour, and day-of week registers twice in a row, and if no change in the read data, the read data is used.

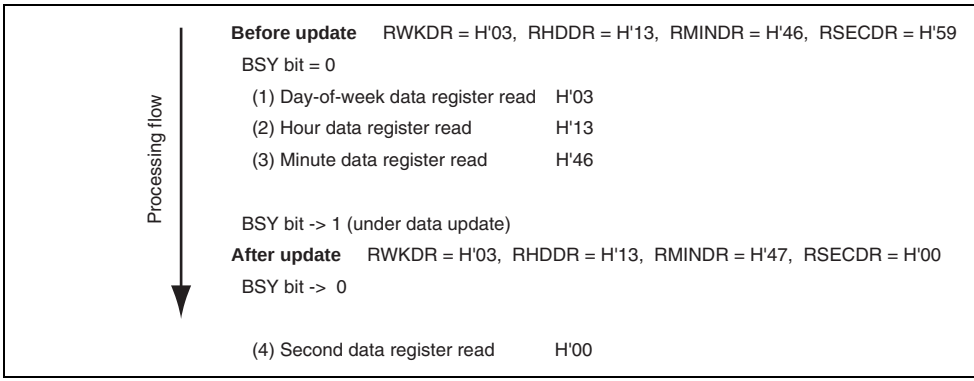


Figure 10.4 Example: Reading of Inaccurate Time Data

Table 10.2 Interrupt Sources

Interrupt Name	Interrupt Source	Interrupt Ena
Overflow interrupt	Occurs when the free running counter is overflowed.	FOIE
Week periodic interrupt	Occurs every week when the day-of-week date register value becomes 0.	WKIE
Day periodic interrupt	Occurs every day when the day-of-week date register is counted.	DYIE
Hour periodic interrupt	Occurs every hour when the hour date register is counted.	HRIE
Minute periodic interrupt	Occurs every minute when the minute date register is counted.	MNIE
Second periodic interrupt	Occurs every second when the second date register is counted.	SCIE

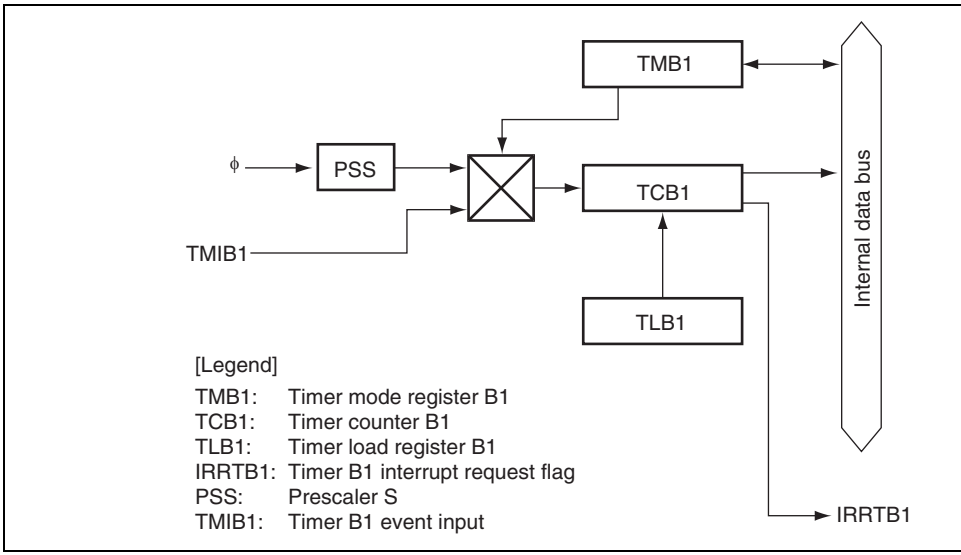


Figure 11.1 Block Diagram of Timer B1

11.2 Input/Output Pin

Table 11.1 shows the timer B1 pin configuration.

Table 11.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer B1 event input	TMIB1	Input	Event input to TCB1

TMB1 selects the auto-reload function and input clock.

Bit	Bit Name	Initial Value	R/W	Description
7	TMB17	0	R/W	Auto-Reload Function Select 0: Interval timer function selected 1: Auto-reload function selected
6 to 3	—	All 1	—	Reserved These bits are always read as 1.
2	TMB12	0	R/W	Clock Select
1	TMB11	0	R/W	000: Internal clock: ϕ/8192
0	TMB10	0	R/W	001: Internal clock: ϕ/2048 010: Internal clock: ϕ/512 011: Internal clock: ϕ/256 100: Internal clock: ϕ/64 101: Internal clock: ϕ/16 110: Internal clock: ϕ/4 111: External event (TMIB1): rising or falling ed Note: * The edge of the external event signal selected by bit IEG1 in the interrupt e select register 1 (IEGR1). See section Interrupt Edge Select Register 1 (IEG details. Before setting TMB12 to TMB IRQ1 in the port mode register 1 (PMI should be set to 1.

TLB1 is an 8-bit write-only register for setting the reload value of TCB1. When a reload
set in TLB1, the same value is loaded into TCB1 as well, and TCB1 starts counting up f
value. When TCB1 overflows during operation in auto-reload mode, the TLB1 value is
into TCB1. Accordingly, overflow periods can be set within the range of 1 to 256 input
TLB1 is allocated to the same address as TCB1. TLB1 is initialized to H'00.

11.4 Operation

11.4.1 Interval Timer Operation

When bit TMB17 in TMB1 is cleared to 0, timer B1 functions as an 8-bit interval timer.
reset, TCB1 is cleared to H'00 and bit TMB17 is cleared to 0, so up-counting and interva
resume immediately. The operating clock of timer B1 is selected from seven internal clo
output by prescaler S, or an external clock input at pin TMB1. The selection is made by
TMB12 to TMB10 in TMB1.

After the count value in TMB1 reaches H'FF, the next clock signal input causes timer B
overflow, setting flag IRRTB1 in IRR2 to 1. If IENTB1 in IENR2 is 1, an interrupt is re
the CPU.

At overflow, TCB1 returns to H'00 and starts counting up again. During interval timer o
(TMB17 = 0), when a value is set in TLB1, the same value is set in TCB1.

TCB1.

11.4.3 Event Counter Operation

Timer B1 can operate as an event counter in which TMIB1 is set to an event input pin. Ex
event counting is selected by setting bits TMB12 to TMB10 in TMB1 to 1. TCB1 counts
rising or falling edge of an external event signal input at pin TMB1.

When timer B1 is used to count external event input, bit IRQ1 in PMR1 should be set to
IEN1 in IENR1 should be cleared to 0 to disable IRQ1 interrupt requests.

11.5 Timer B1 Operating Modes

Table 11.2 shows the timer B1 operating modes.

Table 11.2 Timer B1 Operating Modes

Operating Mode		Reset	Active	Sleep	Subactive	Subsleep	Sta
TCB1	Interval	Reset	Functions	Functions	Halted	Halted	Ha
	Auto-reload	Reset	Functions	Functions	Halted	Halted	Ha
TMB1		Reset	Functions	Retained	Retained	Retained	Re

- Choice of seven clock signals is available.
  Choice of six internal clock sources (ϕ/128, ϕ/64, ϕ/32, ϕ/16, ϕ/8, ϕ/4) or an external
- Counter can be cleared by compare match A or B, or by an external reset signal. If th
  stop function is selected, the counter can be halted when cleared.
- Timer output is controlled by two independent compare match signals, enabling puls
  with an arbitrary duty cycle, PWM output, and other applications.
- Three interrupt sources: compare match A, compare match B, timer overflow
- Counting can be initiated by trigger input at the TRGV pin. The rising edge, falling e
  both edges of the TRGV input can be selected.

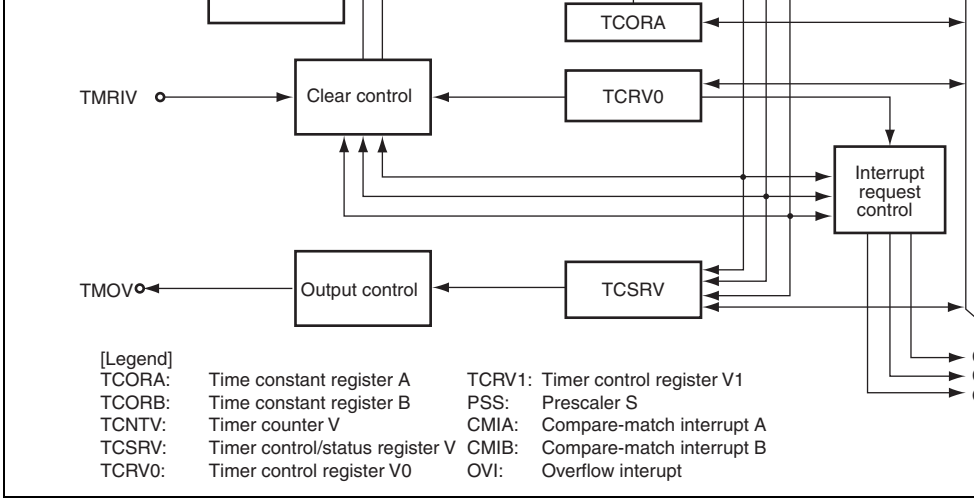


Figure 12.1 Block Diagram of Timer V

12.2 Input/Output Pins

Table 12.1 shows the timer V pin configuration.

Table 12.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer V output	TMOV	Output	Timer V waveform output
Timer V clock input	TMCIV	Input	Clock input to TCNTV
Timer V reset input	TMRIV	Input	External input to reset TCNTV
Trigger input	TRGV	Input	Trigger input to initiate counting

12.3.1 Timer Counter V (TCNTV)

TCNTV is an 8-bit up-counter. The clock source is selected by bits CKS2 to CKS0 in ti
control register V0 (TCRV0). The TCNTV value can be read and written by the CPU at
TCNTV can be cleared by an external reset input signal, or by compare match A or B. T
clearing signal is selected by bits CCLR1 and CCLR0 in TCRV0.

When TCNTV overflows, OVF is set to 1 in timer control/status register V (TCSRV).

TCNTV is initialized to H'00.

12.3.2 Time Constant Registers A, B (TCORA, TCORB)

TCORA and TCORB have the same function.

TCORA and TCORB are 8-bit readable/writable registers.

TCORA and TCNTV are compared at all times. When the TCORA and TCNTV conten
CMFA is set to 1 in TCSRV. If CMIEA is also set to 1 in TCRV0, a CPU interrupt is re
Note that they must not be compared during the T3 state of a TCORA write cycle.

Timer output from the TMOV pin can be controlled by the identifying signal (compare
and the settings of bits OS3 to OS0 in TCSRV.

TCORA and TCORB are initialized to H'FF.

				When this bit is set to 1, interrupt request from CMFA bit in TCSRV is enabled.
5	OVIE	0	R/W	Timer Overflow Interrupt Enable When this bit is set to 1, interrupt request from bit in TCSRV is enabled.
4	CCLR1	0	R/W	Counter Clear 1 and 0
3	CCLR0	0	R/W	These bits specify the clearing conditions of TC 00: Clearing is disabled 01: Cleared by compare match A 10: Cleared by compare match B 11: Cleared on the rising edge of the TMRIV pi operation of TCNTV after clearing depends TRGE in TCRV1.
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	These bits select clock signals to input to TCN
0	CKS0	0	R/W	the counting condition in combination with ICK TCRV1. Refer to table 12.2.

		1	0	Internal clock: counts on ϕ/64, falling
			1	Internal clock: counts on ϕ/128, fallin
1	0	0	—	Clock input prohibited
		1	—	External clock: counts on rising edge
	1	0	—	External clock: counts on falling edg
		1	—	External clock: counts on rising and edge

12.3.4 Timer Control/Status Register V (TCSRV)

TCSRV indicates the status flag and controls outputs by using a compare match.

Bit	Bit Name	Initial Value	R/W	Description
7	CMFB	0	R/W	Compare Match Flag B Setting condition: When the TCNTV value matches the TCORB Clearing condition: After reading CMFB = 1, cleared by writing 0
6	CMFA	0	R/W	Compare Match Flag A Setting condition: When the TCNTV value matches the TCORA Clearing condition: After reading CMFA = 1, cleared by writing 0

2	OS2	0	R/W	These bits select an output method for the TOI the compare match of TCORB and TCNTV. 00: No change 01: 0 output 10: 1 output 11: Output toggles
1	OS1	0	R/W	Output Select 1 and 0
0	OS0	0	R/W	These bits select an output method for the TOI the compare match of TCORA and TCNTV. 00: No change 01: 0 output 10: 1 output 11: Output toggles

OS3 and OS2 select the output level for compare match B. OS1 and OS0 select the outpu
for compare match A. The two output levels can be controlled independently. After a rese
timer output is 0 until the first compare match.

3	TVEG0	0	R/W	These bits select the TRGV input edge. 00: TRGV trigger input is prohibited 01: Rising edge is selected 10: Falling edge is selected 11: Rising and falling edges are both selected
2	TRGE	0	R/W	TCNT starts counting up by the input of the e is selected by TVEG1 and TVEG0. 0: Disables starting counting-up TCNTV by th the TRGV pin and halting counting-up TCN TCNTV is cleared by a compare match. 1: Enables starting counting-up TCNTV by the the TRGV pin and halting counting-up TCN TCNTV is cleared by a compare match.
1	—	1	—	Reserved This bit is always read as 1.
0	ICKS0	0	R/W	Internal Clock Select 0 This bit selects clock signals to input to TCNT combination with CKS2 to CKS0 in TCRV0. Refer to table 12.2.

will be set. The timing at this time is shown in figure 12.4. An interrupt request is sen
CPU when OVIE in TCRV0 is 1.

3. TCNTV is constantly compared with TCORA and TCORB. Compare match flag A o
(CMFA or CMFB) is set to 1 when TCNTV matches TCORA or TCORB, respectivel
compare-match signal is generated in the last state in which the values match. Figure
shows the timing. An interrupt request is generated for the CPU when CMIEA or CM
TCRV0 is 1.
4. When a compare match A or B is generated, the TMOV responds with the output valu
selected by bits OS3 to OS0 in TCSRV. Figure 12.6 shows the timing when the outpu
toggled by compare match A.
5. When CCLR1 or CCLR0 in TCRV0 is 01 or 10, TCNTV can be cleared by the corres
compare match. Figure 12.7 shows the timing.
6. When CCLR1 or CCLR0 in TCRV0 is 11, TCNTV can be cleared by the rising edge
input of TMRIV pin. A TMRIV input pulse-width of at least 1.5 system clocks is nec
Figure 12.8 shows the timing.
7. When a counter-clearing source is generated with TRGE in TCRV1 set to 1, the coun
halted as soon as TCNTV is cleared. TCNTV resumes counting-up when the edge sel
TVEG1 or TVEG0 in TCRV1 is input from the TGRV pin.

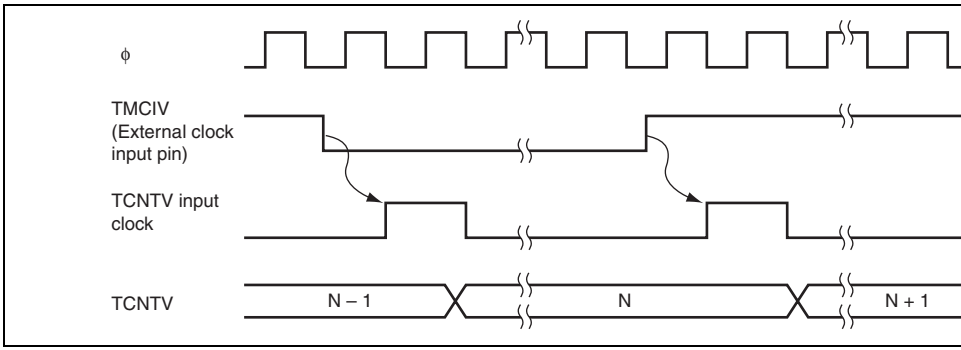


Figure 12.3 Increment Timing with External Clock

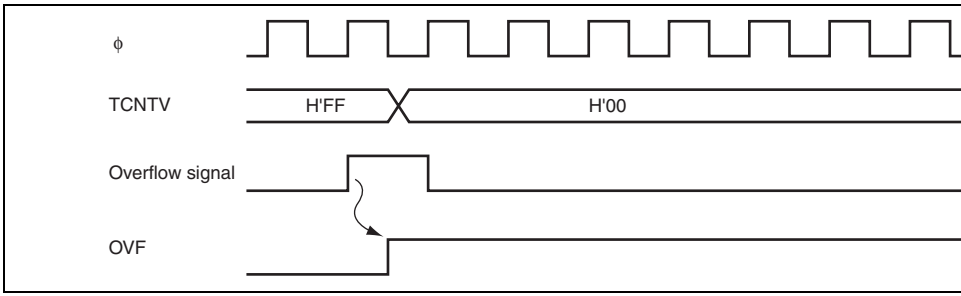


Figure 12.4 OVF Set Timing

Figure 12.5 CMFA and CMFB Set Timing

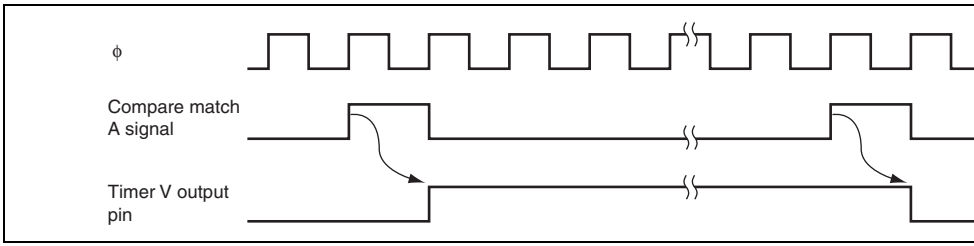


Figure 12.6 TMOV Output Timing

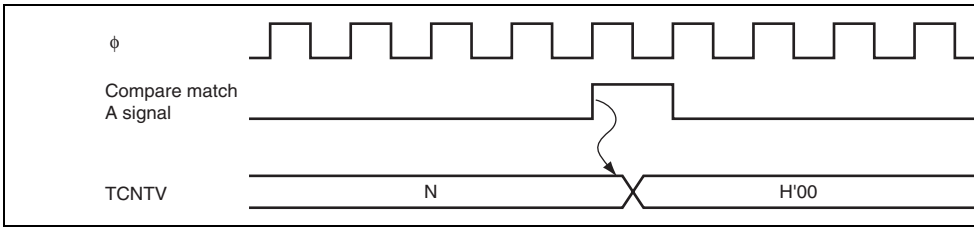


Figure 12.7 Clear Timing by Compare Match

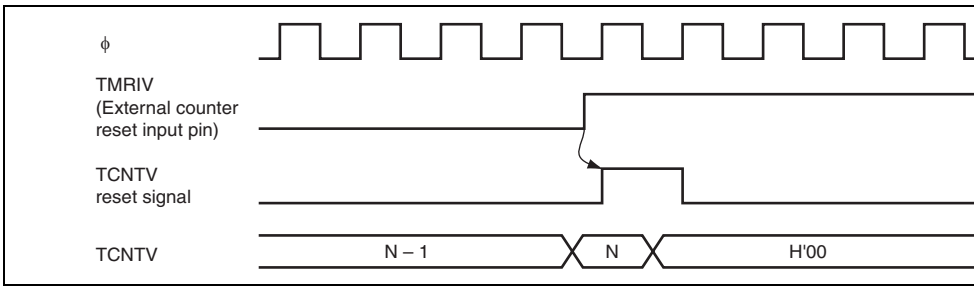


Figure 12.8 Clear Timing by TMRIV Input

3. Set bits CKS2 to CKS0 in TCRV0 and bit ICKS0 in TCRV1 to select the desired clo
4. With these settings, a waveform is output without further software intervention, with determined by TCORA and a pulse width determined by TCORB.

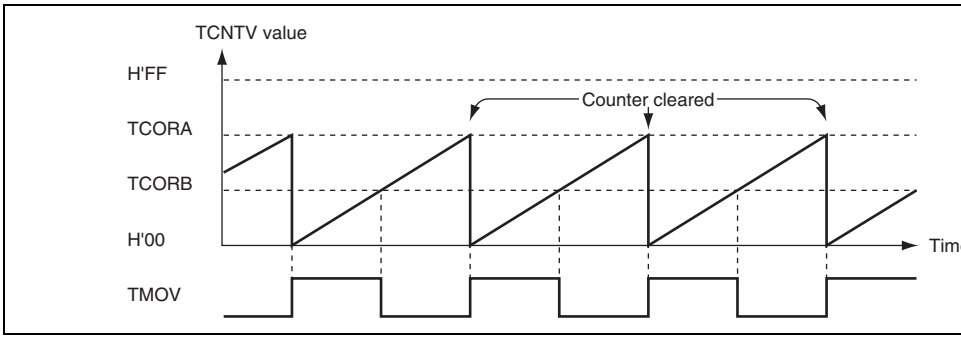


Figure 12.9 Pulse Output Example

input.

4. Set bits CKS2 to CKS0 in TCRV0 and bit ICKS0 in TCRV1 to select the desired cloc
5. With these settings, a pulse waveform will be output without further software interver with a delay determined by TCORA from the TRGV input, and a pulse width determi (TCORB – TCORA).

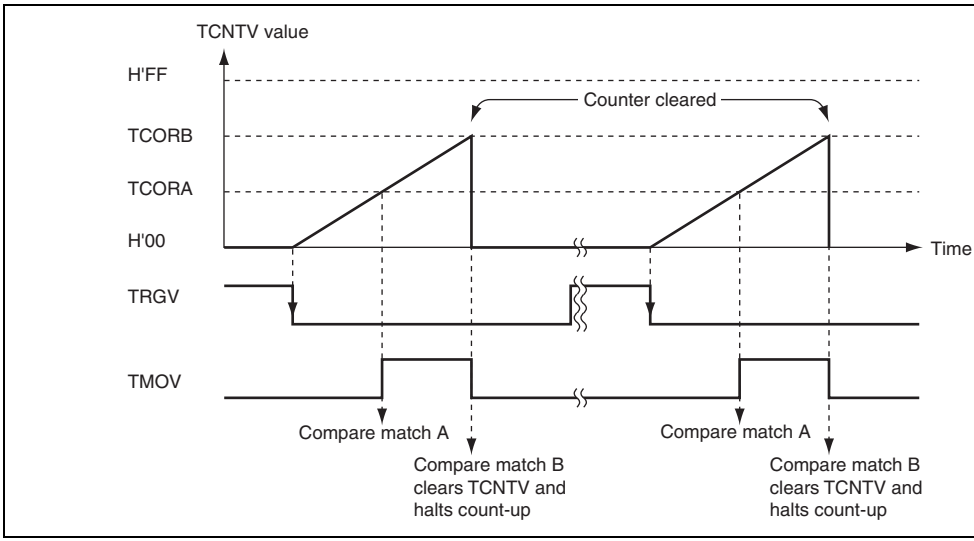


Figure 12.10 Example of Pulse Output Synchronized to TRGV Input

12.12 shows the timing.

3. If compare matches A and B occur simultaneously, any conflict between the output for compare match A and compare match B is resolved by the following priority: to output > output 1 > output 0.
4. Depending on the timing, TCNTV may be incremented by a switch between differe clock sources. When TCNTV is internally clocked, an increment pulse is generated falling edge of an internal clock signal, that is divided system clock (ϕ). Therefore, in figure 12.3 the switch is from a high clock signal to a low clock signal, the switch seen as a falling edge, causing TCNTV to increment. TCNTV can also be incremen switch between internal and external clocks.

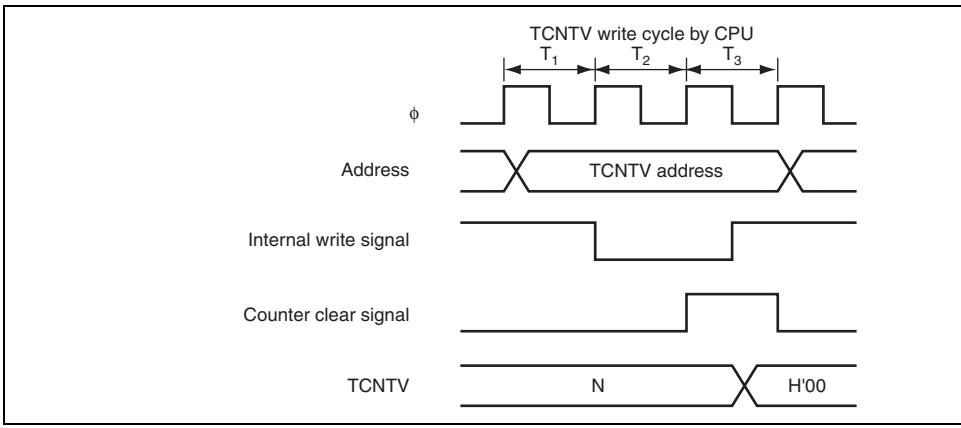


Figure 12.11 Contention between TCNTV Write and Clear

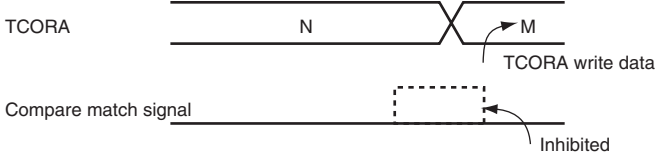


Figure 12.12 Contention between TCORA Write and Compare Match

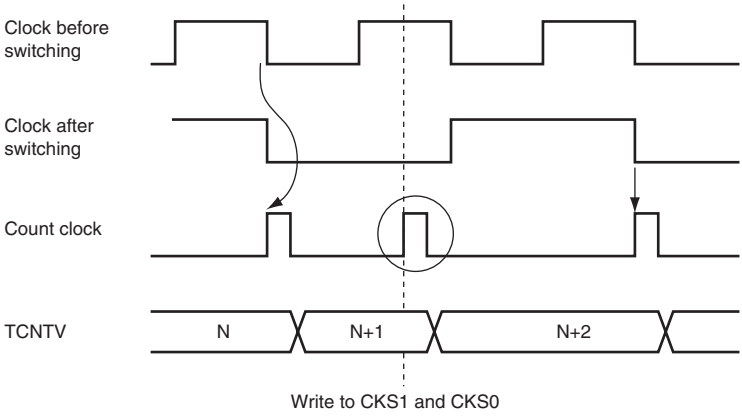


Figure 12.13 Internal Clock Switching and TCNTV Operation

Six internal clocks (ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/32, and ϕ40M which is a 40-MHz/32-MHz clo
from the on-chip oscillator) and an external clock (for counting external events)

- Capability to process up to four pulse outputs or four pulse inputs
- Four general registers
  - Can be used as output compare or input capture registers independently
  - Can be used as buffer registers for the output compare or input capture registers
- Timer inputs and outputs
  - Timer mode

    Waveform output by compare match (Selection of 0 output, 1 output, or toggle o

    Input capture function (Rising edge, falling edge, or both edges)

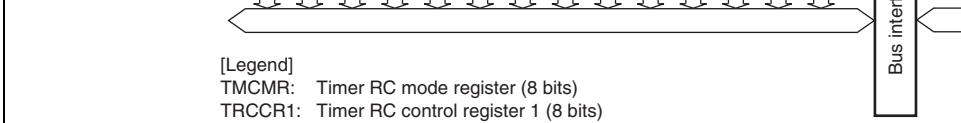
    Counter clearing function (Counters can be cleared by compare match)
  - PWM mode

    Generates up to three-phase PWM output with desired duty cycles.
  - PWM2 mode

    Generates pulses with a desired period and duty cycle.
- Any initial timer output value can be set
- Five interrupt sources

  Four compare match/input capture interrupts and an overflow interrupt.

capture registers)		GRA			GRA in buffer mode)	GRB buff
Counter clearing function		GRA compare match	GRA compare match	—	—	—
		TGRC input	—	—	—	—
Initial output value setting function		—	Yes	Yes	Yes	Yes
Buffer function		—	Yes	Yes	—	—
Compare match output	0	—	Yes	Yes	Yes	Yes
	1	—	Yes	Yes	Yes	Yes
	Toggle	—	Yes	Yes	Yes	Yes
Input capture function		—	Yes	Yes	Yes	Yes
PWM mode		—	—	Yes	Yes	Yes
PWM2 mode		—	—	Yes	—	—
Interrupt sources		Overflow	Compare match/input capture	Compare match/input capture	Compare match/input capture	Com mat capt



[Legend]
TMCMR: Timer RC mode register (8 bits)
TRCCR1: Timer RC control register 1 (8 bits)
TRCCR2: Timer RC control register 2 (8 bits)
TRCIER: Timer RC interrupt enable register (8 bits)
TRCSR: Timer RC status register (8 bits)
TRCIOR0: Timer RC I/O control register 0 (8 bits)
TRCIOR1: Timer RC I/O control register 1 (8 bits)
TRCOER: Timer RC output enable register (8 bits)
TRCDF: Timer RC digital filter function select register (8 bits)
TRCCNT: Timer RC counter (16 bits)
GRA: General register A (input capture/output compare register: 16 bits)
GRB: General register B (input capture/output compare register: 16 bits)
GRC: General register C (input capture/output compare register: 16 bits)
GRD: General register D (input capture/output compare register: 16 bits)

Figure 13.1 Timer RC Block Diagram

			external trigger input pin (TRGC)
Input capture/ output compare B	FTIOB	I/O	Output pin for GRB output compa input pin for GRB input capture/ PWM output pin in PWM mode
Input capture/ output compare C	FTIOC	I/O	Output pin for GRC output compa input pin for GRC input capture/ or PWM output pin in PWM mod
Input capture/ output compare D	FTIOD	I/O	Output pin for GRD output compa input pin for GRD input capture/ or PWM output pin in PWM mod
Timer output control input	$\overline{\text{TRCOI}}$	Input	Input pin for timer output disablin

- Timer RC I/O control register 1 (TRCIOR1)
- Timer RC output enable register (TRCOER)
- Timer RC digital filtering function select register (TRCDF)
- Timer RC counter (TRCCNT)
- General Registers A to D (GRA to GRD)
- General register A (GRA)
- General register B (GRB)
- General register C (GRC)
- General register D (GRD)

				• When 1 is written in CTS [Clearing conditions] • When 0 is written in CTS • In PWM2 mode, when the CSTP bit in TRCC to 1 and a compare match signal is generate
6	—	1	—	Reserved This bit is always read as 1.
5	BUFEB	0	R/W	Buffer Operation B Selects the GRD function. 0: GRD functions as an input capture/output com register 1: GRD functions as the buffer register for GRB
4	BUFEA	0	R/W	Buffer Operation A Selects the GRC function. 0: GRC functions as an input capture/output com register 1: GRC functions as the buffer register for GRA
3	PWM2	1	R/W	PWM2 Mode Selects the output mode of the FTIOB pin. 0: Functions in PWM2 mode. The following settings are invalid: TRCIOR0, TRCIOR1, and the PWMB, PWMC, and PWM TRCMR. 1: Functions in timer mode or PWM mode. The following settings are valid: TRCIOR0, TR and the PWMB, PWMC, and PWMD bits in TR

0	PWMB	0	R/W	PWM Mode B Selects the output mode of the FTIOB pin. 0: Functions in timer mode 1: Functions in PWM mode

5	CKS1	0	R/W	Select the source of the clock input to TRCCNT.
4	CKS0	0	R/W	000: TRCCNT counts the internal clock ϕ 001: TRCCNT counts the internal clock ϕ/2 010: TRCCNT counts the internal clock ϕ/4 011: TRCCNT counts the internal clock ϕ/8 100: TRCCNT counts the internal clock ϕ/32 101: TRCCNT counts the rising edge of the exte event (FTCI) 110: TRCCNT counts the internal clock ϕ40M 111: Reserved (setting prohibited) When the internal clock (ϕ) is selected, TRCCNT the subclock in subactive or subsleep mode. * Note: * When selecting the internal clock ϕ40 on-chip oscillator should be in operat When switching the clock, the counte be halted.
3	TOD	0	R/W	Timer Output Level Setting D Sets the output value of the FTIOD pin until the f compare match D is generated. In PWM mode, the output polarity of the FTIOD pin. 0: Output value is 0* 1: Output value is 1*
2	TOC	0	R/W	Timer Output Level Setting C Sets the output value of the FTIOC pin until the f compare match C is generated. In PWM mode, the output polarity of the FTIOC pin. 0: Output value is 0* 1: Output value is 1*

				1: Output value is 1*

[Legend]
X: Don't care.
Note: * The change of the setting is immediately reflected in the output value.

13.3.3 Timer RC Control Register 2 (TRCCR2)

TRCCR2 specifies the edge of the TRGC signal and an input enable.

Bit	Bit Name	Initial Value	R/W	Description
7	TCEG1	0	R/W	TRGC Input Edge Select
6	TCEG0	0	R/W	These bits select the input edge of the TRGC s function is only enabled when the PWM2 bit in set to 0. 00: A trigger input on TRGC is disabled 01: The rising edge is selected 10: The falling edge is selected 11: Both edges are selected
5	CSTP	0	R/W	Specifies whether TRCCNT counting up is halte continued by the compare match A signal. This only enabled when the PWM2 bit in TRCMR is 0: TRCCNT counting up is continued 1: TRCCNT counting up is halted
4 to 0	—	All 1	—	Reserved These bits are always read as 1.

				These bits are always read as 1.
3	IMIED	0	R/W	Input Capture/Compare Match Interrupt Enable D When this bit is set to 1, an IMID interrupt reques the IMFD flag in TRCSR is enabled.
2	IMIEC	0	R/W	Input Capture/Compare Match Interrupt Enable C When this bit is set to 1, an IMIC interrupt reques the IMFC flag in TRCSR is enabled.
1	IMIEB	0	R/W	Input Capture/Compare Match Interrupt Enable B When this bit is set to 1, an IMIB interrupt reques the IMFB flag in TRCSR is enabled.
0	IMIEA	0	R/W	Input Capture/Compare Match Interrupt Enable A When this bit is set to 1, an IMIA interrupt reques the IMFA flag in TRCSR is enabled.

				Read OVF when OVF = 1, then write 0 in OVF
6 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	IMFD	0	R/W	Input Capture/Compare Match Flag D [Setting conditions] • TRCCNT = GRD when GRD functions as a compare register • The TRCCNT value is transferred to GRD b capture signal when GRD functions as an in capture register • TRCCNT = GRD when the PWMD bit is set the PWM2 bit to 0 in TRCMR [Clearing condition] Read IMFD when IMFD = 1, then write 0 in IMF
2	IMFC	0	R/W	Input Capture/Compare Match Flag C [Setting conditions] • TRCCNT = GRC when GRC functions as a compare register • The TRCCNT value is transferred to GRC b capture signal when GRC functions as an in capture register • TRCCNT = GRC when the PWMC bit is set the PWM2 bit to 0 in TRCMR [Clearing condition] Read IMFC when IMFC = 1, then write 0 in IMF

				PWM2 bit to 0 in TRCMR [Clearing condition] Read IMFB when IMFB = 1, then write 0 in IMFB
0	IMFA	0	R/W	Input Capture/Compare Match Flag A [Setting conditions] • TRCCNT = GRA when GRA functions as an compare register • The TRCCNT value is transferred to GRA by capture signal when GRA functions as an inp capture register • TRCCNT = GRA when the PWMD, PWMC, c bit is set to 1 or the PWM2 bit to 0 in TRCMR [Clearing condition] Read IMFA when IMFA = 1, then write 0 in IMFA

				0: GRB functions as an output compare registe
				1: GRB functions as an input capture register
5	IOB1	0	R/W	I/O Control B1 and B0
4	IOB0	0	R/W	When IOB2 = 0,
				00: No output at compare match
				01: 0 output to the FTIOB pin at GRB compare
				10: 1 output to the FTIOB pin at GRB compare
				11: Output toggles to the FTIOB pin at GRB co match
				When IOB2 = 1,
				00: Input capture at rising edge at the FTIOB pi
				01: Input capture at falling edge at the FTIOB p
				1X: Input capture at rising and falling edges of pin
3	—	1	—	Reserved
				This bit is always read as 1.
2	IOA2	0	R/W	I/O Control A2
				Selects the GRA function.
				0: GRA functions as an output compare registe
				1: GRA functions as an input capture register

00: Input capture at rising edge of the FTIOA pin

01: Input capture at falling edge of the FTIOA pi

1X: Input capture at rising and falling edges of th pin

[Legend]

X: Don't care.

Note: When a GR register functions as a buffer register for a paired GR register, the sett the IOA2 and IOB2 bits in TRCIOR0 and the IOC2 and IOD2 bits in TRCIOR1 of b registers should be the same.

				Selects the GRD function. 0: GRD functions as an output compare registe 1: GRD functions as an input capture register
5	IOD1	0	R/W	I/O Control D1 and D0
4	IOD0	0	R/W	When IOD2 = 0, 00: No output at compare match 01: 0 output to the FTIOD pin at GRD compare 10: 1 output to the FTIOD pin at GRD compare 11: Output toggles to the FTIOD pin at GRD co match When IOD2 = 1, 00: Input capture at rising edge at the FTIOD pi 01: Input capture at falling edge at the FTIOD p 1X: Input capture at rising and falling edges at t pin
3	—	1	—	Reserved This bit is always read as 1.
2	IOC2	0	R/W	I/O Control C2 Selects the GRC function. 0: GRC functions as an output compare registe 1: GRC functions as an input capture register

00: Input capture to GRC at rising edge of the FT

01: Input capture to GRC at falling edge of the F

1X: Input capture to GRC at rising and falling ed
the FTIOC pin

[Legend]

X: Don't care.

Note: When a GR register functions as a buffer register for a paired GR register, the sett
the IOA2 and IOB2 bits in TRCIOR0 and the IOC2 and IOD2 bits in TRCIOR1 of b
registers should be the same.

				1: The ED, EC, EV, EA bits are set to 1 by the input of the TRCOI signal
6 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	ED	1	R/W	Master Enable D 0: The FTIOD output is enabled according to TI TRCIOR0, and TRCIOR1 1: The FTIOD output is disabled regardless of T TRCIOR0, and TRCIOR1 (The FTIOD pin fu an I/O port)
2	EC	1	R/W	Master Enable C 0: The FTIOC output is enabled according to TI TRCIOR0, and TRCIOR1 1: The FTIOC output is disabled regardless of T TRCIOR0, and TRCIOR1 (The FTIOC pin fu an I/O port)
1	EB	1	R/W	Master Enable B 0: The FTIOB output is enabled according to TF TRCIOR0, and TRCIOR1 1: The FTIOB output is disabled regardless of T TRCIOR0, and TRCIOR1 (The FTIOB pin fu an I/O port)
0	EA	1	R/W	Master Enable A 0: The FTIOA output is enabled according to TF and TRCIOR1 1: The FTIOA output is disabled regardless of T and TRCIOR1 (The FTIOA pin functions as a port)

6	DFCK0	0	R/W	00: ϕ/32 01: ϕ/8 10: ϕ 11: Clock specified by bits CKS2 to CKS0 in TI
5	—	0	—	Reserved This bit is always read as 0.
4	DFRG	0	R/W	Enables or disables the digital filter for the TRG 0: Disables the digital filter 1: Enables the digital filter
3	DFD	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter
2	DFC	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter
1	DFB	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter
0	DFA	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter

Each general register is a 16-bit readable/writable register that can function as either an
compare register or an input-capture register. The function is selected by settings in TR
TRCIOR1.

When a general register is used as an input-compare register, its value is constantly com
the TRCCNT value. When the two values match (a compare match), the corresponding
IMFA, IMFB, IMFC, or IMFD bit) in TRCSR is set to 1. An interrupt request is generat
time, when the IMIEA, IMIEB, IMIEC, or IMIED bit in TRCIER is set to 1. A compare
output can be selected in TRCIOR.

When a general register is used as an input-capture register, an external input-capture si
detected and the current TRCCNT value is stored in the general register. The correspond
(the IMFA, IMFB, IMFC, or IMFD bit) in TRCSR is set to 1. If the corresponding inter
enable bit (the IMIEA, IMIEB, IMIEC, or IMIED bit) in TRIER is set to 1 at this time,
interrupt request is generated. The edge of the input-capture signal is selected in TRCIO

GRC and GRD can be used as buffer registers of GRA and GRB, respectively, by settin
and BUFEB in TRCMR.

For example, when GRA is set as an output-compare register and GRC is set as the buff
for GRA, the value in the buffer register GRC is sent to GRA whenever compare match
generated.

When GRA is set as an input-capture register and GRC is set as the buffer register for G
value in TRCCNT is transferred to GRA and the value in the buffer register GRC is tran
GRA whenever an input capture is generated.

GRA to GRD must be written or read in 16-bit units; 8-bit access is not allowed. GRA t
initialized to H'FFFF by a reset.

— Enables PWM2 mode operation by setting the PWM2 bit in TRMR

The FTIOA to FTIOD pins indicate the timer output mode by each register setting.

- FTIOA pin

Register Name	TRCOER	TRCIOR0		
Bit Name	**EA**	**PWM2**	**IOA2 to IOA0**	**Function**
Setting values	0	1	001, 01X	Timer mode waveform output (output co function)
	0	1	1XX	Timer mode (input capture function)
	1			
	Other than above			General I/O port

[Legend]
X: Don't care.

	0	1	0	1XX	Timer mode (input capture fu
	1				
	Other than above				General I/O port

[Legend]
X: Don't care.

- FTIOC pin

Register Name	TRCOER	TRCMR		TRCIOR1	
Bit Name	EC	PWM2	PWMC	IOC2 to IOC0	Function
Setting values	0	1	1	XXX	PWM mode waveform output
	0	1	0	001, 01X	Timer mode waveform output compare function)
	0	1	0	1XX	Timer mode (input capture fu
	1				
	Other than above				General I/O port

[Legend]
X: Don't care.

	Other than above	General I/O port

[Legend]
X: Don't care.

13.4.1 Timer Mode Operation

TRCCNT performs free-running or periodic counting operations. After a reset, TRCCNT
a free-running counter. When the CTS bit in TRCMR is set to 1, TRCCNT starts countin
the TRCCNT value overflows from H'FFFF to H'0000, the OVF flag in TRCSR is set to
OVIE in TRCIER is set to 1, an interrupt request is generated. Figure 13.2 shows an exan
free-running counting.

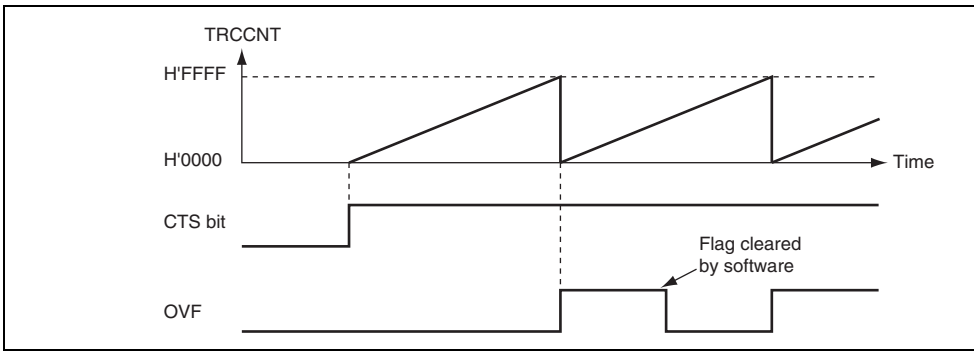


Figure 13.2 Free-Running Counter Operation

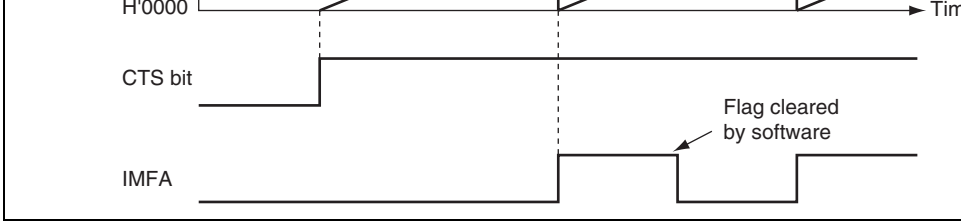


Figure 13.3 Periodic Counter Operation

By setting a general register as an output compare register, the specified level of a signa output on the FTIOA, FTIOB, FTIOC, or FTIOD pin on compare match A, B, C, or D. level can be selected from 0, 1, or toggle. Figure 13.4 shows an example of TRCCNT fu as a free-running counter. In this example, 1 is output on compare match A and 0 is outp compare match B. When the signal level is already at the selected output level, it is not on a compare match.

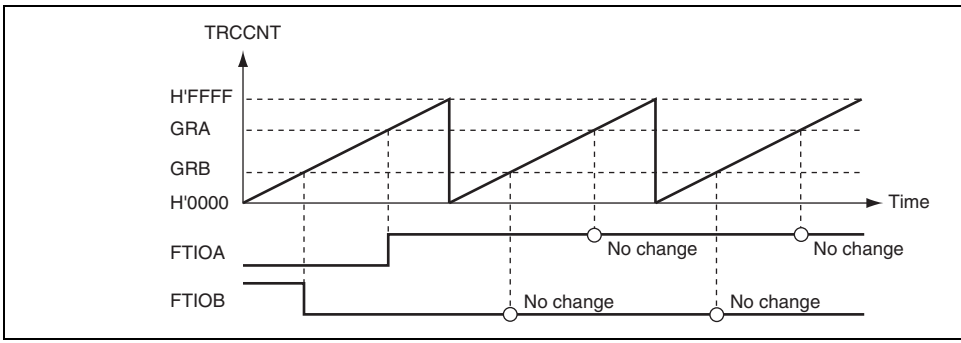


Figure 13.4 0 and 1 Output Example (TOA = 0, TOB = 1)

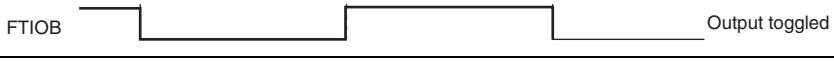


Figure 13.5 Toggle Output Example (TOA = 0, TOB = 1)

Figure 13.6 shows another example of toggled output when TRCCNT functions as a perio
counter on both compare matches A and B.

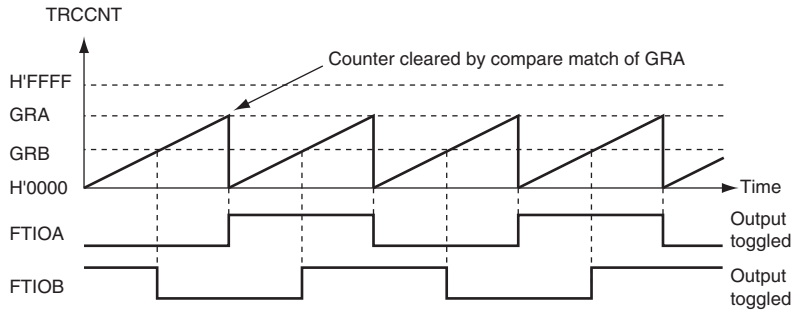


Figure 13.6 Toggle Output Example (TOA = 0, TOB = 1)

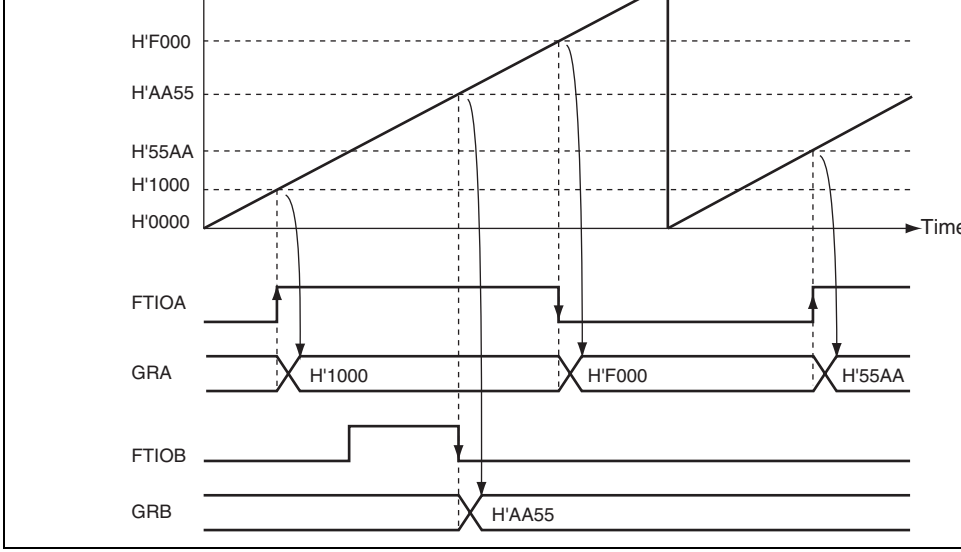


Figure 13.7 Input Capture Operating Example

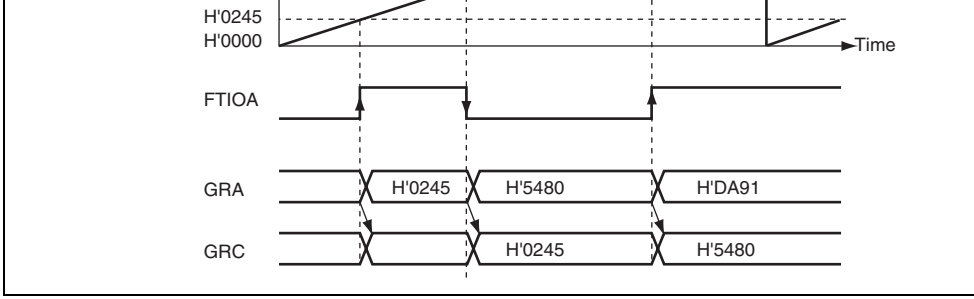


Figure 13.8 Buffer Operation Example (Input Capture)

the same value is set in the cycle register and duty cycle register, output levels are not ch
when a compare match occurs.

Figure 13.9 shows an example of operation in PWM mode. The output signals go 1 (TO
= TOD = 1) and TRCCNT is cleared on compare match A, and the output signals go 0 o
match B, C, and D .

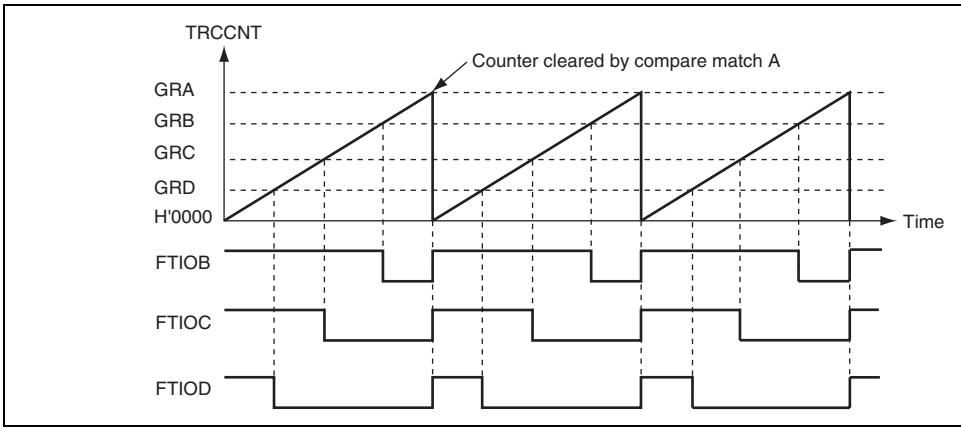


Figure 13.9 PWM Mode Example (1)

Figure 13.10 shows another example of operation in PWM mode. The output signals go
TOC = TOD = 0) and TRCCNT is cleared on compare match A, and the output signals g
compare match B, C, and D .

FTIOD

Figure 13.10 PWM Mode Example (2)

Figure 13.11 shows an example of buffer operation when the FTIOB pin is set to PWM n
GRD is set as the buffer register for GRB. TRCCNT is cleared on compare match A, and
FTIOB pin outputs 1 on compare match B and 0 on compare match A.

Due to the buffer operation, the FTIOB output levels are changed and the value of buffer
GRD is transferred to GRB whenever compare match B occurs. This procedure is repeate
time compare match B occurs.

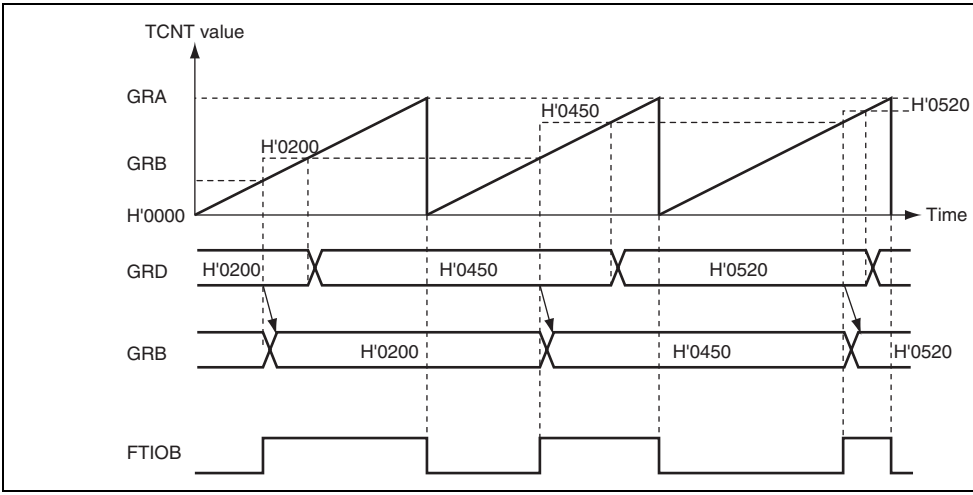


Figure 13.11 Buffer Operation Example (Output Compare)

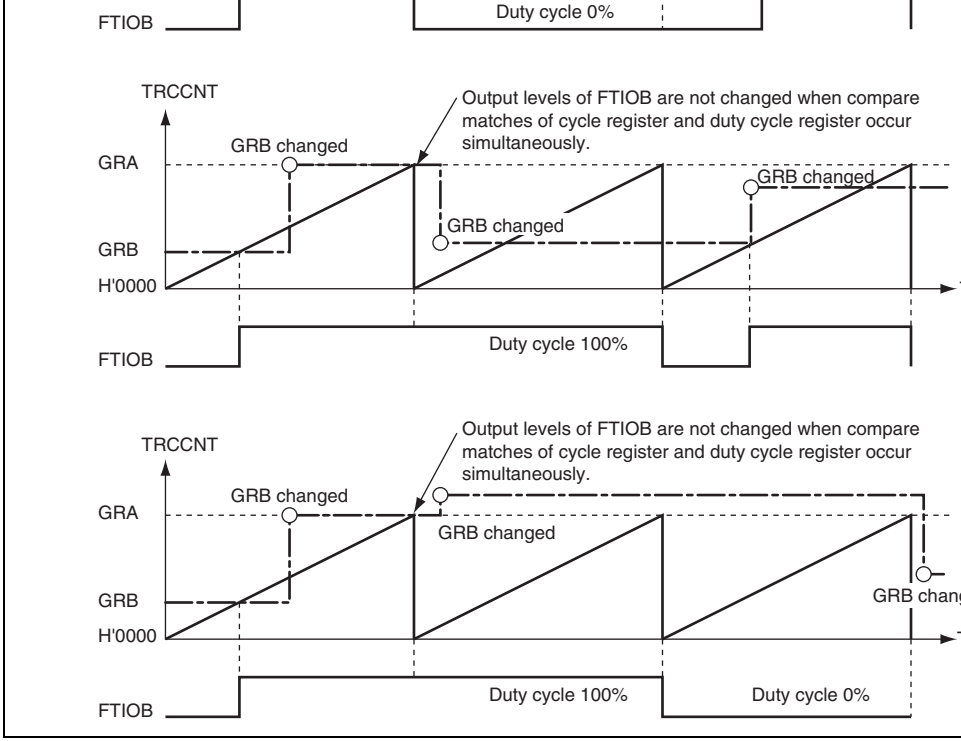


Figure 13.12 PWM Mode Example
(TOB, TOC, and TOD = 0: Initial Output Set to 0)

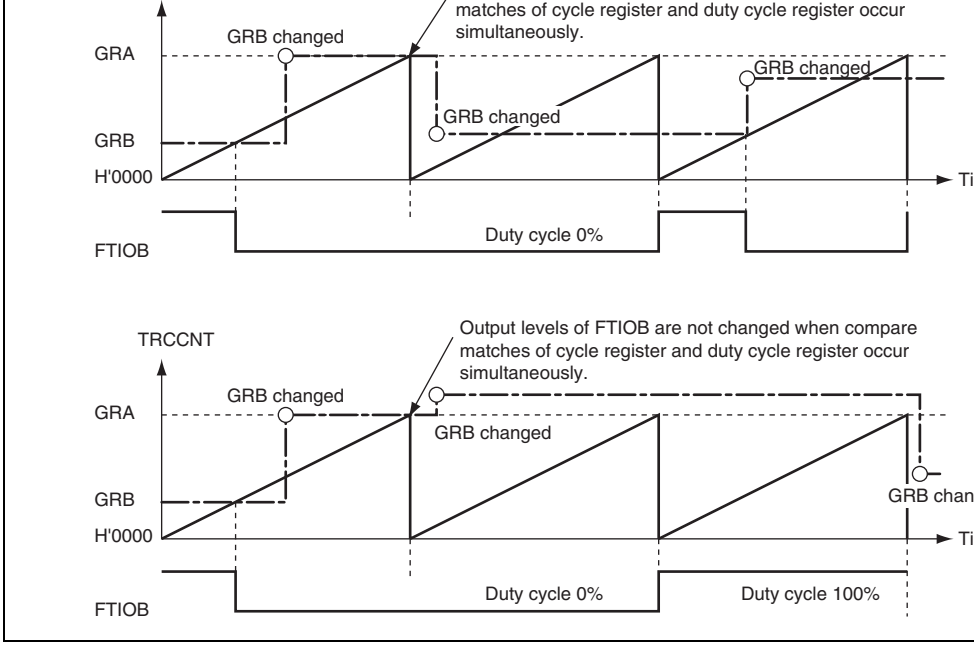


Figure 13.13 PWM Mode Example
(TOB, TOC, and TOD = 1: Initial Output Set to 1)

Figures 13.15 and 13.16 show the GRD and GRB buffer operating timing in PWM2 mo

In PWM2 mode, the value of GRD is transferred to GRB on a compare match of GRA a
counter is cleared. Note, however, that the counter is only cleared when the CCLR bit in
is set to 1. Moreover, when the trigger input is enabled by the TCEG1 and TCEG0 bits i
TRCCR2, the value of GRD is transferred to GRB by the trigger signal and the counter
The input/output pins of timers which do not operate in PWM2 mode are only used as g
ports.

Table 13.3 Pin Configuration in PWM2 Mode and GR Registers

Pin Name	Input/Output	Compare Match Register	Buffer Register
FTIOA	I/O	Port/TRGC	Port/TRGC
FTIOB	Output	GRB	GRD
		GRC	—
FTIOC	I/O	Port	Port
FTIOD	I/O	Port	Port

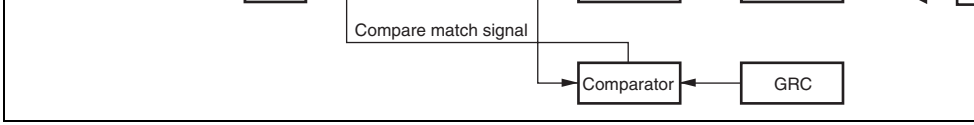


Figure 13.14 Block Diagram in PWM2 Mode

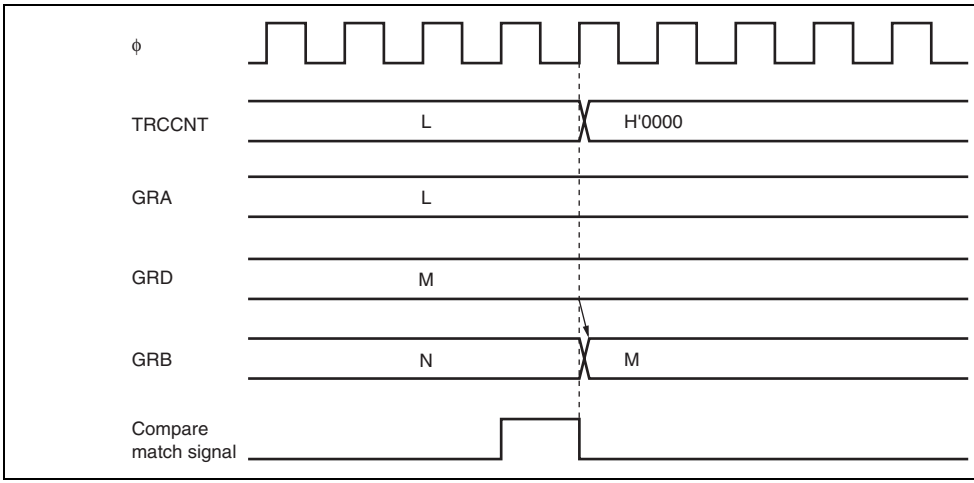


Figure 13.15 GRD and GRB Buffer Operating Timing in PWM2 Mode (1)

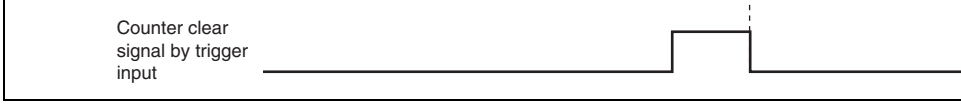


Figure 13.16 GRD and GRB Buffer Operating Timing in PWM2 Mode (2

In PWM2 mode, a pulse with a specified pulse width can be output on the FTIOB pin w specified delay time has elapsed since the TRGC signal was asserted. An assertion of th signal starts counting up. Arbitrary values can be specified for the pulse width and delay

Figures 13.17 and 13.18 show these examples in PWM2 mode. In these examples, the fa of the TRGC input is selected by TRCCR2 (setting the TCEG1 bit to 1 and clearing the bit to 0), TRCCNT continues counting-up on compare match A of GRA (clearing the CS TRCCR2 to 0), and GRD is set as the buffer register (setting the BUFEB bit in TRCMR initial value of the output signal is set to either 0 or 1 by TRCCR1 (clearing the TOB bit setting the TOB bit to 1), TRCCNT is cleared on compare match A (setting the CCLR b TRCCR1 to 1), and the waveform is output from the FTIOB pin (clearing the PWM2 bit TRCMR to 0).

When the TOB bit in TRCCR1 is cleared to 0 with the PWM2 mode function, the input ignored while the FTIOB pin is driven high. Whereas, when the TOB bit is set to 1, the is ignored while the FTIOB pin is driven low. The transfer from GRD to GRB is carried compare match of GRA and the TRGC input. However, if the TRGC input is canceled d change of the FTIOB level, the transfer from GRD to GRB is not carried out.

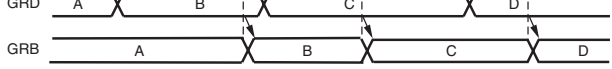


Figure 13.17 Example (1) of TRGC Synchronous Operation in PWM2 Mod

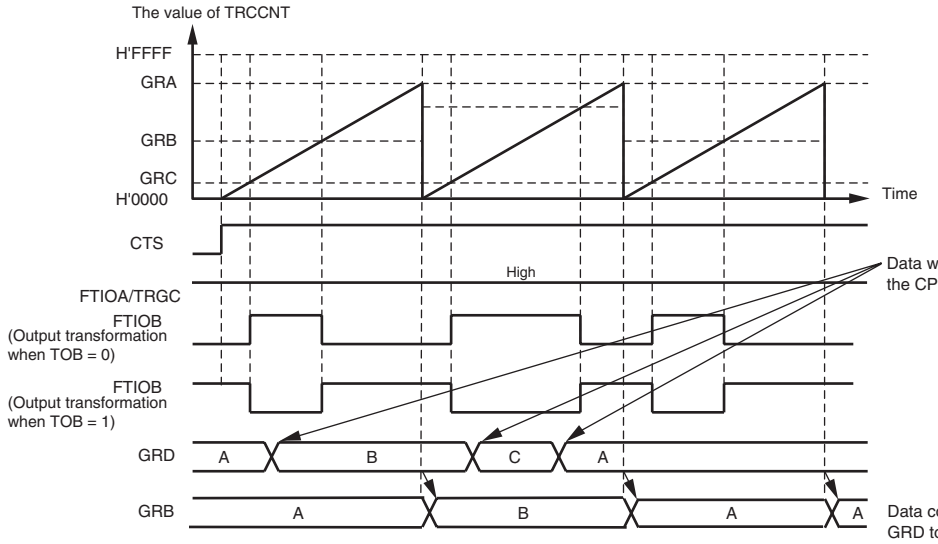


Figure 13.18 Example (2) of TRGC Synchronous Operation in PWM2 Mod

The following is an example of stopping operation of the counter in PWM2 mode. When CSTP bit in TRCCR2 is set to 1 and the CCLR bit in TRCCR1 is set to 1, TRCCNT is cl H'0000 on a compare match of GRA and stops counting. Moreover, TRCCNT is forcibly counting and cleared to the initial value when the CTS bit in TRCMR is cleared to 0. Figu shows such an example when the TOB bit in TRCCR1 is cleared to 0 and set to 1.

Figure 13.19 Example of Stopping Operation of the Counter in PWM2 Mo

The following is an example of output operation of the one-shot pulse waveform in PWI
When the TRGC input is disabled by TRCCR2 (clearing the TCEG1 and TCEG0 bits to
TRCCNT is set to counting-up on compare match A of GRA (setting the CSTP bit in TI
1), TRCCNT is cleared on compare match A (setting the CCLR bit in TRCCR1 to 1), an
initial value of the output signal is set to 0 by TRCCR1 (clearing the TOB bit to 0), TRC
starts counting when the CTS bit in TRCMR is set to 1. Then, TRCCNT is cleared to H'
compare match of GRA and stops counting, and the one-shot pulse waveform is output.
13.20 shows such an example.

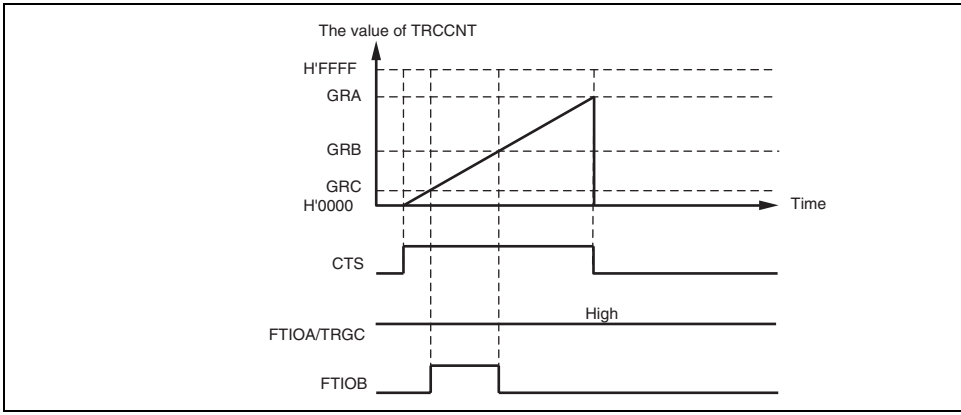


Figure 13.20 Example (1) of Output Operation of One-Shot Pulse Wavefo
in PWM2 Mode

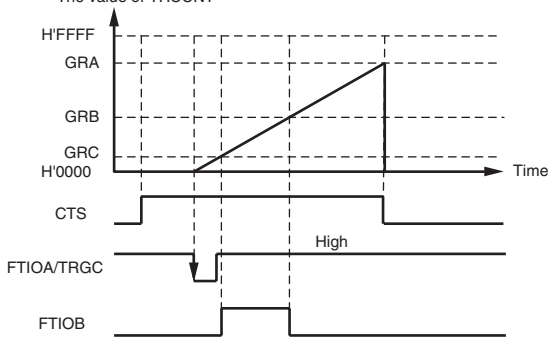


Figure 13.21 Example (2) of Output Operation of One-Shot Pulse Waveform in PWM2 Mode

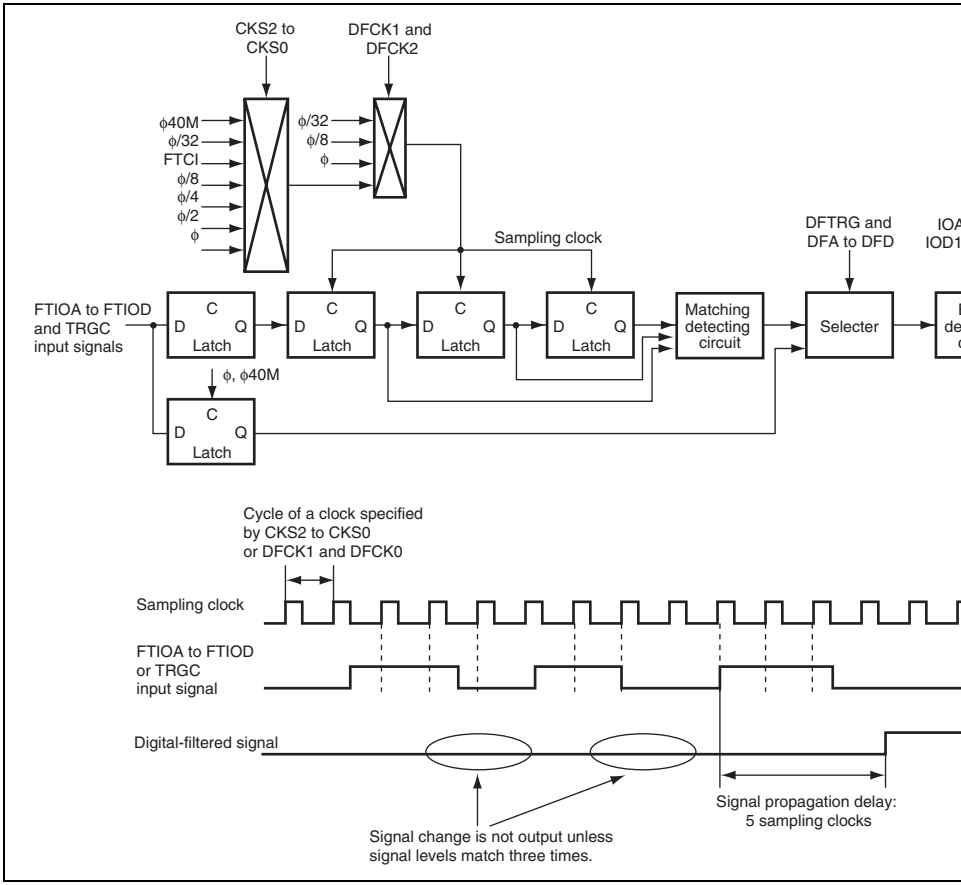


Figure 13.22 Block Diagram of Digital Filter

Figure 13.23 Count Timing for Internal Clock Source

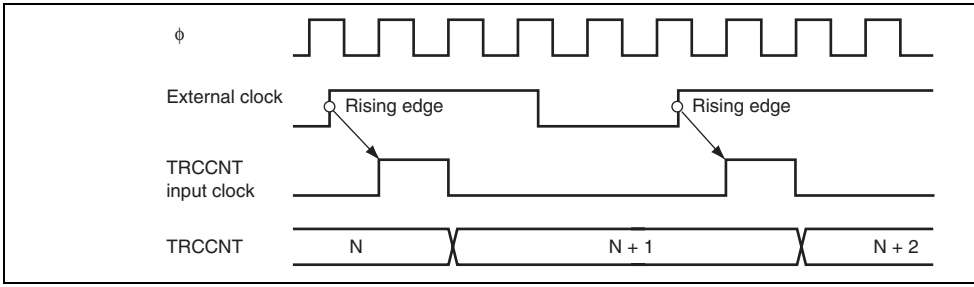


Figure 13.24 Count Timing for External Clock Source

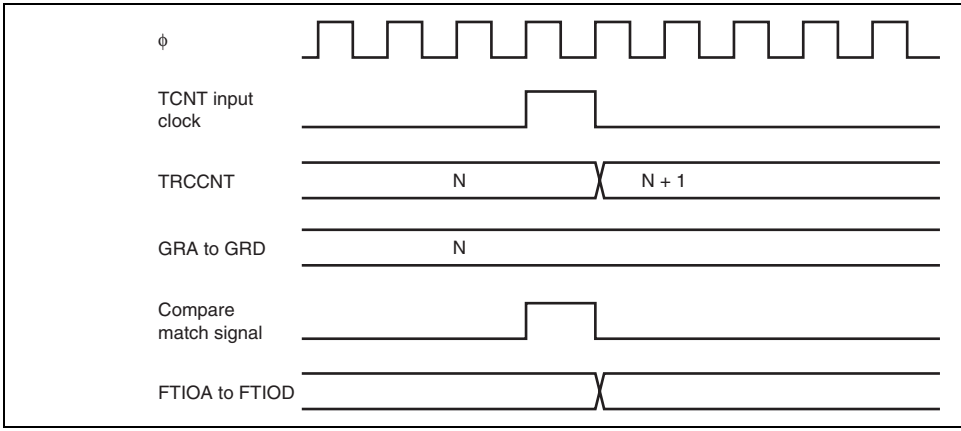


Figure 13.25 Output Compare Output Timing

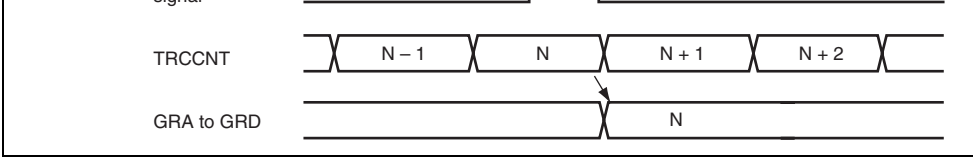


Figure 13.26 Input Capture Input Signal Timing

13.5.4 Timing of Counter Clearing by Compare Match

Figure 13.27 shows the timing when the counter is cleared by compare match A. When th value is N, the counter counts from 0 to N, and its cycle is N + 1.

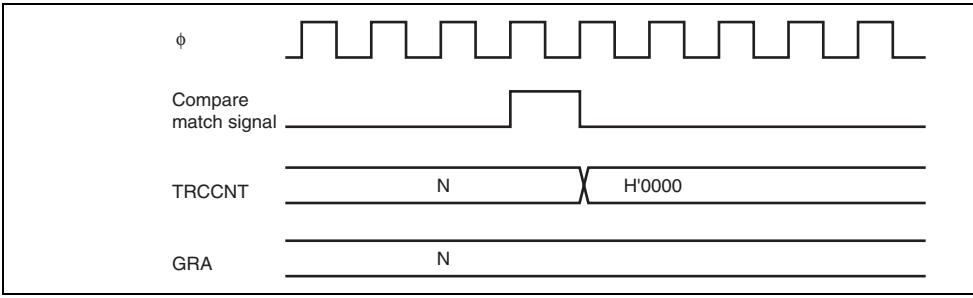


Figure 13.27 Timing of Counter Clearing by Compare Match

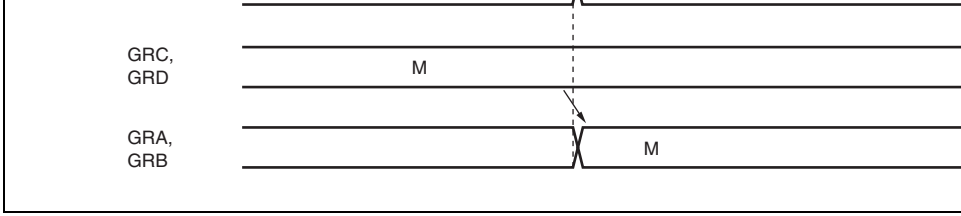


Figure 13.28 Buffer Operation Timing (Compare Match)

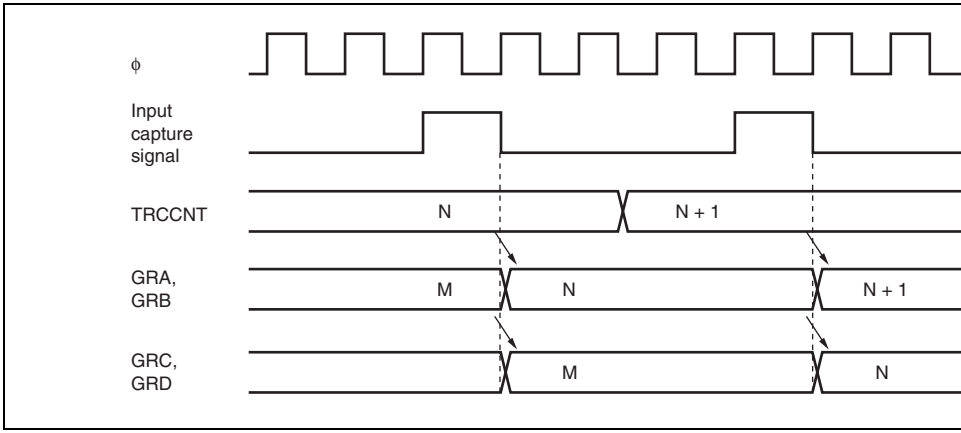


Figure 13.29 Buffer Operation Timing (Input Capture)

Figure 13.30 shows the timing of the IMFA to IMFD flag setting at compare match.

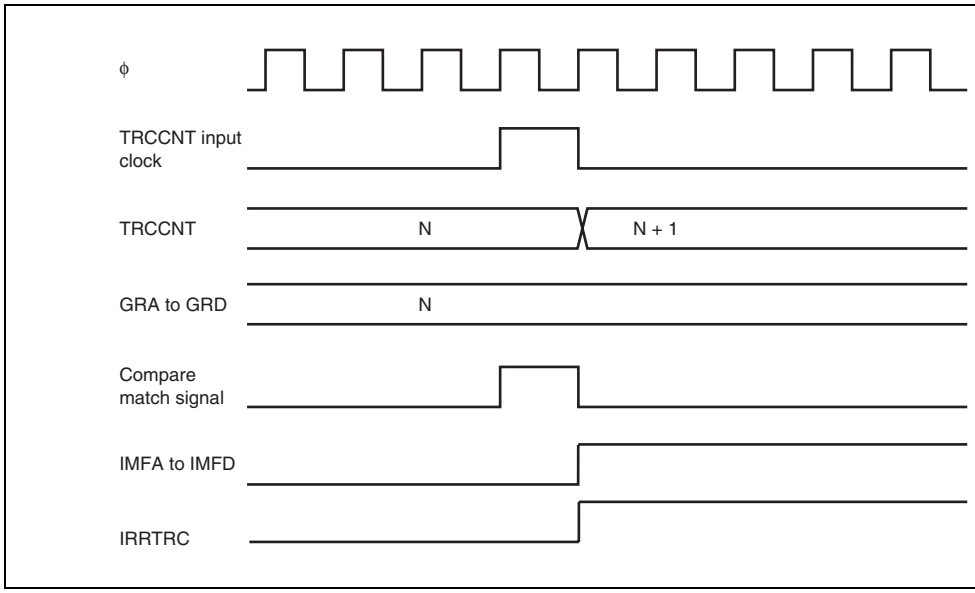


Figure 13.30 Timing of IMFA to IMFD Flag Setting at Compare Match

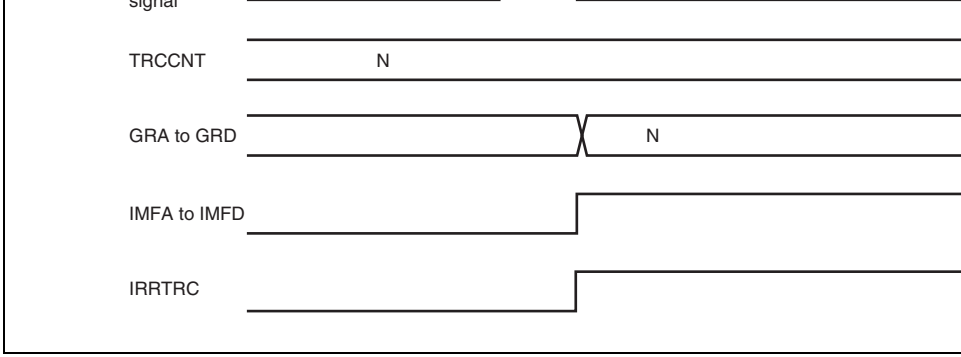


Figure 13.31 Timing of IMFA to IMFD Flag Setting at Input Capture

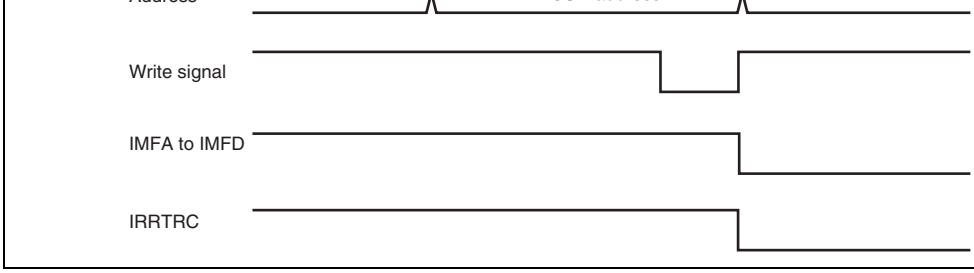


Figure 13.32 Timing of Status Flag Clearing by CPU

takes priority and the write is not performed, as shown in figure 13.33. If counting-u
generated in the TRCCNT write cycle to contend with the TRCCNT counting-up, w
takes precedence.

3. TRCCNT may erroneously count up when switching internal clocks. TRCCNT coun
rising edge of the divided system clock (ϕ) when the internal clock is selected. If clo
switched as shown in figure 13.34, the change from the low level of the previous clo
high level of the new clock is considered as the rising edge. In this case, TRCCNT c
erroneously.
4. If timer RC enters the module standby mode while an interrupt is being requested, th
request cannot be cleared. Before entering the module standby mode, disable interru
requests.

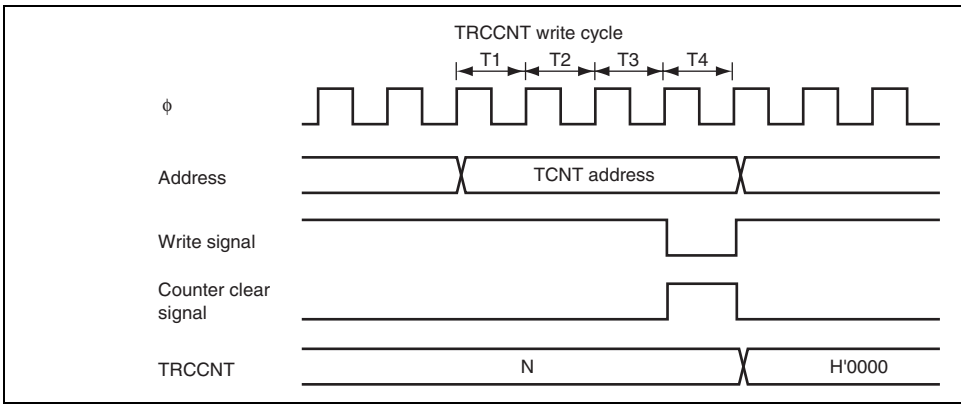


Figure 13.33 Contention between TRCCNT Write and Clear

Figure 13.34 Internal Clock Switching and TRCCNT Operation

5. The TOA to TOD bits in TRCCR1 decide the value of the FTIO pin, which is output first compare match occurs. Once a compare match occurs and this compare match ch values of FTIOA to FTIOD output, the values of the FTIOA to FTIOD pin output and values read from the TOA to TOD bits may differ. Moreover, when the writing to TR and the generation of the compare match A to D occur at the same timing, the writing TRCCR1 has the priority. Thus, output change due to the compare match is not reflec FTIOA to FTIOD pins. Therefore, when bit manipulation instruction is used to write t TRCCR1, the values of the FTIOA to FTIOD pin output may result in an unexpected When TRCCR1 is to be written to while compare match is operating, stop the counter before accessing to TRCCR1, read the port 8 state to reflect the values of FTIOA to F output, to TOA to TOD, and then restart the counter. Figure 13.35 shows an example compare match and the bit manipulation instruction to TRCCR1 occur at the same tim

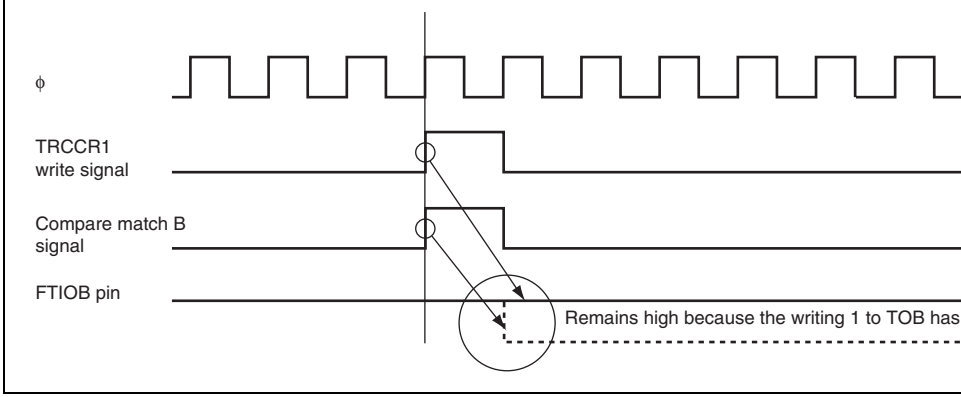


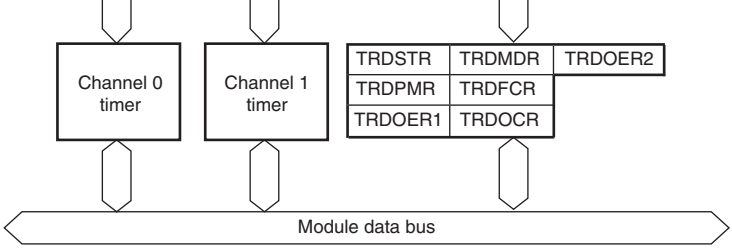
Figure 13.35 When Compare Match and Bit Manipulation Instruction to TR Occur at the Same Timing

14.1 Features

- Capability to process up to eight inputs/outputs 0
- Eight general registers (GR): four registers for each channel
  — Independently assignable output compare or input capture functions
- Selection of seven counter clock sources: six internal clocks (ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/32, a
  which is a 40-MHz/32-MHz clock derived from the on-chip oscillator) and an extern
- Seven selectable operating modes
  — Timer mode
    Output compare function (Selection of 0 output, 1 output, or toggle output)
    Input capture function (Rising edge, falling edge, or both edges)
  — Synchronous operation
    Timer counters_0 and _1 (TRDCNT_0 and TRDCNT_1) can be written simultan
    Simultaneous clearing by compare match or input capture is possible.
  — PWM mode
    Up to six-phase PWM output can be provided with desired duty ratio.
  — PWM3 mode
    One-phase PWM output for non-overlapped normal and counter phases
  — Reset synchronous PWM mode
    Three-phase PWM output for normal and counter phases
  — Complementary PWM mode
    Three-phase PWM output for non-overlapped normal and counter phases
    The A/D conversion start trigger can be set for PWM cycles.
  — Buffer operation
    The input capture register can be consisted of double buffers.
    The output compare register can automatically be modified.

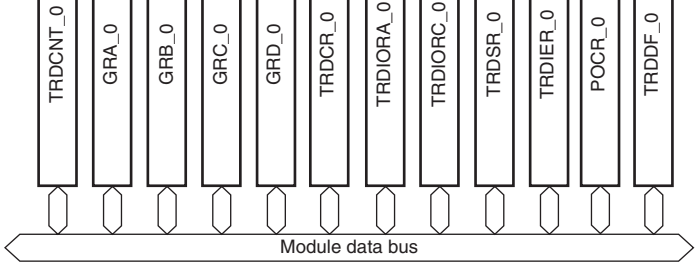
Counter clearing function		Compare match/input capture of GRA_0, GRB_0, GRC_0, or GRD_0	Compare match/input ca GRA_1, GRB_1, GRC_1 GRD_1
Compare match output	0 output	Yes	Yes
	1 output	Yes	Yes
	output	Yes	Yes
Input capture function		Yes	Yes
Synchronous operation		Yes	Yes
PWM mode		Yes	Yes
PWM3 mode		Yes	Yes
Reset synchronous PWM mode		Yes	Yes
Complementary PWM mode		Yes	Yes
Buffer function		Yes	Yes
Interrupt sources		Compare match/ input capture A0 to D0 Overflow	Compare match/ input capture A1 to D1 Overflow Underflow

		FTIOD1
	Shared by channels 0 and 1	$\overline{\text{TRDOI\_0}}$
Timer RD_1	2	FTIOA2
		FTIOB2
		FTIOC2
		FTIOD2
	3	FTIOA3
		FTIOB3
		FTIOC3
		FTIOD3
	Shared by channels 2 and 3	$\overline{\text{TRDOI\_1}}$



[Legend]
TRDSTR: Timer RD start register (8 bits)
TRDMDR: Timer RD mode register (8 bits)
TRDPMR: Timer RD PWM mode register (8 bits)
TRDFCR: Timer RD function control register (8 bits)
TRDOER1: Timer RD output master enable register 1 (8 bits)
TRDOER2: Timer RD output master enable register 2 (8 bits)
TRDOCR: Timer RD output control register (8 bits)
$\overline{\text{ADTRG}}$: A/D conversion start trigger output signal
ITMRD0: Channel 0 interrupt
ITMRD1: Channel 1 interrupt

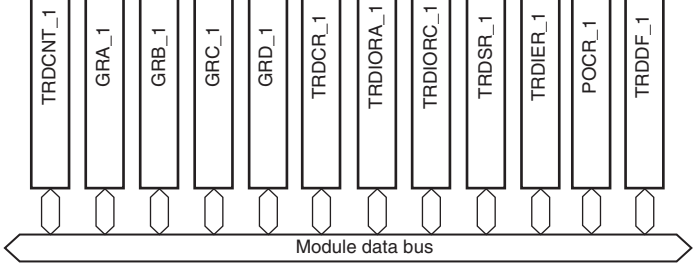
Figure 14.1 Timer RD Block Diagram



[Legend]

TRDCNT_0:	Timer RD counter_0 (16 bits)
GRA_0, GRB_0, GRC_0, GRD_0:	General registers A_0, B_0, C_0, and D_0 (input capture/output compare registers: 16 bits × 4)
TRDCR_0:	Timer RD control register_0 (8 bits)
TRDIORA_0:	Timer RD I/O control register A_0 (8 bits)
TRDIORC_0:	Timer RD I/O control register C_0 (8 bits)
TRDSR_0:	Timer RD status register_0 (8 bits)
TRDIER_0:	Timer RD interrupt enable register_0 (8 bits)
POCR_0:	PWM mode output level control register_0 (8 bits)
TRDDF_0:	Timer RD digital filtering function select register_0 (8 bits)
ITMRD0:	Channel 0 interrupt

Figure 14.2 Timer RD (Channel 0) Block Diagram



[Legend]

TRDCNT_1	Timer RD counter_1 (16 bits)
GRA_1, GRB_1, GRC_1, GRD_1:	General registers A_1, B_1, C_1, and D_1 (input capture/output compare registers: 16 bits × 4)
TRDCR_1:	Timer RD control register_1 (8 bits)
TRDIORA_1:	Timer RD I/O control register A_1 (8 bits)
TRDIORC_1:	Timer RD I/O control register C_1 (8 bits)
TRDSR_1:	Timer RD status register_1 (8 bits)
TRDIER_1:	Timer RD interrupt enable register_1 (8 bits)
POCR_1:	PWM mode output level control register_1 (8 bits)
TRDDF_1:	Timer RD digital filtering function select register_1 (8 bits)
ITMRD1:	Channel 1 interrupt

Figure 14.3 Timer RD (Channel 1) Block Diagram

output compare B0			input capture input, or PWM ou
Input capture/ output compare C0	FTIOC0	Input/output	GRC_0 output compare output input capture input, or PWM synchronous output (in reset synchronous PWM and comple PWM modes)
Input capture/ output compare D0	FTIOD0	Input/output	GRD_0 output compare output input capture input, or PWM ou
Input capture/ output compare A1	FTIOA1	Input/output	GRA_1 output compare output input capture input, or PWM ou reset synchronous PWM and complementary PWM modes)
Input capture/ output compare B1	FTIOB1	Input/output	GRB_1 output compare output input capture input, or PWM ou
Input capture/ output compare C1	FTIOC1	Input/output	GRC_1 output compare output input capture input, or PWM ou
Input capture/ output compare D1	FTIOD1	Input/output	GRD_1 output compare output input capture input, or PWM ou
Timer output control	$\overline{\text{TRDOI}}$	Input	Input pin for timer output disab signal

- Timer RD output master enable register 2 (TRDOER2)
- Timer RD output control register (TRDOCR)

Channel 0

- Timer RD control register_0 (TRDCR_0)
- Timer RD I/O control register A_0 (TRDIORA_0)
- Timer RD I/O control register C_0 (TRDIORC_0)
- Timer RD status register_0 (TRDSR_0)
- Timer RD interrupt enable register_0 (TRDIER_0)
- PWM mode output level control register_0 (POCR_0)
- Timer RD digital filtering function select register_0 (TRDDF_0)
- Timer RD counter_0 (TRDCNT_0)
- General register A_0 (GRA_0)
- General register B_0 (GRB_0)
- General register C_0 (GRC_0)
- General register D_0 (GRD_0)

Channel 1

- Timer RD control register_1 (TRDCR_1)
- Timer RD I/O control register A_1 (TRDIORA_1)
- Timer RD I/O control register C_1 (TRDIORC_1)
- Timer RD status register_1 (TRDSR_1)
- Timer RD interrupt enable register_1 (TRDIER_1)
- PWM mode output level control register_1 (POCR_1)
- Timer RD digital filtering function select register_1 (TRDDF_1)

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1, and cannot b modified.
3	CSTPN1	1	R/W	Channel 1 Counter Stop 0: Counting is stopped on a compare match of TRDCNT_1 and GRA_1 1: Counting is continued on a compare match TRDCNT_1 and GRA_1 Set this bit to 1 to restart counting after the cou been stopped on a compare match.
2	CSTPN0	1	R/W	Channel 0 Counter Stop 0: Counting is stopped on a compare match of TRDCNT_0 and GRA_0 1: Counting is continued on a compare match TRDCNT_0 and GRA_0 Set this bit to 1 to restart counting after the cou been stopped on a compare match.

				while CSTPN1 = 0
0	STR0	0	R/W	Channel 0 Counter Start TRDCNT_0 stops counting when this bit is 0, performs counting when this bit is 1. [Setting condition] • When 1 is written in STR0 [Clearing conditions] • When 0 is written in STR0 while CSTPN0 • When the compare match A0 signal is ge while CSTPN0 = 0

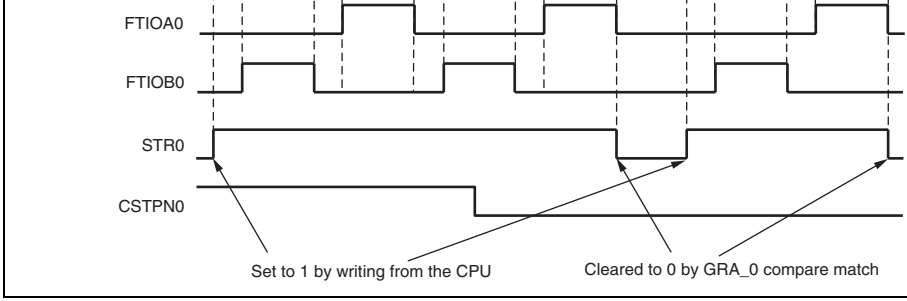


Figure 14.4 Example (1) of Stopping Operation of the Counter (in PWM3 Mo

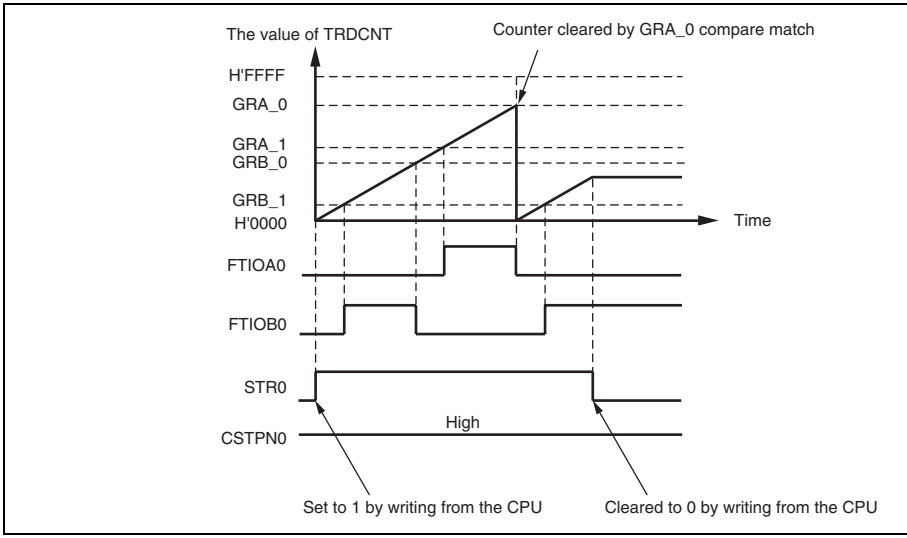


Figure 14.5 Example (2) of Stopping Operation of the Counter (in PWM3 Mo

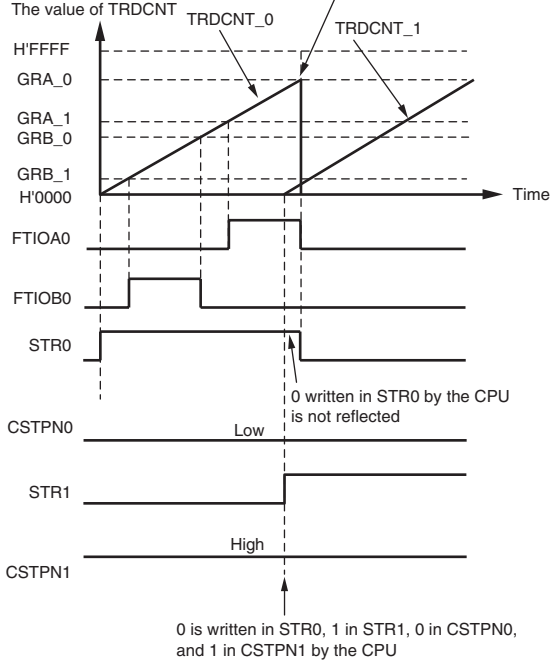


Figure 14.6 Example of Starting and Stopping Operations of Counters (in PWM

6	BFC1	0	R/W	Buffer Operation C1 0: GRC_1 operates normally 1: GRA_1 and GRD_1 are used together for bu operation
5	BFD0	0	R/W	Buffer Operation D0 0: GRD_0 operates normally 1: GRB_0 and GRD_0 are used together for bu operation
4	BFC0	0	R/W	Buffer Operation C0 0: GRC_0 operates normally 1: GRA_0 and GRC_0 are used together for bu operation
3 to 1	—	All 1	—	Reserved These bits are always read as 1, and cannot b modified.
0	SYNC	0	R/W	Timer Synchronization 0: TRDCNT_1 and TRDCNT_0 operate as ind timer counters 1: TRDCNT_1 and TRDCNT_0 operate synchr TRDCNT_1 and TRDCNT_0 can be pre-set cleared synchronously

				1: FTIOD1 operates in PWM mode
5	PWMC1	0	R/W	PWM Mode C1 0: FTIOC1 operates normally 1: FTIOC1 operates in PWM mode
4	PWMB1	0	R/W	PWM Mode B1 0: FTIOB1 operates normally 1: FTIOB1 operates in PWM mode
3	—	1	—	Reserved This bit is always read as 1, and cannot be m
2	PWMD0	0	R/W	PWM Mode D0 0: FTIOD0 operates normally 1: FTIOD0 operates in PWM mode
1	PWMC0	0	R/W	PWM Mode C0 0: FTIOC0 operates normally 1: FTIOC0 operates in PWM mode
0	PWMB0	0	R/W	PWM Mode B0 0: FTIOB0 operates normally 1: FTIOB0 operates in PWM mode

				This bit is valid when both bits CMD1 and CMD cleared to 0. When PWM3 mode is selected, T TRDIORA, and TRDIORC are invalid.
6	STCLK	0	R/W	External Clock Input Select 0: External clock input is disabled 1: External clock input is enabled
5	ADEG	0	R/W	A/D Trigger Edge Select The A/D converter registers should be set so th conversion is started by an external trigger. 0: The A/D trigger signal is asserted when TRD matches GRA_0 in complementary PWM m 1: The A/D trigger signal is asserted when TRD underflows in complementary PWM mode
4	ADTRG	0	R/W	External Trigger Disable 0: A/D trigger for PWM cycles is disabled in complementary PWM mode 1: A/D trigger for PWM cycles is enabled in complementary PWM mode
3	OLS1	0	R/W	Output Level Select 1 Selects the counter-phase output levels in rese synchronous PWM mode or complementary PW mode. 0: Initial output is high and the active level is lo 1: Initial output is low and the active level is hig

1	CMD1	0	R/W	Combination Mode 1 and 0
0	CMD0	0	R/W	00: Channel 0 and channel 1 operate normall 01: Channel 0 and channel 1 are used togeth operate in reset synchronous PWM mode 10: Channel 0 and channel 1 are used togeth operate in complementary PWM mode (tr when TRDCNT_0 matches GRA_0) 11: Channel 0 and channel 1 are used togeth operate in complementary PWM mode (tr when TRDCNT_1 underflows) Note: When the reset synchronous PWM mod complementary PWM mode is selected bits, this setting has the priority to the s PWM mode by each bit in TRDPMR. St TRDCNT_0 and TRDCNT_1 before ma settings for reset synchronous PWM mo complementary PWM mode.

Reset synchronous PWM mode

Complementary PWM mode

Note: Write H'00 to TOCR to start initial outputs after stopping the counter.

Figure 14.7 Example of Outputs in Reset Synchronous PWM Mode and Complementary PWM Mode

14.3.5 Timer RD Output Master Enable Register 1 (TRDOER1)

TRDOER1 enables/disables the outputs for channel 0 and channel 1. When $\overline{\text{TRDOI}}$ is sel inputs, if a low level signal is input to $\overline{\text{TRDOI}}$, the bits in TRDOER1 are set to 1 to disab output for timer RD.

Bit	Bit Name	Initial Value	R/W	Description
7	ED1	1	R/W	Master Enable D1 0: FTIOD1 pin output is enabled according to t TRDPMR, TRDFCR, and TRDIORC_1 setti 1: FTIOD1 pin output is disabled regardless of TRDMR, TRDFCR, and TRDIORC_1 setting (FTIOD1 pin is operated as an I/O port).
6	EC1	1	R/W	Master Enable C1 0: FTIOC1 pin output is enabled according to t TRDPMR, TRDFCR, and TRDIORC_1 setti 1: FTIOC1 pin output is disabled regardless of TRDPMR, TRDFCR, and TRDIORC_1 setti (FTIOC1 pin is operated as an I/O port).

				1: FTIOA1 pin output is disabled regardless o TRDPMR, TRDFCR, and TRDIORA_1 sett (FTIOA1 pin is operated as an I/O port).
3	ED0	1	R/W	Master Enable D0 0: FTIOD0 pin output is enabled according to TRDPMR, TRDFCR, and TRDIORC_0 sett 1: FTIOD0 pin output is disabled regardless o TRDPMR, TRDFCR, and TRDIORC_0 sett (FTIOD0 pin is operated as an I/O port).
2	EC0	1	R/W	Master Enable C0 0: FTIOC0 pin output is enabled according to TRDPMR, TRDFCR, and TRDIORC_0 sett 1: FTIOC0 pin output is disabled regardless o TRDPMR, TRDFCR, and TRDIORC_0 sett (FTIOC0 pin is operated as an I/O port).
1	EB0	1	R/W	Master Enable B0 0: FTIOB0 pin output is enabled according to TRDPMR, TRDFCR, and TRDIORA_0 sett 1: FTIOB0 pin output is disabled regardless o TRDPMR, TRDFCR, and TRDIORA_0 sett (FTIOB0 pin is operated as an I/O port).
0	EA0	1	R/W	Master Enable A0 0: FTIOA0 pin output is enabled according to TRDPMR, TRDFCR, and TRDIORA_0 sett 1: FTIOA0 pin output is disabled regardless o TRDPMR, TRDFCR, and TRDIORA_0 sett (FTIOA0 pin is operated as an I/O port).

6 to 0	—	All 1	—	Reserved These bits are always read as 1.

14.3.7 Timer RD Output Control Register (TRDOCR)

TRDOCR selects the initial outputs before the first occurrence of a compare match. Note
OLS1 and OLS0 in TRDFCR set these initial outputs in reset synchronous PWM mode a
complementary PWM mode.

In PWM3 mode, TRDOCR selects the output level on the FTIOB0 pin.

Bit	Bit Name	Initial Value	R/W	Description
7	TOD1	0	R/W	Output Level Select D1 0: 0 output at the FTIOD1 pin* 1: 1 output at the FTIOD1 pin*
6	TOC1	0	R/W	Output Level Select C1 0: 0 output at the FTIOC1 pin* 1: 1 output at the FTIOC1 pin*
5	TOB1	0	R/W	Output Level Select B1 0: 0 output at the FTIOB1 pin* 1: 1 output at the FTIOB1 pin*

				1: 1 output at the FTIOC0 pin*
1	TOB0	0	R/W	Output Level Select B0 • In modes other than PWM3 mode 0: 0 output at the FTIOB0 pin* 1: 1 output at the FTIOB0 pin* • In PWM3 mode 0: 1 output at the FTIOB0 pin on GRB_1 com match and 0 output at the FTIOB0 pin on G compare match 1: 0 output at the FTIOB0 pin on GRB_1 com match and 1 output at the FTIOB0 pin on G compare match
0	TOA0	0	R/W	Output Level Select A0 • In modes other than PWM3 mode 0: 0 output at the FTIOA0 pin* 1: 1 output at the FTIOA0 pin* • In PWM3 mode 0: 1 output at the FTIOB0 pin on GRA_1 com match and 0 output at the FTIOB0 pin on G compare match 1: 0 output at the FTIOB0 pin on GRA_1 com match and 1 output at the FTIOB0 pin on G compare match

Note: * The change of the setting is immediately reflected in the output value.

set to 1. When TRDCNT_1 underflows, an UDF flag in TRDSR is set to 1. The TRDCNT counters cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit. TRDCNT is initialized to H'0000 by a reset.

14.3.9 General Registers A, B, C, and D (GRA, GRB, GRC, and GRD)

GR are 16-bit registers. Timer RD has eight general registers (GR), four for each channel registers are dual function 16-bit readable/writable registers, functioning as either output or input capture registers. Functions can be switched by TRDIORA and TRDIORC.

The values in GR and TRDCNT are constantly compared with each other when the GR re are used as output compare registers. When the both values match, the IMFA to IMFD fla TSR are set to 1. Compare match outputs can be selected by TRDIORA and TRDIORC.

When the GR registers are used as input capture registers, the TRDCNT value is stored a detecting external signals. At this point, IMFA to IMFD flags in the corresponding TRDS to 1. Detection edges for input capture signals can be selected by TRDIORA and TRDIO

When PWM mode, complementary PWM mode, or reset synchronous PWM mode is sele values in TRDIORA and TRDIORC are ignored. Upon reset, the GR registers are set as c compare registers (no output) and initialized to H'FFFF. The GR registers cannot be acce bit units; they must always be accessed as a 16-bit unit.

				010: Clears TRDCNT by GRB compare matc capture*1
				011: Synchronization clear; Clears TRDCNT i synchronous with counter clearing of the channel's timer*2
				100: Disables TRDCNT clearing
				101: Clears TRDCNT by GRC compare matc capture*1
				110: Clears TRDCNT by GRD compare matc capture*1
				111: Synchronization clear; Clears TRDCNT i synchronous with counter clearing of the channel's timer*2
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	00: Count at rising edge
				01: Count at falling edge
				1X: Count at both edges

111: Reserved (setting prohibited)

Notes: 1. When selecting the internal clock ϕ, subclock is counted in subactive an subsleep modes.

2. When selecting the internal clock ϕ4 chip oscillator should be in operatio switching the clock, the counter sho halted.

[Legend] X: Don't care

Notes: 1. When GR functions as an output compare register, TRDCNT is cleared by co match. When GR functions as input capture, TRDCNT is cleared by input capt

2. Synchronous operation is set by TRDMDR.

TRDIORA also selects the function of FTIOA or FTIOB pin.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved This bit is always read as 1.
6	IOB2	0	R/W	I/O Control B2 Selects the GRB function. 0: GRB functions as an output compare regis 1: GRB functions as an input capture register
5	IOB1	0	R/W	I/O Control B1 and B0
4	IOB0	0	R/W	When IOB2 = 0, 00: No output at compare match 01: 0 output to the FTIOB pin at GRB compar 10: 1 output to the FTIOB pin at GRB compar 11: Output toggles to the FTIOB pin at GRB c match When IOB2 = 1, 00: Input capture to GRB at rising edge at the pin 01: Input capture to GRB at falling edge at the pin 1X: Input capture to GRB at rising and falling the FTIOB pin

00: No output at compare match

01: 0 output to the FTIOA pin at GRA compare

10: 1 output to the FTIOA pin at GRA compare

11: Output toggles to the FTIOA pin at GRA co match

When IOA2 = 1,

00: Input capture to GRA at rising edge at the pin

01: Input capture to GRA at falling edge at the pin

1X: Input capture to GRA at rising and falling e the FTIOA pin

[Legend]

X: Don't care.

Note: When a GR register functions as a buffer register for a paired GR register, the sett the IOA2 and IOB2 bits in TRDIORA and the IOC2 and IOD2 bits in TRDIORC of b registers should be the same.

				0: GRD is used as GR for the FTIOB pin
				1: GRD is used as GR for the FTIOD pin
6	IOD2	0	R/W	I/O Control D2 Selects the GRD function. 0: GRD functions as an output compare regis 1: GRD functions as an input capture register
5	IOD1	0	R/W	I/O Control D1 and D0
4	IOD0	0	R/W	When IOD3 = 0, 00: No output at compare match 01: 0 output to the FTIOB pin at GRD compar 10: 1 output to the FTIOB pin at GRD compar 11: Output toggles to the FTIOB pin at GRD c match When IOD3 = 1 and IOD2 = 0, 00: No output at compare match 01: 0 output to the FTIOD pin at GRD compar 10: 1 output to the FTIOD pin at GRD compar 11: Output toggles to the FTIOD pin at GRD c match When IOD3 = 1 and IOD2 = 1, 00: Input capture to GRD at rising edge at the pin 01: Input capture to GRD at falling edge at the pin 1X: Input capture to GRD at rising and falling the FTIOD pin

				1: GRC functions as an input capture register
1	IOC1	0	R/W	I/O Control C1 and C0
0	IOC0	0	R/W	When IOC3 = 0, 00: No output at compare match 01: 0 output to the FTIOA pin at GRC compare 10: 1 output to the FTIOA pin at GRC compare 11: Output toggles to the FTIOA pin at GRC co match When IOC3 = 1 and IOC2 = 0, 00: No output at compare match 01: 0 output to the FTIOC pin at GRC compare 10: 1 output to the FTIOC pin at GRC compare 11: Output toggles to the FTIOC pin at GRC co match When IOC3 = 1 and IOC2 = 1, 00: Input capture to GRC at rising edge at the pin 01: Input capture to GRC at falling edge at the pin 1X: Input capture to GRC at rising and falling e the FTIOC pin

[Legend]

X: Don't care.

Note: When a GR register functions as a buffer register for a paired GR register, the sett the IOA2 and IOB2 bits in TRDIORA and the IOC2 and IOD2 bits in TRDIORC of b registers should be the same.

				These bits are always read as 1.
5	UDF*	0	R/W	Underflow Flag [Setting condition] • When TRDCNT_1 underflows [Clearing condition] • When 0 is written to UDF after reading UD
4	OVF	0	R/W	Overflow Flag [Setting condition] • When the TRDCNT value underflows [Clearing condition] • When 0 is written to OVF after reading OV
3	IMFD	0	R/W	Input Capture/Compare Match Flag D [Setting conditions] • When TRDCNT = GRD and GRD is functi output compare register • When TRDCNT = GRD while the FTIOD p operates in PWM mode • When TRDCNT = GRD in PWM3 mode, r synchronous PWM mode, or complement mode • When TRDCNT value is transferred to GR capture signal and GRD is functioning as capture register [Clearing condition] • When 0 is written to IMFD after reading IM

				mode • When TRDCNT value is transferred to GRC capture signal and GRC is functioning as in capture register [Clearing condition] • When 0 is written to IMFC after reading IMF
1	IMFB	0	R/W	Input Capture/Compare Match Flag B [Setting conditions] • When TRDCNT = GRB and GRB is functio output compare register • When TRDCNT = GRB while the FTIOB pi operates in PWM mode • When TRDCNT = GRB in PWM mode, PW mode, reset synchronous PWM mode, or complementary PWM mode (in reset synch PWM mode, however, while TRDCNT_0 = and TRDCNT_0 = GRB_0) • When TRDCNT value is transferred to GRB capture signal and GRB is functioning as in capture register [Clearing condition] • When 0 is written to IMFB after reading IMF

and TRDCNT_0 = GRA_0)

- When TRDCNT value is transferred to GR
  capture signal and GRA is functioning as
  capture register

[Clearing condition]

- When 0 is written to IMFA after reading IM

Note: Bit 5 is not the UDF flag in TRDSR_0. It is a reserved bit. It is always read as 1.

				0: Interrupt requests (OVI) by OVF or UDF flag disabled
				1: Interrupt requests (OVI) by OVF or UDF flag enabled
3	IMIED	0	R/W	Input Capture/Compare Match Interrupt Enable
				0: Interrupt requests (IMID) by IMFD flag are d
				1: Interrupt requests (IMID) by IMFD flag are e
2	IMIEC	0	R/W	Input Capture/Compare Match Interrupt Enable
				0: Interrupt requests (IMIC) by IMFC flag are d
				1: Interrupt requests (IMIC) by IMFC flag are e
1	IMIEB	0	R/W	Input Capture/Compare Match Interrupt Enable
				0: Interrupt requests (IMIB) by IMFB flag are di
				1: Interrupt requests (IMIB) by IMFB flag are en
0	IMIEA	0	R/W	Input Capture/Compare Match Interrupt Enable
				0: Interrupt requests (IMIA) by IMFA flag are di
				1: Interrupt requests (IMIA) by IMFA flag are en

				0: The output level of FTIOD is low-active 1: The output level of FTIOD is high-active
1	POLC	0	R/W	PWM Mode Output Level Control C 0: The output level of FTIOC is low-active 1: The output level of FTIOC is high-active
0	POLB	0	R/W	PWM Mode Output Level Control B 0: The output level of FTIOB is low-active 1: The output level of FTIOB is high-active

6	DFCK0	0	R/W	filter. 00: ϕ/32 01: ϕ/8 10: ϕ 11: Clock specified by bits TPSC2 to TPSC0 in
5	—	0	—	Reserved
4	—	0	—	These bits are always read as 0.
3	DFD	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter
2	DFC	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter
1	DFB	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter
0	DFA	0	R/W	Enables or disables the digital filter for the FTI 0: Disables the digital filter 1: Enables the digital filter

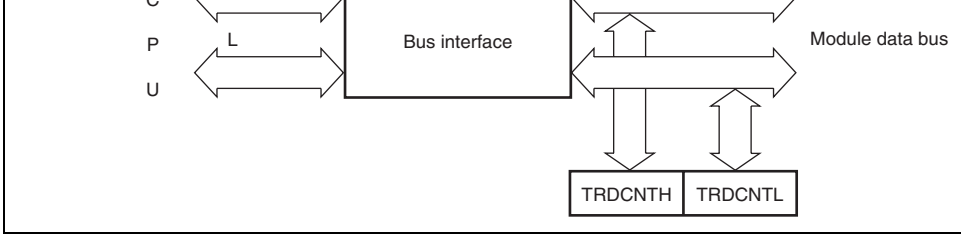


Figure 14.8 Accessing Operation of 16-Bit Register (between CPU and TRDCNT

(2) 8-Bit Register

Registers other than TRDCNT and GR are 8-bit registers that are connected internally w
CPU in an 8-bit width. Figure 14.9 shows an example of accessing the 8-bit registers.

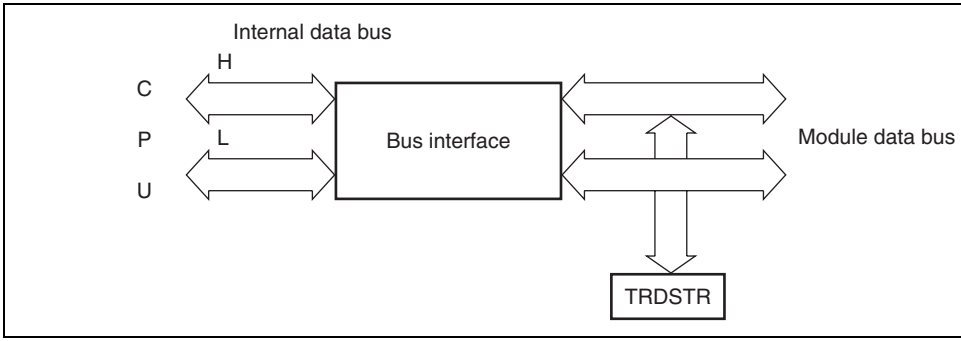


Figure 14.9 Accessing Operation of 8-Bit Register (between CPU and TRDSTR

— Enables PWM3 mode operation by setting the PWM3 bit in TRDFCR

- Reset synchronous PWM mode operation
  — Enables reset synchronous PWM mode operation by setting the CMD1 and CMD0
  TRDFCR
- Complementary PWM mode operation
  — Enables complementary PWM mode operation by setting the CMD1 and CMD0 b
  TRDFCR

The FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pins indicate the timer operation mode
register setting.

- FTIOA0 pin

Register Name	TRDOER1		TRCMR		TRDIORA	
Bit Name	**EA0**	**STCLK**	**CMD1, CMD0**	**PWM3**	**IOA2 to IOA0**	**Function**
Setting values	0	0	00	0	XXX	PWM3 mode wavef
	0	0	00	1	001, 01X	Timer mode wavefo (output compare fu
	0	1	XX	1	1XX	Timer mode (input c function)
	1					
	Other than above					General I/O port

[Legend]
X: Don't care.

					out
0	00	1	1	XXX	PWM mode wa
0	00	1	0	001, 01X	Timer mode wa output (output function)
0	00	1	0	1XX	Timer mode (in function)
1					
		Other than above			General I/O po

[Legend]

X: Don't care.

0	00	1	0	001, 01X	Timer mode wa output (output c function)
0	00	1	0	1XX	Timer mode (inp function)
1					
Other than above					General I/O port

[Legend]

X: Don't care.

	0	00	1	0	001, 01X	Timer mode wa output (output function)
	0	00	1	0	1XX	Timer mode (in function)
	1					
	Other than above					General I/O po

[Legend]

X: Don't care.

- FTIOA1 pin

Register Name	TRDOER1	TRDFCR		TRDIORA	
Bit Name	**EA1**	**CMD1, CMD0**	**PWM3**	**IOA2 to IOA0**	**Function**
Setting values	0	10, 11	X	XXX	Complementary PWM mode output
	0	01	X	XXX	Reset synchronous PWM mo output
	0	00	1	001, 01X	Timer mode waveform output compare function)
	0	00	1	1XX	Timer mode (input capture fu
	1				
	Other than above				General I/O port

[Legend]

X: Don't care.

	0	00	1	0	001, 01X	Timer mode wave (output compare f
	0	00	1	0	1XX	Timer mode (inpu function)
	1					
	Other than above					General I/O port

[Legend]
X: Don't care.

- FTIOC1 pin

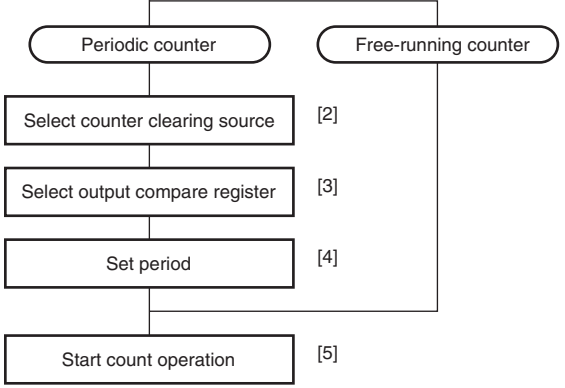
Register Name	TRDOER1	TRDFCR		TRDPMR	TRDIORC	
Bit Name	EC1	CMD1, CMD0	PWM3	PWMC1	IOC2 to IOC0	Function
Setting values	0	10, 11	X	X	XXX	Complementary P waveform output
	0	01	X	X	XXX	Reset synchronou mode waveform o
	0	00	1	1	XXX	PWM mode wave
	0	00	1	0	001, 01X	Timer mode wave (output compare f
	0	00	1	0	1XX	Timer mode (inpu function)
	1					
	Other than above					General I/O port

[Legend]
X: Don't care.

0	00	1	0	001, 01X	Timer mode wav (output compare
0	00	1	0	1XX	Timer mode (inp function)
1					
Other than above					General I/O port

[Legend]

X: Don't care.



[2] For periodic counter operation, se
the TRDCNT clearing source with
CCLR2 to CCLR0 in TRDCR.
[3] Designate the general register
selected in [2] as an output compa
register by means of TRDIOR.
[4] Set the periodic counter cycle in t
general register selected in [2].
[5] Set the STR bit in TRDSTR to 1 t
start the counter operation.

Figure 14.10 Example of Counter Operation Setting Procedure

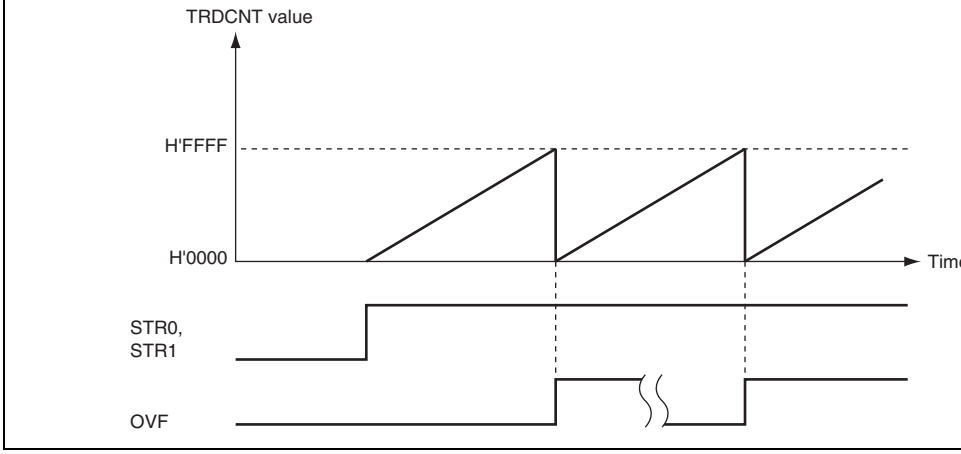


Figure 14.11 Free-Running Counter Operation

When compare match is selected as the TRDCNT clearing source, the TRDCNT counte
relevant channel performs periodic count operation. The GR registers for setting the per
designated as output compare registers, and counter clearing by compare match is select
means of bits CCLR1 and CCLR0 in TRDCR. After the settings have been made, TRDC
an increment operation as a periodic counter when the corresponding bit in TRDSTR is
When the count value matches the value in GR, the IMFA, IMFB, IMFC, or IMFD flag
is set to 1 and TRDCNT is cleared to H'0000.

If the value of the corresponding IMIEA, IMIEB, IMIEC, or IMIED bit in TRDIER is 1
point, timer RD requests an interrupt. After a compare match, TRDCNT starts an increm
operation again from H'0000.

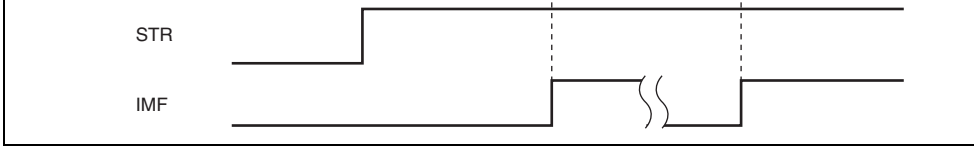


Figure 14.12 Periodic Counter Operation

(2) TRDCNT Count Timing

- Internal clock operation

  A system clock (ϕ), four types of clocks (ϕ/2, ϕ/4, ϕ/8, or ϕ/32) that are generated by d
  the system clock, or on-chip oscillator clock (ϕ40M) can be selected by bits TPSC2 to
  in TRDCR.

  Figure 14.13 illustrates this timing.

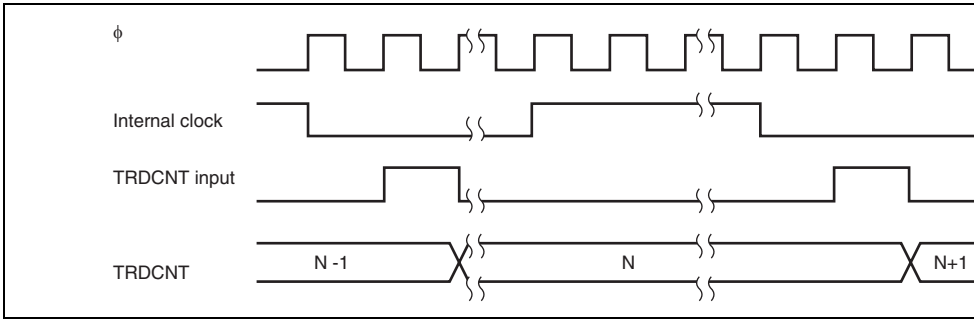


Figure 14.13 Count Timing at Internal Clock Operation

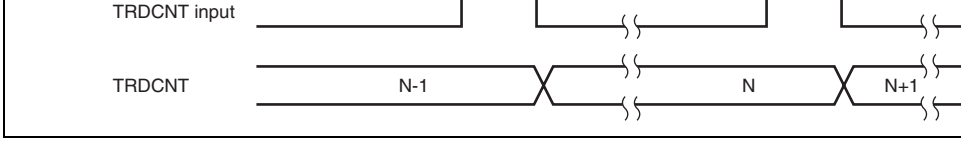


Figure 14.14 Count Timing at External Clock Operation (Both Edges Detec

14.4.2 Waveform Output by Compare Match

Timer RD can perform 0, 1, or toggle output from the corresponding FTIOA, FTIOB, F
FTIOD output pin using compare match A, B, C, or D.

Figure 14.15 shows an example of the setting procedure for waveform output by compa

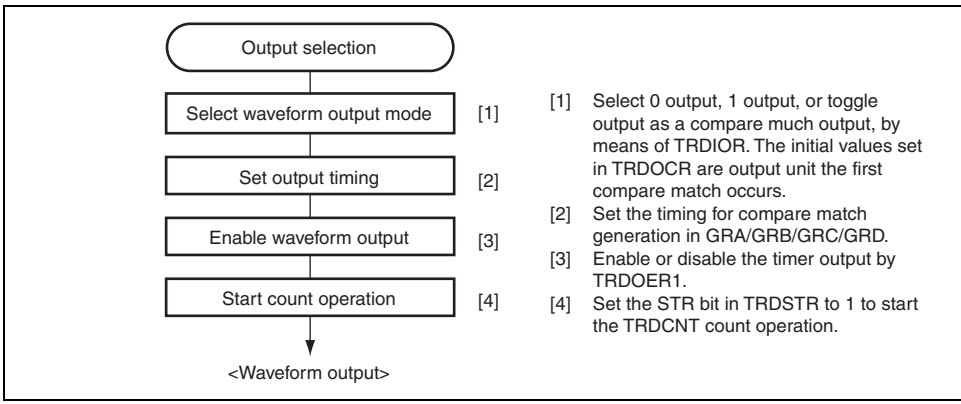


Figure 14.15 Example of Setting Procedure for Waveform Output by Compare

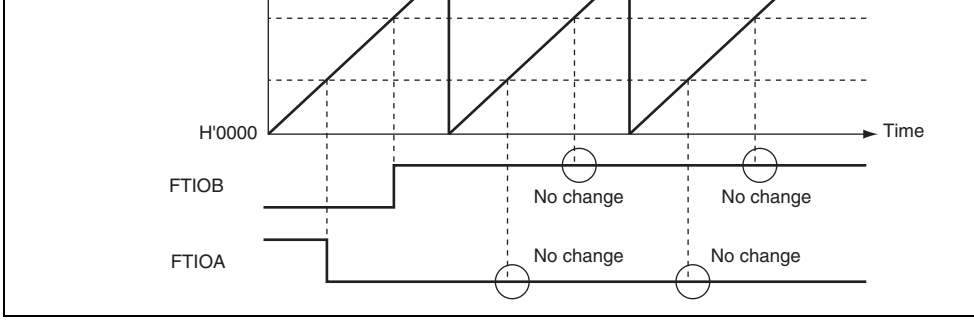


Figure 14.16 Example of 0 Output/1 Output Operation

Figure 14.17 shows an example of toggle output.

In this example, TRDCNT has been designated as a periodic counter (with counter clearin
compare match B), and settings have been made such that the output is toggled by both co
match A and compare match B.

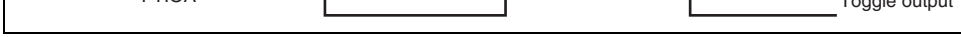


Figure 14.17 Example of Toggle Output Operation

(2) Output Compare Timing

The compare match signal is generated in the last state in which TRDCNT and GR matc
TRDCNT changes from the matching value to the next value). When the compare match
generated, the output value selected in TRDIOR is output at the compare match output p
(FTIOA, FTIOB, FTIOC, or FTIOD). When TRDCNT matches GR, the compare match
generated only after the next TRDCNT input clock pulse is input.

Figure 14.18 shows an example of the output compare timing.

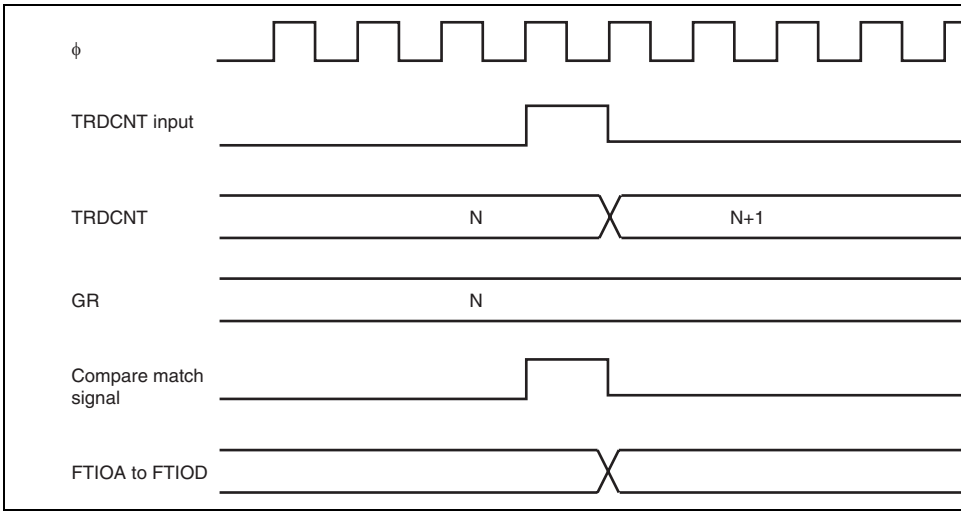
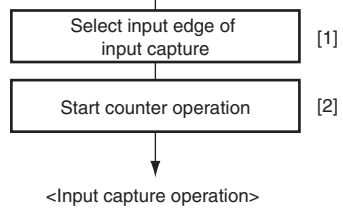


Figure 14.18 Output Compare Timing



[1] Designate GR as an input capture register by means of TRDIOR, and select rising edge, falling edge, or both edges as the input edge of the input capture signal.

[2] Set the STR bit in TRDSTR to 1 to start the TRDCNT counter operation.

Figure 14.19 Example of Input Capture Operation Setting Procedure

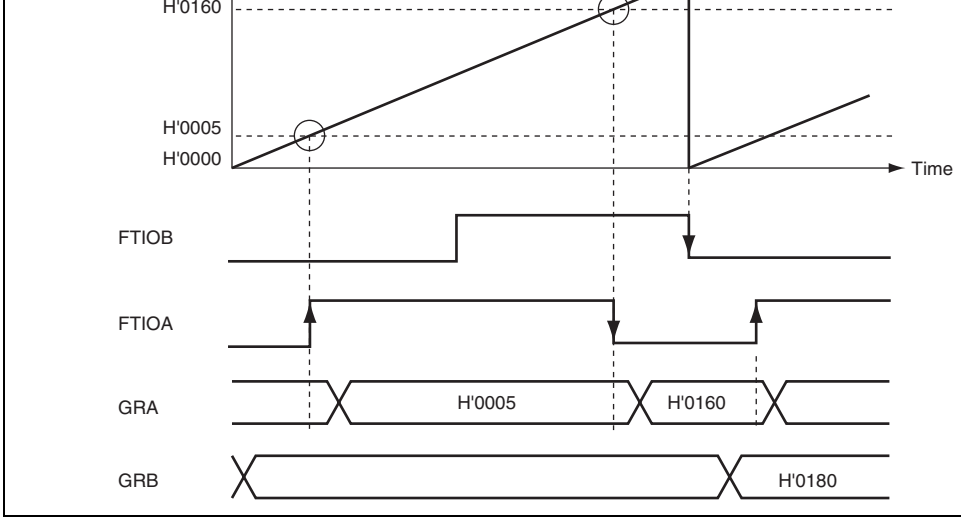


Figure 14.20 Example of Input Capture Operation

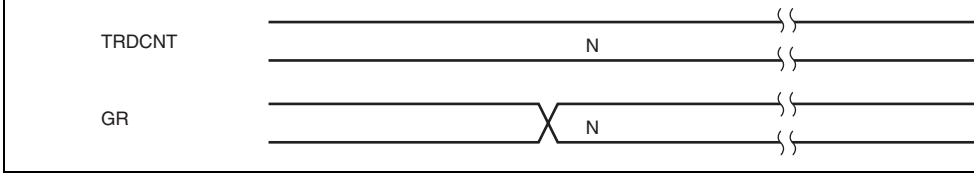
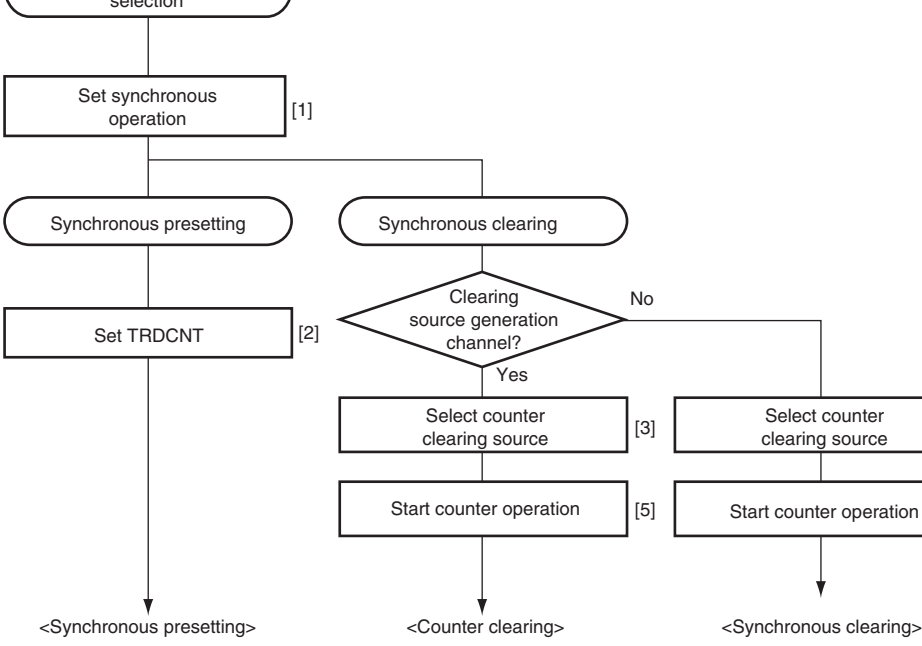


Figure 14.21 Input Capture Signal Timing



[1] Set the SYNC bits in TRDMDR to 1.
[2] When a value is written to either of the TRDCNT counters, the same value is simultaneously written to t
TRDCNT counter.
[3] Set bits CCLR1 and CCLR0 in TRDCR to specify counter clearing by compare match/input capture.
[4] Set bits CCLR1 and CCLR0 in TRDCR to designate synchronous clearing for the counter clearing sourc
[5] Set the STR bit in TRDSTR to 1 to start the count operation.

Figure 14.22 Example of Synchronous Operation Setting Procedure

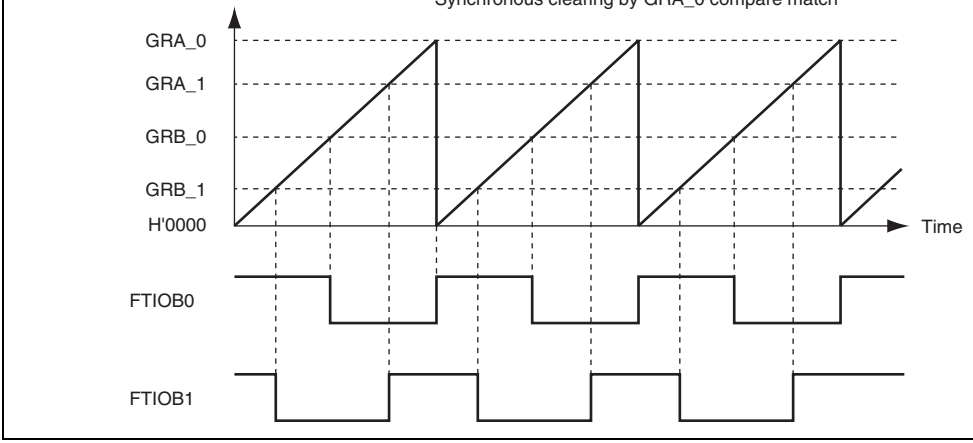


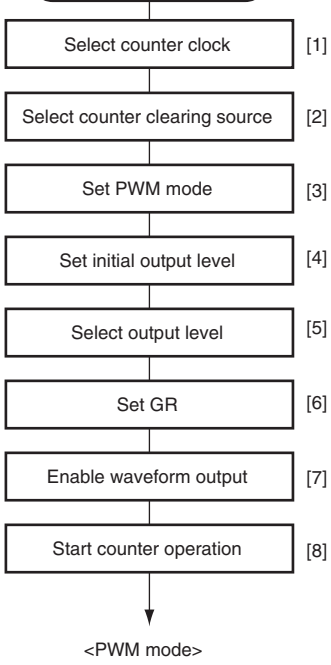
Figure 14.23 Example of Synchronous Operation

14.4.5 PWM Mode

In PWM mode, PWM waveforms are output from the FTIOB, FTIOC, and FTIOD outpu with GRA as a cycle register and GRB, GRC, and GRD as duty registers. The initial outp of the corresponding pin depends on the setting values of TRDOCR and POCR. Table 14 an example of the initial output level of the FTIOB0 pin.

The output level is determined by the POLB to POLD bits corresponding to POCR. Whe is 0, the FTIOB output pin is set to 0 by compare match B and set to 1 by compare match POLB is 1, the FTIOB output pin is set to 1 by compare match B and cleared to 0 by com match A. In PWM mode, maximum 6-phase PWM outputs are possible.

Figure 14.24 shows an example of the PWM mode setting procedure.



[1] Select the counter clock with bits TPSC2 to TOSC0 in TRDCR. When an external clock is selected, select the external clock edge with bits CKEG1 and CKEG0 in TRDCR.

[2] Use bits CCLR2 to CCLR0 in TRDCR to select the counter clearing source.

[3] Select the PWM mode with bits PWMB0 to PWMD0 and PWMB1 to PWMD1 in TRDPMR.

[4] Set the initial output value with bits TOB0 to TOD0 and TOB1 to TOD1 in TRDOCR.

[5] Set the output level with bits POLB to POLD in POCR.

[6] Set the cycle in GRA, and set the duty in the other GR.

[7] Enable or disable the timer output by TRDOER1.

[8] Set the STR bit in TRDSTR to 1 and start the counter operation.

Figure 14.24 Example of PWM Mode Setting Procedure

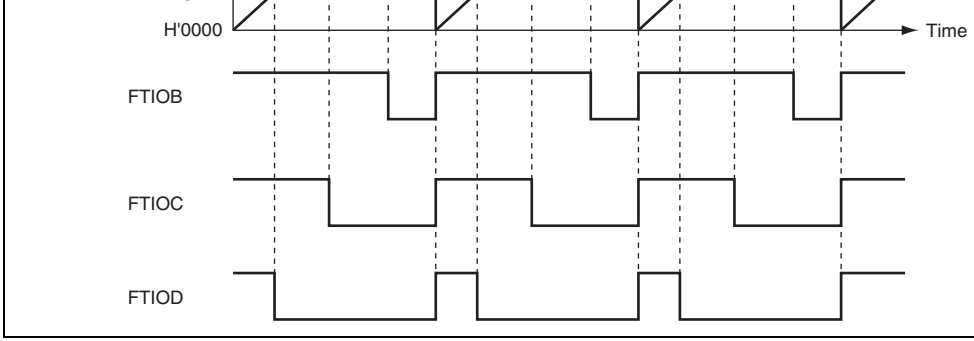


Figure 14.25 Example of PWM Mode Operation (1)

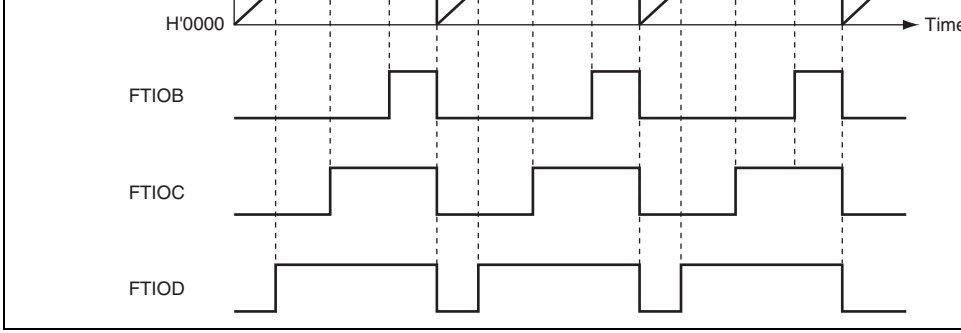


Figure 14.26 Example of PWM Mode Operation (2)

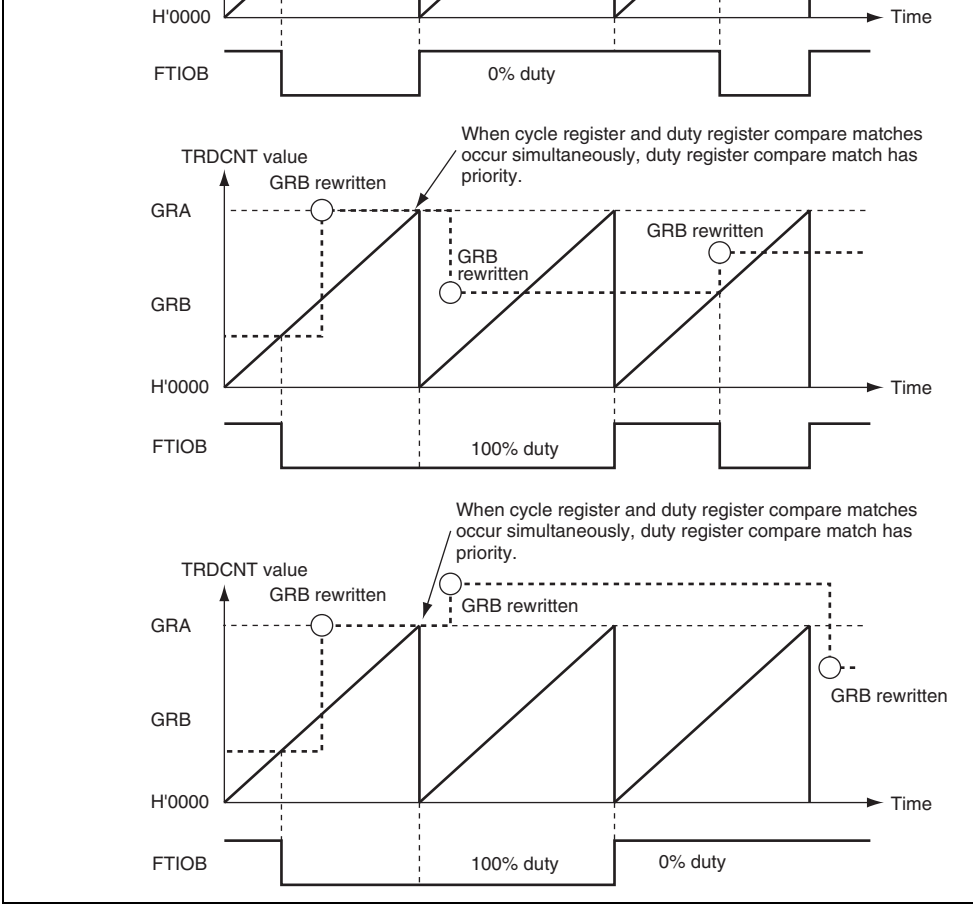


Figure 14.27 Example of PWM Mode Operation (3)

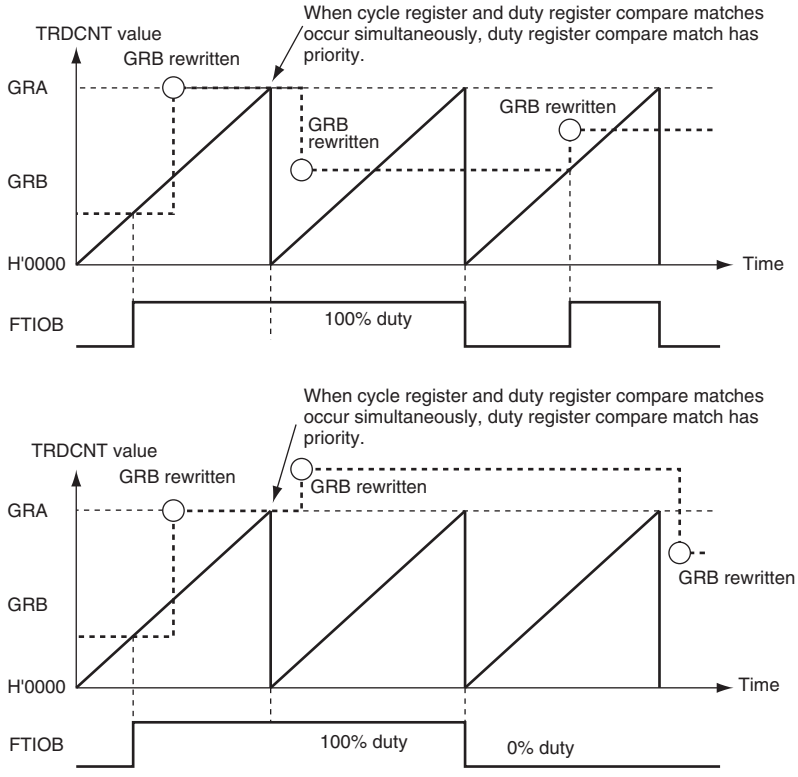


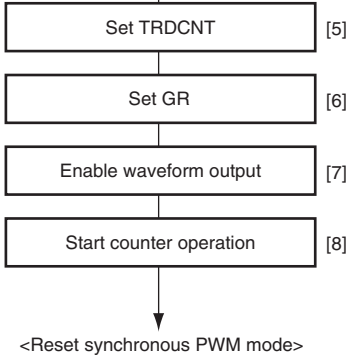
Figure 14.28 Example of PWM Mode Operation (4)

Table 14.5 Output Pins in Reset Synchronous PWM Mode

Channel	Pin Name	Input/Output	Pin Function
0	FTIOC0	Output	Toggle output in synchronous with PWM cycle
0	FTIOB0	Output	PWM output 1
0	FTIOD0	Output	PWM output 1 (counter-phase waveform of PW output 1)
1	FTIOA1	Output	PWM output 2
1	FTIOC1	Output	PWM output 2 (counter-phase waveform of PW output 2)
1	FTIOB1	Output	PWM output 3
1	FTIOD1	Output	PWM output 3 (counter-phase waveform of PW output 3)

Table 14.6 Register Settings in Reset Synchronous PWM Mode

Register	Description
TRDCNT_0	Initial setting of H'0000
TRDCNT_1	Not used (independently operates)
GRA_0	Sets counter cycle of TRDCNT_0
GRB_0	Set a changing point of the PWM waveform output from pins FTIOB0 an FTIOD0.
GRA_1	Set a changing point of the PWM waveform output from pins FTIOA1 an FTIOC1.
GRB_1	Set a changing point of the PWM waveform output from pins FTIOB1 an FTIOD1.



become PWM output pins automatically.

[5] Set TRDCNT_0 as H'0000. TRDCNT_1 does not need to be set.

[6] GRA_0 is a cycle register. Set a cycle for GRA_0. Set the changing point timing of the PWM output waveform for GRB_0, GRA_1, and GRB_1.

[7] Enable or disable the timer output by TRDOER1.

[8] Set the STR bit in TRDSTR to 1 and start the counter operation.

Figure 14.29 Example of Reset Synchronous PWM Mode Setting Procedu

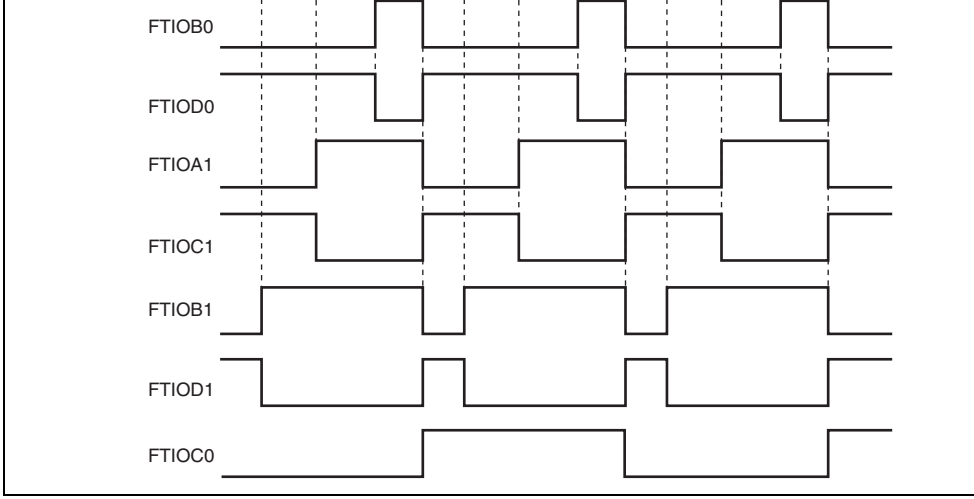


Figure 14.30 Example of Reset Synchronous PWM Mode Operation (OLS0 = OL

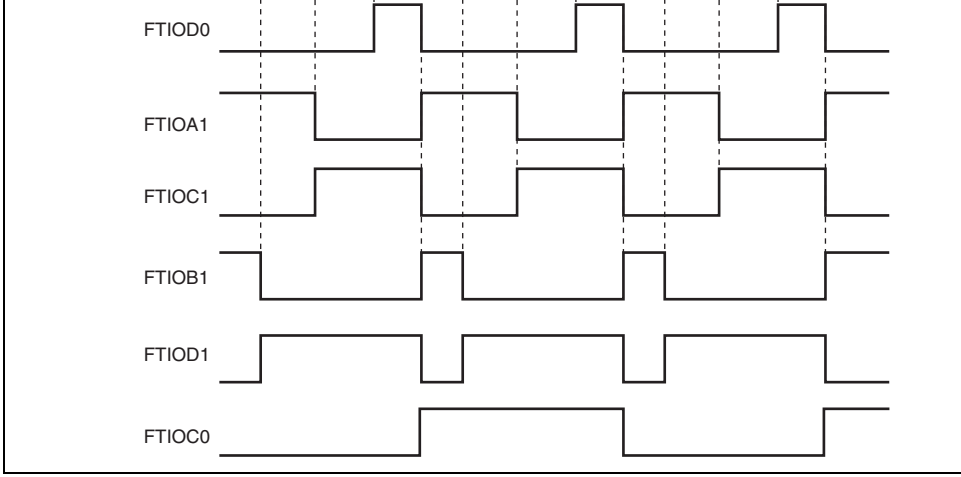


Figure 14.31 Example of Reset Synchronous PWM Mode Operation (OLS0 = O

In reset synchronous PWM mode, TRDCNT_0 and TRDCNT_1 perform increment and independent operations, respectively. However, GRA_1 and GRB_1 are separated from TRDCNT_1. When a compare match occurs between TRDCNT_0 and GRA_0, a count cleared and an increment operation is restarted from H'0000.

The PWM pin outputs 0 or 1 whenever a compare match between GRB_0, GRA_1, GR TRDCNT_0 or counter clearing occur.

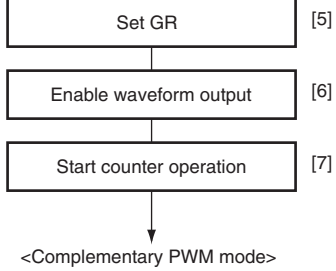
For details on operations when reset synchronous PWM mode and buffer operation are simultaneously set, refer to section 14.4.9, Buffer Operation.

Table 14.7 Output Pins in Complementary PWM Mode

Channel	Pin Name	Input/Output	Pin Function
0	FTIOC0	Output	Toggle output in synchronous with PWM cycle
0	FTIOB0	Output	PWM output 1
0	FTIOD0	Output	PWM output 1 (counter-phase waveform non-overlapped with PWM output 1)
1	FTIOA1	Output	PWM output 2
1	FTIOC1	Output	PWM output 2 (counter-phase waveform non-overlapped with PWM output 2)
1	FTIOB1	Output	PWM output 3
1	FTIOD1	Output	PWM output 3 (counter-phase waveform non-overlapped with PWM output 3)

Table 14.8 Register Settings in Complementary PWM Mode

Register	Description
TRDCNT_0	Initial setting of non-overlapped periods (non-overlapped periods are diff with TRDCNT_1)
TRDCNT_1	Initial setting of H'0000
GRA_0	Sets (upper limit value – 1) of TRDCNT_0
GRB_0	Set a changing point of the PWM waveform output from pins FTIOB0 an FTIOD0.
GRA_1	Set a changing point of the PWM waveform output from pins FTIOA1 an FTIOC1.
GRB_1	Set a changing point of the PWM waveform output from pins FTIOB1 an FTIOD1.



FTIOD1 automatically become PWM output pins.

[4] TRDCNT_1 must be H'0000. Set a non-overlapped period to TRDCNT_0.

[5] GRA_0 is a cycle register. Set the cycle to GRA_0. Set the timing to change the PWM output waveform to GRB_0, GRA_1, and GRB_1. The settings must be set so that a compare match occurs on TRDCNT_0 and TRDCNT_1. $T \leq X$ (X: Initial value in GRB_0, GRA_1, or GRB_1).

[6] Use TRDOER1 to enable or disable the timer output.

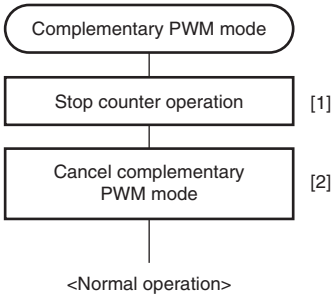
[7] Set the STR0 and STR1 bits in TRDSTR to 1 to start the count operation.

Note: To modify the settings for the complementary PWM mode, clear settings other than those for the mode. After that, repeat setting from step [1].

Figure 14.32 Example of Complementary PWM Mode Setting Procedur

(1) Canceling Procedure of Complementary PWM Mode

Figure 14.33 shows the complementary PWM mode canceling procedure.



[1] Clear bit CMD1 in TRDFCR to 0, and set channels 0 and 1 to normal operation.

[2] After setting channels 0 and 1 to normal operation, clear bits STR0 and STR1 in TRDSTR to 0 and stop TRDCNT_0 and TRDCNT_1.

Figure 14.33 Canceling Procedure of Complementary PWM Mode

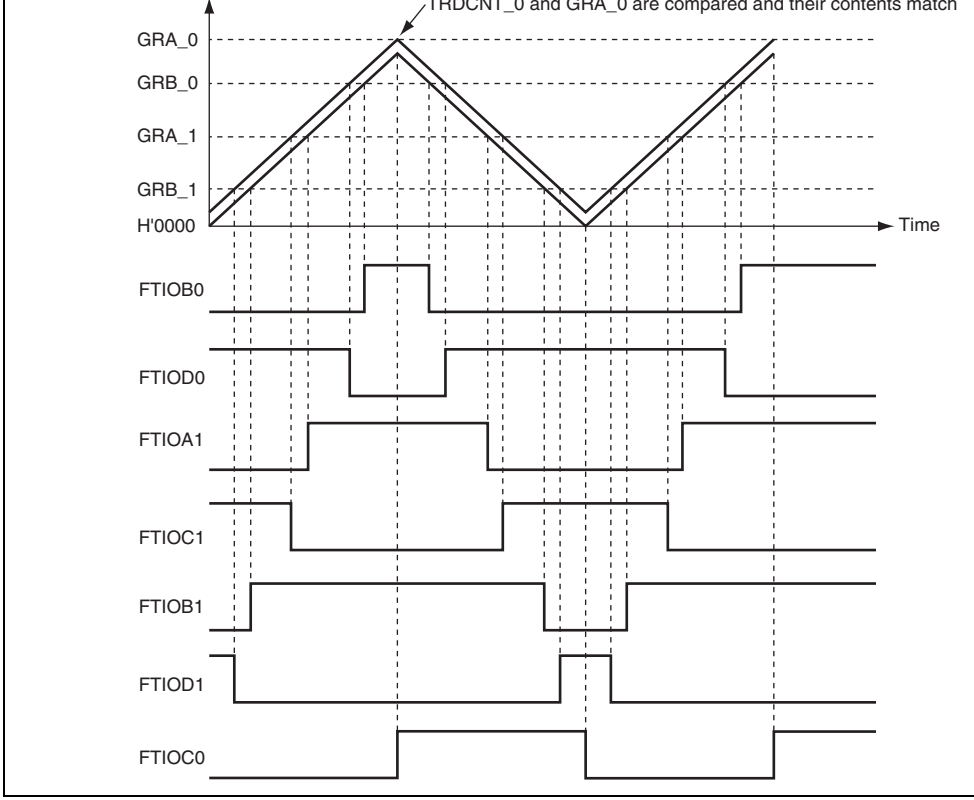


Figure 14.34 Example of Complementary PWM Mode Operation (1)

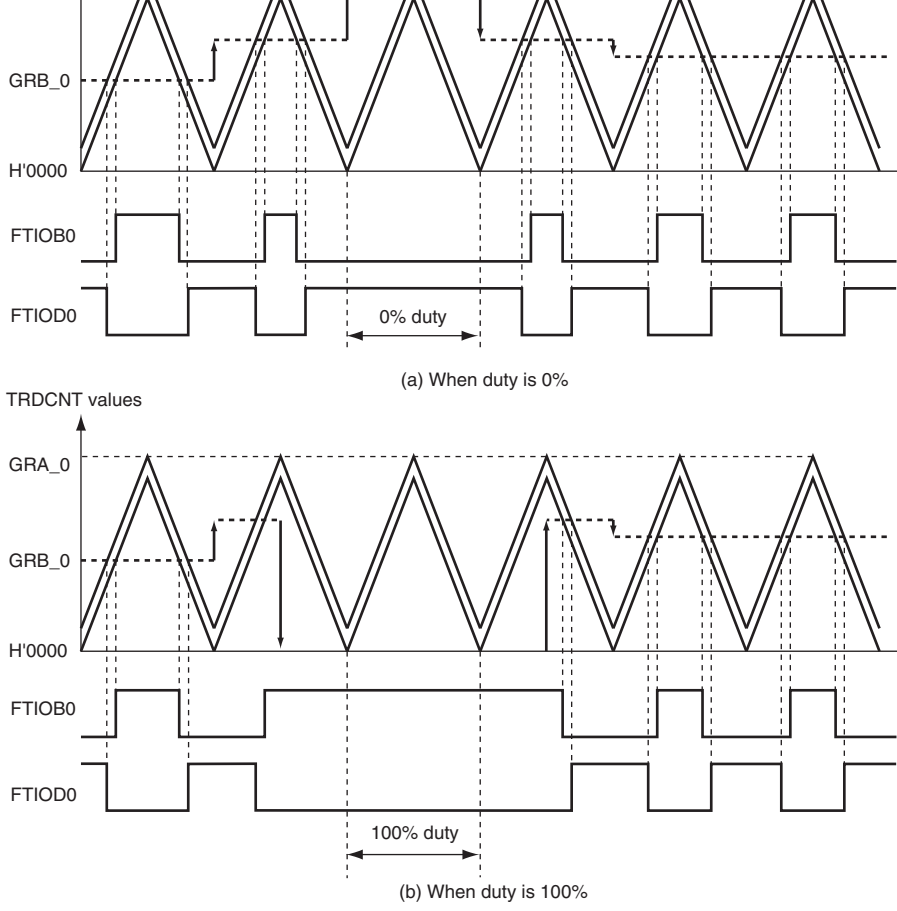


Figure 14.35 Example of Complementary PWM Mode Operation (2)

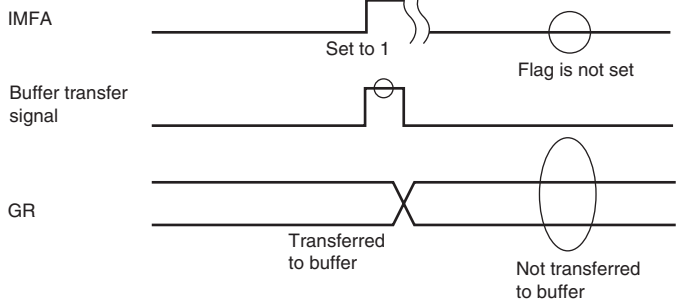


Figure 14.36 Timing of Overshooting

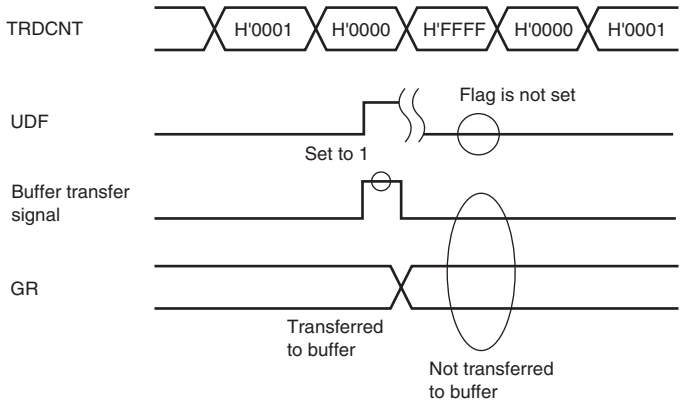


Figure 14.37 Timing of Undershooting

1. Initial value
   - H'0000 to T – 1 (T: Initial value of TRDCNT_0) must not be set for the initial va
   - GRA_0 – (T – 1) or more must not be set for the initial value.
   - When using buffer operation, the same values must be set in the buffer registers a corresponding general registers.
2. Modifying the setting value
   - Use the buffer operation to change the GR value. If the GR value is changed by w it directly, the intended waveform may not be output.
   - Do not change settings of GRA_0 during operation.

match of GRA_0 on the FTIOA0 pin.

- When TOA0 = 1, 0 is output on a compare match of GRA_1 and 1 is output on a com match of GRA_0 on the FTIOA0 pin.
- When TOB0 = 0, 1 is output on a compare match of GRB_1 and 0 is output on a com match of GRB_0 on the FTIOB0 pin.
- When TOB0 = 1, 0 is output on a compare match of GRB_1 and 1 is output on a com match of GRB_0 on the FTIOB0 pin.

Table 14.9 lists the correspondence between pin functions and GR registers, figure 14.38 block diagram in PWM3 mode, and figure 14.39 shows a flowchart of setting in PWM3 m

When the buffer operation is used, set TRDMDR. The timer input/output pins, which are in PWM3 mode, can be used as general port pins. When the buffer operation is not set, si or GRD is not used, a compare match interrupt can be generated when GRC or GRD mat TRDCNT_1.

1	FTIOA1	
	FTIOB1	
	FTIOC1	
	FTIOD1	

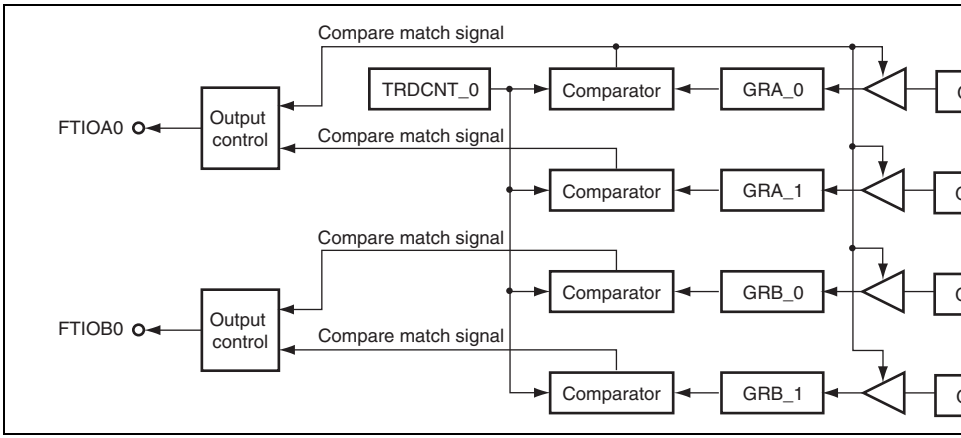
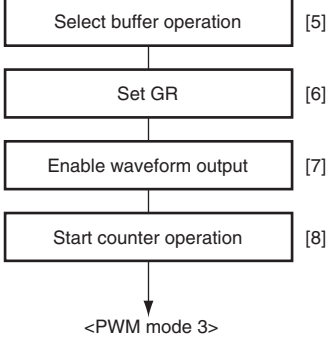


Figure 14.38 Block Diagram in PWM3 Mode



[5] Set the GR buffer operation with bits BFC0, BFC1, BFD0, and TOD1 in TRDMDR.

[6] Set a cycle in GRA. Set the duty cycle in other GR registers.

[7] Enable or disable the timer output by TRDOER.

[8] Set the STR bit in TRDSTR to 1 and start the counter operation.

Figure 14.39 Flowchart of Setting in PWM3 Mode

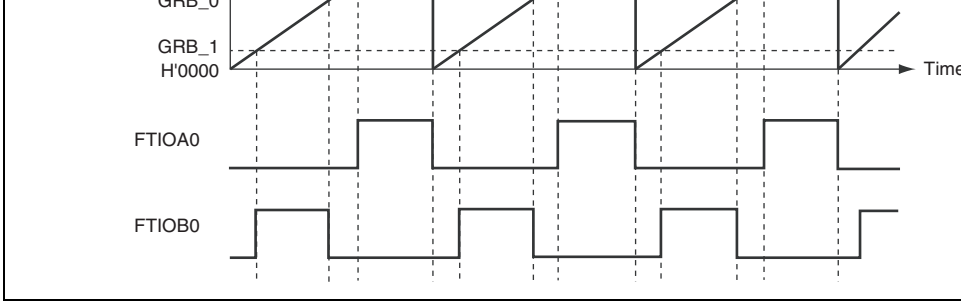


Figure 14.40 Example of Non-Overlap Pulses

GRA	GRC
GRB	GRD

(1) When GR is an Output Compare Register

When a compare match occurs, the value in GR of the corresponding channel is transferr
general register.

This operation is illustrated in figure 14.41.

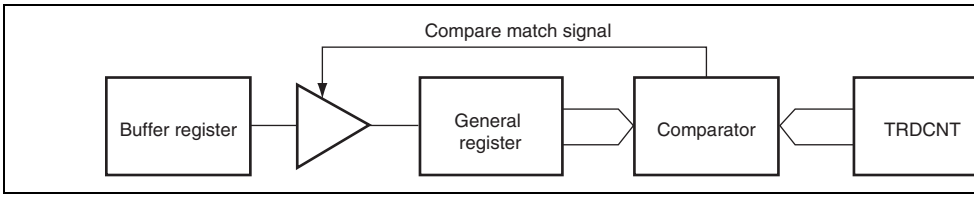


Figure 14.41 Compare Match Buffer Operation

Figure 14.42 Input Capture Buffer Operation

(3) PWM3 Mode

When compare match A0 occurs, the value of the buffer register is transferred to GR.

(4) Complementary PWM Mode

When the counter switches from counting up to counting down or vice versa, the value o
buffer register is transferred to GR. Here, the value of the buffer register is transferred to
following timing:

- When TRDCNT_0 and GRA_0 are compared and their contents match
- When TRDCNT_1 underflows

(5) Reset Synchronous PWM Mode

When compare match A0 occurs, the value in the buffer register is transferred to GR.

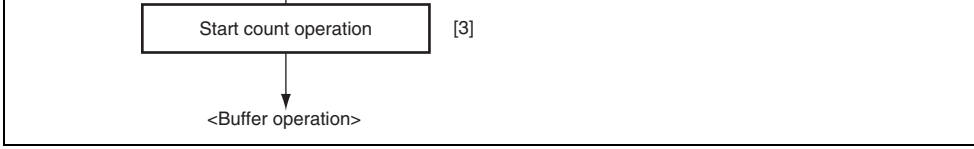


Figure 14.43 Example of Buffer Operation Setting Procedure

The timing to transfer data is shown in figure 14.45.

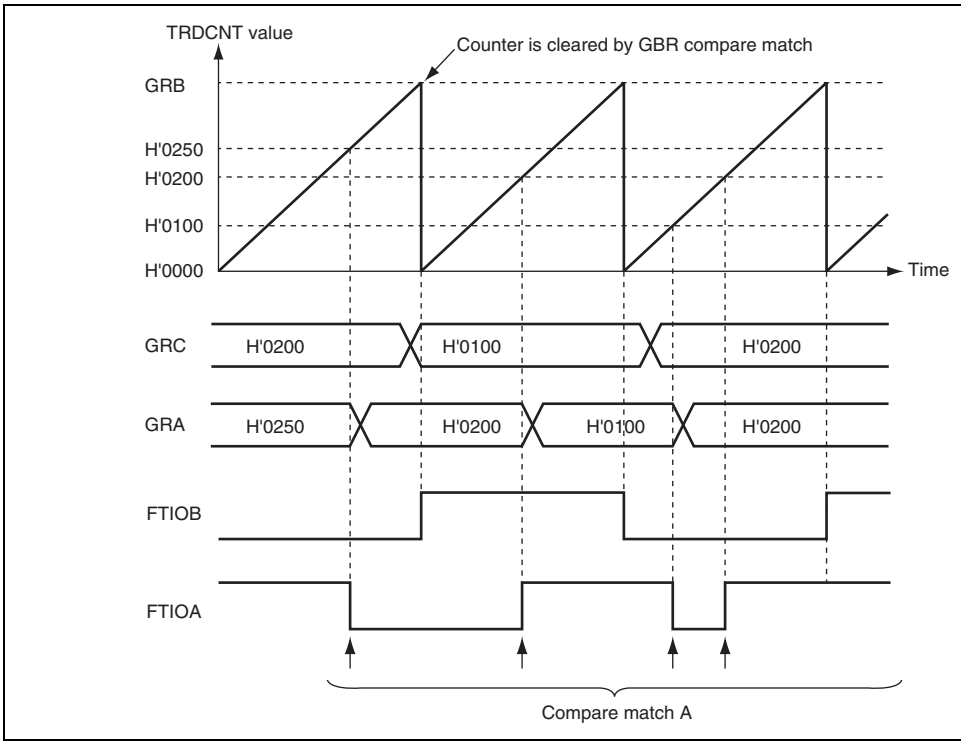


Figure 14.44 Example of Buffer Operation (1)
(Buffer Operation for Output Compare Register)

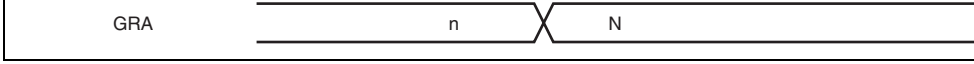


Figure 14.45 Example of Compare Match Timing for Buffer Operation

Figure 14.46 shows an operation example in which GRA has been designated as an input
register, and buffer operation has been designated for GRA and GRC.

Counter clearing by input capture B has been set for TRDCNT, and falling edges have be
selected as the FIOCB pin input capture input edge. And both rising and falling edges hav
selected as the FIOCA pin input capture input edge.

As buffer operation has been set, when the TRDCNT value is stored in GRA upon the oc
of input capture A, the value previously stored in GRA is simultaneously transferred to G
transfer timing is shown in figure 14.47.

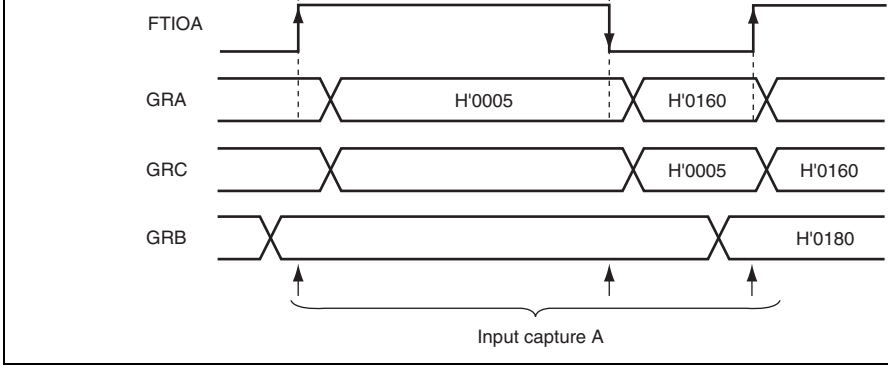


Figure 14.46 Example of Buffer Operation (2)
(Buffer Operation for Input Capture Register)

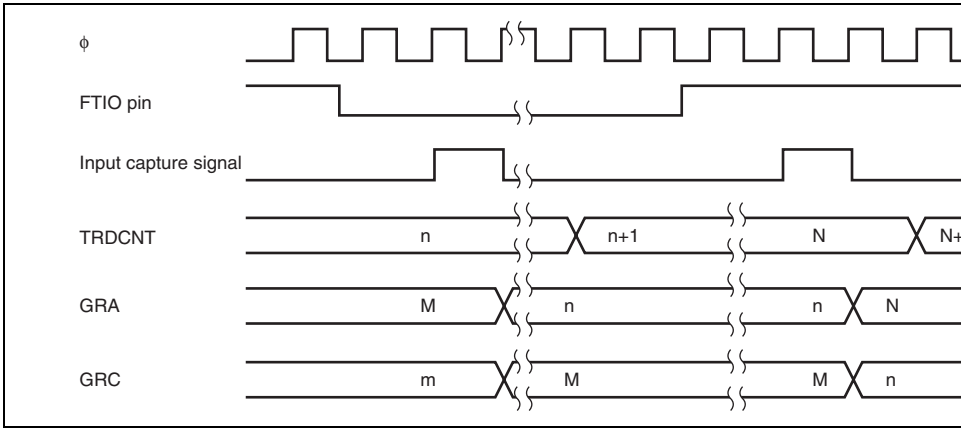


Figure 14.47 Input Capture Timing of Buffer Operation

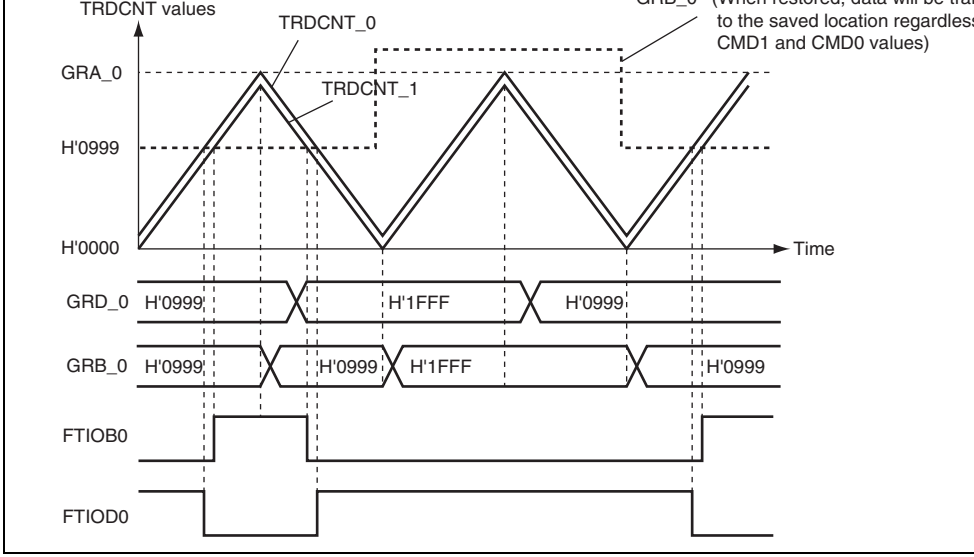


Figure 14.48 Buffer Operation (3)
(Buffer Operation in Complementary PWM Mode CMD1 = CMD0 = 1)

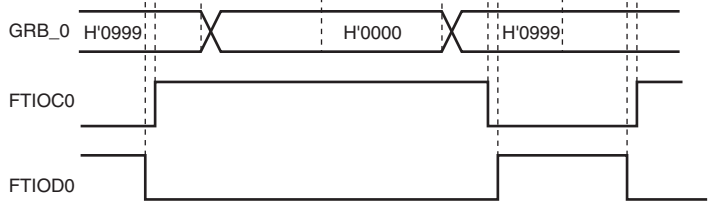


Figure 14.49 Buffer Operation (4)
(Buffer Operation in Complementary PWM Mode CMD1 =1, CMD0 = 0)

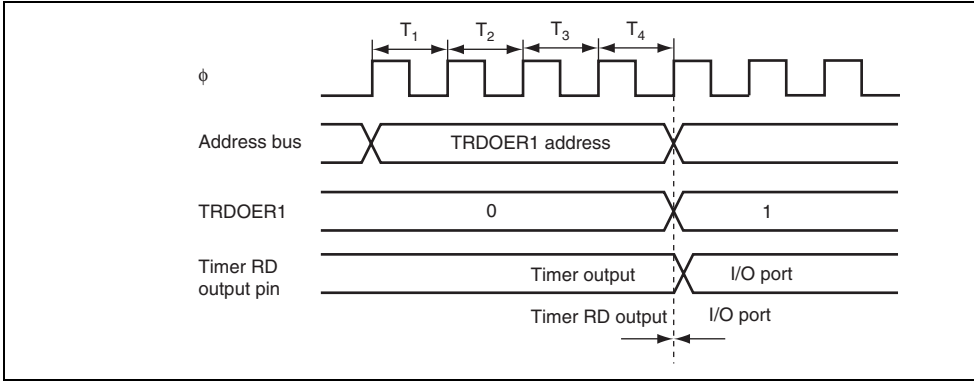


Figure 14.50 Example of Output Disable Timing of Timer RD by Writing to TRD

(2) Output Disable Timing of Timer RD by External Trigger

When PH5/$\overline{\text{TRDOI\_0}}$ (or PH6/$\overline{\text{TRDOI\_1}}$) is set as a $\overline{\text{TRDOI}}$ input pin, and low level is in $\overline{\text{TRDOI}}$, the master enable bit in TRDOER1 is set to 1 and the output of timer RD will be

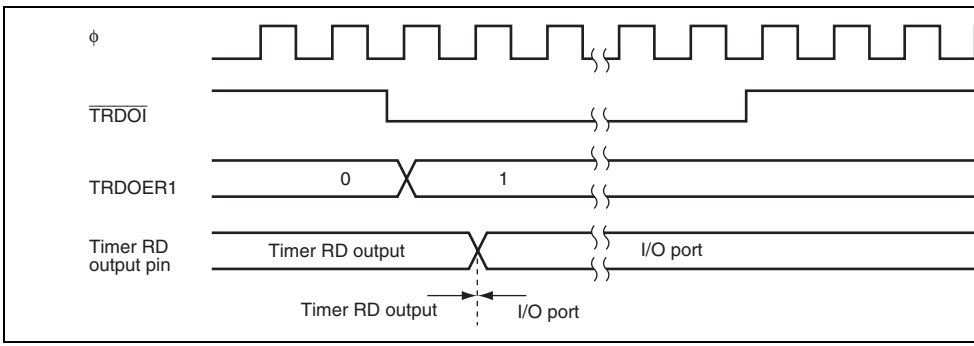


Figure 14.51 Example of Output Disable Timing of Timer RD by External Tri

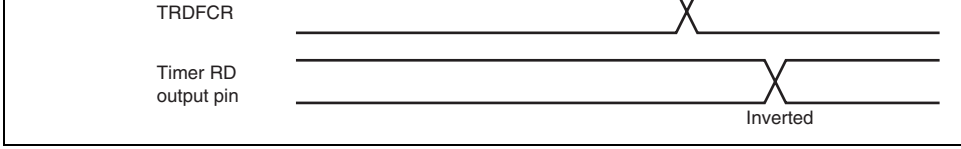


Figure 14.52 Example of Output Inverse Timing of Timer RD by Writing to TR

(4) Output Inverse Timing by POCR

The output level can be inverted by inverting the POLD, POLC, and POLB bits in POCR mode. Figure 14.53 shows the timing.

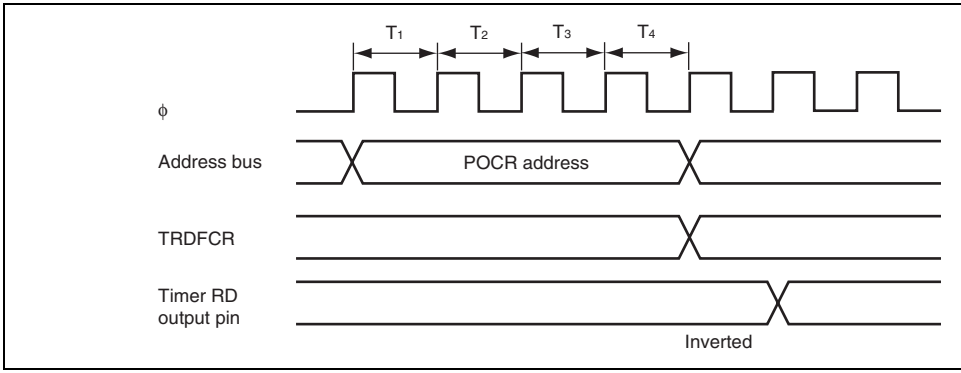


Figure 14.53 Example of Output Inverse Timing of Timer RD by Writing to P

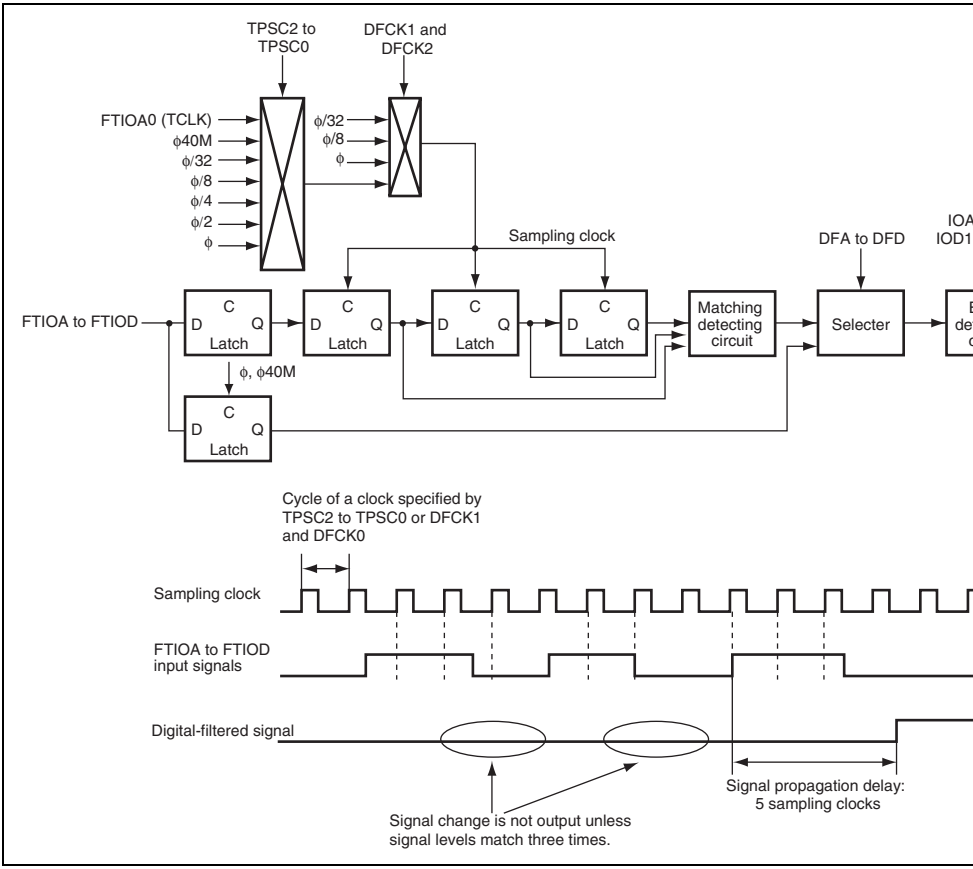


Figure 14.54 Block Diagram of Digital Filter

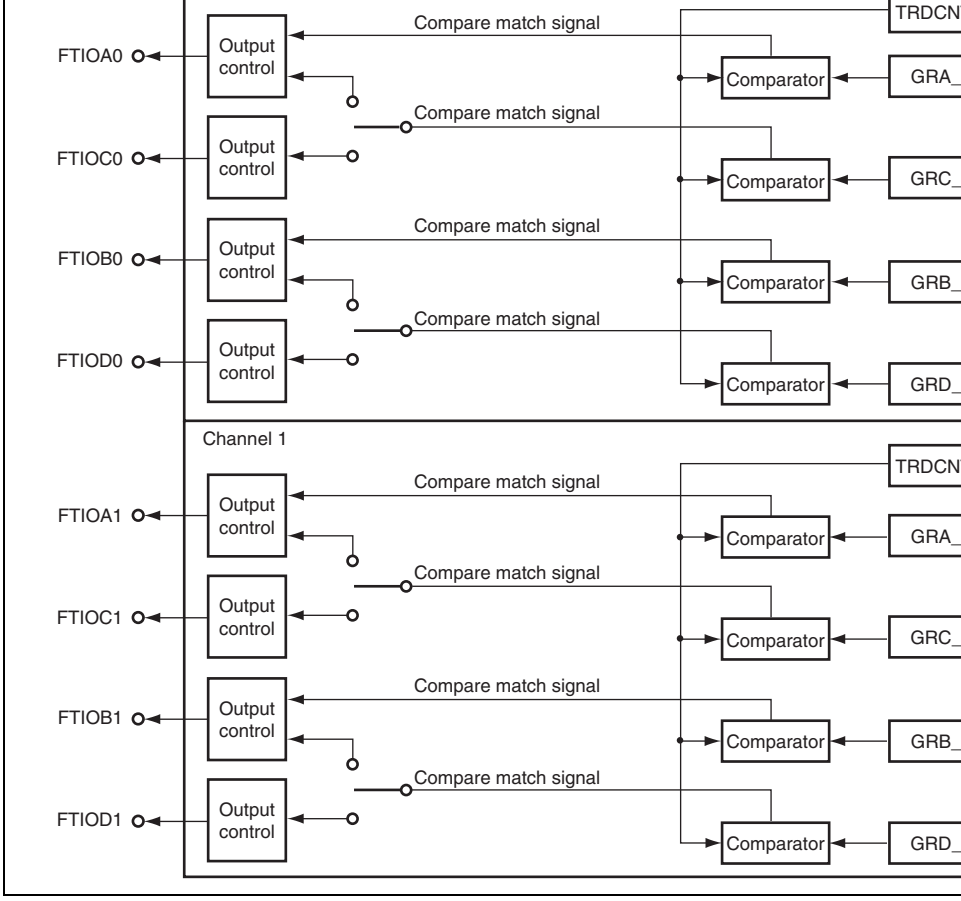


Figure 14.55 Block Diagram of Output Pins for GR

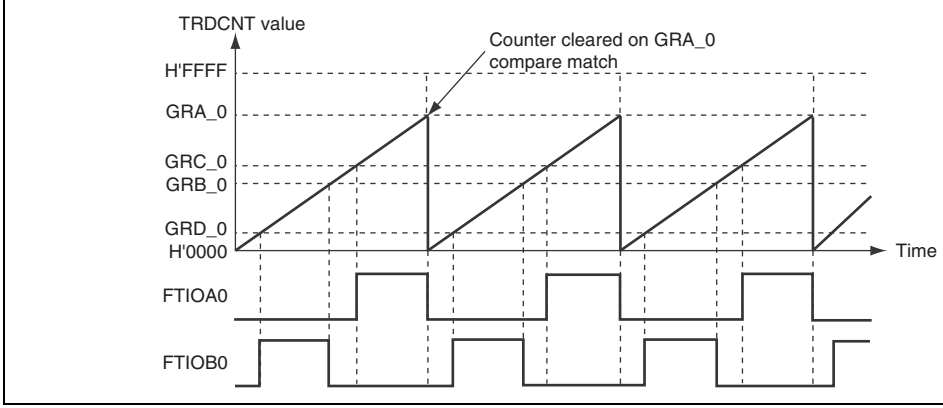


Figure 14.56 Example of Non-Overlapped Pulses Output on Pins FTIOA0 and F (TRDCNT_0 Used)

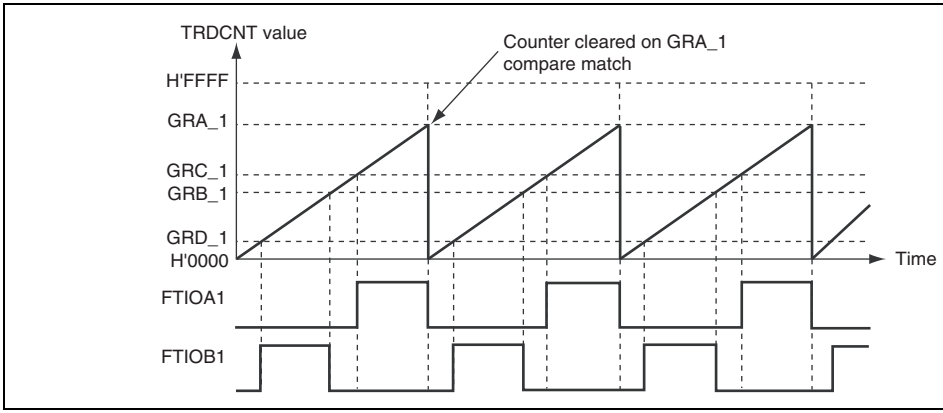


Figure 14.57 Example of Non-Overlapped Pulses Output on Pins FTIOA1 and F (TRDCNT_1 Used)

the TRDCNT. The compare match signal is generated at the last state of matching (timi
update the counter value when the GR and TRDCNT match). Therefore, when the TRD
GR matches, the compare match signal will not be generated until the TRDCNT input c
generated. Figure 14.58 shows the timing to set the IMF flag.

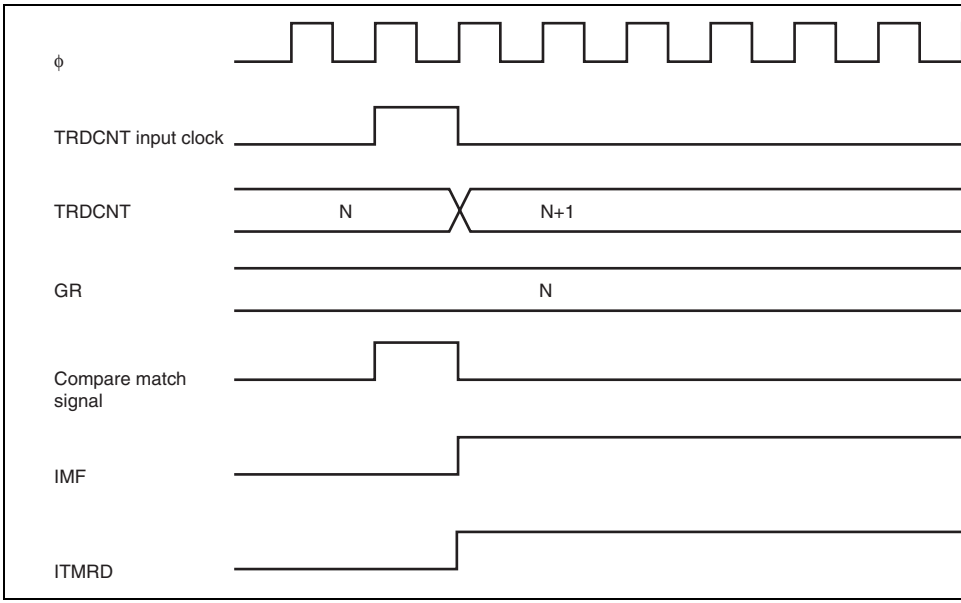


Figure 14.58 IMF Flag Set Timing when Compare Match Occurs

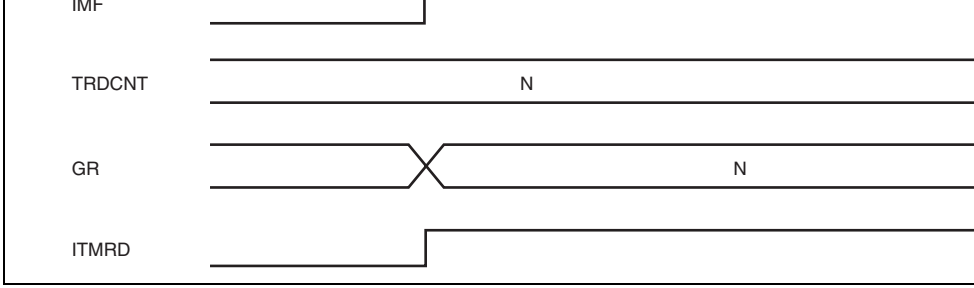


Figure 14.59 IMF Flag Set Timing at Input Capture

(3) Overflow Flag (OVF) Set Timing

The overflow flag is set to 1 when the TRDCNT overflows. Figure 14.60 shows the timin

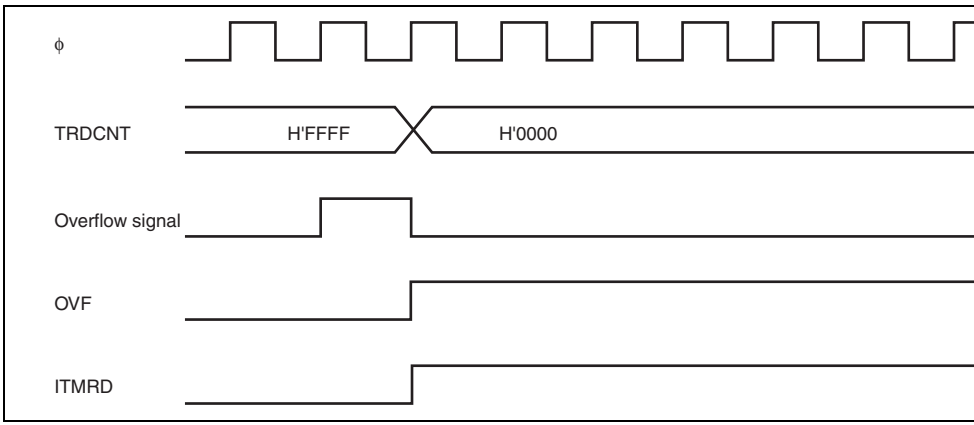


Figure 14.60 OVF Flag Set Timing

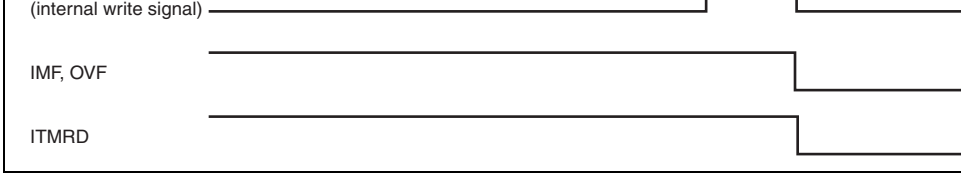


Figure 14.61 Status Flag Clearing Timing

14.6 Usage Notes

(1) Input Pulse Width of Input Clock Signal and Input Capture Signal

The pulse width of the input clock signal and the input capture signal must be at least thr
clock (ϕ) cycles when bits TPSC2 to TPSC0 in TRDCR = B'0XX or B'10X, or at least th
chip oscillator clock (ϕ40M) cycles when B'110; shorter pulses will not be detected corr

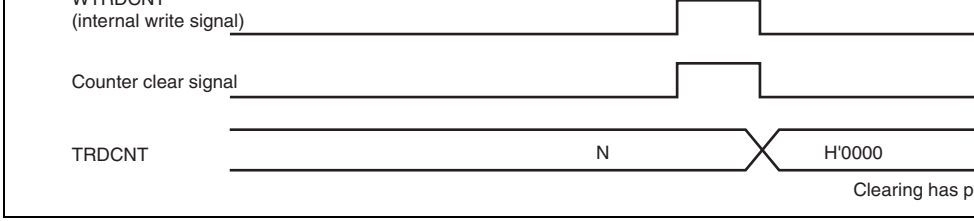


Figure 14.62 Conflict between TRDCNT Write and Clear Operations

(3) Conflict between TRDCNT Write and Increment Operations

If TRDCNT is incremented in the T_4 state of a TRDCNT write cycle, writing has priority 14.63 shows the timing in this case.

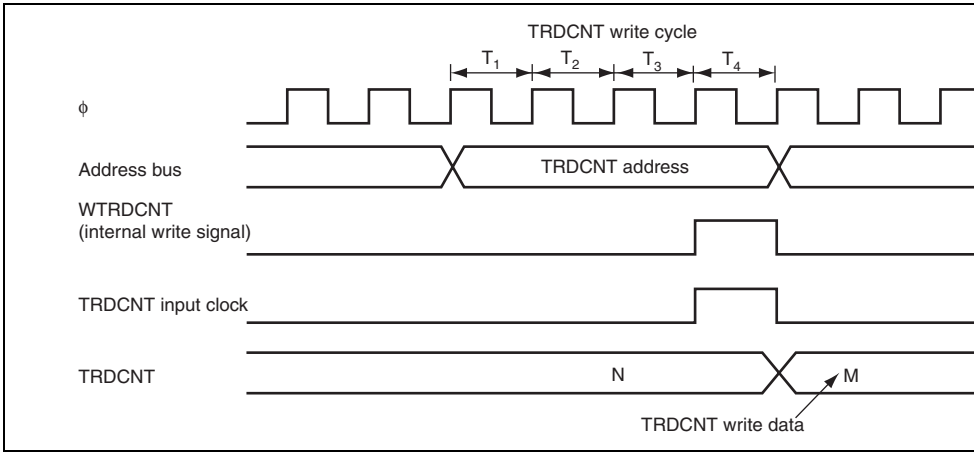


Figure 14.63 Conflict between TRDCNT Write and Increment Operations

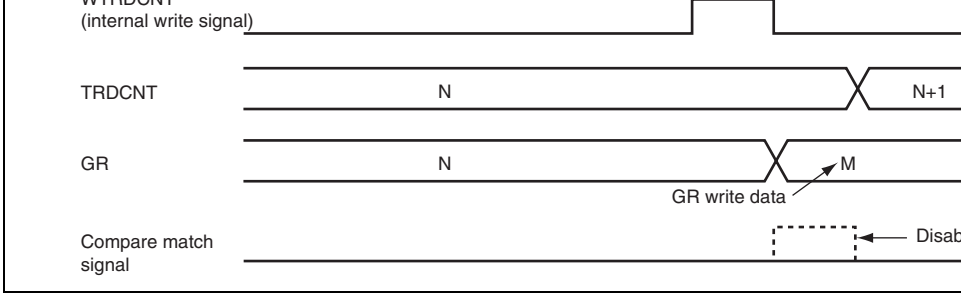


Figure 14.64 Conflict between GR Write and Compare Match

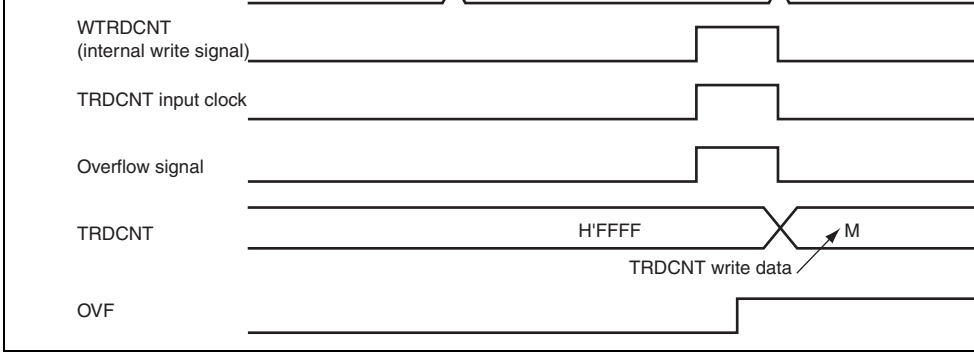


Figure 14.65 Conflict between TRDCNT Write and Overflow

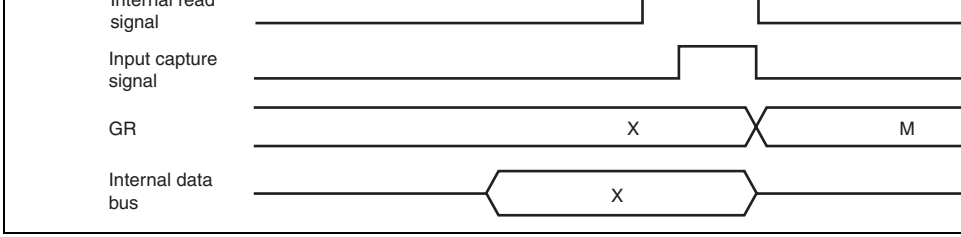


Figure 14.66 Conflict between GR Read and Input Capture

(7) Conflict between Count Clearing and Increment Operations by Input Captur

If an input capture and increment signals are simultaneously generated, count clearing b
capture operation has priority without an increment operation. The TRDCNT contents b
clearing counter are transferred to GR. Figure 14.67 shows the timing in this case.

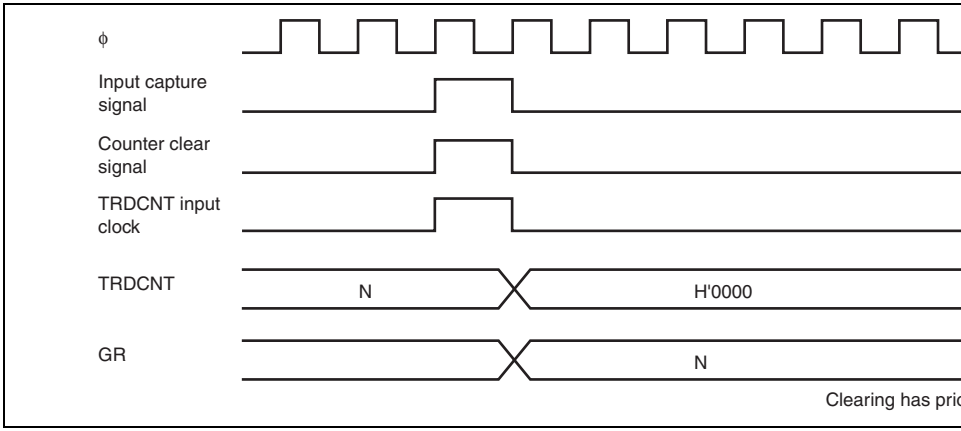


Figure 14.67 Conflict between Count Clearing and Increment Operation by Input Capture

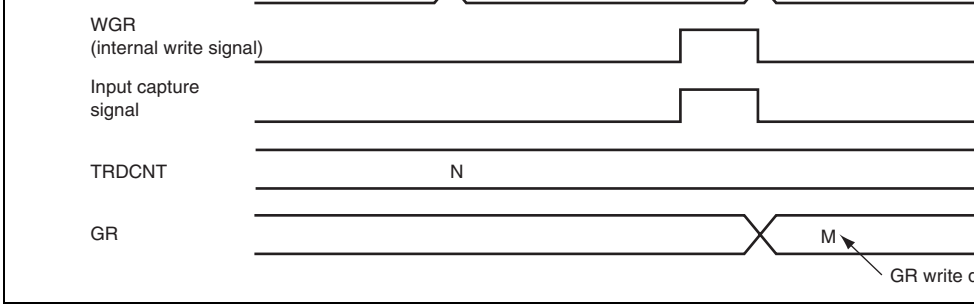


Figure 14.68 Conflict between GR Write and Input Capture

(9) Notes on Setting Reset Synchronous PWM Mode/Complementary PWM Mode

When bits CMD1 and CMD0 in TRDFCR are set, note the following:

- Write bits CMD1 and CMD0 while TRDCNT_1 and TRDCNT_0 are halted.
- Changing the settings of reset synchronous PWM mode to complementary PWM mod versa is disabled. Set reset synchronous PWM mode or complementary PWM mode a normal operation (bits CMD1 and CMD0 are cleared to 0) has been set.

FTIOA1 to FTIOD1 pin output may result in an unexpected result. When TRDOCR is to
written to while compare match is operating, stop the counter once before accessing to T
read the port 6 state to reflect the values of FTIOA0 to FTIOD0 and FTIOA1 to FTIOD
to TOA0 to TOD0 and TOA1 to TOD1, and then restart the counter. Figure 14.69 shows
example when the compare match and the bit manipulation instruction to TRDOCR occ
same timing.

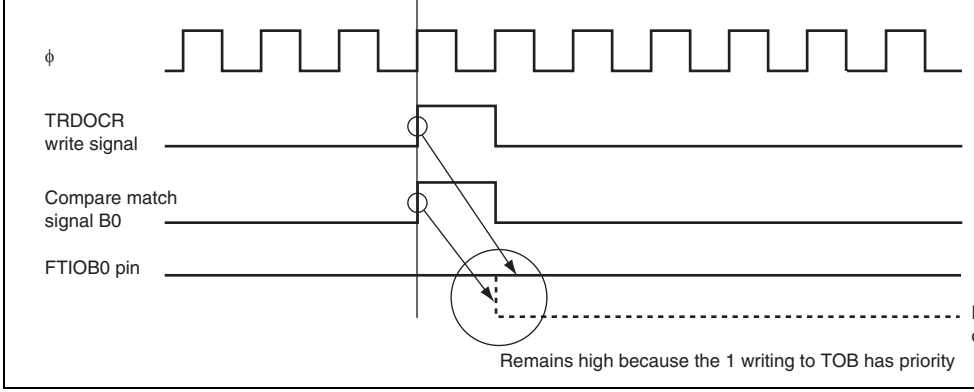


Figure 14.69 When Compare Match and Bit Manipulation Instruction to TRD Occur at the Same Timing

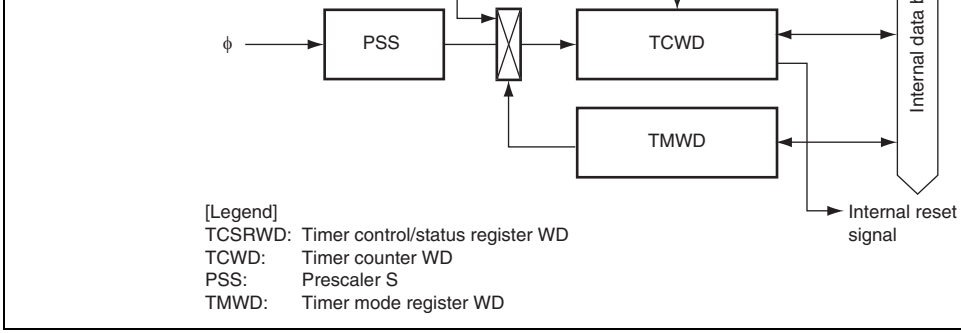


Figure 15.1 Block Diagram of Watchdog Timer

15.1 Features

- Selectable from nine counter input clocks.

  Eight clock sources (ϕ/64, ϕ/128, ϕ/256, ϕ/512, ϕ/1024, ϕ/2048, ϕ/4096, and ϕ/8192) WDT dedicated internal oscillator can be selected as the timer-counter clock. When dedicated internal oscillator is selected, it can operate as the watchdog timer in any c mode.
- Reset signal generated on counter overflow

  An overflow period of 1 to 256 times the selected clock can be set.
- The watchdog timer is enabled in the initial state.

  It starts operating after the reset state is lifted.

TCSRWD performs the TCSRWD and TCWD write control. TCSRWD also controls the
watchdog timer operation and indicates the operating state. TCSRWD must be rewritten
the MOV instruction. The bit manipulation instruction cannot be used to change the setti

Bit	Bit Name	Initial Value	R/W	Description
7	B6WI	1	R/W	Bit 6 Write Inhibit The TCWE bit can be written only when the write the B6WI bit is 0. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable TCWD can be written when the TCWE bit is set When writing data to this bit, the value for bit 7 m
5	B4WI	1	R/W	Bit 4 Write Inhibit The TCSRWE bit can be written only when the w value of the B4WI bit is 0. This bit is always read
4	TCSRWE	0	R/W	Timer Control/Status Register WD Write Enable The WDON and WRST bits can be written when TCSRWE bit is set to 1. When writing data to this bit, the value for bit 5 m
3	B2WI	1	R/W	Bit 2 Write Inhibit This bit can be written to the WDON bit only whe write value of the B2WI bit is 0. This bit is always read as 1.

				[Clearing condition] • When 0 is written to the WDON bit and 0 is the B2WI bit while the TCSRWE bit = 1
1	B0WI	1	R/W	Bit 0 Write Inhibit This bit can be written to the WRST bit only wh write value of the B0WI bit is 0. This bit is alway 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When TCWD overflows and an internal rese generated [Clearing conditions] • Reset by the $\overline{\text{RES}}$ pin • When 0 is written to the WRST bit and 0 is the B0WI bit while the TCSRWE bit = 1

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	CKS3	1	R/W	Clock Select 3 to 0
2	CKS2	1	R/W	Select the clock to be input to TCWD.
1	CKS1	1	R/W	1000: Internal clock: counts on ϕ/64
0	CKS0	1	R/W	1001: Internal clock: counts on ϕ/128 1010: Internal clock: counts on ϕ/256 1011: Internal clock: counts on ϕ/512 1100: Internal clock: counts on ϕ/1024 1101: Internal clock: counts on ϕ/2048 1110: Internal clock: counts on ϕ/4096 1111: Internal clock: counts on ϕ8192 0XXX: WDT dedicated internal oscillator For the overflow periods of the WDT dedicated i oscillator, see section 23, Electrical Characteristi

[Legend]
X: Don't care

Figure 15.2 shows an example of watchdog timer operation.

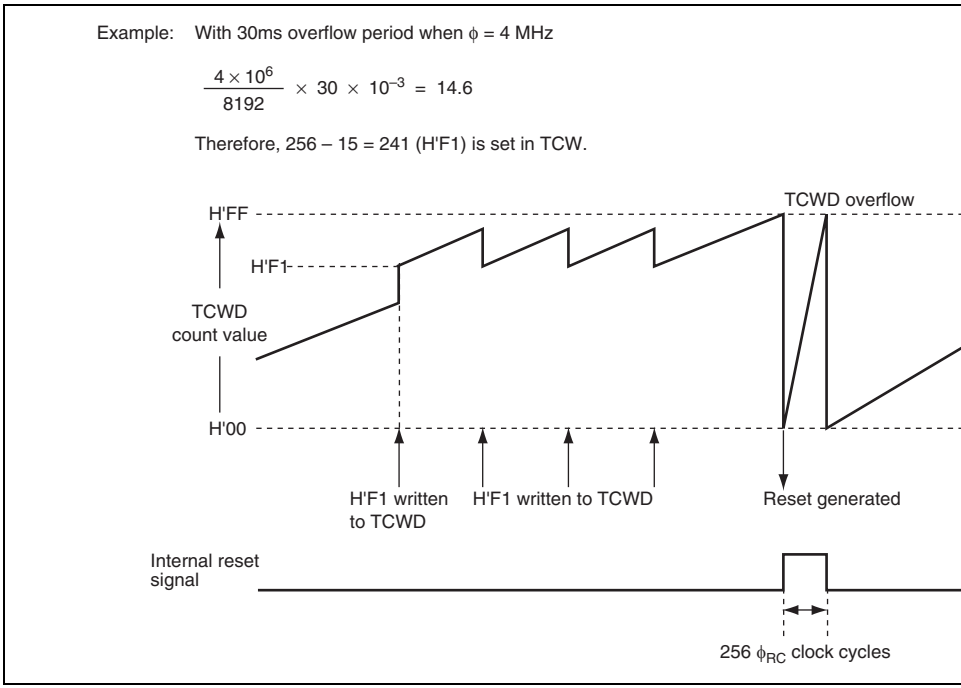


Figure 15.2 Watchdog Timer Operation Example

- Pulse division method for less ripple

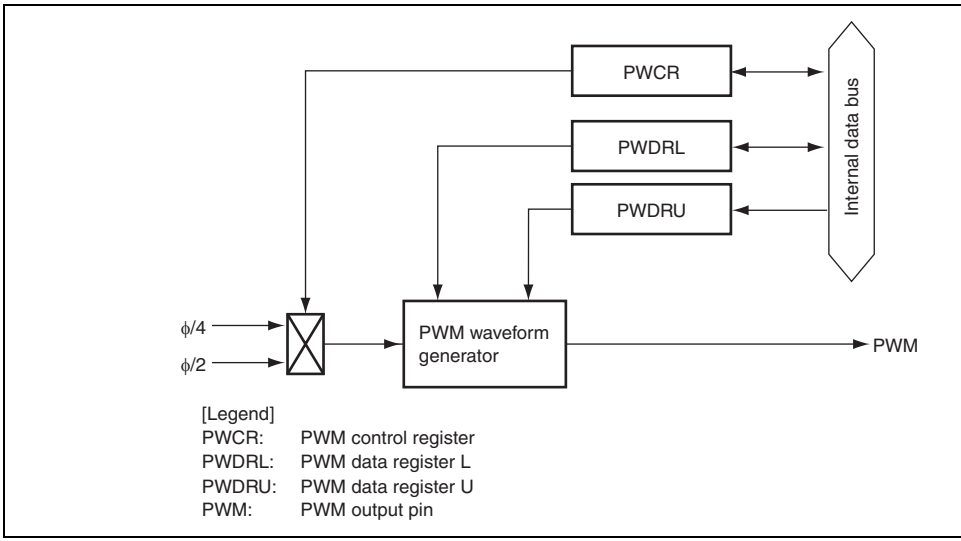


Figure 16.1 Block Diagram of 14-Bit PWM

16.2 Input/Output Pin

Table 16.1 shows the 14-bit PWM pin configuration.

Table 16.1 Pin Configuration

Name	Abbreviation	I/O	Function
14-bit PWM square-wave output	PWM	Output	14-bit PWM square-wave o

PWCR selects the conversion period.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved
6	—	1	—	These bits are always read as 1, and cannot b modified.
5	—	1	—	
4	—	1	—	
3	—	1	—	
2	—	1	—	
1	—	1	—	
0	PWCR0	0	R/W	Clock Select 0: The input clock is $\phi/2$ ($t\phi = 2/\phi$) — The conversion period is $16384/\phi$, with minimum modulation width of $1/\phi$ 1: The input clock is $\phi/4$ ($t\phi = 4/\phi$) — The conversion period is $32768/\phi$, with minimum modulation width of $2/\phi$

[Legend] $t\phi$: Period of PWM clock input

PWDRU and PWDRL are initialized to H'C000.

16.4 Operation

When using the 14-bit PWM, set the registers in this sequence:

1. Set the PWM bit in the port mode register 1 (PMR1) to set the P11/PWM pin to func PWM output pin.
2. Set the PWCR0 bit in PWCR to select a conversion period of either.
3. Set the output waveform data in PWDRU and PWDRL. Be sure to write byte data fi PWDRL and then to PWDRU. When the data is written in PWDRU, the contents of registers are latched in the PWM waveform generator, and the PWM waveform gene data is updated in synchronization in synchronization with internal signals.

One conversion period consists of 64 pulses, as shown in figure 16.2. The total high-lev during this period (T_H) corresponds to the data in PWDRU and PWDRL. This relation c expressed as follows:

$$T_H = (\text{data value in PWDRU and PWDRL} + 64) \times t\phi/2$$

where $t\phi$ is the period of PWM clock input: $2/\phi$ (bit PWCR0 = 0) or $4/\phi$ (bit PWCR0 = 1 If the data value in PWDRU and PWDRL is from H'FFC0 to H'FFFF, the PWM output When the data value is H'C000, T_H is calculated as follows:

$$T_H = 64 \times t\phi/2 = 32\ t\phi$$

SCI3). Since basic functions are identical for each of the three channels (SCI3, SCI3_2, a
SCI3_3), separate explanations are not given in this section.

17.1 Features

- Choice of asynchronous or clock synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and re
  be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuou
  transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected
- External clock or on-chip baud rate generator can be selected as a transfer clock sou
- Six interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, overrun error, framing error, a
  error.
- Noise canceller (only for SCI3_3)

Asynchronous mode:

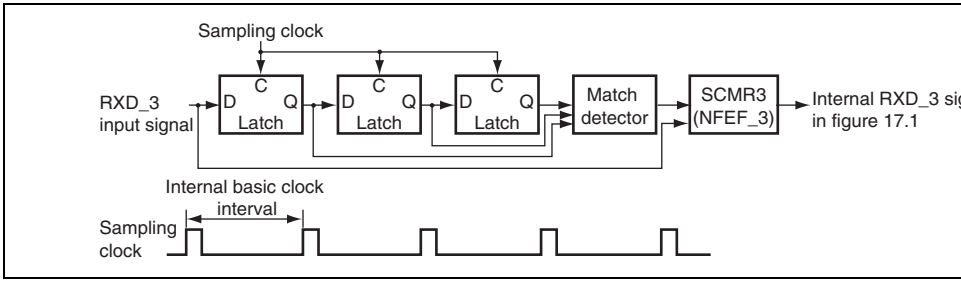
- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RXD pin level directly in the
  framing error

			SCR3	H'FFFFAA	
			TDR	H'FFFFAB	
			SSR	H'FFFFAC	
			RDR	H'FFFFAD	
			RSR	—	
			TSR	—	
Channel 2	SCI3_2	SCK3_2 RXD_2 TXD_2	SMR_2	H'FFF740	Nor
			BRR_2	H'FFF741	
			SCR3_2	H'FFF742	
			TDR_2	H'FFF743	
			SSR_2	H'FFF744	
			RDR_2	H'FFF745	
			RSR_2	—	
			TSR_2	—	
Channel 3	SCI3_3	SCK3_3 RXD_3 TXD_3	SMR_3	H'FFF600	Yes
			BRR_3	H'FFF601	
			SCR3_3	H'FFF602	
			TDR_3	H'FFF603	
			SSR_3	H'FFF604	
			RDR_3	H'FFF605	
			RSR_3	—	
			TSR_3	—	
			SMCR_3*[1]	H'FFF608	

2	NFEN_3	0	R/W	Noise Cancel Function Select When COM in SMR is cleared to 0 and this bit is se noise in the RXD_3 input signal is taken.
1	TXD_3	0	R/W	TXD_3 Pin Select Selects PH2/TXD_3 pin function. 0: General input pin is selected 1: TXD_3 output pin is selected
0	MSTS3_3	0	R/W	SCI3_3 Module Standby When this bit is set to 1, SCI3_3 enters in the stand

- Noise canceller

  The RXD_3 input signal is loaded internally via the noise canceller. The noise cance consists of three latch circuits and match detection circuit connected in series. The R input signal is sampled on the basic clock with a frequency 16 times the transfer rate level is passed forward to the next circuit when outputs of three latches match. Wher outputs are not match, previous value is retained. In other word, when the same leve retained more than three clocks, the input signal is acknowledged as a signal. When changed within three clocks, the change is acknowledged as not a signal change but



Block Diagram of Noise Canceller

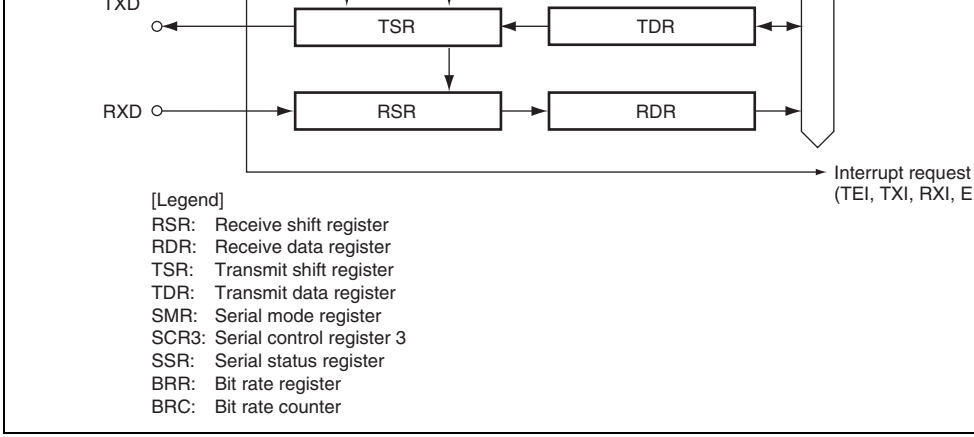


Figure 17.1 Block Diagram of SCI3

17.2 Input/Output Pins

Table 17.2 shows the SCI3 pin configuration.

Table 17.2 Pin Configuration

Pin Name	Abbreviation	I/O	Function
SCI3 clock	SCK3	I/O	SCI3 clock input/output
SCI3 receive data input	RXD	Input	SCI3 receive data input
SCI3 transmit data output	TXD	Output	SCI3 transmit data output

- Serial status register (SSR)
- Bit rate register (BRR)
- Serial mode control register 3 (SMCR3)

17.3.1 Receive Shift Register (RSR)

RSR is a shift register that is used to receive serial data input from the RXD pin and con
parallel data. When one frame of data has been received, it is transferred to RDR automa
RSR cannot be directly accessed by the CPU.

17.3.2 Receive Data Register (RDR)

RDR is an 8-bit register that stores received data. When the SCI3 has received one fram
data, it transfers the received serial data from RSR to RDR, where it is stored. After this
receive-enabled. As RSR and RDR function as a double buffer in this way, continuous r
operations are possible. After confirming that the RDRF bit in SSR is set to 1, read RDR
once. RDR cannot be written to by the CPU. RDR is initialized to H'00.

17.3.3 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the
transfers transmit data from TDR to TSR automatically, then sends the data that starts fr
LSB to the TXD pin. TSR cannot be directly accessed by the CPU.

17.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI3's serial transfer format and select the baud rate generator clo source.

Bit	Bit Name	Initial Value	R/W	Description
7	COM	0	R/W	Communication Mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mo 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to tran before transmission, and the parity bit is checked in r
4	PM	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits For reception, only the first stop bit is checked, regar the value in the bit. If the second stop bit is 0, it is tre the start bit of the next transmit character.

				01: ϕ/4 clock (n = 1) 10: ϕ/16 clock (n = 2) 11: ϕ/64 clock (n = 3) For the relationship between the bit rate register set the baud rate, see section 17.3.8, Bit Rate Register is the decimal representation of the value of n in BR section 17.3.8, Bit Rate Register (BRR)).

17.3.6 Serial Control Register 3 (SCR3)

SCR3 is a register that enables or disables SCI3 transfer operations and interrupt request
also used to select the transfer clock source. For details on interrupt requests, see section
Interrupt Requests.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, the TXI interrupt requ enabled.
6	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrup are enabled.
5	TE	0	R/W	Transmit Enable When this bit s set to 1, transmission is enabl
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled.

2	TEIE	0	R/W	Transmit End Interrupt Enable When this bit is set to 1, TEI interrupt request i enabled.
1	CKE1	0	R/W	Clock Enable 0 and 1
0	CKE0	0	R/W	Selects the clock source. • Asynchronous mode 00: On-chip baud rate generator 01: On-chip baud rate generator Outputs a clock of the same frequency as t rate from the SCK3 pin. 10: External clock Inputs a clock with a frequency 16 times th from the SCK3 pin. 11: Reserved • Clock synchronous mode 00: On-chip clock (SCK3 pin functions as clock 01: Reserved 10: External clock (SCK3 pin functions as clock 11: Reserved

				• When the TE bit in SCR3 is 0 • When data is transferred from TDR to TSR [Clearing conditions] • When 0 is written to TDRE after reading TDRE • When the transmit data is written to TDR
6	RDRF	0	R/W	Receive Data Register Full Indicates that the received data is stored in RDR [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • When 0 is written to RDRF after reading RDRF • When data is read from RDR
5	OER	0	R/W	Overrun Error [Setting condition] • When an overrun error occurs in reception [Clearing condition] • When 0 is written to OER after reading OER

				[Clearing condition] • When 0 is written to PER after reading PER
2	TEND	1	R	Transmit End [Setting conditions] • When the TE bit in SCR3 is 0 • When TDRE = 1 at transmission of the last 1-frame serial transmit character [Clearing conditions] • When 0 is written to TDRE after reading TDR • When the transmit data is written to TDR
1	MPBR	0	R	Multiprocessor Bit Receive MPBR stores the multiprocessor bit in the received character data. When the RE bit in SCR3 is cleared to 0, its state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer MPBT stores the multiprocessor bit to be added to the transmit character data.

[Asynchronous Mode]

$$N = \frac{\phi}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

$$\text{Error (\%)} = \left\{ \frac{\phi \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

[Clock Synchronous Mode]

$$N = \frac{\phi}{8 \times 2^{2n-1} \times B} \times 10^6 - 1$$

[Legend]

B: Bit rate (bit/s)

N: BRR setting for baud rate generator ($0 \leq N \leq 255$)

ϕ: Operating frequency (MHz)

n: CSK1 and CSK0 settings in SMR ($0 \leq n \leq 3$)

2400	0	51	0.16	0	63	0.00	0	64	0.16	0	77
4800	0	25	0.16	0	31	0.00	0	32	–1.36	0	38
9600	0	12	0.16	0	15	0.00	0	15	1.73	0	19
19200	0	6	–6.99	0	7	0.00	0	7	1.73	0	9
31250	0	3	0.00	0	4	–1.70	0	4	0.00	0	5
38400	0	2	8.51	0	3	0.00	0	3	1.73	0	4

	Operating Frequency ϕ (MHz)									
	6.144			7.3728			8			9.8
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N
110	2	108	0.08	2	130	–0.07	2	141	0.03	2	174
150	2	79	0.00	2	95	0.00	2	103	0.16	2	127
300	1	159	0.00	1	191	0.00	1	207	0.16	1	255
600	1	79	0.00	1	95	0.00	1	103	0.16	1	127
1200	0	159	0.00	0	191	0.00	0	207	0.16	0	255
2400	0	79	0.00	0	95	0.00	0	103	0.16	0	127
4800	0	39	0.00	0	47	0.00	0	51	0.16	0	63
9600	0	19	0.00	0	23	0.00	0	25	0.16	0	31
19200	0	9	0.00	0	11	0.00	0	12	0.16	0	15
31250	0	5	2.40	0	6	5.33	0	7	0.00	0	9
38400	0	4	0.00	0	5	0.00	0	6	-6.99	0	7

[Legend]

—: A setting is available but error occurs

2400	0	129	0.16	0	155	0.16	0	159	0.00	0	18
4800	0	64	0.16	0	77	0.16	0	79	0.00	0	90
9600	0	32	–1.36	0	38	0.16	0	39	0.00	0	45
19200	0	15	1.73	0	19	–2.34	0	19	0.00	0	22
31250	0	9	0.00	0	11	0.00	0	11	2.40	0	13
38400	0	7	1.73	0	9	–2.34	0	9	0.00	—	—

	Operating Frequency ϕ (MHz)										
	14.7456			16			18				
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N
110	3	64	0.70	3	70	0.03	3	79	–0.12	3	88
150	2	191	0.00	2	207	0.16	2	233	0.16	3	64
300	2	95	0.00	2	103	0.16	2	116	0.16	2	12
600	1	191	0.00	1	207	0.16	1	233	0.16	2	64
1200	1	95	0.00	1	103	0.16	1	116	0.16	1	12
2400	0	191	0.00	0	207	0.16	0	233	0.16	1	64
4800	0	95	0.00	0	103	0.16	0	116	0.16	0	12
9600	0	47	0.00	0	51	0.16	0	58	–0.96	0	64
19200	0	23	0.00	0	25	0.16	0	28	1.02	0	32
31250	0	14	–1.70	0	15	0.00	0	17	0.00	0	19
38400	0	11	0.00	0	12	0.16	0	14	–2.34	0	15

[Legend]

—: A setting is available but error occurs

10	312500	0	0	20	625000	0	

Table 17.5 Examples of BRR Settings for Various Bit Rates (Clock Synchronous Mode

Bit Rate (bit/s)	Operating Frequency ϕ (MHz)										
	4		8		10		16		18		
	n	N	n	N	n	N	n	N	n	N	n
110	—	—	—	—	—	—			—	—	—
250	2	249	3	124	—	—	3	249	—	—	—
500	2	124	2	249	—	—	3	124	3	140	3
1k	1	249	2	124	—	—	2	249	3	69	3
2.5k	1	99	1	199	1	249	2	99	2	112	2
5k	0	199	1	99	1	124	1	199	1	224	1
10k	0	99	0	199	0	249	1	99	1	112	1
25k	0	39	0	79	0	99	0	159	0	179	0
50k	0	19	0	39	0	49	0	79	0	89	0
100k	0	9	0	19	0	24	0	39	0	44	0
250k	0	3	0	7	0	9	0	15	0	17	0
500k	0	1	0	3	0	4	0	7	0	8	0
1M	0	0*	0	1	—	—	0	3	0	4	0
2M			0	0*	—	—	0	1	—	—	—
2.5M					0	0*	—	—	—	—	0
4M							0	0*	—	—	—

[Legend]

Blank: No setting is available.

—: A setting is available but error occurs.

*: Continuous transfer is not possible.

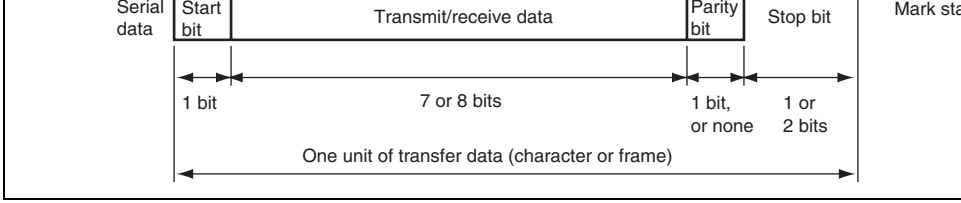


Figure 17.2 Data Format in Asynchronous Communication

17.4.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external cloc the SCK3 pin can be selected as the SCI3's serial clock, according to the setting of the C SMR and the CKE0 and CKE1 bits in SCR3. When an external clock is input at the SCI clock frequency should be 16 times the bit rate used.

When the SCI3 is operated on an internal clock, the clock can be output from the SCK3 frequency of the clock output in this case is equal to the bit rate, and the phase is such th rising edge of the clock is in the middle of the transmit data, as shown in figure 17.3.

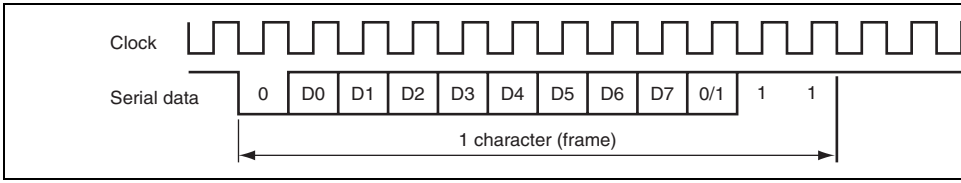
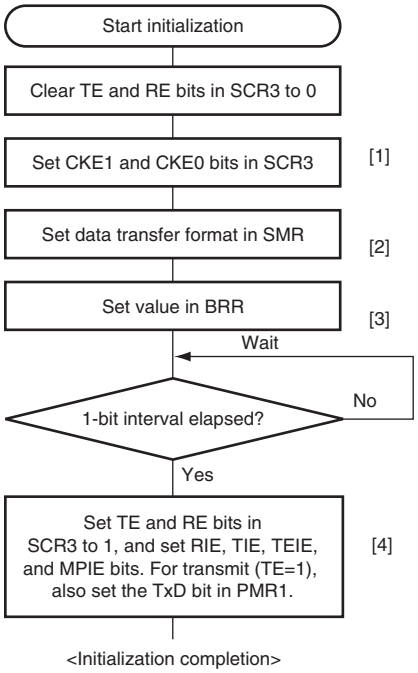


Figure 17.3 Relationship between Output Clock and Transfer Data Phas (Asynchronous Mode)(Example with 8-Bit Data, Parity, Two Stop Bits)



[1] Set the clock selection in SCR3. Be sure to clear bits RIE, TIE, TEIE, and MPIE, and bits TE and RE, to 0.

When the clock output is selected in asynchronous mode, clock is output immediately after CKE1 and CKE0 settings are made. When the clock output is selected at reception in clocked synchronous mode, clock is output immediately after CKE1, CKE0, and RE are set to 1.

[2] Set the data transfer format in SMR.

[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external clock is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR3 to 1. RE settings enable the RXD pin to be used. For transmission, set the TXD bit in PMR1 to 1 to enable the TXD output pin to be used. Also set the RIE, TIE, TEIE, and MPIE bits, depending on whether interrupts are required. In asynchronous mode, the output pin level is in the mark state for transmission and the input in level is in the idle state for reception. SCI3 waites for a start bit in the idle state. SCI3 is ready for transmission after 1 is output for a signal frame.

Figure 17.4 Sample SCI3 Initialization Flowchart

to TDR before transmission of the current transmit data has been completed.

3. The SCI3 checks the TDRE flag at the timing for sending the stop bit.
4. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, a serial transmission of the next frame is started.
5. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then state" is entered, in which 1 is output. If the TEIE bit in SCR3 is set to 1 at this time, interrupt request is generated.
6. Figure 17.6 shows a sample flowchart for transmission in asynchronous mode.

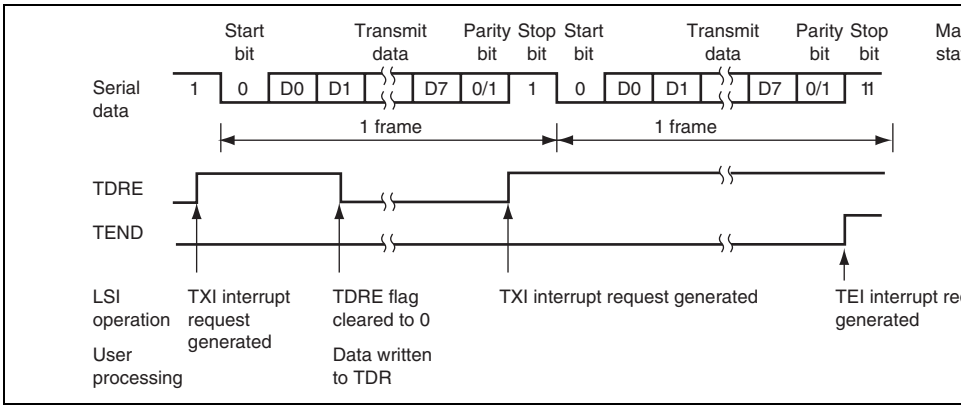


Figure 17.5 Example of SCI3 Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

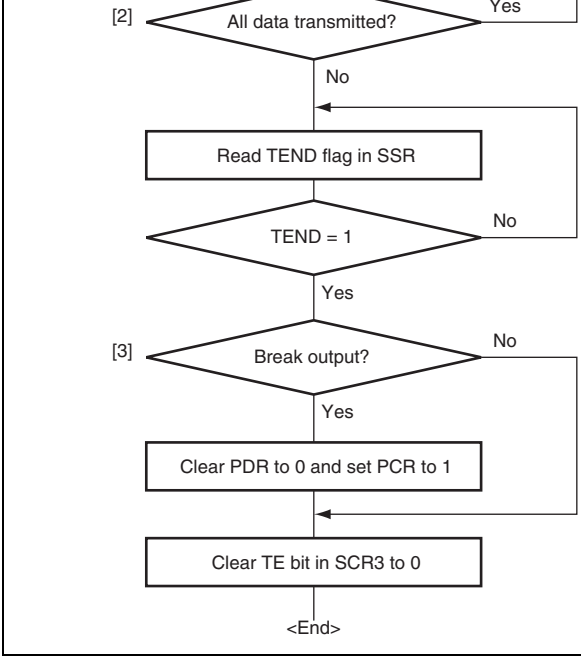


Figure 17.6 Sample Serial Transmission Data Flowchart (Asynchronous Mo

5. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transfer RDR. If the RIE bit in SCR3 is set to 1 at this time, an ERI interrupt request is gener
4. If a framing error is detected (when the stop bit is 0), the FER bit in SSR is set to 1 a data is transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an ERI inte request is generated.
5. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive d transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an RXI interrupt re generated. Continuous reception is possible because the RXI interrupt routine reads t data transferred to RDR before reception of the next receive data has been completed

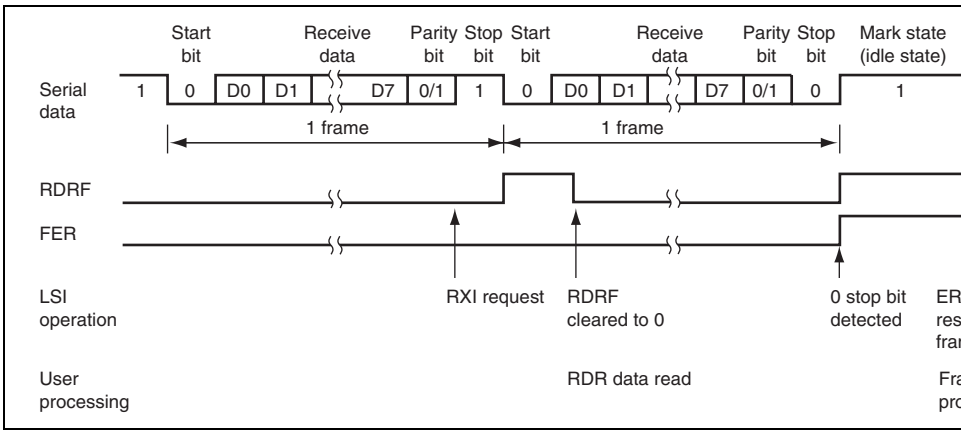
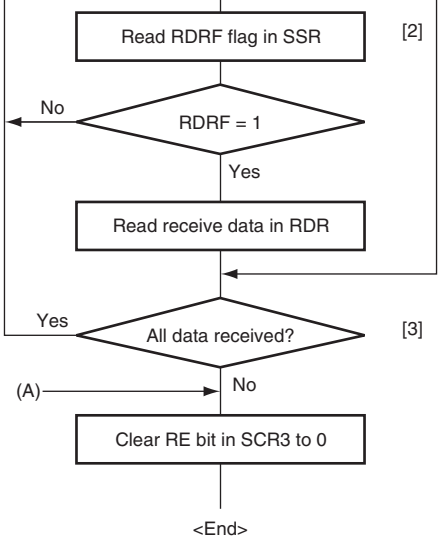


Figure 17.7 Example of SCI3 Reception in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

0	0	1	0	Transferred to RDR	Framing error
0	0	0	1	Transferred to RDR	Parity error
1	1	1	0	Lost	Overrun error + framin
1	1	0	1	Lost	Overrun error + parity
0	0	1	1	Transferred to RDR	Framing error + parity
1	1	1	1	Lost	Overrun error + framin parity error

Note: * The RDRF flag retains the state it had before data reception.



The RDRF flag is cleared automatic

[4] If a receive error occurs, read the O and FER flags in SSR to identify th After performing the appropriate er processing, ensure that the OER, F FER flags are all cleared to 0. Rec cannot be resumed if any of these set to 1. In the case of a framing e break can be detected by reading t of the input port corresponding to th pin.

Figure 17.8 Sample Serial Reception Data Flowchart (Asynchronous Mode)

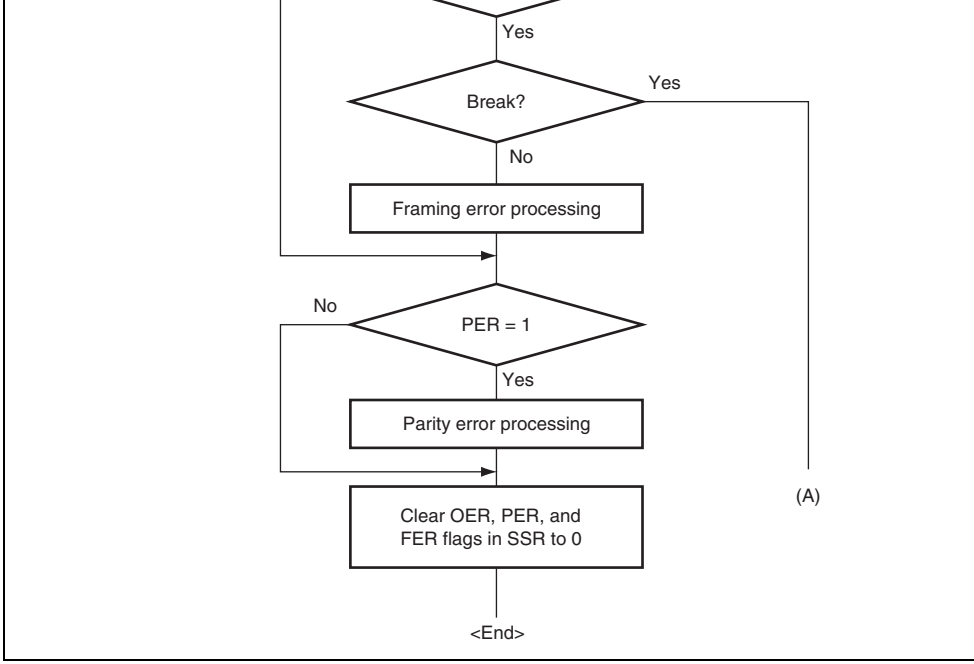


Figure 17.8 Sample Serial Reception Data Flowchart (Asynchronous Mode)

communication through the use of a common clock. Both the transmitter and the receive
have a double-buffered structure, so data can be read or written during transmission or r
enabling continuous data transfer.

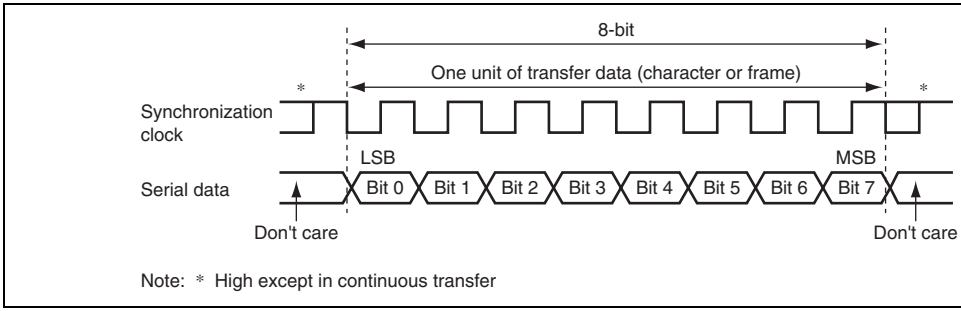


Figure 17.9 Data Format in Clock Synchronous Communication

17.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK3 pin can be selected, according to the setting of bit in SMR and CKE0 and CKE1 bits in SCR3. When the SCI3 is operated on an interna the synchronization clock is output from the SCK3 pin. Eight synchronization clock pul output in the transfer of one character, and when no transfer is performed the clock is fi

17.5.2 SCI3 Initialization

Before transmitting and receiving data, the SCI3 should be initialized as described in a s flowchart in figure 17.4.

mode has been specified, and synchronized with the input clock when use of an exter
has been specified. Serial data is transmitted sequentially from the LSB (bit 0), from t
pin.

4. The SCI3 checks the TDRE flag at the timing for sending the MSB (bit 7).
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial trans
of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TDRE flag mai
output state of the last bit. If the TEIE bit in SCR3 is set to 1 at this time, a TEI interru
request is generated.
7. The SCK3 pin is fixed high at the end of transmission.

Figure 17.11 shows a sample flow chart for serial data transmission. Even if the TDRE fl
cleared to 0, transmission will not start while a receive error flag (OER, FER, or PER) is
Make sure that the receive error flags are cleared to 0 before starting transmission.

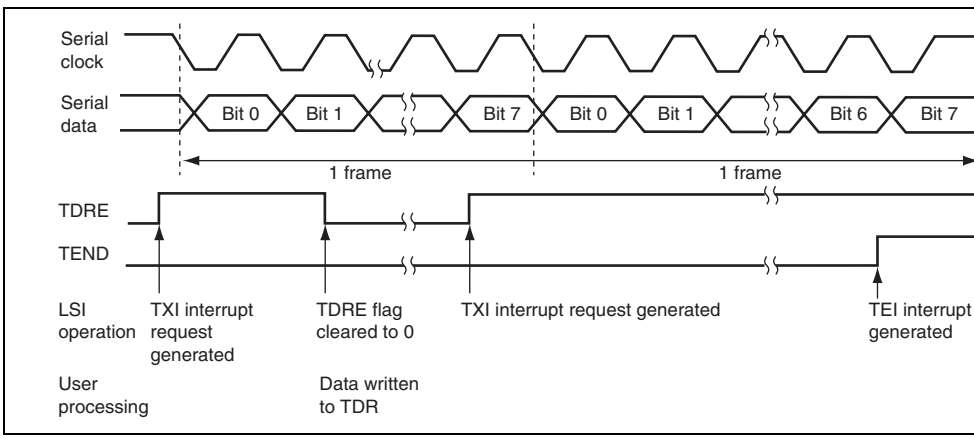


Figure 17.10 Example of SCI3 Transmission in Clock Synchronous Mode

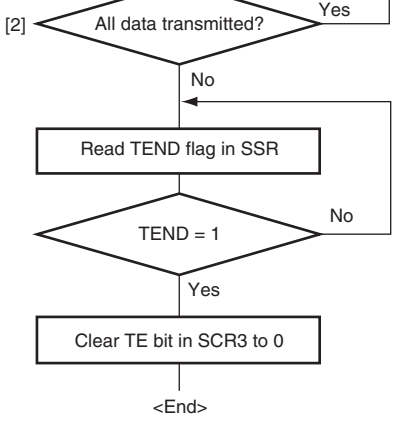


Figure 17.11 Sample Serial Transmission Flowchart (Clock Synchronous M

time, an ERI interrupt request is generated, receive data is not transferred to RDR, and
RDRF flag remains to be set to 1.

4. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive da
transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an RXI interrupt req
generated.

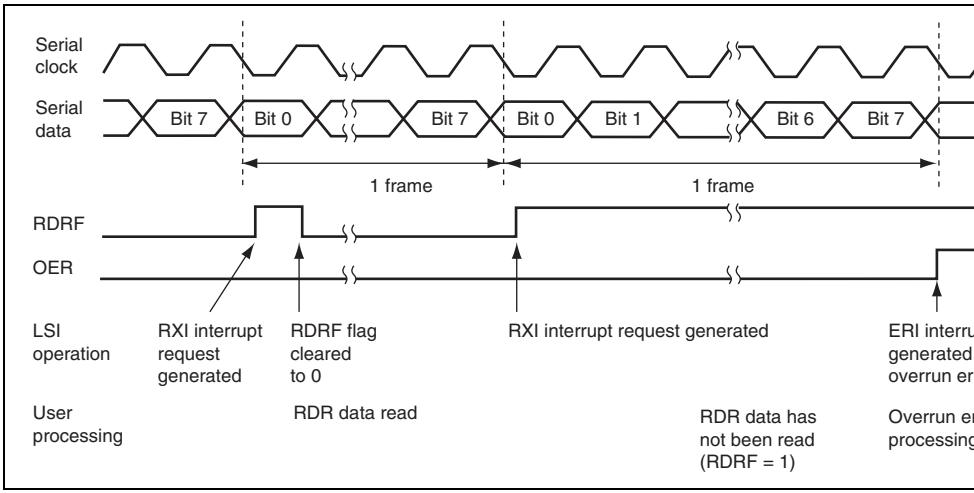
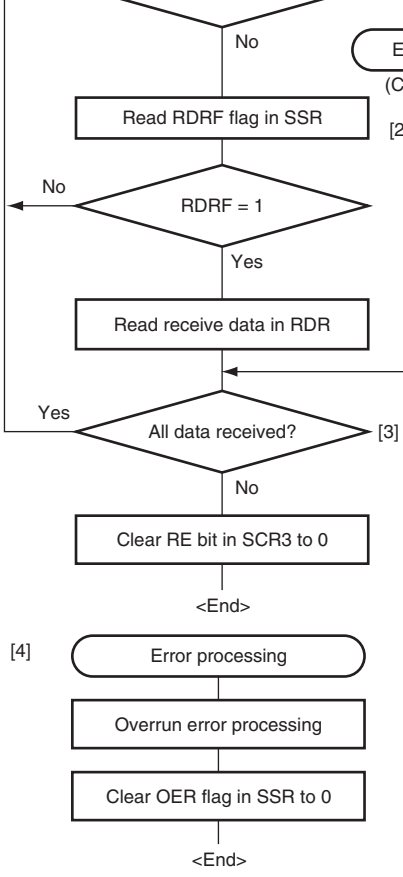


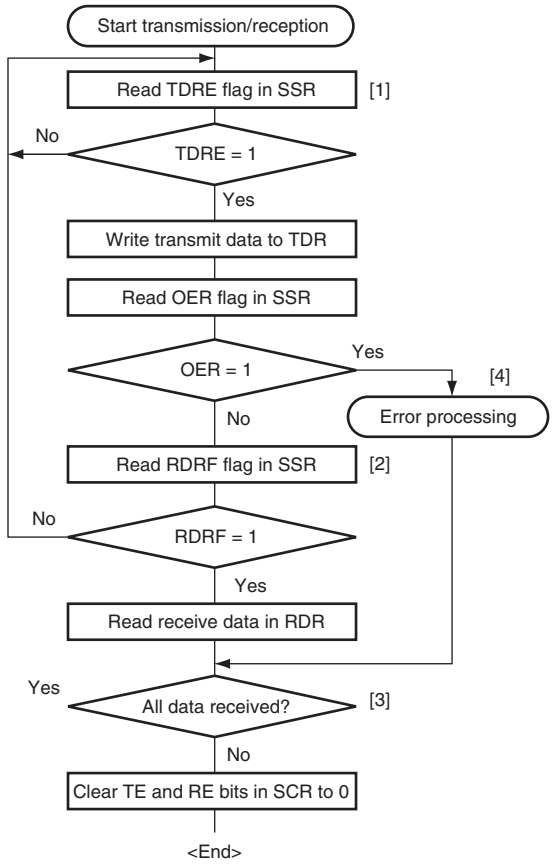
Figure 17.12 Example of SCI3 Reception in Clock Synchronous Mode



[3] To continue serial reception, before
MSB (bit 7) of the current frame is
reading the RDRF flag and reading
should be finished. When data is re
RDR, the RDRF flag is automatica
cleared to 0.

[4] If an overrun error occurs, read the
flag in SSR, and after performing th
appropriate error processing, clear
flag to 0. Reception cannot be res
the OER flag is set to 1.

Figure 17.13 Sample Serial Reception Flowchart (Clock Synchronous Mod



[1] Read SSR and check that the TDR is set to 1, then write transmit data TDR.
When data is written to TDR, the TD flag is automatically cleared to 0.

[2] Read SSR and check that the RDR is set to 1, then read the receive da RDR.
When data is read from RDR, the R flag is automatically cleared to 0.

[3] To continue serial transmission/ reception, before the MSB (bit 7) of current frame is received, finish rea the RDRF flag, reading RDR. Also, before the MSB (bit 7) of the curren frame is transmitted, read 1 from th TDRE flag to confirm that writing is possible. Then write data to TDR.
When data is written to TDR, the TD flag is automatically cleared to 0. W data is read from RDR, the RDRF fl automatically cleared to 0.

[4] If an overrun error occurs, read the flag in SSR, and after performing th appropriate error processing, clear OER flag to 0. Transmission/recep cannot be resumed if the OER flag to 1.
For overrun error processing, see fi 17.13.

Figure 17.14 Sample Flowchart of Simultaneous Serial Transmit and Receive Op (Clock Synchronous Mode)

cycle is a data transmission cycle. Figure 17.13 shows an example of inter-processor
communication using the multiprocessor format. The transmitting station first sends the
of the receiving station with which it wants to perform serial communication as data wit
multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit
When data with a 1 multiprocessor bit is received, the receiving station compares that da
own ID. The station whose ID matches then receives the data sent next. Stations whose
match continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI3 uses the MPIE bit in SCR3 to implement this function. When the MPIE bit is
transfer of receive data from RSR to RDR, error flag detection, and setting the SSR statu
RDRF, FER, and OER, to 1, are inhibited until data with a 1 multiprocessor bit is receiv
reception of a receive character with a 1 multiprocessor bit, the MPBR bit in SSR is set
the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE bit i
set to 1 at this time, an RXI interrupt is generated.

When the multiprocessor format is selected, the parity bit setting is rendered invalid. Al
settings are the same as those in normal asynchronous mode. The clock used for multipr
communication is the same as that in normal asynchronous mode.

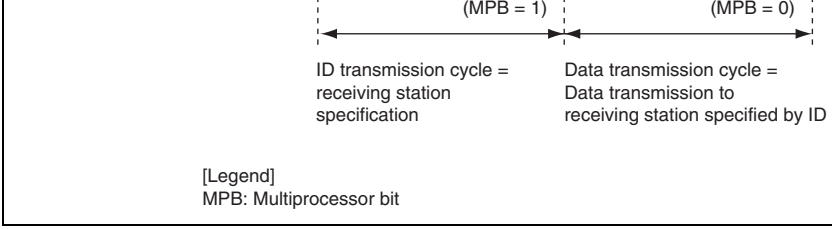
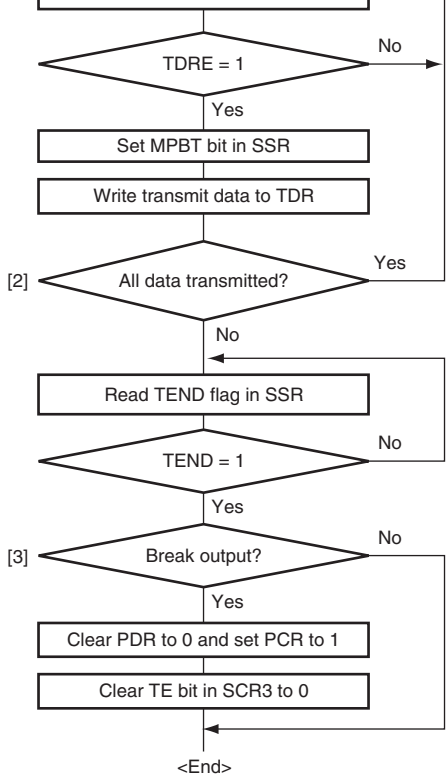


Figure 17.15 Example of Inter-Processor Communication Using Multiprocessor F
(Transmission of Data H'AA to Receiving Station A)

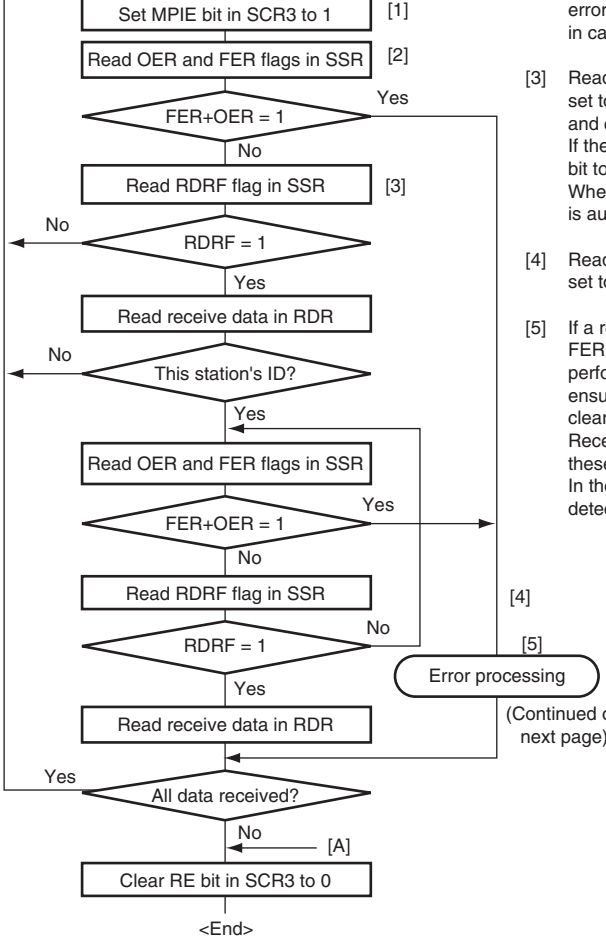


TDR, the TDRE flag is automatically cleared to 0.

[2] To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

[3] To output a break in serial transmission, set the port PCR to 1, clear PDR to 0, then clear the TE bit in SCR3 to 0.

Figure 17.16 Sample Multiprocessor Serial Transmission Flowchart



errors. Receive error processing is perfo
in cases where a receive error occurs.

[3] Read SSR and check that the RDRF flag
set to 1, then read the receive data in RD
and compare it with this station's ID.
If the data is not this station's ID, set the
bit to 1 again.
When data is read from RDR, the RDRF
is automatically cleared to 0.

[4] Read SSR and check that the RDRF flag
set to 1, then read the data in RDR.

[5] If a receive error occurs, read the OER a
FER flags in SSR to identify the error. Af
performing the appropriate error process
ensure that the OER and FER flags are a
cleared to 0.
Reception cannot be resumed if either of
these flags is set to 1.
In the case of a framing error, a break ca
detected by reading the RxD pin value.

Figure 17.17 Sample Multiprocessor Serial Reception Flowchart (1)

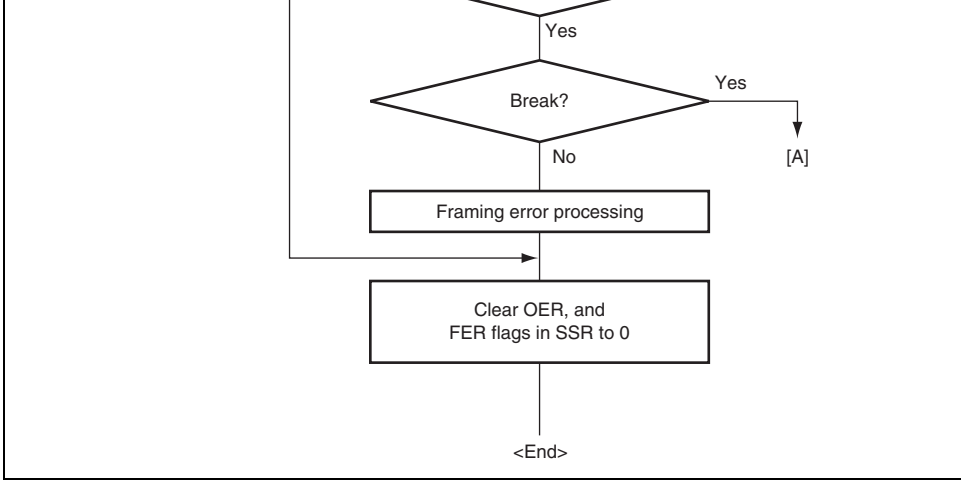


Figure 17.17 Sample Multiprocessor Serial Reception Flowchart (2)

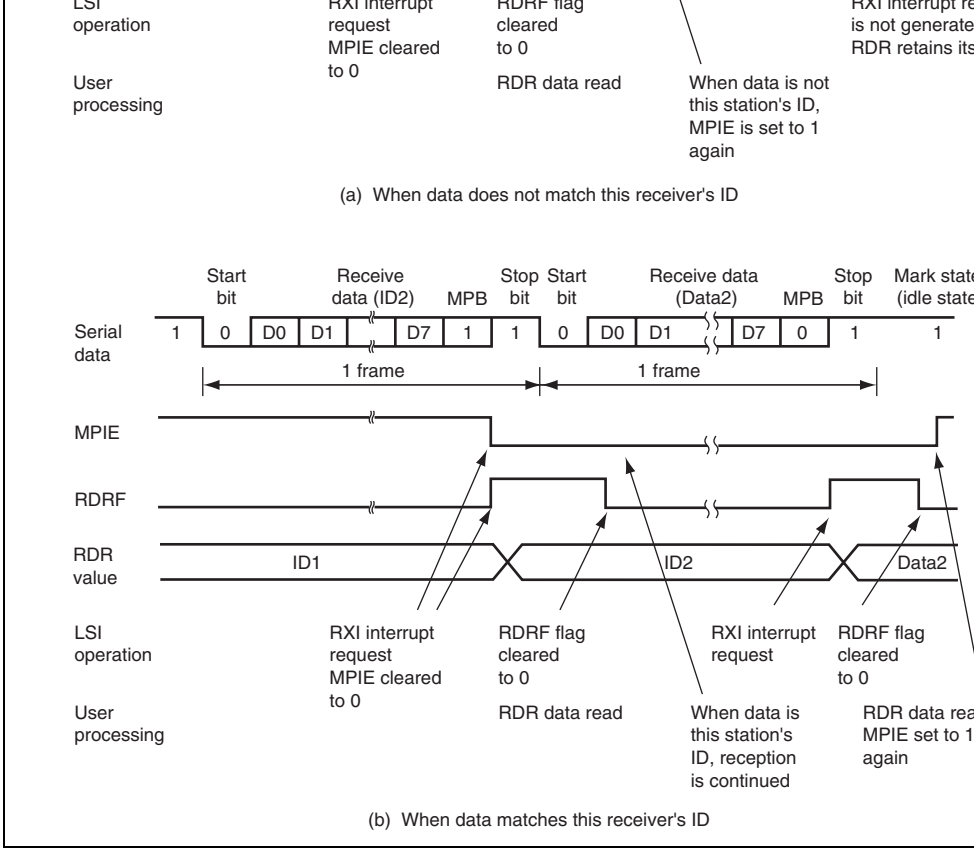


Figure 17.18 Example of SCI3 Reception Using Multiprocessor Format (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

Transmission End	TEI	Setting TEND in SSR
Receive Error	ERI	Setting OER, FER, and PER in SSR

The initial value of the TDRE flag in SSR is 1. Thus, when the TIE bit in SCR3 is set to
transferring the transmit data to TDR, a TXI interrupt request is generated even if the tra
is not ready. The initial value of the TEND flag in SSR is 1. Thus, when the TEIE bit in
set to 1 before transferring the transmit data to TDR, a TEI interrupt request is generated
the transmit data has not been sent. It is possible to make use of the most of these interru
requests efficiently by transferring the transmit data to TDR in the interrupt routine. To
the generation of these interrupt requests (TXI and TEI), set the enable bits (TIE and TE
correspond to these interrupt requests to 1, after transferring the transmit data to TDR.

When the TXD or TXD2 bit in PMR1 or the TXD_3 bit in SMCR is 1, the TXD pin is us
I/O port whose direction (input or output) and level are determined by PCR and PDR. Th
used to set the TXD pin to mark state (high level) or send a break during serial data transm
To maintain the communication line at mark state until TE is set to 1, set both PCR and P
and also set the TXD bit to 1. Then, the TXD pin becomes an I/O port, and 1 is output fro
TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to
then set the TXD bit to 1. At this time, regardless of the current transmission state, the TX
becomes an I/O port, and 0 is output from the TXD pin.

17.8.3 Receive Error Flags and Transmit Operations (Clock Synchronous Mode

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1,
the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting
transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is
to 0.

... Formula (1)

[Legend]

N: Ratio of bit rate to clock (N = 16)

D: Clock duty (D = 0.5 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0 formula (1), the reception margin can be given by the formula.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allow system design.

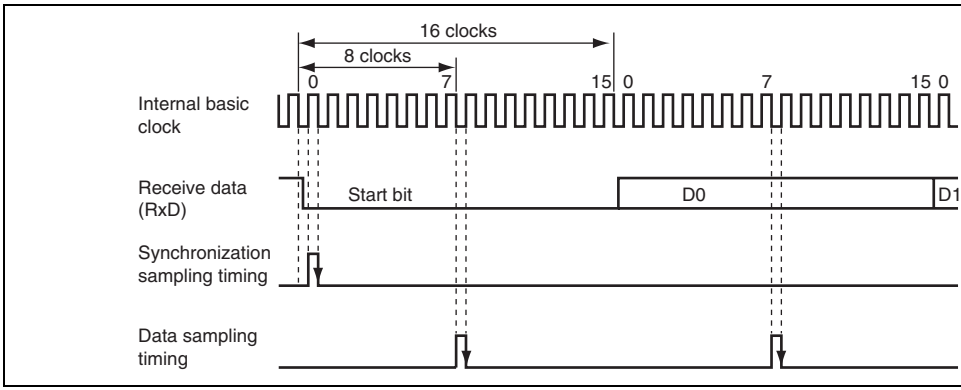


Figure 17.19 Receive Data Sampling Timing in Asynchronous Mode

18.1 Features

- Selection of I^2C format or clocked synchronous serial format
- Continuous transmission/reception

  Since the shift register, transmit data register, and receive data register are independe each other, the continuous transmission/reception can be performed.

I^2C bus format:

- Start and stop conditions generated automatically in master mode
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Bit synchronization/wait function

  In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically.

  If transmission/reception is not yet possible, set the SCL to low until preparations ar completed.
- Six interrupt sources

  Transmit data empty (including slave-address match), transmit end, receive data full slave-address match), arbitration lost, NACK detection, and stop condition detection
- Direct bus drive

  Two pins, SCL and SDA pins, function as NMOS open-drain outputs when the bus d function is selected.

Clocked synchronous format:

- Four interrupt sources

  Transmit-data-empty, transmit-end, receive-data-full, and overrun error

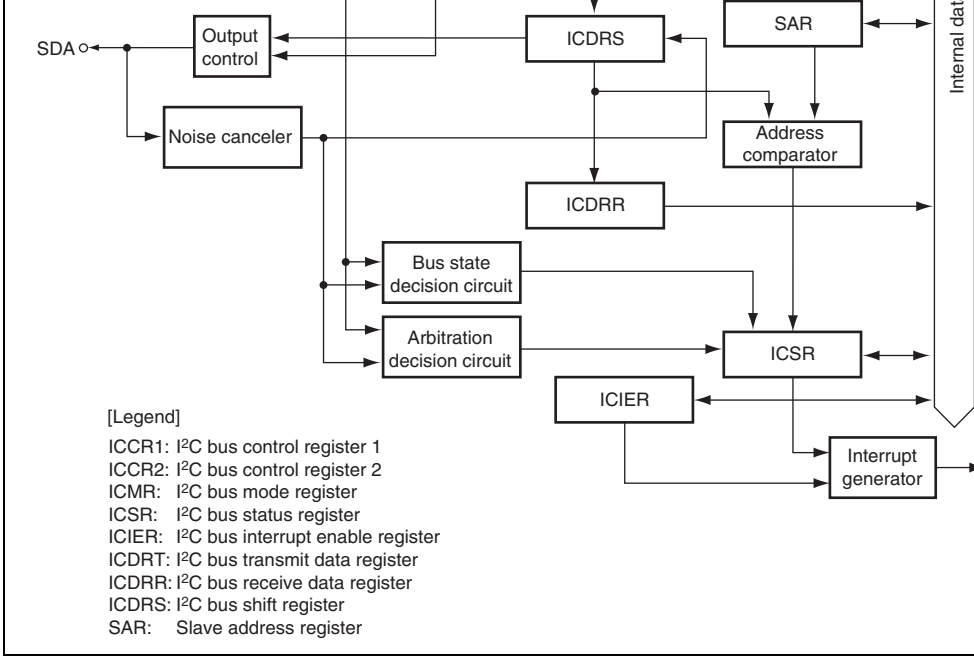


Figure 18.1 Block Diagram of I²C Bus Interface 2

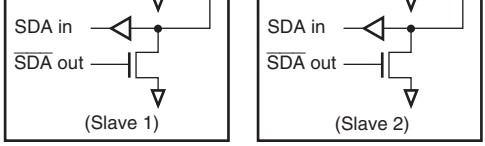


Figure 18.2 External Circuit Connections of I/O Pins

18.2 Input/Output Pins

Table 18.1 summarizes the input/output pins used by the I²C bus interface 2.

Table 18.1 Pin Configuration

Name	Abbreviation	I/O	Function
Serial clock	SCL	I/O	IIC serial clock input/output
Serial data	SDA	I/O	IIC serial data input/output

- I²C bus transmit data register (ICDRT)
- I²C bus receive data register (ICDRR)
- I²C bus shift register (ICDRS)

18.3.1 I²C Bus Control Register 1 (ICCR1)

ICCR1 enables or disables the I²C bus interface 2, controls transmission or reception, and
master or slave mode, transmission or reception, and transfer clock frequency in master m

Bit	Bit Name	Initial Value	R/W	Description
7	ICE	0	R/W	I²C Bus Interface Enable 0: This module is halted. (SCL and SDA pins a port function.) 1: This bit is enabled for transfer operations. (S SDA pins are bus drive state.)
6	RCVD	0	R/W	Reception Disable This bit enables or disables the next operation TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception

				agree with the slave address that is set to SA eighth bit is 1, TRS is automatically set to 1. I overrun error occurs in master mode with the synchronous serial format, MST is cleared to slave receive mode is entered. Operating modes are described below accord MST and TRS combination. When clocked sy serial format is selected and MST is 1, clock i 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode
3	CKS3	0	R/W	Transfer Clock Select 3 to 0
2	CKS2	0	R/W	These bits should be set according to the nec transfer rate (see table 18.2) in master mode. mode, these bits are used for reservation of t time in transmit mode. The time is 10 t_{cyc} when 0 and 20 t_{cyc} when CKS3 = 1.
1	CKS1	0	R/W	
0	CKS0	0	R/W	

		1	0	φ/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz
			1	φ/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz
1	0	0	0	φ/56	89.3 kHz	143 kHz	179 kHz	286 kHz
			1	φ/80	62.5 kHz	100 kHz	125 kHz	200 kHz
		1	0	φ/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz
			1	φ/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz
	1	0	0	φ/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz
			1	φ/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz
		1	0	φ/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz
			1	φ/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz

				format, this bit has no meaning. With the I²C b this bit is set to 1 when the SDA level change high to low under the condition of SCL = high that the start condition has been issued. This cleared to 0 when the SDA level changes fro high under the condition of SCL = high, assu the stop condition has been issued. Write 1 to and 0 to SCP to issue a start condition. Also f procedure when a repeated start condition is Write 0 in BBSY and 0 in SCP to issue a stop To issue start/stop conditions, use the MOV i
6	SCP	1	W	Start/Stop Issue Condition Disable The SCP bit controls the issue of start/stop co master mode. To issue a start condition, write 1 in BBSY an SCP. A repeated start condition is issued in th way. To issue a stop condition, write 0 in BBS SCP. This bit is always read as 1. If 1 is writte data is not stored.
5	SDAO	1	R/W	SDA Output Value Control This bit is used with SDAOP when modifying level of SDA. This bit should not be manipulat transfer. 0: When reading, SDA pin outputs low. When writing, SDA pin is changed to outpu 1: When reading, SDA pin outputs high. When writing, SDA pin is changed to outpu (outputs high by external pull-up resistance

2	—	1	—	Reserved This bit is always read as 1.
1	IICRST	0	R/W	IIC Control Part Reset This bit resets the control part except for I^2C re this bit is set to 1 when hang-up occurs becaus communication failure during I^2C operation, I^2C part can be reset without setting ports and initia registers.
0	—	1	—	Reserved This bit is always read as 1.

				Set this bit to 0 when the I²C bus format is use
6	WAIT	0	R/W	Wait Insertion Bit In master mode with the I²C bus format, this b whether to insert a wait after data transfer exc acknowledge bit. When WAIT is set to 1, after the clock for the final data bit, low period is ex two transfer clocks. If WAIT is cleared to 0, da acknowledge bits are transferred consecutive wait inserted. The setting of this bit is invalid in slave mode I²C bus format or with the clocked synchronou format.
5	—	1	—	Reserved
4	—	1	—	These bits are always read as 1.
3	BCWP	1	R/W	BC Write Protect This bit controls the BC2 to BC0 modifications modifying BC2 to BC0, this bit should be clea and use the MOV instruction. In clock synchro serial mode, BC should not be modified. 0: When writing, values of BC2 to BC0 are se 1: When reading, 1 is always read. When writing, settings of BC2 to BC0 are inva

the clock synchronous serial format, these bits
not be modified.

I^2C Bus Format	Clock Synchronous Seria
000: 9 bits	000: 8 bits
001: 2 bits	001: 1 bits
010: 3 bits	010: 2 bits
011: 4 bits	011: 3 bits
100: 5 bits	100: 4 bits
101: 6 bits	101: 5 bits
110: 7 bits	110: 6 bits
111: 8 bits	111: 7 bits

				disabled. 1: Transmit data empty interrupt request (TXI enabled.
6	TEIE	0	R/W	Transmit End Interrupt Enable This bit enables or disables the transmit end i (TEI) at the rising of the ninth clock while the in ICSR is 1. TEI can be canceled by clearing bit or the TEIE bit to 0. 0: Transmit end interrupt request (TEI) is disa 1: Transmit end interrupt request (TEI) is ena
5	RIE	0	R/W	Receive Interrupt Enable This bit enables or disables the receive data f interrupt request (RXI) and the overrun error i request (ERI) with the clocked synchronous fo when a receive data is transferred from ICDR ICDRR and the RDRF bit in ICSR is set to 1. be canceled by clearing the RDRF or RIE bit 0: Receive data full interrupt request (RXI) an error interrupt request (ERI) with the clocke synchronous format are disabled. 1: Receive data full interrupt request (RXI) an error interrupt request (ERI) with the clocke synchronous format are enabled.

3	STIE	0	R/W	Stop Condition Detection Interrupt Enable 0: Stop condition detection interrupt request (S disabled. 1: Stop condition detection interrupt request (S enabled.
2	ACKE	0	R/W	Acknowledge Bit Judgment Select 0: The value of the receive acknowledge bit is and continuous transfer is performed. 1: If the receive acknowledge bit is 1, continuo transfer is halted.
1	ACKBR	0	R	Receive Acknowledge In transmit mode, this bit stores the acknowled that are returned by the receive device. This bi be modified. 0: Receive acknowledge = 0 1: Receive acknowledge = 1
0	ACKBT	0	R/W	Transmit Acknowledge In receive mode, this bit specifies the bit to be the acknowledge timing. 0: 0 is sent at the acknowledge timing. 1: 1 is sent at the acknowledge timing.

				• When TRS is set • When a start condition (including re-transf been issued • When transmit mode is entered from rece in slave mode [Clearing conditions] • When 0 is written in TDRE after reading T • When data is written to ICDRT with an ins
6	TEND	0	R/W	Transmit End [Setting conditions] • When the ninth clock of SCL rises with the format while the TDRE flag is 1 • When the final bit of transmit frame is sen clock synchronous serial format [Clearing conditions] • When 0 is written in TEND after reading T • When data is written to ICDRT with an ins
5	RDRF	0	R/W	Receive Data Register Full [Setting condition] • When a receive data is transferred from IC ICDRR [Clearing conditions] • When 0 is written in RDRF after reading R • When ICDRR is read with an instruction

3	STOP	0	R/W	Stop Condition Detection Flag [Setting condition] • When a stop condition is detected after fra transfer [Clearing condition] • When 0 is written in STOP after reading ST
2	AL/OVE	0	R/W	Arbitration Lost Flag/Overrun Error Flag This flag indicates that arbitration was lost in m mode with the I^2C bus format and that the final been received while RDRF = 1 with the clocke synchronous format. When two or more master devices attempt to s bus at nearly the same time, if the I^2C bus inter detects data differing from the data it sent, it se 1 to indicate that the bus has been taken by an master. [Setting conditions] • If the internal SDA and SDA pin disagree a of SCL in master transmit mode • When the SDA pin outputs high in master r while a start condition is detected • When the final bit is received with the clock synchronous format while RDRF = 1 [Clearing condition] • When 0 is written in AL/OVE after reading AL/OVE=1

				receive mode. [Clearing condition] • When 0 is written in AAS after reading AA
0	ADZ	0	R/W	General Call Address Recognition Flag This bit is valid in I²C bus format slave receive [Setting condition] • When the general call address is detected receive mode [Clearing condition] • When 0 is written in ADZ after reading AD

18.3.6 Slave Address Register (SAR)

SAR selects the communication format and sets the slave address. When the chip is in s with the I²C bus format, if the upper 7 bits of SAR match the upper 7 bits of the first fra received after a start condition, the chip operates as the slave device.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	SVA6 to SVA0	All 0	R/W	Slave Address 6 to 0 These bits set a unique address in bits SVA6 differing form the addresses of other slave de connected to the I²C bus.
0	FS	0	R/W	Format Select 0: I²C bus format is selected. 1: Clocked synchronous serial format is selec

ICDRR is an 8-bit register that stores the receive data. When data of one byte is received, transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDR receive-only register, therefore the CPU cannot write to this register. The initial value of H'FF.

18.3.9 I^2C Bus Shift Register (ICDRS)

ICDRS is a register that is used to transfer/receive data. In transmission, data is transferre ICDRT to ICDRS and the data is sent from the SDA pin. In reception, data is transferred ICDRS to ICDRR after data of one byte is received. This register cannot be read directly CPU.

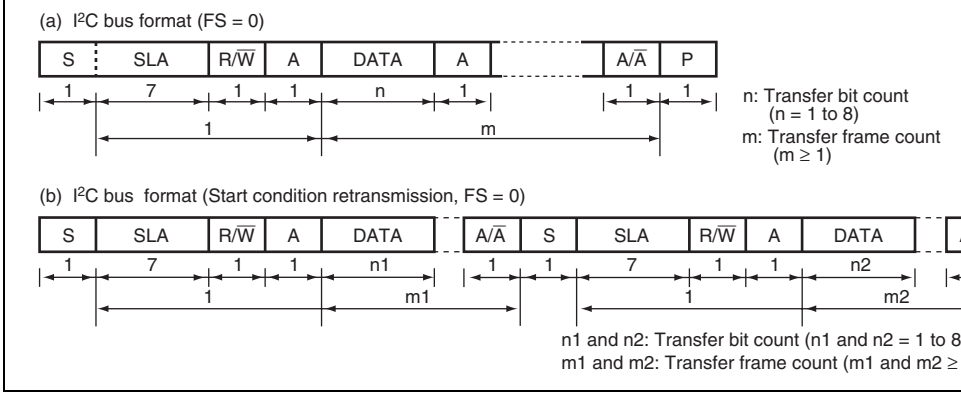


Figure 18.3 I²C Bus Formats

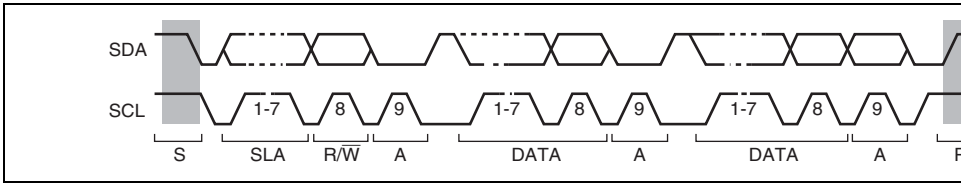


Figure 18.4 I²C Bus Timing

[Legend]

S: Start condition. The master device drives SDA from high to low while SCL is high

SLA: Slave address

R/W: Indicates the direction of data transfer: from the slave device to the master device R/W is 1, or from the master device to the slave device when R/W is 0.

A: Acknowledge. The receive device drives SDA to low.

DATA: Transfer data

P: Stop condition. The master device drives SDA from low to high while SCL is high

instruction. (Start condition issued) This generates the start condition.

3. After confirming that TDRE in ICSR has been set, write the transmit data (the first by show the slave address and R/$\overline{W}$) to ICDRT. At this time, TDRE is automatically clea and data is transferred from ICDRT to ICDRS. TDRE is set again.
4. When transmission of one byte data is completed while TDRE is 1, TEND in ICSR is at the rise of the 9th transmit clock pulse. Read the ACKBR bit in ICIER, and confirm slave device has been selected. Then, write second byte data to ICDRT. When ACKB the slave device has not been acknowledged, so issue the stop condition. To issue the condition, write 0 to BBSY and SCP using MOV instruction. SCL is fixed low until t transmit data is prepared or the stop condition is issued.
5. The transmit data after the second byte is written to ICDRT every time TDRE is set.
6. Write the number of bytes to be transmitted to ICDRT. Wait until TEND is set (the en byte data transmission) while TDRE is 1, or wait for NACK (NACKF in ICSR = 1) fr receive device while ACKE in ICIER is 1. Then, issue the stop condition to clear TEN NACKF.
7. When the STOP bit in ICSR is set to 1, the operation returns to the slave receive mod

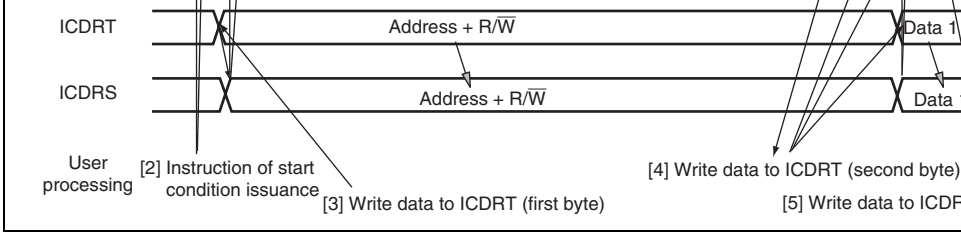


Figure 18.5 Master Transmit Mode Operation Timing (1)

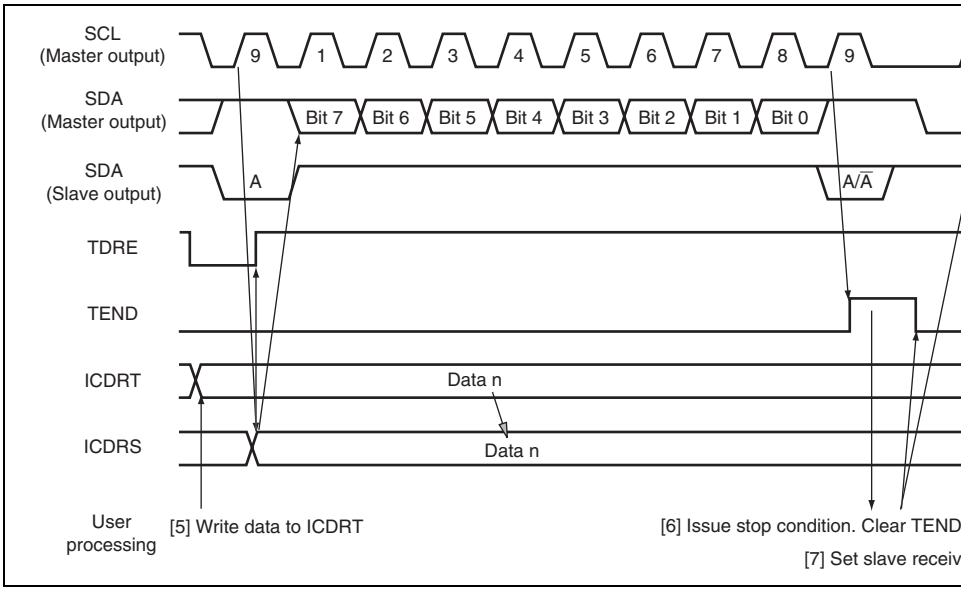


Figure 18.6 Master Transmit Mode Operation Timing (2)

level specified by ACKBT in ICIER to SDA, at the 9th receive clock pulse.

3. After the reception of first frame data is completed, the RDRF bit in ICST is set to 1 a of 9th receive clock pulse. At this time, the receive data is read by reading ICDRR, an is cleared to 0.
4. The continuous reception is performed by reading ICDRR every time RDRF is set. If receive clock pulse falls after reading ICDRR by the other processing while RDRF is fixed low until ICDRR is read.
5. If next frame is the last receive data, set the RCVD bit in ICCR1 to 1 before reading I This enables the issuance of the stop condition after the next reception.
6. When the RDRF bit is set to 1 at rise of the 9th receive clock pulse, issue the stage co
7. When the STOP bit in ICSR is set to 1, read ICDRR. Then clear the RCVD bit to 0.
8. The operation returns to the slave receive mode.

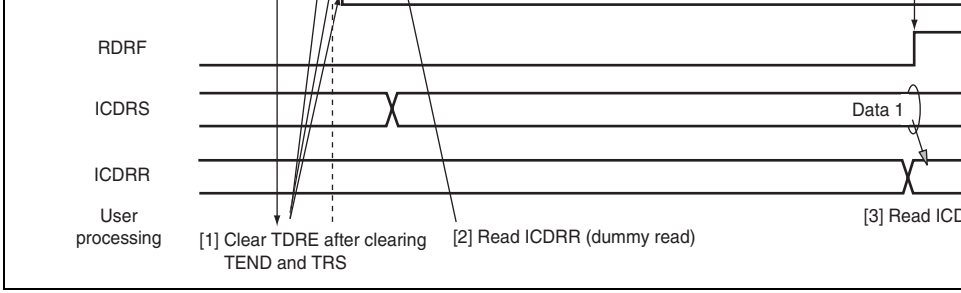


Figure 18.7 Master Receive Mode Operation Timing (1)

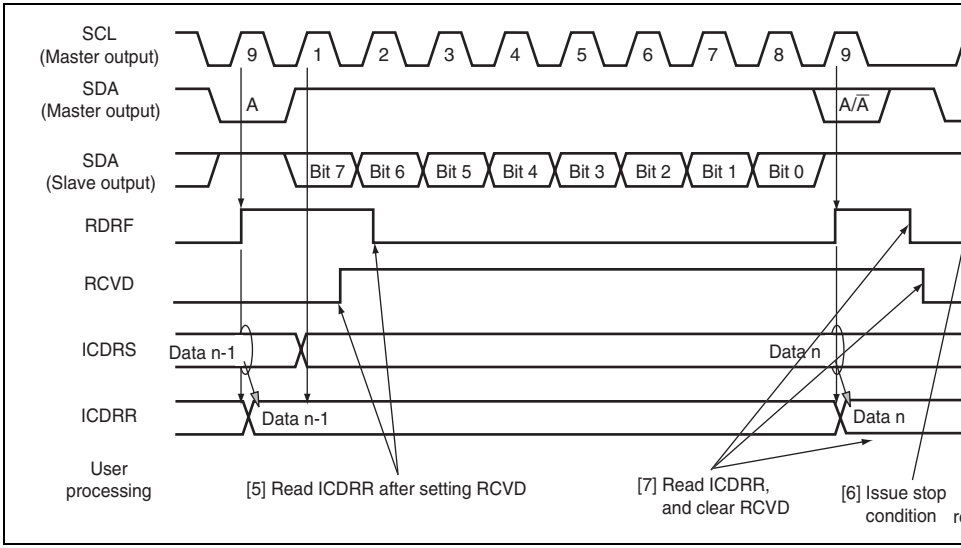


Figure 18.8 Master Receive Mode Operation Timing (2)

2. When the slave address matches in the first frame following detection of the start con the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise o clock pulse. At this time, if the 8th bit data (R/$\overline{W}$) is 1, the TRS and ICSR bits in ICC set to 1, and the mode changes to slave transmit mode automatically. The continuous transmission is performed by writing transmit data to ICDRT every time TDRE is set
3. If TDRE is set after writing last transmit data to ICDRT, wait until TEND in ICSR is with TDRE = 1. When TEND is set, clear TEND.
4. Clear TRS for the end processing, and read ICDRR (dummy read). SCL is free.
5. Clear TDRE.

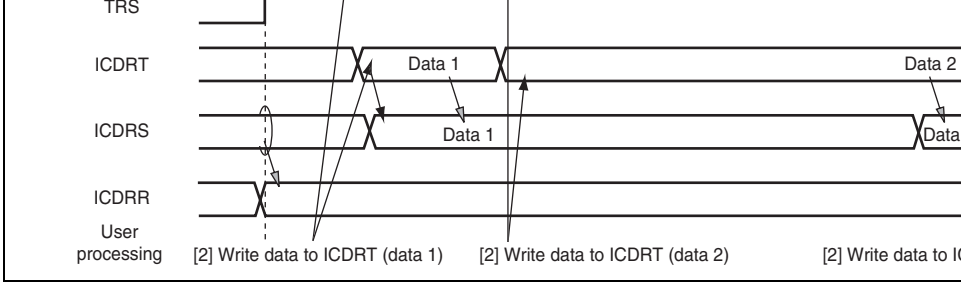


Figure 18.9 Slave Transmit Mode Operation Timing (1)

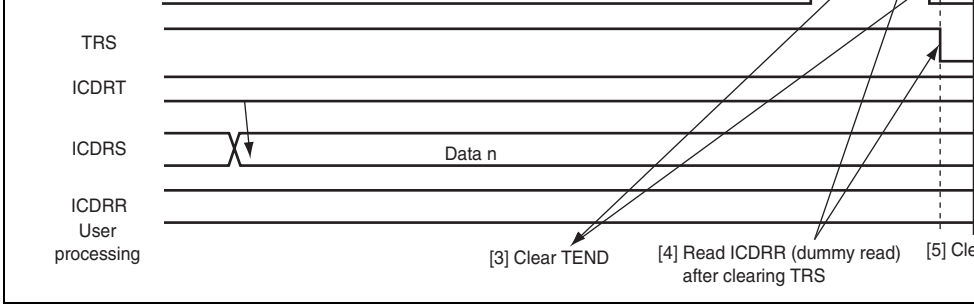


Figure 18.10 Slave Transmit Mode Operation Timing (2)

2. When the slave address matches in the first frame following detection of the start co
the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise
clock pulse. At the same time, RDRF in ICSR is set to read ICDRR (dummy read). (
read data show the slave address and R/$\overline{W}$, it is not used.)
3. Read ICDRR every time RDRF is set. If 8th receive clock pulse falls while RDRF is
fixed low until ICDRR is read. The change of the acknowledge before reading ICDR
returned to the master device, is reflected to the next transmit frame.
4. The last byte data is read by reading ICDRR.

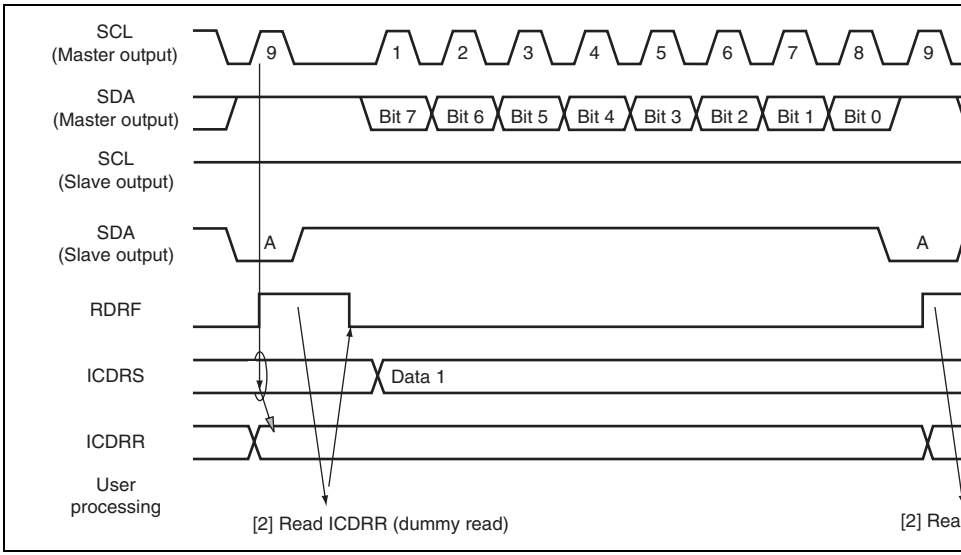


Figure 18.11 Slave Receive Mode Operation Timing (1)

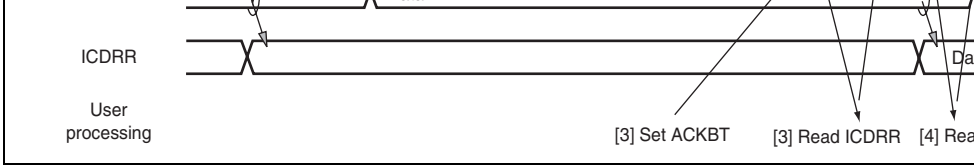


Figure 18.12 Slave Receive Mode Operation Timing (2)

18.4.6 Clocked Synchronous Serial Format

This module can be operated with the clocked synchronous serial format, by setting the F
SAR to 1. When the MST bit in ICCR1 is 1, the transfer clock output from SCL is selecte
MST is 0, the external clock input is selected.

(1) Data Transfer Format

Figure 18.13 shows the clocked synchronous serial transfer format.

The transfer data is output from the rise to the fall of the SCL clock, and the data at the ri
of the SCL clock is guaranteed. The MLS bit in ICMR sets the order of data transfer, in e
MSB first or LSB first. The output level of SDA can be changed during the transfer wait,
SDAO bit in ICCR2.

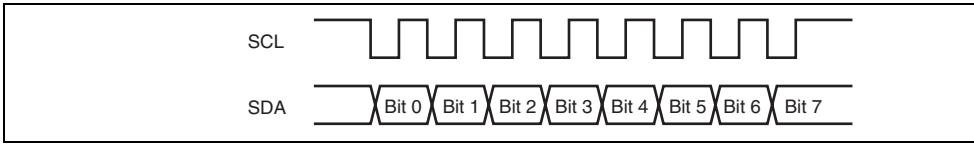


Figure 18.13 Clocked Synchronous Serial Transfer Format

transferred from ICDRT to ICDRS, and TDRE is set automatically. The continuous transmission is performed by writing data to ICDRT every time TDRE is set. When from transmit mode to receive mode, clear TRS while TDRE is 1.

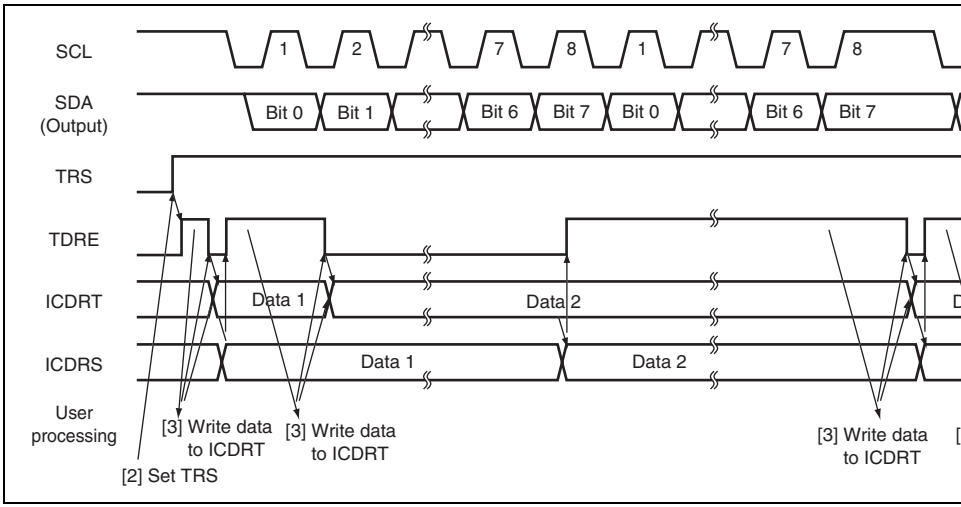


Figure 18.14 Transmit Mode Operation Timing

continually output. The continuous reception is performed by reading ICDRR every ti
RDRF is set. When the 8th clock is risen while RDRF is 1, the overrun is detected and
AL/OVE in ICSR is set. At this time, the previous reception data is retained in ICDRI

4. To stop receiving when MST = 1, set RCVD in ICCR1 to 1, then read ICDRR. Then,
fixed high after receiving the next byte data.

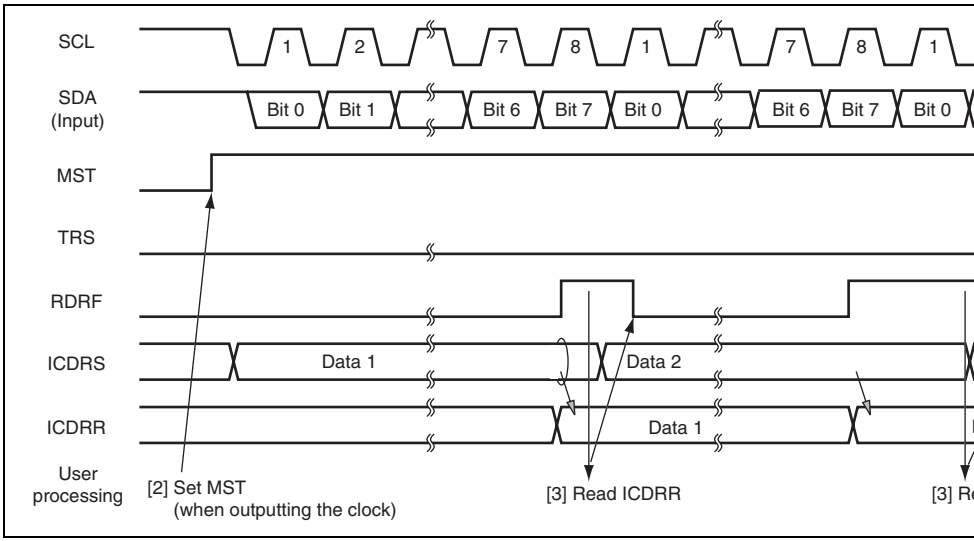


Figure 18.15 Receive Mode Operation Timing

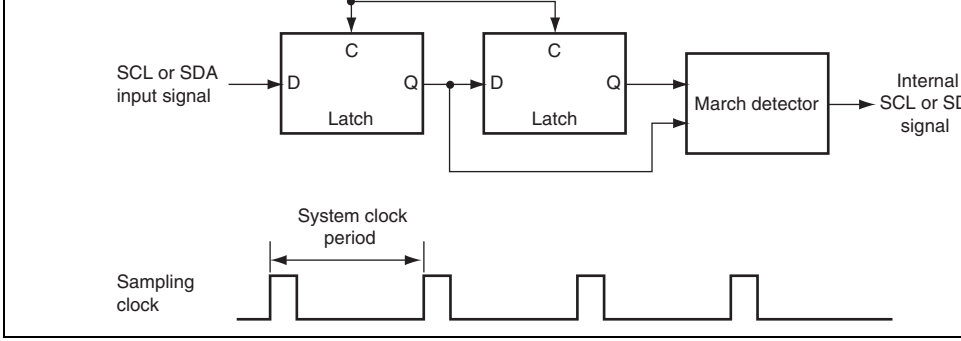


Figure 18.16 Block Diagram of Noise Canceller

18.4.8 Example of Use

Flowcharts in respective modes that use the I^2C bus interface are shown in figures 18.17

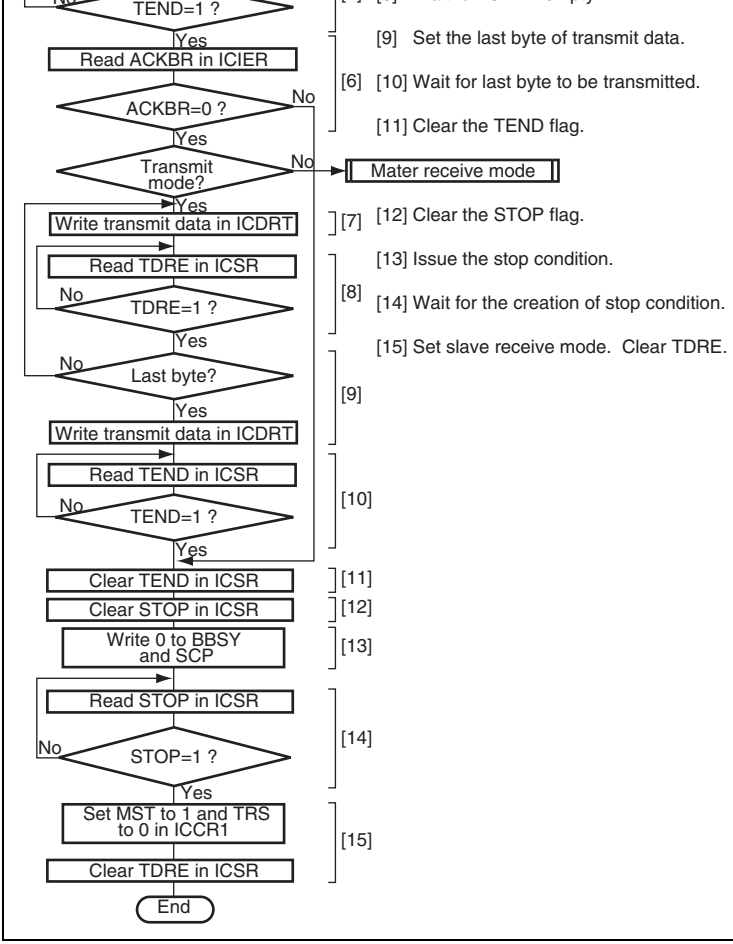
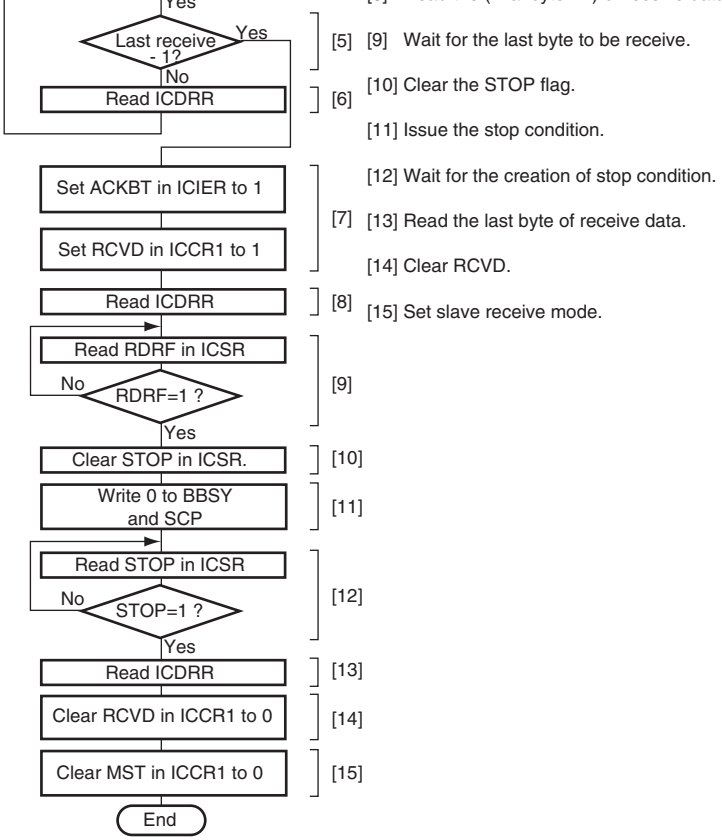


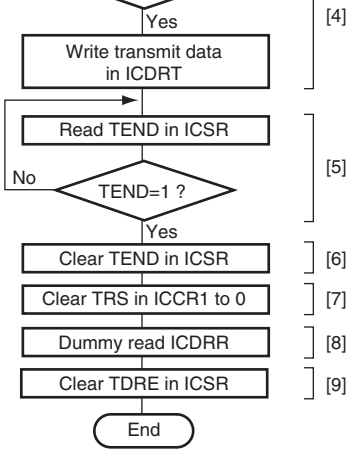
Figure 18.17 Sample Flowchart for Master Transmit Mode



Note: Do not activate an interrupt during the execution of steps [1] to [3].

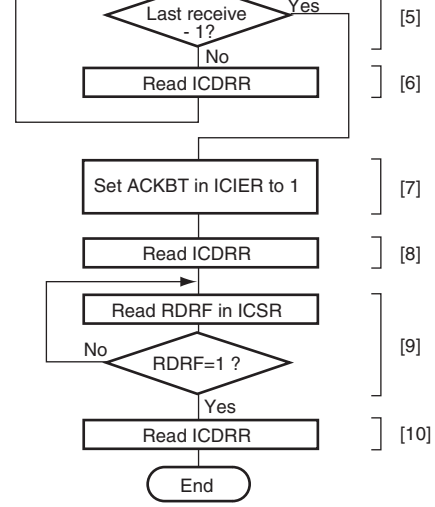
Supplementary explanation: When one byte is received, steps [2] to [6] are skipped after step [1], before jumping
The step [8] is dummy-read in ICDRR.

Figure 18.18 Sample Flowchart for Master Receive Mode



[9] Clear the TDRE flag.

Figure 18.19 Sample Flowchart for Slave Transmit Mode



Supplementary explanation: When one byte is received, steps [2] to [6] are skipped after step [1], before jumping to step [7]. The step [8] is dummy-read in ICDRR.

Figure 18.20 Sample Flowchart for Slave Receive Mode

Transmit Data Empty	TXI	(TDRE=1) • (TIE=1)	○	○
Transmit End	TEI	(TEND=1) • (TEIE=1)	○	○
Receive Data Full	RXI	(RDRF=1) • (RIE=1)	○	○
STOP Recognition	STPI	(STOP=1) • (STIE=1)	○	×
NACK Receive	NAKI	{(NACKF=1)+(AL=1)} • (NAKIE=1)	○	×
Arbitration Lost/Overrun Error			○	○

When interrupt conditions described in table 18.3 are 1 and the I bit in CCR is 0, the CPU executes an interrupt exception processing. Interrupt sources should be cleared in the exc processing. TDRE and TEND are automatically cleared to 0 by writing the transmit data ICDRT. RDRF are automatically cleared to 0 by reading ICDRR. TDRE is set to 1 again same time when transmit data is written to ICDRT. When TDRE is cleared to 0, then an e data of one byte may be transmitted.

Figure 18.21 shows the timing of the bit synchronous circuit and table 18.4 shows the ti
SCL output changes from low to Hi-Z then SCL is monitored.

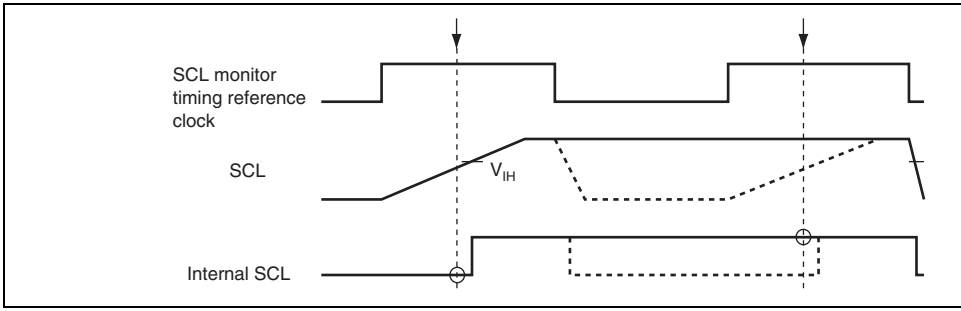
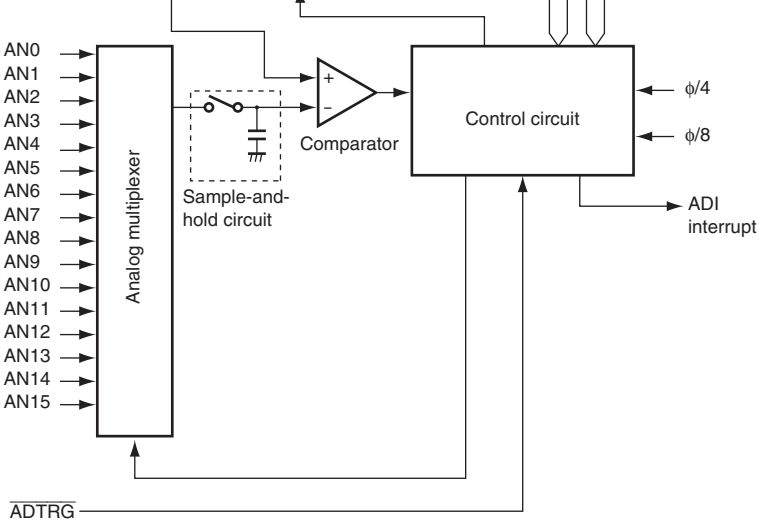


Figure 18.21 Timing of Bit Synchronous Circuit

Table 18.4 Time for Monitoring SCL

CKS3	CKS2	Time for Monitoring SCL
0	0	7.5 tcyc
	1	19.5 tcyc
1	0	17.5 tcyc
	1	41.5 tcyc

- Two operating modes
  Single mode: Single-channel A/D conversion
  Scan mode: Continuous A/D conversion on one to four channels
- Four data registers
  Conversion results are held in a data register for each channel
- Sample-and-hold function
- Two conversion start methods
  Software
  External trigger signal
- Interrupt source
  An A/D conversion end interrupt (ADI) request can be generated



[Legend]
ADCR: A/D control register
ADCSR: A/D control/status register
ADDRA: A/D data register A
ADDRB: A/D data register B
ADDRC: A/D data register C
ADDRD: A/D data register D

Figure 19.1 Block Diagram of A/D Converter

Pin Name	Abbreviation	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog block power supply
Analog input pin 0	AN0	Input	Group 0 analog input
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	Group 1 analog input
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
Analog input pin 8	AN8	Input	Group 2 analog input
Analog input pin 9	AN9	Input	
Analog input pin 10	AN10	Input	
Analog input pin 11	AN11	Input	
Analog input pin 12	AN12	Input	Group 3 analog input
Analog input pin 13	AN13	Input	
Analog input pin 14	AN14	Input	
Analog input pin 15	AN15	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger input for sta conversion

19.3.1 A/D Data Registers A to D (ADDRA to ADDRD)

There are four 16-bit read-only ADDR registers; ADDRA to ADDRD, used to store the r
A/D conversion. The ADDR registers, which store a conversion result for each analog inp
channel, are shown in table 19.2.

The converted 10-bit data is stored in bits 15 to 6. The lower 6 bits are always read as 0.

The data bus width between the CPU and the A/D converter is 8 bits. The upper byte can
directly from the CPU, however the lower byte should be read via a temporary register. T
temporary register contents are transferred from the ADDR when the upper byte data is re
Therefore byte access to ADDR should be done by reading the upper byte first then the lo
Word access is also possible. ADDR is initialized to H'0000.

Table 19.2 Analog Input Channels and Corresponding ADDR Registers

Analog Input Channel				
CH3 = 0		CH3 = 1		
Group 0 (CH2 = 0)	Group 1 (CH2 = 1)	Group 2 (CH2 = 0)	Group 3 (CH2 = 1)	A/D Data Register to St Results of A/D Convers
AN0	AN4	AN8	AN12	ADDRA
AN1	AN5	AN9	AN13	ADDRB
AN2	AN6	AN10	AN14	ADDRC
AN3	AN7	AN11	AN15	ADDRD

				selected in scan mode [Clearing condition] When 0 is written after reading ADF = 1
6	ADIE	0	R/W	A/D Interrupt Enable A/D conversion end interrupt request (ADI) is by ADF when this bit is set to 1
5	ADST	0	R/W	A/D Start Setting this bit to 1 starts A/D conversion. In s mode, this bit is cleared to 0 automatically wh conversion on the specified channel is comple scan mode, conversion continues sequentially specified channels until this bit is cleared to 0 software, a reset, or a transition to standby m
4	SCAN	0	R/W	Scan Mode Selects single mode or scan mode as the A/D conversion operating mode. 0: Single mode 1: Scan mode
3	CKS	0	R/W	Clock Select Selects the A/D conversions time. 0: Conversion time = 134 states (max.) 1: Conversion time = 70 states (max.) Clear the ADST bit to 0 before switching the c time.

0100: AN4	0100: AN4
0101: AN5	0101: AN4 and AN5
0110: AN6	0110: AN4 to AN6
0111: AN7	0111: AN4 to AN7
1000: AN8	1000: AN8
1001: AN9	1001: AN8 and AN9
1010: AN10	1010: AN8 to AN10
1011: AN11	1011: AN8 to AN11
1100: AN12	1100: AN12
1101: AN13	1101: AN12 and AN
1110: AN14	1110: AN12 to AN14
1111: AN15	1111: AN12 to AN15

				PMRG2 in port mode register G (PMRG). The falling or rising edge of the external $\overline{\text{ADTI}}$ is selected by bits PMRG2 and PMRG1.
6 to 4	—	All 1	—	Reserved These bits are always read as 1.
3, 2	—	All 0	R/W	Reserved The write value should always be 0.
1	—	1	—	Reserved This bit is always read as 1.
0	CH3	0	R/W	Reserved Selects the analog input channel according to to CH0 in ADCSR.

channel as follows:

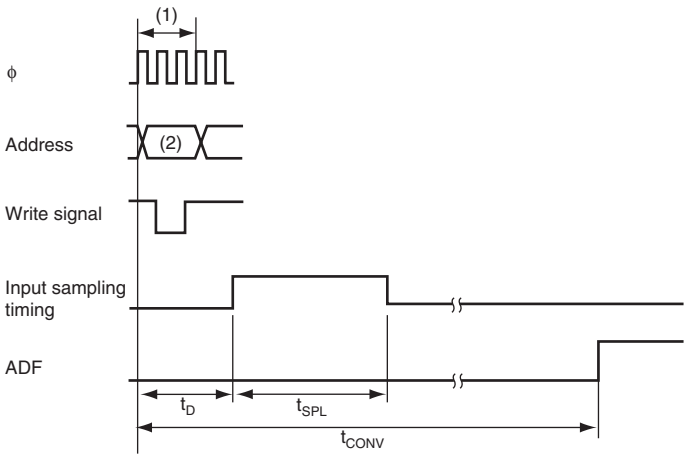
1. A/D conversion is started when the ADST bit in ADCSR is set to 1, according to soft external trigger input.
2. When A/D conversion is completed, the result is transferred to the corresponding A/D register of the channel.
3. On completion of conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is se this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D conversion ends, t bit is automatically cleared to 0 and the A/D converter enters the wait state.

19.4.2 Scan Mode

In scan mode, A/D conversion is performed sequentially for the analog input of the speci channels (four channels maximum) as follows:

1. When the ADST bit in ADCSR is set to 1 by software or external trigger input, A/D conversion starts on the first channel in the group (AN0 when CH3 and CH2 = B'00, A when CH3 and CH2 = B'01, AN8 when CH3 and CH2 = B'10, AN12 when CH3 and B'11).
2. When A/D conversion for each channel is completed, the result is sequentially transfe the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF flag in ADCSR i If the ADIE bit is set to 1 at this time, an ADI interrupt requested is generated. A/D co starts again on the first channel in the group.
4. The ADST bit is not automatically cleared to 0. Steps [2] and [3] are repeated as long ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops.

In scan mode, the values given in table 19.3 apply to the first conversion time. In the sec
subsequent conversions, the conversion time is 128 states (fixed) when CKS = 0 and 66
(fixed) when CKS = 1.



[Legend]
(1): ADCSR write cycle
(2): ADCSR address
t_D: A/D conversion start delay time
t_{SPL}: Input sampling time
t_{CONV}: A/D conversion time

Figure 19.2 A/D Conversion Timing

19.4.4 External Trigger Input Timing

A/D conversion can also be started by an external trigger input. When the TRGE bit in A set to 1, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge at the $\overline{\text{ADTRG}}$ pin sets the ADST bit in ADCSR to 1, starting A/D conversion. Other operations, in both and scan modes, are the same as when the bit ADST has been set to 1 by software. Figure shows the timing.

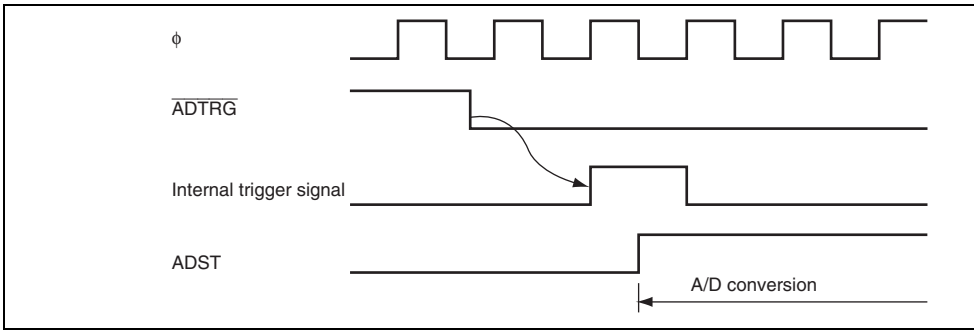


Figure 19.3 External Trigger Input Timing

when the digital output changes from the minimum voltage value 0000000000 to 00
(see figure 19.5).

- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion chara
  when the digital output changes from 1111111110 to 1111111111 (see figure 19.5).

- Nonlinearity error

  The deviation from the ideal A/D conversion characteristic as the voltage changes fr
  full scale. This does not include the offset error, full-scale error, or quantization erro

- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset e
  scale error, quantization error, and nonlinearity error.

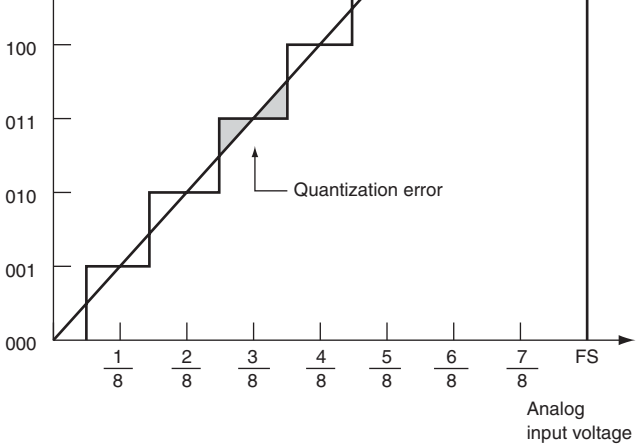


Figure 19.4 A/D Conversion Accuracy Definitions (1)

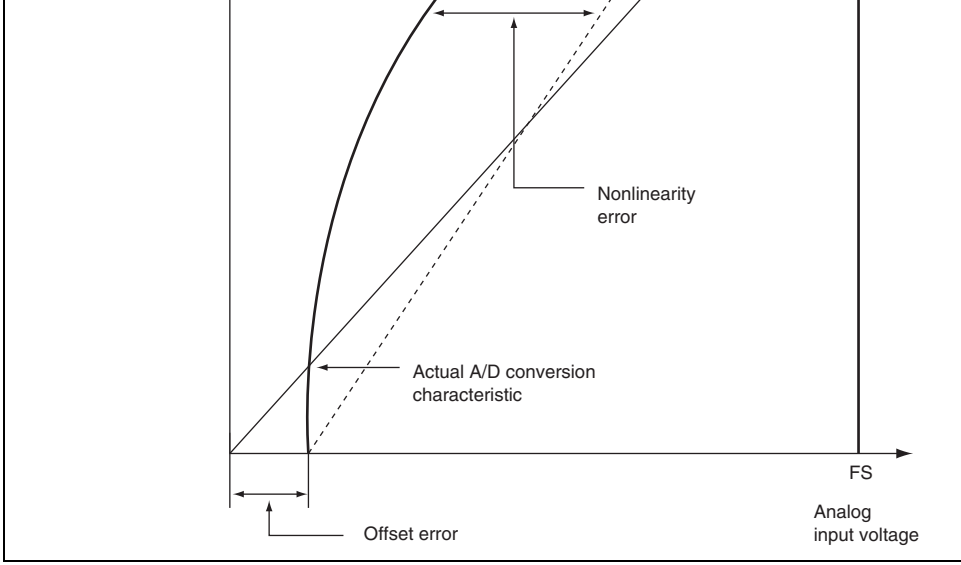


Figure 19.4 A/D Conversion Accuracy Definitions (2)

input resistance of 10 kΩ, and the signal source impedance is ignored. However, as a low filter effect is obtained in this case, it may not be possible to follow an analog signal with differential coefficient (e.g., 5 mV/μs or greater) (see figure 19.5). When converting a hig analog signal or converting in scan mode, a low-impedance buffer should be inserted.

19.6.2 Influences on Absolute Accuracy

Adding capacitance results in coupling with GND, and therefore noise in GND may adve affect absolute accuracy. Be sure to make the connection to an electrically stable GND.

Care is also required to ensure that filter circuits do not interfere with digital signals or ac antennas on the board.

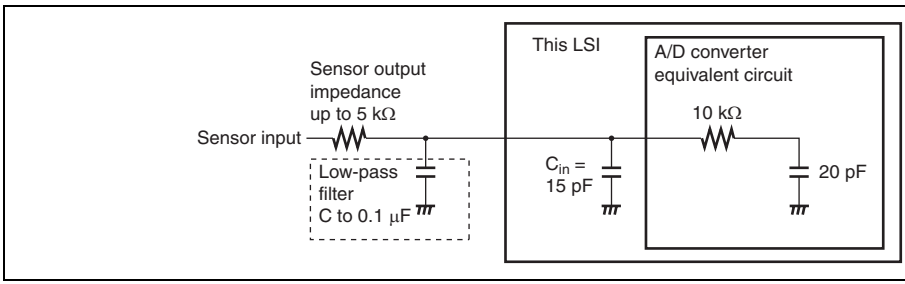


Figure 19.5 Analog Input Circuit Example

and LVDR (reset by low voltage detect) circuits.

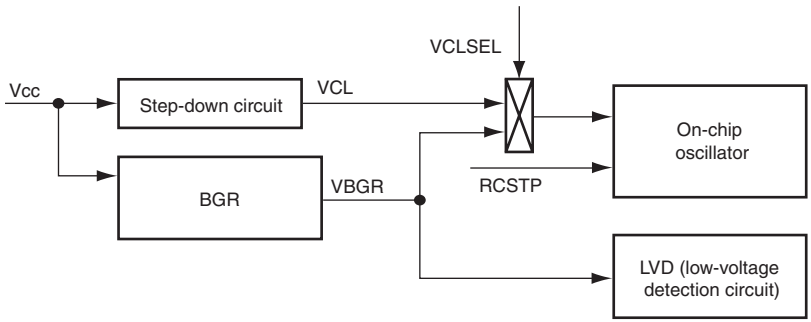
This circuit is used to prevent abnormal operation (runaway execution) from occurring d
power supply voltage fall and to recreate the state before the power supply voltage fall w
power supply voltage rises again.

Even if the power supply voltage falls, the unstable state when the power supply voltage
below the guaranteed operating voltage can be removed by entering standby mode when
exceeding the guaranteed operating voltage and during normal operation. Thus, system s
can be improved. If the power supply voltage falls more, the reset state is automatically
the power supply voltage rises again, the reset state is held for a specified period, then ac
is automatically entered.

Figure 20.2 is a block diagram of the power-on reset circuit and the low-voltage detectio

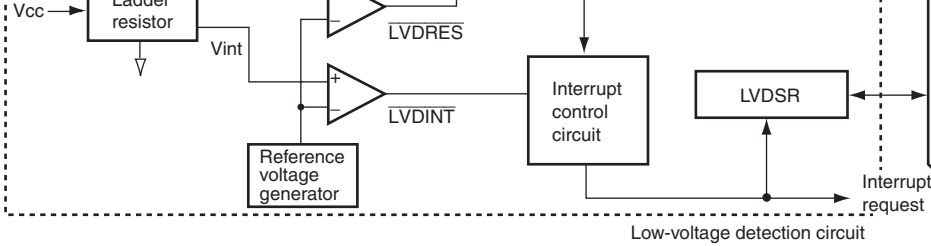
LVDI: Monitors the power-supply voltage, and generates an interrupt when the voltag
below or rises above respective specified values.

Two pairs of detection levels for reset generation voltage are available: when only the
circuit is used, or when the LVDI and LVDR circuits are both used.



[Legend]
Vcc: Power supply
VCL: Internal power supply generated from Vcc by the step-down circuit
VBGR: Reference voltage from BGR
VCLSEL: Select signal for the source of the on-chip oscillator power supply
RCSTP: On-chip oscillator stop signal

Figure 20.1 Block Diagram around BGR



[Legend]

PSS:	Prescaler S
LVDCR:	Low-voltage-detection control register
LVDSR:	Low-voltage-detection status register
$\overline{\text{LVDRES}}$:	Low-voltage-detection reset signal
$\overline{\text{LVDINT}}$:	Low-voltage-detection interrupt signal
Vreset:	Reset detection voltage
Vint:	Power-supply fall/rise detection voltage

Figure 20.2 Block Diagram of Power-On Reset Circuit and Low-Voltage Detection Circuit

the LVDR function, enable or disable the LVDR function, and enable or disable generatio
interrupt when the power-supply voltage rises above or falls below the respective levels.

Table 20.1 shows the relationship between the LVDCR settings and select functions. LVI
should be set according to table 20.1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1. Data write is i
3	LVDSEL	1	R/W	LVDR Detection Level Select 0: Reset detection voltage is 2.3 V (typ.) 1: Reset detection voltage is 3.6 V (typ.) When the falling or rising voltage detection inte used, reset detection voltage of 2.3 V (typ.) sho used. When only a reset detection interrupt is u reset detection voltage of 3.6 V (typ.) should be This bit is initialized by a LVDR reset.
2	—	1	—	Reserved This bit is always read as 1. Data write is inhibi
1	LVDDE	0	R/W	Voltage-Fall-Interrupt Enable 0: Interrupt on the power-supply voltage falling the selected detection level disabled 1: Interrupt on the power-supply voltage falling the selected detection level enabled

LVDSEL	LVDDE	LVDUE	Power-On Reset	LVDR Reset	Low-Voltage-Detection Falling Interrupt	Low-V Detec Risin
1	0	0	√	√	—	—
0	1	0	√	√	√	—
0	1	1	√	√	√	√

1	LVDDF	0	R/W	LVD Power-Supply Voltage Fall Flag [Setting condition] When the power-supply voltage falls below Vin (typ. = 3.7 V) [Clearing condition] Writing 0 to this bit after reading it as 1
0	LVDUF	0*	R/W	LVD Power-Supply Voltage Rise Flag [Setting condition] When the power supply voltage falls below Vin while the LVDUE bit in LVDCR is set to 1, then above Vint (U) (typ. = 4.0 V) before falling belo Vreset1 (typ. = 2.3 V) [Clearing condition] Writing 0 to this bit after reading it as 1

Note: * Initialized by LVDR.

131,072 clock (ϕ) cycles. The noise cancellation circuit of approximately 100 ns is incor
prevent the incorrect operation of this LSI by noise on the $\overline{\text{RES}}$ signal.

To achieve stable operation of this LSI, the power supply needs to rise to its full level ar
within the specified time. The maximum time required for the power supply to rise and s
power has been supplied (t_{PWON}) is determined by the oscillation frequency (f_{OSC}) and capa
which is connected to $\overline{\text{RES}}$ pin ($C_{\overline{\text{RES}}}$). If t_{PWON} means the time required to reach 90 % of
supply voltage, the power supply circuit should be designed to satisfy the following form

$$t_{PWON}\ (\text{ms}) \leq 90 \times C_{\overline{\text{RES}}}\ (\mu\text{F}) + 162/f_{OSC}\ (\text{MHz})$$

($t_{PWON} \leq 3000$ ms, $C_{\overline{\text{RES}}} \geq 0.22$ μF, and $f_{OSC} = 10$ in 4-MHz to 10-MHz operatio

Note that the power supply voltage (Vcc) must fall below Vpor = 100 mV and rise after
the $\overline{\text{RES}}$ pin is removed. To remove charge on the $\overline{\text{RES}}$ pin, it is recommended that a dio
be placed near Vcc. If the power supply voltage (Vcc) rises from the point above Vpor,
on reset may not occur.

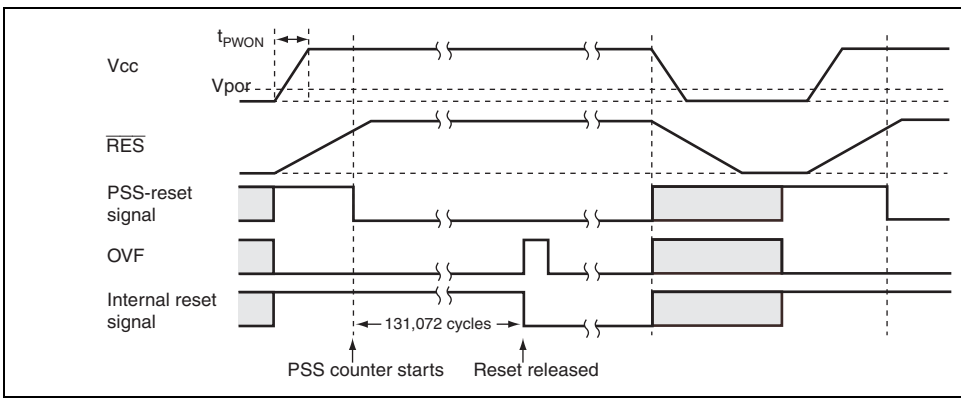


Figure 20.3 Operational Timing of Power-On Reset Circuit

cycles, and then releases the internal reset signal. Since the LVDSEL bit in the LVDCR i initialized to 1 at this point, Vreset during Vcc rising remains 3.6 V, even if the LVDSEL been set to 0.

Note that if the power supply voltage (Vcc) falls below $V_{LVDRmin}$ = 1.0 V and then rises fro point, the low-voltage detection reset may not occur.

If the power supply voltage (Vcc) falls below Vpor = 100 mV, a power-on reset occurs.

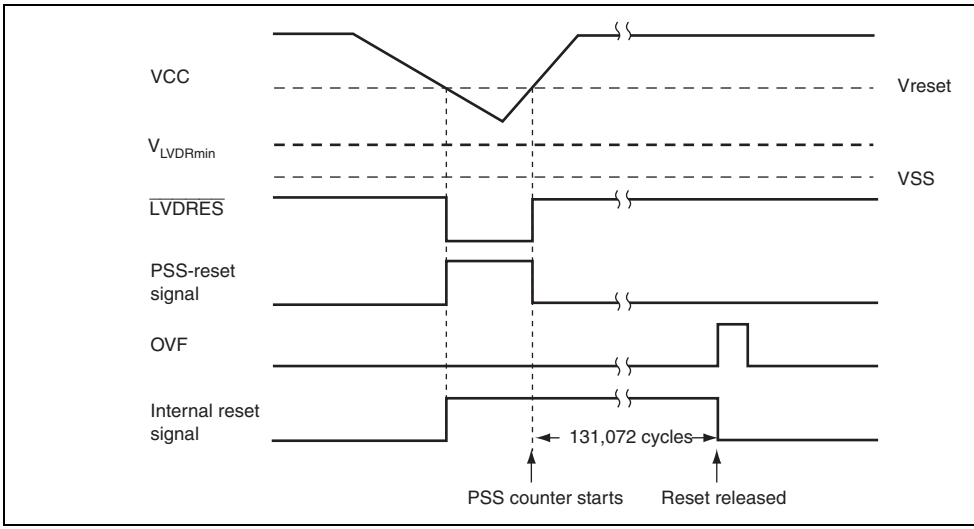


Figure 20.4 Operational Timing of LVDR Circuit

When the power-supply voltage does not fall below Vreset1 (typ. = 2.3 V) voltage but ri
Vint (U) (typ. = 4.0 V) voltage, the LVDI sets the $\overline{\text{LVDINT}}$ signal to 1. If the LVDUE b
this time, the LVDUF bit in LVDSR is set to 1 and an IRQ0 interrupt request is simultar
generated.

If the power supply voltage (Vcc) falls below Vreset1 (typ. = 2.3 V) voltage, the LVDR
is performed.

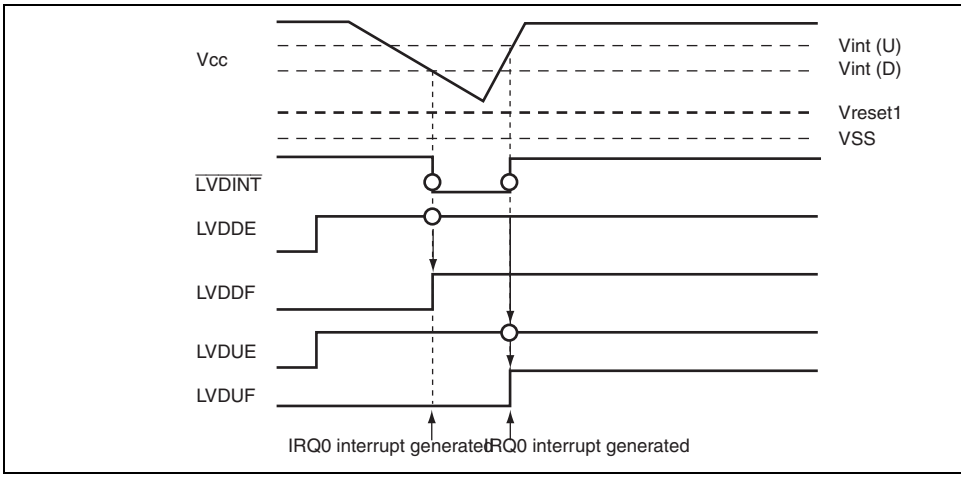


Figure 20.5 Operational Timing of LVDI Circuit

21.1 When Using Internal Power Supply Step-Down Circuit

Connect the external power supply to the V_{cc} pin, and connect a capacitance of approxin
μF between V_{cl} and V_{ss}, as shown in figure 21.1. The internal step-down circuit is made
simply by adding this external circuit. In the external circuit interface, the external powe
voltage connected to V_{cc} and the GND potential connected to V_{ss} are the reference levels
example, for port input/output levels, the V_{cc} level is the reference for the high level, and
level is that for the low level. The A/D converter analog power supply is not affected by
internal step-down circuit.

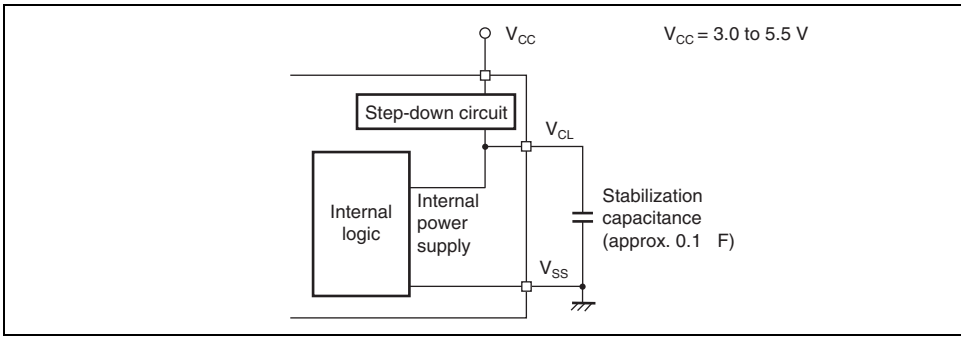


Figure 21.1 Power Supply Connection when Internal Step-Down Circuit is U

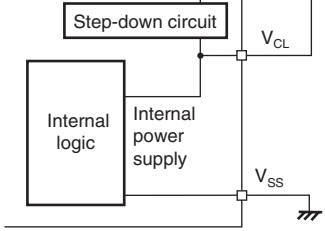


Figure 21.2 Power Supply Connection when Internal Step-Down Circuit is Not

- The number of access states is indicated.

2. Register bits
- Bit configurations of the registers are described in the same order as the register addr
- Reserved bits are indicated by — in the bit name column.
- When registers consist of 16 bits, bits are described from the MSB side.

3. Register states in each operating mode
- Register states are described in the same order as the register addresses.
- The register states described here are for the basic operating modes. If there is a spec
  for an on-chip peripheral module, refer to the section on that on-chip peripheral mod

				(Channel 0)	
General register A_0	GRA_0	16	H'FFF102	Timer RD (Channel 0)	16*[1]
General register B_0	GRB_0	16	H'FFF104	Timer RD (Channel 0)	16*[1]
General register C_0	GRC_0	16	H'FFF106	Timer RD (Channel 0)	16*[1]
General register D_0	GRD_0	16	H'FFF108	Timer RD (Channel 0)	16*[1]
Timer RD counter_1	TRDCNT_1	16	H'FFF10A	Timer RD (Channel 1)	16*[1]
General register A_1	GRA_1	16	H'FFF10C	Timer RD (Channel 1)	16*[1]
General register B_1	GRB_1	16	H'FFF10E	Timer RD (Channel 1)	16*[1]
General register C_1	GRC_1	16	H'FFF110	Timer RD (Channel 1)	16*[1]
General register D_1	GRD_1	16	H'FFF112	Timer RD (Channel 1)	16*[1]
Timer RD counter_2	TRDCNT_2	16	H'FFF140	Timer RD (Channel 2)	16*[1]
General register A_2	GRA_2	16	H'FFF142	Timer RD (Channel 2)	16*[1]
General register B_2	GRB_2	16	H'FFF144	Timer RD (Channel 2)	16*[1]
General register C_2	GRC_2	16	H'FFF146	Timer RD (Channel 2)	16*[1]

				(Channel 3)	
General register D_3	GRD_3	16	H'FFF152	Timer RD (Channel 3)	16*[1]
Timer RC counter	TRCCNT	16	H'FFF180	Timer RC	16*[1]
General register A	GRA	16	H'FFF182	Timer RC	16*[1]
General register B	GRB	16	H'FFF184	Timer RC	16*[1]
General register C	GRC	16	H'FFF186	Timer RC	16*[1]
General register D	GRD	16	H'FFF188	Timer RC	16*[1]
Serial mode register_3	SMR_3	8	H'FFF600	SCI3_3	8
Bit rate register_3	BRR_3	8	H'FFF601	SCI3_3	8
Serial control register 3_3	SCR3_3	8	H'FFF602	SCI3_3	8
Transmit data register_3	TDR_3	8	H'FFF603	SCI3_3	8
Serial status register_3	SSR_3	8	H'FFF604	SCI3_3	8
Receive data register_3	RDR_3	8	H'FFF605	SCI3_3	8
Serial mode control register_3	SMCR_3	8	H'FFF608	SCI3_3	8
A/D data register A	ADDRA	16	H'FFF610	A/D converter	8
A/D data register B	ADDRB	16	H'FFF612	A/D converter	8
A/D data register C	ADDRC	16	H'FFF614	A/D converter	8
A/D data register D	ADDRD	16	H'FFF616	A/D converter	8
A/D control/status register	ADCSR	8	H'FFF618	A/D converter	8
A/D control register	ADCR	8	H'FFF619	A/D converter	8
Port data register D	PDRD	8	H'FFF624	I/O port	8
Port data register E	PDRE	8	H'FFF625	I/O port	8
Port data register F	PDRF	8	H'FFF626	I/O port	8

Port control register G	PCRG	8	H'FFF637	I/O port	8
Port control register H	PCRH	8	H'FFF638	I/O port	8
Port control register J	PCRJ	8	H'FFF639	I/O port	8
Module standby control register 4	MSTCR4	8	H'FFF64F	Power-down modes	8
Timer RD control register_0	TRDCR_0	8	H'FFF654	Timer RD (Channel 0)	8
Timer RD I/O control register A_0	TRDIORA_0	8	H'FFF655	Timer RD (Channel 0)	8
Timer RD I/O control register C_0	TRDIORC_0	8	H'FFF656	Timer RD (Channel 0)	8
Timer RD status register_0	TRDSR_0	8	H'FFF657	Timer RD (Channel 0)	8
Timer RD interrupt enable register_0	TRDIER_0	8	H'FFF658	Timer RD (Channel 0)	8
PWM mode output level control register_0	POCR_0	8	H'FFF659	Timer RD (Channel 0)	8
Timer RD digital filtering function select register_0	TRDDF_0	8	H'FFF65A	Timer RD (Channel 0)	8
Timer RD control register_1	TRDCR_1	8	H'FFF65B	Timer RD (Channel 1)	8
Timer RD I/O control register A_1	TRDIORA_1	8	H'FFF65C	Timer RD (Channel 1)	8
Timer RD I/O control register C_1	TDRIORC_1	8	H'FFF65D	Timer RD (Channel 1)	8
Timer RD status register_1	TRDSR_1	8	H'FFF65E	Timer RD (Channel 1)	8

Timer RD mode register_01	TRDMDR_01	8	H'FFF663	Timer RD (Channel 0 and 1 common)	8
Timer RD PWM mode register_01	TRDPMR_01	8	H'FFF664	Timer RD (Channel 0 and 1 common)	8
Timer RD function control register_01	TRDFCR_01	8	H'FFF665	Timer RD (Channel 0 and 1 common)	8
Timer output master enable register 1_01	TRDOER1_01	8	H'FFF666	Timer RD (Channel 0 and 1 common)	8
Timer output master enable register 2_01	TRDOER2_01	8	H'FFF667	Timer RD (Channel 0 and 1 common)	8
Timer RD output control register_01	TRDOCR_01	8	H'FFF668	Timer RD (Channel 0 and 1 common)	8
Timer RD control register_2	TRDCR_2	8	H'FFF694	Timer RD (Channel 2)	8
Timer RD I/O control register A_2	TRDIORA_2	8	H'FFF695	Timer RD (Channel 2)	8
Timer RD I/O control register C_2	TDRIORC_2	8	H'FFF696	Timer RD (Channel 2)	8
Timer RD status register_2	TRDSR_2	8	H'FFF697	Timer RD (Channel 2)	8
Timer RD interrupt enable register_2	TRDIER_2	8	H'FFF698	Timer RD (Channel 2)	8

				(Channel 3)	
Timer RD status register_3	TRDSR_3	8	H'FFF69E	Timer RD (Channel 3)	8
Timer RD interrupt enable register_3	TRDIER_3	8	H'FFF69F	Timer RD (Channel 3)	8
PWM mode output level control register_3	POCR_3	8	H'FFF6A0	Timer RD (Channel 3)	8
Timer RD digital filtering function select register_3	TRDDF_3	8	H'FFF6A1	Timer RD (Channel 3)	8
Timer RD start register_23	TRDSTR_23	8	H'FFF6A2	Timer RD (Channel 2 and 3 common)	8
Timer RD mode register_23	TRDMDR_23	8	H'FFF6A3	Timer RD (Channel 2 and 3 common)	8
Timer RD PWM mode register_23	TRDPMR_23	8	H'FFF6A4	Timer RD (Channel 2 and 3 common)	8
Timer RD function control register_23	TRDFCR_23	8	H'FFF6A5	Timer RD (Channel 2 and 3 common)	8
Timer RD output master enable register 1_23	TRDOER1_23	8	H'FFF6A6	Timer RD (Channel 2 and 3 common)	8
Timer RD output master enable register 2_23	TRDOER2_23	8	H'FFF6A7	Timer RD (Channel 2 and 3 common)	8

Timer RC I/O control register 1	TRCIOR1	8	H'FFF6CF	Timer RC	8
Timer RC control register 2	TRCCR2	8	H'FFF6D0	Timer RC	8
Timer RC digital filtering function select register	TRCDF	8	H'FFF6D1	Timer RC	8
Timer RC output enable register	TRCOER	8	H'FFF6D2	Timer RC	8
Second data register/free running counter data register	RSECDR	8	H'FFF728	RTC	8
Minute data register	RMINDR	8	H'FFF729	RTC	8
Hour data register	RHRDR	8	H'FFF72A	RTC	8
Day-of-week data register	RWKDR	8	H'FFF72B	RTC	8
RTC control register 1	RTCCR1	8	H'FFF72C	RTC	8
RTC control register 2	RTCCR2	8	H'FFF72D	RTC	8
Clock source select register	RTCCSR	8	H'FFF72F	RTC	8
Low-voltage-detection control register	LVDCR	8	H'FFF730	LVD	8
Low-voltage-detection status register	LVDSR	8	H'FFF731	LVD	8
Clock control status register	CKCSR	8	H'FFF734	Clock pulse generator	8
RC control register	RCCR	8	H'FFF738	On-chip oscillator	8
RC trimming data protect register	RCTRMDPR	8	H'FFF739	On-chip oscillator	8
RC trimming register	RCTRMDR	8	H'FFF73A	On-chip oscillator	8
Interrupt control register A	ICRA	8	H'FFF73C	Interrupt	8

Serial status register_2	SSR_2	8	H'FFF744	SCI3_2	8
Receive data register_2	RDR_2	8	H'FFF745	SCI3_2	8
I^2C bus control register 1	ICCR1	8	H'FFF748	IIC2	8
I^2C bus control register 2	ICCR2	8	H'FFF749	IIC2	8
I^2C bus mode register	ICMR	8	H'FFF74A	IIC2	8
I^2C bus interrupt enable register	ICIER	8	H'FFF74B	IIC2	8
I^2C bus status register	ICSR	8	H'FFF74C	IIC2	8
Slave address register	SAR	8	H'FFF74D	IIC2	8
I^2C bus transmit data register	ICDRT	8	H'FFF74E	IIC2	8
I^2C bus receive data register	ICDRR	8	H'FFF74F	IIC2	8
Timer mode register B1	TMB1	8	H'FFF760	Timer B1	8
Timer counter B1	TCB1	8	H'FFF761	Timer B1	8
Timer load register B1	TLB1	8	H'FFF761	Timer B1	8
Flash memory control register 1	FLMCR1	8	H'FFFF90	ROM	8
Flash memory control register 2	FLMCR2	8	H'FFFF91	ROM	8
Flash memory power control register	FLPWCR	8	H'FFFF92	ROM	8
Erase block register 1	EBR1	8	H'FFFF93	ROM	8
Flash memory enable register	FENR	8	H'FFFF9B	ROM	8
Timer control register V0	TCRV0	8	H'FFFFA0	Timer V	8
Timer control/status register V	TCSRV	8	H'FFFFA1	Timer V	8
Time constant register A	TCORA	8	H'FFFFA2	Timer V	8
Time constant register B	TCORB	8	H'FFFFA3	Timer V	8
Timer counter V	TCNTV	8	H'FFFFA4	Timer V	8

PWM data register L	PWDRL	8	H'FFFFBC	14-bit PWM	8
PWM data register U	PWDRU	8	H'FFFFBD	14-bit PWM	8
PWM control register	PWCR	8	H'FFFFBE	14-bit PWM	8
Timer control/status register WD	TCSRWD	8	H'FFFFC0	WD*[2]	8
Timer counter WD	TCWD	8	H'FFFFC1	WD*[2]	8
Timer mode register WD	TMWD	8	H'FFFFC2	WD*[2]	8
Address break control register	ABRKCR	8	H'FFFFC8	Address break	8
Address break status register	ABRKSR	8	H'FFFFC9	Address break	8
Break address register H	BARH	8	H'FFFFCA	Address break	8
Break address register L	BARL	8	H'FFFFCB	Address break	8
Break data register H	BDRH	8	H'FFFFCC	Address break	8
Break data register L	BDRL	8	H'FFFFCD	Address break	8
Break address register E	BARE	8	H'FFFFCF	Address break	8
Port pull-up control register 1	PUCR1	8	H'FFFFD0	I/O Port	8
Port pull-up control register 5	PUCR5	8	H'FFFFD1	I/O Port	8
Port data register 1	PDR1	8	H'FFFFD4	I/O Port	8
Port data register 2	PDR2	8	H'FFFFD5	I/O Port	8
Port data register 3	PDR3	8	H'FFFFD6	I/O Port	8
Port data register 5	PDR5	8	H'FFFFD8	I/O Port	8
Port data register 7	PDR7	8	H'FFFFDA	I/O Port	8
Port data register 8	PDR8	8	H'FFFFDB	I/O Port	8
Port data register C	PDRC	8	H'FFFFDE	I/O Port	8
Port mode register 1	PMR1	8	H'FFFFE0	I/O Port	8
Port mode register 5	PMR5	8	H'FFFFE1	I/O Port	8

Port control register C	PCRC	8	H'FFFFEE	I/O port	8
System control register 3	SYSCR3	8	H'FFFFEF	Power-down modes	8
System control register 1	SYSCR1	8	H'FFFFF0	Power-down modes	8
System control register 2	SYSCR2	8	H'FFFFF1	Power-down modes	8
Interrupt edge select register 1	IEGR1	8	H'FFFFF2	Interrupt	8
Interrupt edge select register 2	IEGR2	8	H'FFFFF3	Interrupt	8
Interrupt enable register 1	IENR1	8	H'FFFFF4	Interrupt	8
Interrupt enable register 2	IENR2	8	H'FFFFF5	Interrupt	8
Interrupt flag register 1	IRR1	8	H'FFFFF6	Interrupt	8
Interrupt flag register 2	IRR2	8	H'FFFFF7	Interrupt	8
Wakeup interrupt flag register	IWPR	8	H'FFFFF8	Interrupt	8
Module standby control register 1	MSTCR1	8	H'FFFFF9	Power-down modes	8
Module standby control register 2	MSTCR2	8	H'FFFFFA	Power-down modes	8

Notes: 1. These registers can be accessed by word size only.
2. WDT: Watchdog timer

	GRA0L7	GRA0L6	GRA0L5	GRA0L4	GRA0L3	GRA0L2	GRA0L1	GRA0L0
GRB_0	GRB0H7	GRB0H6	GRB0H5	GRB0H4	GRB0H3	GRB0H2	GRB0H1	GRB0H0
	GRB0L7	GRB0L6	GRB0L5	GRB0L4	GRB0L3	GRB0L2	GRB0L1	GRB0L0
GRC_0	GRC0H7	GRC0H6	GRC0H5	GRC0H4	GRC0H3	GRC0H2	GRC0H1	GRC0H0
	GRC0L7	GRC0L6	GRC0L5	GRC0L4	GRC0L3	GRC0L2	GRC0L1	GRC0L0
GRD_0	GRD0H7	GRD0H6	GRD0H5	GRD0H4	GRD0H3	GRD0H2	GRD0H1	GRD0H0
	GRD0L7	GRD0L6	GRD0L5	GRD0L4	GRD0L3	GRD0L2	GRD0L1	GRD0L0
TRDCNT_1	TCNT1H7	TCNT1H6	TCNT1H5	TCNT1H4	TCNT1H3	TCNT1H2	TCNT1H1	TCNT1H0
	TCNT1L7	TCNT1L6	TCNT1L5	TCNT1L4	TCNT1L3	TCNT1L2	TCNT1L1	TCNT1L0
GRA_1	GRA1H7	GRA1H6	GRA1H5	GRA1H4	GRA1H3	GRA1H2	GRA1H1	GRA1H0
	GRA1L7	GRA1L6	GRA1L5	GRA1L4	GRA1L3	GRA1L2	GRA1L1	GRA1L0
GRB_1	GRB1H7	GRB1H6	GRB1H5	GRB1H4	GRB1H3	GRB1H2	GRB1H1	GRB1H0
	GRB1L7	GRB1L6	GRB1L5	GRB1L4	GRB1L3	GRB1L2	GRB1L1	GRB1L0
GRC_1	GRC1H7	GRC1H6	GRC1H5	GRC1H4	GRC1H3	GRC1H2	GRC1H1	GRC1H0
	GRC1L7	GRC1L6	GRC1L5	GRC1L4	GRC1L3	GRC1L2	GRC1L1	GRC1L0
GRD_1	GRD1H7	GRD1H6	GRD1H5	GRD1H4	GRD1H3	GRD1H2	GRD1H1	GRD1H0
	GRD1L7	GRD1L6	GRD1L5	GRD1L4	GRD1L3	GRD1L2	GRD1L1	GRD1L0
TRDCNT_2	TCNT2H7	TCNT2H6	TCNT2H5	TCNT2H4	TCNT2H3	TCNT2H2	TCNT2H1	TCNT2H0
	TCNT2L7	TCNT2L6	TCNT2L5	TCNT2L4	TCNT2L3	TCNT2L2	TCNT2L1	TCNT2L0
GRA_2	GRA2H7	GRA2H6	GRA2H5	GRA2H4	GRA2H3	GRA2H2	GRA2H1	GRA2H0
	GRA2L7	GRA2L6	GRA2L5	GRA2L4	GRA2L3	GRA2L2	GRA2L1	GRA2L0
GRB_2	GRB2H7	GRB2H6	GRB2H5	GRB2H4	GRB2H3	GRB2H2	GRB2H1	GRB2H0
	GRB2L7	GRB2L6	GRB2L5	GRB2L4	GRB2L3	GRB2L2	GRB2L1	GRB2L0

	GRA3L7	GRA3L6	GRA3L5	GRA3L4	GRA3L3	GRA3L2	GRA3L1	GRA3L0	
GRB_3	GRB3H7	GRB3H6	GRB3H5	GRB3H4	GRB3H3	GRB3H2	GRB3H1	GRB3H0	
	GRB3L7	GRB3L6	GRB3L5	GRB3L4	GRB3L3	GRB3L2	GRB3L1	GRB3L0	
GRC_3	GRC3H7	GRC3H6	GRC3H5	GRC3H4	GRC3H3	GRC3H2	GRC3H1	GRC3H0	
	GRC3L7	GRC3L6	GRC3L5	GRC3L4	GRC3L3	GRC3L2	GRC3L1	GRC3L0	
GRD_3	GRD3H7	GRD3H6	GRD3H5	GRD3H4	GRD3H3	GRD3H2	GRD3H1	GRD3H0	
	GRD3L7	GRD3L6	GRD3L5	GRD3L4	GRD3L3	GRD3L2	GRD3L1	GRD3L0	
TRCCNT	TCNTH7	TCNTH6	TCNTH5	TCNTH4	TCNTH3	TCNTH2	TCNTH1	TCNTH0	T
	TCNTL7	TCNTL6	TCNTL5	TCNTL4	TCNTL3	TCNTL2	TCNTL1	TCNTL0	
GRA	GRAH7	GRAH6	GRAH5	GRAH4	GRAH3	GRAH2	GRAH1	GRAH0	
	GRAL7	GRAL6	GRAL5	GRAL4	GRAL3	GRAL2	GRAL1	GRAL0	
GRB	GRBH7	GRBH6	GRBH5	GRBH4	GRBH3	GRBH2	GRBH1	GRBH0	
	GRBL7	GRBL6	GRBL5	GRBL4	GRBL3	GRBL2	GRBL1	GRBL0	
GRC	GRCH7	GRCH6	GRCH5	GRCH4	GRCH3	GRCH2	GRCH1	GRCH0	
	GRCL7	GRCL6	GRCL5	GRCL4	GRCL3	GRCL2	GRCL1	GRCL0	
GRD	GRDH7	GRDH6	GRDH5	GRDH4	GRDH3	GRDH2	GRDH1	GRDH0	
	GRDL7	GRDL6	GRDL5	GRDL4	GRDL3	GRDL2	GRDL1	GRDL0	
SMR_3	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0	S
BRR_3	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0	
SCR3_3	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_3	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	
SSR_3	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT	
RDR_3	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0	
SMCR_3	—	—	—	—	—	NFEN_3	TXD_3	MSTS3_3	

	AD1	AD0	—	—	—	—	—	—
ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
ADCR	TRGE	—	—	—	—	—	—	CH3
PDRD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PDRE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
PDRF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
PDRG	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
PDRH	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
PDRJ	—	—	—	—	—	—	PJ1	PJ0
PMRF	—	—	—	—	—	—	—	PMRF0
PMRG	PMRG7	PMRG6	PMRG5	—	PMRG3	PMRG2	PMRG1	PMRG0
PCRD	PCRD7	PCRD6	PCRD5	PCRD4	PCRD3	PCRD2	PCRD1	PCRD0
PCRE	PCRE7	PCRE6	PCRE5	PCRE4	PCRE3	PCRE2	PCRE1	PCRE0
PCRG	PCRG7	PCRG6	PCRG5	PCRG4	PCRG3	PCRG2	PCRG1	PCRG0
PCRH	PCRH7	PCRH6	PCRH5	PCRH4	PCRH3	PCRH2	PCRH1	PCRH0
PCRJ	—	—	—	—	—	—	PCRJ1	PCRJ0
MSTCR4	MSTTRC	MSTAD	MSTTRD0	MSTTRD1	—	—	—	—
TRDCR_0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
TRDIORA_0	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
TRDIORC_0	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
TRDSR_0	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA
TRDIER_0	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
POCR_0	—	—	—	—	—	POLD	POLC	POLB
TRDDF_0	DFCK1	DFCK0	—	—	DFD	DFC	DFB	DFA

TRDSTR_01	—	—	—	—	CSTPN1	CSTPN0	STR1	STR0	T
TRDMDR_01	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC	(C a
TRDPMR_01	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0	c
TRDFCR_01	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0	
TRDOER1_01	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0	
TRDOER2_01	PTO	—	—	—	—	—	—	—	
TRDOCR_01	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0	
TRDCR_2	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	T
TRDIORA_2	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	(C
TRDIORC_2	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
TRDSR_2	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA	
TRDIER_2	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA	
POCR_2	—	—	—	—	—	POLD	POLC	POLB	
TRDDF_2	DFCK1	DFCK0	—	—	DFD	DFC	DFB	DFA	
TRDCR_3	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	T
TRDIORA_3	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	(C
TRDIORC_3	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
TRDSR_3	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
TRDIER_3	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA	
POCR_3	—	—	—	—	—	POLD	POLC	POLB	
TRDDF_3	DFCK1	DFCK0	—	—	DFD	DFC	DFB	DFA	
TRDSTR_23	—	—	—	—	CSTPN1	CSTPN0	STR1	STR0	T
TRDMDR_23	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC	(C a
TRDPMR_23	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0	c

TRCSR	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
TRCIOR0	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
TRCIOR1	—	IOD2	IOD1	IOD0	—	IOC2	IOC1	IOC0
TRCCR2	TCEG1	TCEG0	CSTP	—	—	—	—	—
TRCDF	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
TRCOER	PTO	—	—	—	ED	EC	EB	EA
RSECDR	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00
RMINDR	BSY	MN12	MN11	MN10	MN03	MN02	MN01	MN00
RHRDR	BSY	—	HR11	HR10	HR03	HR02	HR01	HR00
RWKDR	BSY	—	—	—	—	WK2	WK1	WK0
RTCCR1	RUN	12/24	PM	RST	INT	—	—	—
RTCCR2	—	—	FOIE	WKIE	DYIE	HRIE	MNIE	SEIE
RTCCSR	—	RCS6	RCS5	—	RCS3	RCS2	RCS1	RCS0
LVDCR	—	—	—	—	LVDSEL	—	LVDDE	LVDUE
LVDSR	—	—	—	—	—	—	LVDDF	LVDUF
CKCSR	PMRJ1	PMRJ0	—	OSCSEL	CKSWIE	CKSWIF	—	CKSTA
RCCR	RCSTP	FSEL	VCLSEL	—	—	—	RCPSC1	RCPSC0
RCTRMDPR	WRI	PRWE	LOCKDW	TRMDRWE	—	—	—	—
RCTRMDR	TRMD7	TRMD6	TRMD5	TRMD4	TRMD3	TRMD2	TRMD1	TRMD0
ICRA	ICRA7	ICRA6	ICRA5	ICRA4	ICRA3	ICRA2	ICRA1	—
ICRB	—	ICRB6	ICRB5	ICRB4	—	—	—	—
ICRC	ICRC7	—	—	ICRC4	—	ICRC2	ICRC1	ICRC0
ICRD	ICRD7	ICRD6	ICRD5	ICRD4	ICRD3	—	—	—

ICCR2	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—	
ICMR	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0	
ICIER	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT	
ICSR	TDRE	TEND	RDRF	NACKF	STOP	AL/OVE	AAS	ADZ	
SAR	SVA6	SAV5	SAV4	SAV3	SVA2	SAV1	SAV0	FS	
ICDRT	ICDRT7	ICDRT6	ICDRT5	ICDRT4	ICDRT3	ICDRT2	ICDRT1	ICDRT0	
ICDRR	ICDRR7	ICDRR6	ICDRR5	ICDRR4	ICDRR3	ICDRR2	ICDRR1	ICDRR0	
TMB1	TMB17	—	—	—	—	TMB12	TMB11	TMB10	T
TCB1	TCB17	TCB16	TCB15	TCB14	TCB13	TCB12	TCB11	TCB10	
TLB1	TLB17	TLB16	TLB15	TLB14	TLB13	TLB12	TLB11	TLB10	
FLMCR1	—	SWE	ESU	PSU	EV	PV	E	P	R
FLMCR2	FLER	—	—	—	—	—	—	—	
FLPWCR	PDWND	—	—	—	—	—	—	—	
EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	
FENR	FLSHE	—	—	—	—	—	—	—	
TCRV0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	T
TCSRV	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	
TCORA	TCORA7	TCORA6	TCORA5	TCORA4	TCORA3	TCORA2	TCORA1	TCORA0	
TCORB	TCORB7	TCORB6	TCORB5	TCORB4	TCORB3	TCORB2	TCORB1	TCORB0	
TCNTV	TCNTV7	TCNTV6	TCNTV5	TCNTV4	TCNTV3	TCNTV2	TCNTV1	TCNTV0	
TCRV1	—	—	—	TVEG1	TVEG0	TRGE	—	ICKS0	
SMR	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0	S
BRR	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0	
SCR3	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	

TOWD	TOWD7	TOWD6	TOWD5	TOWD4	TOWD3	TOWD2	TOWD1	TOWD0
TMWD	—	—	—	—	CKS3	CKS2	CKS1	CKS0
ABRKCR	RTINTE	CSEL1	CSEL0	ACMP2	ACMP1	ACMP0	DCMP1	DCMP0
ABRKSR	ABIF	ABIE	—	—	—	—	—	—
BARH	BARH7	BARH6	BARH5	BARH4	BARH3	BARH2	BARH1	BARH0
BARL	BARL7	BARL6	BARL5	BARL4	BARL3	BARL2	BARL1	BARL0
BDRH	BDRH7	BDRH6	BDRH5	BDRH4	BDRH3	BDRH2	BDRH1	BDRH0
BDRL	BDRL7	BDRL6	BDRL5	BDRL4	BDRL3	BDRL2	BDRL1	BDRL0
BARE	BARE7	BARE6	BARE5	BARE4	BARE3	BARE2	BARE1	BARE0
PUCR1	PUCR17	PUCR16	PUCR15	PUCR14	—	PUCR12	PUCR11	PUCR10
PUCR5	—	—	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50
PDR1	P17	P16	P15	P14	—	P12	P11	P10
PDR2	P27	P26	P25	P24	P23	P22	P21	P20
PDR3	P37	P36	P35	P34	P33	P32	P31	P30
PDR5	P57	P56	P55	P54	P53	P52	P51	P50
PDR7	P77	P76	P75	P74	—	P72	P71	P70
PDR8	P87	P86	P85	—	—	—	—	—
PDRC	—	—	—	—	PC3	PC2	PC1	PC0
PMR1	IRQ3	IRQ2	IRQ1	IRQ0	TXD2	PWM	TXD	TMOW
PMR5	POF57	POF56	WKP5	WKP4	WKP3	WKP2	WKP1	WKP0
PMR3	POF27	POF26	POF25	POF24	POF23	—	—	—
PCR1	PCR17	PCR16	PCR15	PCR14	—	PCR12	PCR11	PCR10
PCR2	PCR27	PCR26	PCR25	PCR24	PCR23	PCR22	PCR21	PCR20
PCR3	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	PCR30

IEGR1	NMIEG	—	—	—	IEG3	IEG2	IEG1	IEG0	A
IEGR2	—	—	WPEG5	WPEG4	WPEG3	WPEG2	WPEG1	WPEG0	b
IENR1	IENDT	IENTA	IENWP	—	IEN3	IEN2	IEN1	IEN0	
IENR2	—	—	IENTB1	—	—	—	—	—	
IRR1	IRRDT	IRRTA	—	—	IRRI3	IRRI2	IRRI1	IRRI0	
IRR2	—	—	IRRTB1	—	—	—	—	—	
IWPR	—	—	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0	
MSTCR1	—	MSTIIC	MSTS3	—	MSTWD	—	MSTTV	MSTTA	P
MSTCR2	MSTS3_2	—	—	MSTTB1	—	—	—	MSTPWM	m

Note: * WDT: Watchdog timer

GRA_1	Initialized	—	—	—	—	—	(Cha
GRB_1	Initialized	—	—	—	—	—	
GRC_1	Initialized	—	—	—	—	—	
GRD_1	Initialized	—	—	—	—	—	
TRDCNT_2	Initialized	—	—	—	—	—	Time
GRA_2	Initialized	—	—	—	—	—	(Cha
GRB_2	Initialized	—	—	—	—	—	
GRC_2	Initialized	—	—	—	—	—	
GRD_2	Initialized	—	—	—	—	—	
TRDCNT_3	Initialized	—	—	—	—	—	Time
GRA_3	Initialized	—	—	—	—	—	(Cha
GRB_3	Initialized	—	—	—	—	—	
GRC_3	Initialized	—	—	—	—	—	
GRD_3	Initialized	—	—	—	—	—	
TRCCNT	Initialized	—	—	—	—	—	Time
GRA	Initialized	—	—	—	—	—	
GRB	Initialized	—	—	—	—	—	
GRC	Initialized	—	—	—	—	—	
GRD	Initialized	—	—	—	—	—	

ADDRB	Initialized	—	—	Initialized	Initialized	Initialized	
ADDRC	Initialized	—	—	Initialized	Initialized	Initialized	
ADDRD	Initialized	—	—	Initialized	Initialized	Initialized	
ADCSR	Initialized	—	—	Initialized	Initialized	Initialized	
ADCR	Initialized	—	—	Initialized	Initialized	Initialized	
PDRD	Initialized	—	—	—	—	—	I/O po
PDRE	Initialized	—	—	—	—	—	
PDRF	Initialized	—	—	—	—	—	
PDRG	Initialized	—	—	—	—	—	
PDRH	Initialized	—	—	—	—	—	
PDRJ	Initialized	—	—	—	—	—	
PMRF	Initialized	—	—	—	—	—	
PMRG	Initialized	—	—	—	—	—	
PCRD	Initialized	—	—	—	—	—	
PCRE	Initialized	—	—	—	—	—	
PCRG	Initialized	—	—	—	—	—	
PCRH	Initialized	—	—	—	—	—	
PCRJ	Initialized	—	—	—	—	—	
MSTCR4	Initialized	—	—	—	—	—	Powe mode

TRDIORA_1	Initialized	—	—	—	—	—	(Cha
TRDIORC_1	Initialized	—	—	—	—	—	
TRDSR_1	Initialized	—	—	—	—	—	
TRDIER_1	Initialized	—	—	—	—	—	
POCR_1	Initialized	—	—	—	—	—	
TRDDF_1	Initialized	—	—	—	—	—	
TRDSTR_01	Initialized	—	—	—	—	—	Time
TRDMDR_01	Initialized	—	—	—	—	—	(Cha
TRDPMR_01	Initialized	—	—	—	—	—	1 co
TRDFCR_01	Initialized	—	—	—	—	—	
TRDOER1_01	Initialized	—	—	—	—	—	
TRDOER2_01	Initialized	—	—	—	—	—	
TRDOCR_01	Initialized	—	—	—	—	—	
TRDCR_2	Initialized	—	—	—	—	—	Time
TRDIORA_2	Initialized	—	—	—	—	—	(Cha
TRDIORC_2	Initialized	—	—	—	—	—	
TRDSR_2	Initialized	—	—	—	—	—	
TRDIER_2	Initialized	—	—	—	—	—	
POCR_2	Initialized	—	—	—	—	—	
TRDDF_2	Initialized	—	—	—	—	—	

TRDMDR_23	Initialized	—	—	—	—	—	(Chan 3 com
TRDPMR_23	Initialized	—	—	—	—	—	
TRDFCR_23	Initialized	—	—	—	—	—	
TRDOER1_23	Initialized	—	—	—	—	—	
TRDOER2_23	Initialized	—	—	—	—	—	
TRDOCR_23	Initialized	—	—	—	—	—	
TRCMR	Initialized	—	—	—	—	—	Timer
TRCCR1	Initialized	—	—	—	—	—	
TRCIER	Initialized	—	—	—	—	—	
TRCSR	Initialized	—	—	—	—	—	
TRCIOR0	Initialized	—	—	—	—	—	
TRCIOR1	Initialized	—	—	—	—	—	
TRCCR2	Initialized	—	—	—	—	—	
TRCDF	Initialized	—	—	—	—	—	
TRCOER	Initialized	—	—	—	—	—	
RSECDR	Initialized	—	—	—	—	—	RTC
RMINDR	Initialized	—	—	—	—	—	
RHRDR	Initialized	—	—	—	—	—	
RWKDR	Initialized	—	—	—	—	—	
RTCCR1	Initialized	—	—	—	—	—	
RTCCR2	Initialized	—	—	—	—	—	
RTCCSR	Initialized	—	—	—	—	—	

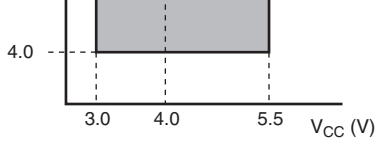
ICRB	Initialized						
ICRC	Initialized	—	—	—	—	—	
ICRD	Initialized	—	—	—	—	—	
SMR_2	Initialized	—	—	Initialized	Initialized	Initialized	SCI3
BRR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SCR3_2	Initialized	—	—	Initialized	Initialized	Initialized	
TDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SSR_2	Initialized	—	—	Initialized	Initialized	Initialized	
RDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
ICCR1	Initialized	—	—	—	—	—	IIC2
ICCR2	Initialized	—	—	—	—	—	
ICMR	Initialized	—	—	—	—	—	
ICIER	Initialized	—	—	—	—	—	
ICSR	Initialized	—	—	—	—	—	
SAR	Initialized	—	—	—	—	—	
ICDRT	Initialized	—	—	—	—	—	
ICDRR	Initialized	—	—	—	—	—	
TMB1	Initialized	—	—	—	—	—	Time
TCB1	Initialized	—	—	—	—	—	
TLB1	Initialized	—	—	—	—	—	

TCORB	Initialized	—	—	Initialized	Initialized	Initialized	
TCNTV	Initialized	—	—	Initialized	Initialized	Initialized	
TCRV1	Initialized	—	—	Initialized	Initialized	Initialized	
SMR	Initialized	—	—	Initialized	Initialized	Initialized	SCI3
BRR	Initialized	—	—	Initialized	Initialized	Initialized	
SCR3	Initialized	—	—	Initialized	Initialized	Initialized	
TDR	Initialized	—	—	Initialized	Initialized	Initialized	
SSR	Initialized	—	—	Initialized	Initialized	Initialized	
RDR	Initialized	—	—	Initialized	Initialized	Initialized	
PWDRL	Initialized	—	—	—	—	—	14-bit
PWDRU	Initialized	—	—	—	—	—	
PWCR	Initialized	—	—	—	—	—	
TCSRWD	Initialized	—	—	—	—	—	WDT[3]
TCWD	Initialized	—	—	—	—	—	
TMWD	Initialized	—	—	—	—	—	
ABRKCR	Initialized	—	—	—	—	—	Addre
ABRKSR	Initialized	—	—	—	—	—	
BARH	Initialized	—	—	—	—	—	
BARL	Initialized	—	—	—	—	—	
BDRH	Initialized	—	—	—	—	—	
BDRL	Initialized	—	—	—	—	—	
BARE	Initialized	—	—	—	—	—	

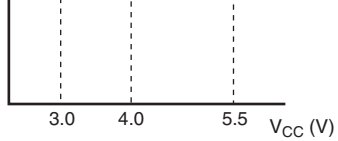
PDRC	Initialized	—	—	—	—	—	
PMR1	Initialized	—	—	—	—	—	
PMR5	Initialized	—	—	—	—	—	
PMR3	Initialized	—	—	—	—	—	
PCR1	Initialized	—	—	—	—	—	
PCR2	Initialized	—	—	—	—	—	
PCR3	Initialized	—	—	—	—	—	
PCR5	Initialized	—	—	—	—	—	
PCR7	Initialized	—	—	—	—	—	
PCR8	Initialized	—	—	—	—	—	
PCRC	Initialized	—	—	—	—	—	
SYSCR3	Initialized	—	—	—	—	—	Pow
SYSCR1	Initialized	—	—	—	—	—	mod
SYSCR2	Initialized	—	—	—	—	—	
IEGR1	Initialized	—	—	—	—	—	Inter
IEGR2	Initialized	—	—	—	—	—	
IENR1	Initialized	—	—	—	—	—	
IENR2	Initialized	—	—	—	—	—	
IRR1	Initialized	—	—	—	—	—	
IRR2	Initialized	—	—	—	—	—	
IWPR	Initialized	—	—	—	—	—	

	and X1			
	Ports F, G		–0.3 to AV_{CC} +0.3	V
	X1		–0.3 to 4.3	V
Operating temperature		T_{opr}	Regular specifications:	°C
			–20 to +75	
			Wide-range specifications:	°C
			–40 to +85	
Storage temperature		T_{stg}	–55 to +125	°C

Note: * Permanent damage may result if maximum ratings are exceeded. Normal oper should be under the conditions specified in Electrical Characteristics. Exceedin values can result in incorrect operation and reduced reliability.

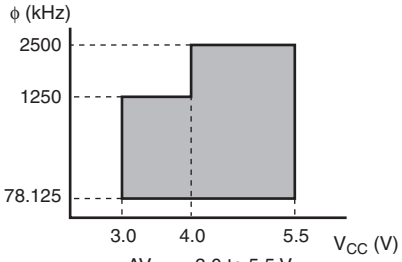


- AV_{CC} = 3.0 to 5.5 V
- Active mode
- Sleep mode



- AV_{CC} = 3.0 to 5.5 V
- All operating modes

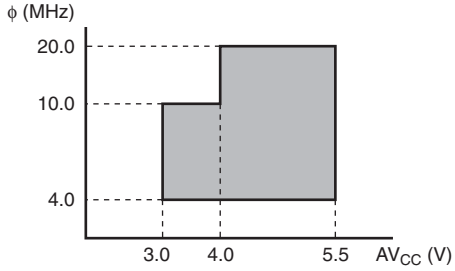
• Active mode
• Sleep mode
(When MA2 in SYSCR2 = 0)



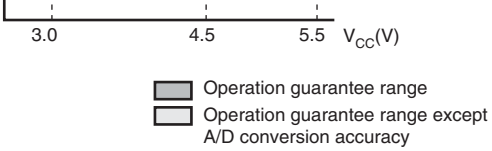
• AV_{CC} = 3.0 to 5.5 V
• Active mode
• Sleep mode
(When MA2 in SYSCR2 = 1)

• Subactive mode
• Subsleep mode

(3) Analog Power Supply Voltage and A/D Converter Accuracy Guarantee Rang



• V_{CC} = 3.0 to 5.5 V
• Active mode
• Sleep mode



23.2.2 DC Characteristics

Table 23.2 DC Characteristics (1)

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C/–40 to +85°C, unless otherwise indicat

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	N
				Min.	Typ.	Max.		
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$, TMIB1, TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, FTIOA2 to FTIOD2, FTIOA3 to FTIOD3, FTIOA to FTIOD, SCK3, SCK3_2, SCK3_3, TRGV, FTCI, TRGC, $\overline{TRCOI}$, $\overline{TRDOI\_0}$, $\overline{TRDOI\_1}$	V_{CC} = 4.0 to 5.5 V	V_{CC} × 0.8	—	V_{CC} + 0.3	V	
				V_{CC} × 0.9	—	V_{CC} + 0.3	V	

PC0 to PC3, PD0 to PD7, PE0 to PE7, PH0 to PH7, PJ0, PJ1					
PF0 to PF7, PG0 to PG7	AV_{cc} = 4.0 to 5.5 V	AV_{cc} × 0.7	—	AV_{cc} + 0.3	V
	AV_{cc} = 3.0 to 5.5 V	AV_{cc} × 0.8	—	AV_{cc} + 0.3	V
OSC1	V_{cc} = 4.0 to 5.5 V	V_{cc} – 0.5	—	V_{cc} + 0.3	V
		V_{cc} – 0.3	—	V_{cc} + 0.3	V

Note: Connect the TEST pin to Vss.

SCK3, SCK3_2, SCK3_3, TRGV, FTCI, TRGC, $\overline{\text{TRCOI}}$, $\overline{\text{TRDOI\_0}}$, $\overline{\text{TRODI\_1}}$					
RXD, RXD_2, RXD_3, SCL, SDA, P10 to P12, P14 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P72, P74 to P77, P85 to P87, PC0 to PC3 PD0 to PD7 PE0 to PE7 PH0 to PH7 PJ0, PJ1	V_{cc} = 4.0 to 5.5 V	–0.3	—	V_{cc} × 0.3	V
		–0.3	—	V_{cc} × 0.2	V
PF0 to PF7 PG0 to PG7	AV_{cc} = 4.0 to 5.5 V	–0.3	—	AV_{cc} × 0.3	V
	AV_{cc} = 3.0 to 5.5 V	–0.3	—	AV_{cc} × 0.2	V
OSC1	V_{cc} = 4.0 to 5.5 V	–0.3	—	0.5	V
		–0.3	—	0.3	V

		PH0 to PH7, PJ0, PJ1					
		PG0 to PG7	$-I_{OH}$ = 0.1 mA	AV_{CC} – 0.5	—	—	V
		P56, P57	4.0 V ≤ V_{CC} ≤ 5.5 V $-I_{OH}$ = 0.1 mA	V_{CC} – 2.5	—	—	V
			3.0 V ≤ V_{CC} < 4.0 V $-I_{OH}$ = 0.1 mA	V_{CC} – 2.2	—	—	V
Output low voltage	V_{OL}	P10 to P12, P14 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P72, P74 to P77, P85 to P87, PC0 to PC3, PH0 to PH3, PJ0, PJ1	V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.6	V
			I_{OL} = 0.2 mA	—	—	0.4	V
		PG0 to PG7	I_{OL} = 0.2 mA	—	—	0.4	V
		PD0 to PD7, PE0 to PE7, PH4 to PH7	V_{CC} = 4.0 to 5.5 V I_{OL} = 20.0 mA	—	—	1.5	V
			V_{CC} = 4.0 to 5.5 V I_{OL} = 10.0 mA	—	—	1.0	V
			V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.4	V
			I_{OL} = 0.4 mA	—	—	0.4	V
		SCL, SDA	V_{CC} = 4.0 to 5.5 V I_{OL} = 6.0 mA	—	—	0.6	V
			I_{OL} = 3.0 mA	—	—	0.4	V

		RXD_2, SCK3_2, RXD_3, SCK3_3, SCL, SDA, TMIB1, FTCI, TRGC, $\overline{\text{TRCOI}}$, $\overline{\text{TRDOI\_0}}$, $\overline{\text{TRDOI\_1}}$ P10 to P12, P14 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P72, P74 to P77, P85 to P87, PC0 to PC3, PD0 to PD7, PE0 to PE7, PH0 to PH7, PJ0, PJ1	V_{IN} = 0.5 V or higher (V_{CC} – 0.5 V)	—	—	1.0	µA	
		PF0 to PF7, PG0 to PG7	V_{IN} = 0.5 V or higher (AV_{CC} – 0.5 V)	—	—	1.0	µA	
Pull-up MOS current	$-I_p$	P10 to P12, P14 to P17, P50 to P55	V_{CC} = 5.0 V, V_{IN} = 0.0 V	50.0	—	300.0	µA	
			V_{CC} = 3.0 V, V_{IN} = 0.0 V	—	60.0	—	µA	P v
Input capacitance	C_{in}	All input pins except power supply pins	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	—	—	15.0	pF	

			V_{CC} = 3.0 V, f_{OSC} = 10 MHz				
Sleep mode supply current	I_{SLEEP1}	V_{CC}	Sleep mode 1 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	22.0	30.0	mA
			Sleep mode 1 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	12.0	—	
	I_{SLEEP2}	V_{CC}	Sleep mode 2 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	5.0	6.5	mA
			Sleep mode 2 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	4.5	—	
Subactive mode supply current	I_{SUB}	V_{CC}	V_{CC} = 3.0 V 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	130	150	µA
				—	50	70	
			V_{CC} = 3.0 V 32-kHz crystal resonator not used ($\phi_{SUB} = \phi_W/8$)	—	100	—	
				—	40	—	
Subsleep mode supply current	I_{SUBSP1}	V_{CC}	Subsleep mode 1 V_{CC} = 3.0 V 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	110	140	µA
				—	40	50	
	I_{SUBSP2}	V_{CC}	Subsleep mode 2 V_{CC} = 3.0 V 32-kHz crystal resonator not used	—	110	135	
				—	—	6.0	

pull-up MOS transistors and output buffers).

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	Oscillator Pins
Active mode 1	V_{CC}	Operates	V_{CC}	Main clock: ceramic or crystal res
Active mode 2		Operates (ϕ/64)		Subclock: Pin X1 = V_{SS}
Sleep mode 1	V_{CC}	Only timers operate	V_{CC}	
Sleep mode 2		Only timers operate (ϕ/64)		
Subactive mode	V_{CC}	Operates	V_{CC}	Main clock: ceramic or crystal res
Subsleep mode 1		Only timers operate	V_{CC}	Subclock: crystal resonator On-chip oscillator sto
Subsleep mode 2	V_{CC}	CPU and timers both stop	V_{CC}	Main clock: ceramic or crystal res
Standby mode				Subclock: Pin X1 = V_{SS} On-chip oscillator sto

		SCL, and SDA				
		Ports D, E, PH4 to PH7		—	—	10.0
		SCL, SDA		—	—	6.0
		Port G		—	—	0.4
Allowable output low current (total)	$\sum I_{OL}$	Output pins except ports D, E, PH4 to PH7, SCL, and SDA	V_{CC} = 4.0 to 5.5 V	—	—	40.0
		Ports D, E, PH4 to PH7, SCL, and SDA		—	—	120.0
		Output pins except ports D, E, G, PH4 to PH7		—	—	20.0
		Ports D, E, PH4 to PH7, SCL, and SDA		—	—	60.0
		Port G		—	—	3.2
Allowable output high current (per pin)	$\lvert -I_{OH} \rvert$	All output pins except P56, P57, and port G	V_{CC} = 4.0 to 5.5 V	—	—	5.0
				—	—	0.2
		P56, P57	V_{CC} = 4.0 to 5.5 V	—	—	0.4
				—	—	0.2
		Port G		—	—	0.2
Allowable output high current (total)	$\lvert -\sum I_{OH} \rvert$	All output pins	V_{CC} = 4.0 to 5.5 V	—	—	50.0
				—	—	8.0
		Port G		—	—	1.6

time				—	—	12.8	µs	
Subclock oscillation frequency	f_W	X1, X2		—	32.768	—	kHz	
Watch clock (ϕ_W) cycle time	t_W	X1, X2		—	30.5	—	µs	
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			2	—	8	t_W	*
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}	
Oscillation stabilization time (crystal resonator)	t_{rc}	OSC1, OSC2		—	—	10.0	ms	
Oscillation stabilization time (ceramic resonator)	t_{rc}	OSC1, OSC2		—	—	5.0	ms	
Oscillation stabilization time	t_{rcx}	X1, X2		—	—	2.0	s	
External clock high width	t_{CPH}	OSC1	V_{CC} = 4.0 to 5.5 V	20.0	—	—	ns	R
				40.0	—	—		
External clock low width	t_{CPL}	OSC1	V_{CC} = 4.0 to 5.5 V	20.0	—	—	ns	
				40.0	—	—		
External clock rise time	t_{CPr}	OSC1	V_{CC} = 4.0 to 5.5 V	—	—	10.0	ns	
				—	—	15.0		
External clock fall time	t_{CPf}	OSC1	V_{CC} = 4.0 to 5.5 V	—	—	10.0	ns	
				—	—	15.0		
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$	At power-on and in modes other than those below	t_{rc}	—	—	ms	R
			In active mode and sleep mode operation	1500	—	—	ns	

		TMCIV, TMRIV, TRGV, $\overline{\text{ADTRG}}$,				
		FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, FTIOA2 to FTIOD2, FTIOA3 to FTIOD3, FTIOA to FTIOD, FTCI, TRGC, $\overline{\text{TRCOI}}$, $\overline{\text{TRDOI\_0}}$, $\overline{\text{TRDOI\_1}}$	3	—	—	t_{cyc} t_{subcyc} ϕ40M
Input pin low width	t_{IL}	TMBI1, $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$, $\overline{\text{WKP0}}$ to $\overline{\text{WKP5}}$, TMCIV, TMRIV, TRGV, $\overline{\text{ADTRG}}$	3	—	—	t_{cyc} t_{subcyc}
		FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, FTIOA2 to FTIOD2, FTIOA3 to FTIOD3, FTIOA to FTIOD, FTCI, TRGC, $\overline{\text{TRCOI}}$, $\overline{\text{TRDOI\_0}}$, $\overline{\text{TRDOI\_1}}$	3	—	—	t_{cyc} t_{subcyc} ϕ40M

FSEL = 1 VCLSEL = 0				
V_{cc} = 4.0 to 5.5V Ta = -40°C to +85°C FSEL = 1 VCLSEL = 0	38.40	40.00	41.60	MHz
Ta = -20°C to +75°C FSEL = 1 VCLSEL = 0	38.40	40.00	41.60	MHz
Ta = -40°C to +85°C FSEL = 1 VCLSEL = 0	38.00	40.00	42.00	MHz
V_{cc} = 4.0 to 5.5V Ta = 25°C FSEL = 0 VCLSEL = 0	31.52	32.00	32.48	MHz
Ta = 25°C FSEL = 0 VCLSEL = 0	31.36	32.00	32.64	MHz
V_{cc} = 4.0 to 5.5V Ta = -20°C to +75°C FSEL = 0 VCLSEL = 0	31.04	32.00	32.96	MHz
V_{cc} = 4.0 to 5.5V Ta = -40°C to +85°C FSEL = 0 VCLSEL = 0	30.72	32.00	33.28	MHz
Ta = -20°C to +75°C FSEL = 0 VCLSEL = 0	30.72	32.00	33.28	MHz

Item	Symbol	Test Condition	Values			Unit
			Min.	Typ.	Max.	
SCL input cycle time	t_{SCL}		$12t_{cyc}$ + 600	—	—	ns
SCL input high width	t_{SCLH}		$3t_{cyc}$ + 300	—	—	ns
SCL input low width	t_{SCLL}		$5t_{cyc}$ + 300	—	—	ns
SCL and SDA input fall time	t_{Sf}		—	—	300	ns
SCL and SDA input spike pulse removal time	t_{SP}		—	—	$1t_{cyc}$	ns
SDA input bus-free time	t_{BUF}		$5t_{cyc}$	—	—	ns
Start condition input hold time	t_{STAH}		$3t_{cyc}$	—	—	ns
Retransmission start condition input setup time	t_{STAS}		$3t_{cyc}$	—	—	ns
Setup time for stop condition input	t_{STOS}		$3t_{cyc}$	—	—	ns
Data-input setup time	t_{SDAS}		$1t_{cyc}$+20	—	—	ns
Data-input hold time	t_{SDAH}		0	—	—	ns
Capacitive load of SCL and SDA	c_b		0	—	400	pF
SCL and SDA output fall time	t_{Sf}	V_{CC} = 4.0 to 5.5 V	—	—	250	ns
			—	—	300	

Input clock pulse width	t_{SCKW}	SCK3		0.4	—	0.6	t_{Scyc}	
Transmit data delay time (clocked synchronous)	t_{TXD}	TXD	V_{CC} = 4.0 to 5.5 V	—	—	1	t_{cyc}	F
				—	—	1		
Receive data setup time (clocked synchronous)	t_{RXS}	RXD	V_{CC} = 4.0 to 5.5 V	50.0	—	—	ns	
				100.0	—	—		
Receive data hold time (clocked synchronous)	t_{RXH}	RXD	V_{CC} = 4.0 to 5.5 V	50.0	—	—	ns	
				100.0	—	—		

		AN15					
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 5.0 V f_{OSC} = 20 MHz	—	—	2.0	mA
	AI_{STOP1}	AV_{CC}		—	50	—	µA
	AI_{STOP2}	AV_{CC}		—	—	5.0	µA
Analog input capacitance	C_{AIN}	AN0 to AN15		—	—	30.0	pF
Allowable signal source impedance	R_{AIN}	AN0 to AN15		—	—	5.0	kΩ
Resolution (data length)				10	10	10	Bit
Conversion time (single mode)		AN0 to AN15	AV_{CC} = 3.0 to 5.5 V	134	—	—	t_{cyc}
Nonlinearity error				—	—	±7.5	LSB
Offset error				—	—	±7.5	LSB
Full-scale error				—	—	±7.5	LSB
Quantization error				—	—	±0.5	LSB
Absolute accuracy				—	—	±8.0	LSB
Conversion time (single mode)		AN0 to AN15	AV_{CC} = 4.0 to 5.5 V	70	—	—	t_{cyc}
Nonlinearity error				—	—	±7.5	LSB
Offset error				—	—	±7.5	LSB
Full-scale error				—	—	±7.5	LSB
Quantization error				—	—	±0.5	LSB
Absolute accuracy				—	—	±8.0	LSB

Conversion time (single mode)	AN8 to AN15	AV_{CC} = 4.0 to 5.5 V	—	—	t_{cyc}	
Nonlinearity error			—	—	±5.5	LSB
Offset error			—	—	±5.5	LSB
Full-scale error			—	—	±5.5	LSB
Quantization error			—	—	±0.5	LSB
Absolute accuracy			—	—	±6.0	LSB

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at reset and in standby, subactive, and subsleep modes w A/D converter is idle.

23.2.5 Watchdog Timer Characteristics

Table 23.7 Watchdog Timer Characteristics

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C/–40 to +85°C, unless otherwise indicat

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	N
				Min.	Typ.	Max.		
Internal oscillator overflow time	t_{OVF}			0.2	0.4	—	s	*

Note: * Shows the time to count from 0 to 255, at which point an internal reset is gene when the internal oscillator is selected.

Reprogramming count		N_{WEC}		1000	10000	—
Programming	Wait time after SWE bit setting*[1]	x		1	—	—
	Wait time after PSU bit setting*[1]	y		50	—	—
	Wait time after P bit setting*[1]*[4]	z1	$1 \leq n \leq 6$	28	30	32
		z2	$7 \leq n \leq 1000$	198	200	202
		z3	Additional-programming	8	10	12
	Wait time after P bit clear*[1]	α		5	—	—
	Wait time after PSU bit clear*[1]	β		5	—	—
	Wait time after PV bit setting*[1]	γ		4	—	—
	Wait time after dummy write*[1]	ε		2	—	—
	Wait time after PV bit clear*[1]	η		2	—	—
	Wait time after SWE bit clear*[1]	θ		100	—	—
	Maximum programming count *[1]*[4]*[5]	N		—	—	1000

Wait time after dummy write*[1]	ε	2	—	—
Wait time after EV bit clear*[1]	η	4	—	—
Wait time after SWE bit clear*[1]	θ	100	—	—
Maximum erase count *[1]*[6]*[7]	N	—	—	120

Notes: 1. Make the time settings in accordance with the program/erase algorithms.

2. The programming time for 128 bytes. (Indicates the total time for which the P b flash memory control register 1 (FLMCR1) is set. The program-verify time is no included.)

3. The time required to erase one block. (Indicates the time for which the E bit in memory control register 1 (FLMCR1) is set. The erase-verify time is not includ

4. Maximum programming time (t_P (max.)) = wait time after P bit setting (z) × max programming count (N)

5. Set the maximum programming count (N) according to the actual set values of and z3, so that it does not exceed the maximum programming time (t_P (max.)). time after P bit setting (z1, z2) should be changed as follows according to the v the programming count (n).

   Programming count (n)

   $1 \leq n \leq 6$ z1 = 30 µs

   $7 \leq n \leq 1000$ z2 = 200 µs

6. Maximum erase time (t_E (max.)) = wait time after E bit setting (z) × maximum e count (N)

7. Set the maximum erase count (N) according to the actual set value of (z), so th does not exceed the maximum erase time (t_E (max.)).

voltage					
Reset detection voltage 1*[1]	Vreset1	LVDSEL = 0	—	2.3	2.6
Reset detection voltage 2*[2]	Vreset2	LVDSEL = 1	3.3	3.6	3.9
Lower-limit voltage of LVDR operation	$V_{LVDRmin}$		1.0	—	—

Notes: 1. This voltage should be used when the falling and rising voltage detection func
used.
2. Select the low-voltage reset 2 when only the low-voltage detection reset is us

Note: * The power-supply voltage (Vcc) must fall below Vpor = 100 mV and then rise a
charge of the $\overline{RES}$ pin is removed completely. In order to remove charge of the
pin, it is recommended that the diode be placed in the Vcc side. If the power-su
voltage (Vcc) rises from the point over 100 mV, a power-on reset may not occu

23.3 Operation Timing

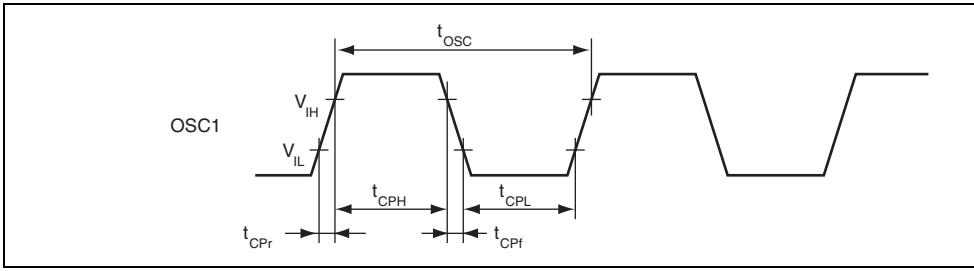


Figure 23.1 System Clock Input Timing

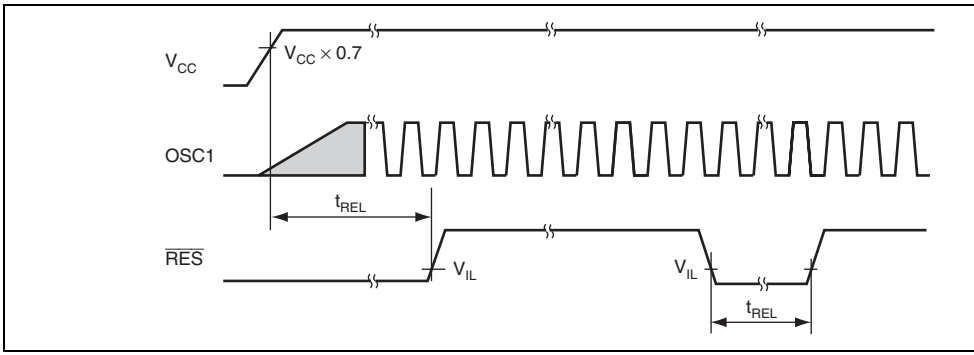
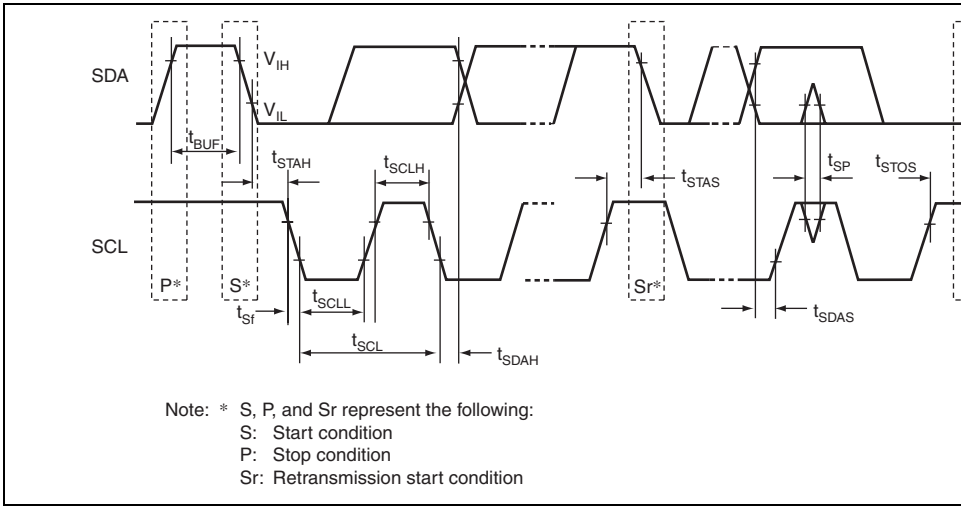


Figure 23.2 $\overline{RES}$ Low Width Timing



Note: * S, P, and Sr represent the following:
S: Start condition
P: Stop condition
Sr: Retransmission start condition

Figure 23.4 I²C Bus Interface Input/Output Timing

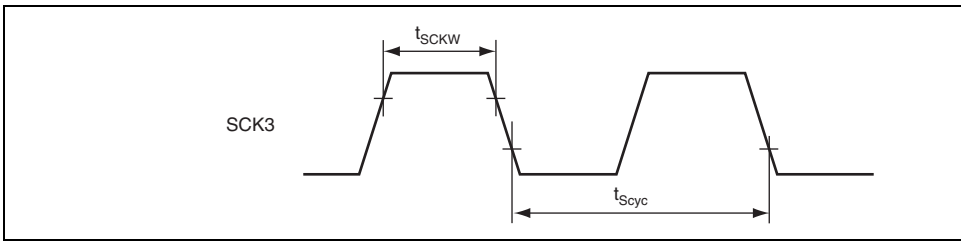


Figure 23.5 SCK3 Input Clock Timing

Note: * Output timing reference levels
Output high: V_{OH} = 2.0 V
Output low: V_{OL} = 0.8 V
Load conditions are shown in figure 23.7.

Figure 23.6 SCI Input/Output Timing in Clocked Synchronous Mode

23.4 Output Load Condition

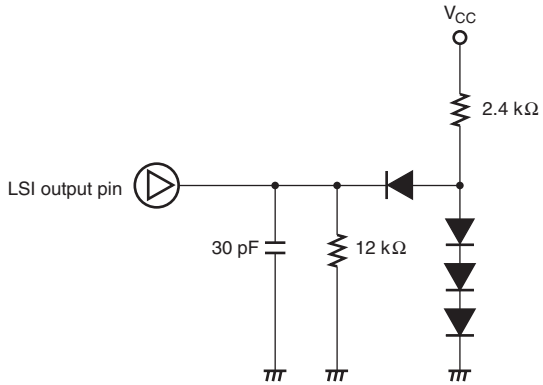


Figure 23.7 Output Load Circuit

Rd	General destination register
Rs	General source register
Rn	General register
ERd	General destination register (address register or 32-bit register)
ERs	General source register (address register or 32-bit register)
ERn	General register (32-bit register)
(EAd)	Destination operand
(EAs)	Source operand
PC	Program counter
SP	Stack pointer
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
disp	Displacement
→	Transfer from the operand on the left to the operand on the right, or trans the state on the left to the state on the right
+	Addition of the operands on both sides
–	Subtraction of the operand on the right from the operand on the left
×	Multiplication of the operands on both sides
÷	Division of the operand on the left by the operand on the right

1	Set to 1
—	Not affected by execution of the instruction
Δ	Varies depending on conditions, described in notes

Note: General registers include 8-bit registers (R0H to R7H and R0L to R7L) and 16-bit r
(R0 to R7 and E0 to E7).

	MOV.B @ERs, Rd	B			2						@ERs → Rd8	—	—	↕	↕	0
	MOV.B @(d:16, ERs), Rd	B				4					@(d:16, ERs) → Rd8	—	—	↕	↕	0
	MOV.B @(d:24, ERs), Rd	B				8					@(d:24, ERs) → Rd8	—	—	↕	↕	0
	MOV.B @ERs+, Rd	B					2				@ERs → Rd8 ERs32+1 → ERs32	—	—	↕	↕	0
	MOV.B @aa:8, Rd	B						2			@aa:8 → Rd8	—	—	↕	↕	0
	MOV.B @aa:16, Rd	B						4			@aa:16 → Rd8	—	—	↕	↕	0
	MOV.B @aa:24, Rd	B						6			@aa:24 → Rd8	—	—	↕	↕	0
	MOV.B Rs, @ERd	B			2						Rs8 → @ERd	—	—	↕	↕	0
	MOV.B Rs, @(d:16, ERd)	B				4					Rs8 → @(d:16, ERd)	—	—	↕	↕	0
	MOV.B Rs, @(d:24, ERd)	B				8					Rs8 → @(d:24, ERd)	—	—	↕	↕	0
	MOV.B Rs, @–ERd	B					2				ERd32–1 → ERd32 Rs8 → @ERd	—	—	↕	↕	0
	MOV.B Rs, @aa:8	B						2			Rs8 → @aa:8	—	—	↕	↕	0
	MOV.B Rs, @aa:16	B						4			Rs8 → @aa:16	—	—	↕	↕	0
	MOV.B Rs, @aa:24	B						6			Rs8 → @aa:24	—	—	↕	↕	0
	MOV.W #xx:16, Rd	W	4								#xx:16 → Rd16	—	—	↕	↕	0
	MOV.W Rs, Rd	W		2							Rs16 → Rd16	—	—	↕	↕	0
	MOV.W @ERs, Rd	W			2						@ERs → Rd16	—	—	↕	↕	0
	MOV.W @(d:16, ERs), Rd	W				4					@(d:16, ERs) → Rd16	—	—	↕	↕	0
	MOV.W @(d:24, ERs), Rd	W				8					@(d:24, ERs) → Rd16	—	—	↕	↕	0
	MOV.W @ERs+, Rd	W					2				@ERs → Rd16 ERs32+2 → @ERd32	—	—	↕	↕	0
	MOV.W @aa:16, Rd	W						4			@aa:16 → Rd16	—	—	↕	↕	0
	MOV.W @aa:24, Rd	W						6			@aa:24 → Rd16	—	—	↕	↕	0
	MOV.W Rs, @ERd	W			2						Rs16 → @ERd	—	—	↕	↕	0
	MOV.W Rs, @(d:16, ERd)	W				4					Rs16 → @(d:16, ERd)	—	—	↕	↕	0
	MOV.W Rs, @(d:24, ERd)	W				8					Rs16 → @(d:24, ERd)	—	—	↕	↕	0

	MOV.L ERs, ERd	L		2								ERs32 → ERd32	—	—	↕	↕	0	
	MOV.L @ERs, ERd	L			4							@ERs → ERd32	—	—	↕	↕	0	
	MOV.L @(d:16, ERs), ERd	L				6						@(d:16, ERs) → ERd32	—	—	↕	↕	0	
	MOV.L @(d:24, ERs), ERd	L				10						@(d:24, ERs) → ERd32	—	—	↕	↕	0	
	MOV.L @ERs+, ERd	L					4					@ERs → ERd32 ERs32+4 → ERs32	—	—	↕	↕	0	
	MOV.L @aa:16, ERd	L						6				@aa:16 → ERd32	—	—	↕	↕	0	
	MOV.L @aa:24, ERd	L						8				@aa:24 → ERd32	—	—	↕	↕	0	
	MOV.L ERs, @ERd	L			4							ERs32 → @ERd	—	—	↕	↕	0	
	MOV.L ERs, @(d:16, ERd)	L				6						ERs32 → @(d:16, ERd)	—	—	↕	↕	0	
	MOV.L ERs, @(d:24, ERd)	L				10						ERs32 → @(d:24, ERd)	—	—	↕	↕	0	
	MOV.L ERs, @–ERd	L					4					ERd32–4 → ERd32 ERs32 → @ERd	—	—	↕	↕	0	
	MOV.L ERs, @aa:16	L						6				ERs32 → @aa:16	—	—	↕	↕	0	
	MOV.L ERs, @aa:24	L						8				ERs32 → @aa:24	—	—	↕	↕	0	
POP	POP.W Rn	W									2	@SP → Rn16 SP+2 → SP	—	—	↕	↕	0	
	POP.L ERn	L									4	@SP → ERn32 SP+4 → SP	—	—	↕	↕	0	
PUSH	PUSH.W Rn	W									2	SP–2 → SP Rn16 → @SP	—	—	↕	↕	0	
	PUSH.L ERn	L									4	SP–4 → SP ERn32 → @SP	—	—	↕	↕	0	
MOVFPE	MOVFPE @aa:16, Rd	B						4				Cannot be used in this LSI	Cannot be used in this LSI					
MOVTPE	MOVTPE Rs, @aa:16	B						4				Cannot be used in this LSI	Cannot be used in this LSI					

	ADD.L #xx:32, ERd	L	6									ERd32+#xx:32 → ERd32	—	(2)	↕	↕	↕
	ADD.L ERs, ERd	L		2								ERd32+ERs32 → ERd32	—	(2)	↕	↕	↕
ADDX	ADDX.B #xx:8, Rd	B	2									Rd8+#xx:8 +C → Rd8	—	↕	↕	(3)	↕
	ADDX.B Rs, Rd	B		2								Rd8+Rs8 +C → Rd8	—	↕	↕	(3)	↕
ADDS	ADDS.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	—	—	—
	ADDS.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	—	—	—
	ADDS.L #4, ERd	L		2								ERd32+4 → ERd32	—	—	—	—	—
INC	INC.B Rd	B		2								Rd8+1 → Rd8	—	—	↕	↕	↕
	INC.W #1, Rd	W		2								Rd16+1 → Rd16	—	—	↕	↕	↕
	INC.W #2, Rd	W		2								Rd16+2 → Rd16	—	—	↕	↕	↕
	INC.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	↕	↕	↕
	INC.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	↕	↕	↕
DAA	DAA Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*
SUB	SUB.B Rs, Rd	B		2								Rd8–Rs8 → Rd8	—	↕	↕	↕	↕
	SUB.W #xx:16, Rd	W	4									Rd16–#xx:16 → Rd16	—	(1)	↕	↕	↕
	SUB.W Rs, Rd	W		2								Rd16–Rs16 → Rd16	—	(1)	↕	↕	↕
	SUB.L #xx:32, ERd	L	6									ERd32–#xx:32 → ERd32	—	(2)	↕	↕	↕
	SUB.L ERs, ERd	L		2								ERd32–ERs32 → ERd32	—	(2)	↕	↕	↕
SUBX	SUBX.B #xx:8, Rd	B	2									Rd8–#xx:8–C → Rd8	—	↕	↕	(3)	↕
	SUBX.B Rs, Rd	B		2								Rd8–Rs8–C → Rd8	—	↕	↕	(3)	↕
SUBS	SUBS.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	—	—	—
	SUBS.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	—	—	—
	SUBS.L #4, ERd	L		2								ERd32–4 → ERd32	—	—	—	—	—
DEC	DEC.B Rd	B		2								Rd8–1 → Rd8	—	—	↕	↕	↕
	DEC.W #1, Rd	W		2								Rd16–1 → Rd16	—	—	↕	↕	↕
	DEC.W #2, Rd	W		2								Rd16–2 → Rd16	—	—	↕	↕	↕

	MULXU. W Rs, ERd	W		2							Rd16 × Rs16 → ERd32 (unsigned multiplication)	—	—	—	—	—
MULXS	MULXS. B Rs, Rd	B		4							Rd8 × Rs8 → Rd16 (signed multiplication)	—	—	↕	↕	—
	MULXS. W Rs, ERd	W		4							Rd16 × Rs16 → ERd32 (signed multiplication)	—	—	↕	↕	—
DIVXU	DIVXU. B Rs, Rd	B		2							Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (unsigned division)	—	—	(6)	(7)	—
	DIVXU. W Rs, ERd	W		2							ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (unsigned division)	—	—	(6)	(7)	—
DIVXS	DIVXS. B Rs, Rd	B		4							Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (signed division)	—	—	(8)	(7)	—
	DIVXS. W Rs, ERd	W		4							ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (signed division)	—	—	(8)	(7)	—
CMP	CMP.B #xx:8, Rd	B	2								Rd8–#xx:8	—	↕	↕	↕	↕
	CMP.B Rs, Rd	B		2							Rd8–Rs8	—	↕	↕	↕	↕
	CMP.W #xx:16, Rd	W	4								Rd16–#xx:16	—	(1)	↕	↕	↕
	CMP.W Rs, Rd	W		2							Rd16–Rs16	—	(1)	↕	↕	↕
	CMP.L #xx:32, ERd	L	6								ERd32–#xx:32	—	(2)	↕	↕	↕
	CMP.L ERs, ERd	L		2							ERd32–ERs32	—	(2)	↕	↕	↕

	EXTU.L ERd	L		2								0 → (<bits 31 to 16> of ERd32)	—	—	0	↕	0
EXTS	EXTS.W Rd	W		2								(<bit 7> of Rd16) → (<bits 15 to 8> of Rd16)	—	—	↕	↕	0
	EXTS.L ERd	L		2								(<bit 15> of ERd32) → (<bits 31 to 16> of ERd32)	—	—	↕	↕	0

	AND.L #xx:32, ERd	L	6									ERd32∧#xx:32 → ERd32	—	—	↕	↕	0	-
	AND.L ERs, ERd	L		4								ERd32∧ERs32 → ERd32	—	—	↕	↕	0	-
OR	OR.B #xx:8, Rd	B	2									Rd8∨#xx:8 → Rd8	—	—	↕	↕	0	-
	OR.B Rs, Rd	B		2								Rd8∨Rs8 → Rd8	—	—	↕	↕	0	-
	OR.W #xx:16, Rd	W	4									Rd16∨#xx:16 → Rd16	—	—	↕	↕	0	-
	OR.W Rs, Rd	W		2								Rd16∨Rs16 → Rd16	—	—	↕	↕	0	-
	OR.L #xx:32, ERd	L	6									ERd32∨#xx:32 → ERd32	—	—	↕	↕	0	-
	OR.L ERs, ERd	L		4								ERd32∨ERs32 → ERd32	—	—	↕	↕	0	-
XOR	XOR.B #xx:8, Rd	B	2									Rd8⊕#xx:8 → Rd8	—	—	↕	↕	0	-
	XOR.B Rs, Rd	B		2								Rd8⊕Rs8 → Rd8	—	—	↕	↕	0	-
	XOR.W #xx:16, Rd	W	4									Rd16⊕#xx:16 → Rd16	—	—	↕	↕	0	-
	XOR.W Rs, Rd	W		2								Rd16⊕Rs16 → Rd16	—	—	↕	↕	0	-
	XOR.L #xx:32, ERd	L	6									ERd32⊕#xx:32 → ERd32	—	—	↕	↕	0	-
	XOR.L ERs, ERd	L		4								ERd32⊕ERs32 → ERd32	—	—	↕	↕	0	-
NOT	NOT.B Rd	B		2								¬ Rd8 → Rd8	—	—	↕	↕	0	-
	NOT.W Rd	W		2								¬ Rd16 → Rd16	—	—	↕	↕	0	-
	NOT.L ERd	L		2								¬ Rd32 → Rd32	—	—	↕	↕	0	-

	SHAR.W Rd	W		2								—	—	↕	↕	0
	SHAR.L ERd	L		2								—	—	↕	↕	0
SHLL	SHLL.B Rd	B		2								—	—	↕	↕	0
	SHLL.W Rd	W		2								—	—	↕	↕	0
	SHLL.L ERd	L		2								—	—	↕	↕	0
SHLR	SHLR.B Rd	B		2								—	—	↕	↕	0
	SHLR.W Rd	W		2								—	—	↕	↕	0
	SHLR.L ERd	L		2								—	—	↕	↕	0
ROTXL	ROTXL.B Rd	B		2								—	—	↕	↕	0
	ROTXL.W Rd	W		2								—	—	↕	↕	0
	ROTXL.L ERd	L		2								—	—	↕	↕	0
ROTXR	ROTXR.B Rd	B		2								—	—	↕	↕	0
	ROTXR.W Rd	W		2								—	—	↕	↕	0
	ROTXR.L ERd	L		2								—	—	↕	↕	0
ROTL	ROTL.B Rd	B		2								—	—	↕	↕	0
	ROTL.W Rd	W		2								—	—	↕	↕	0
	ROTL.L ERd	L		2								—	—	↕	↕	0
ROTR	ROTR.B Rd	B		2								—	—	↕	↕	0
	ROTR.W Rd	W		2								—	—	↕	↕	0
	ROTR.L ERd	L		2								—	—	↕	↕	0

	BSET Rn, @ERd	B			4							(Rn8 of @ERd) ← 1	—	—	—	—	—
	BSET Rn, @aa:8	B						4				(Rn8 of @aa:8) ← 1	—	—	—	—	—
BCLR	BCLR #xx:3, Rd	B		2								(#xx:3 of Rd8) ← 0	—	—	—	—	—
	BCLR #xx:3, @ERd	B			4							(#xx:3 of @ERd) ← 0	—	—	—	—	—
	BCLR #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) ← 0	—	—	—	—	—
	BCLR Rn, Rd	B		2								(Rn8 of Rd8) ← 0	—	—	—	—	—
	BCLR Rn, @ERd	B			4							(Rn8 of @ERd) ← 0	—	—	—	—	—
	BCLR Rn, @aa:8	B						4				(Rn8 of @aa:8) ← 0	—	—	—	—	—
BNOT	BNOT #xx:3, Rd	B		2								(#xx:3 of Rd8) ← ¬ (#xx:3 of Rd8)	—	—	—	—	—
	BNOT #xx:3, @ERd	B			4							(#xx:3 of @ERd) ← ¬ (#xx:3 of @ERd)	—	—	—	—	—
	BNOT #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) ← ¬ (#xx:3 of @aa:8)	—	—	—	—	—
	BNOT Rn, Rd	B		2								(Rn8 of Rd8) ← ¬ (Rn8 of Rd8)	—	—	—	—	—
	BNOT Rn, @ERd	B			4							(Rn8 of @ERd) ← ¬ (Rn8 of @ERd)	—	—	—	—	—
	BNOT Rn, @aa:8	B						4				(Rn8 of @aa:8) ← ¬ (Rn8 of @aa:8)	—	—	—	—	—
BTST	BTST #xx:3, Rd	B		2								¬ (#xx:3 of Rd8) → Z	—	—	—	↕	—
	BTST #xx:3, @ERd	B			4							¬ (#xx:3 of @ERd) → Z	—	—	—	↕	—
	BTST #xx:3, @aa:8	B						4				¬ (#xx:3 of @aa:8) → Z	—	—	—	↕	—
	BTST Rn, Rd	B		2								¬ (Rn8 of @Rd8) → Z	—	—	—	↕	—
	BTST Rn, @ERd	B			4							¬ (Rn8 of @ERd) → Z	—	—	—	↕	—
	BTST Rn, @aa:8	B						4				¬ (Rn8 of @aa:8) → Z	—	—	—	↕	—
BLD	BLD #xx:3, Rd	B		2								(#xx:3 of Rd8) → C	—	—	—	—	—

BST	BST #xx:3, Rd	B		2								C → (#xx:3 of Rd8)	—	—	—	—	—
	BST #xx:3, @ERd	B			4							C → (#xx:3 of @ERd24)	—	—	—	—	—
	BST #xx:3, @aa:8	B						4				C → (#xx:3 of @aa:8)	—	—	—	—	—
BIST	BIST #xx:3, Rd	B		2								¬ C → (#xx:3 of Rd8)	—	—	—	—	—
	BIST #xx:3, @ERd	B			4							¬ C → (#xx:3 of @ERd24)	—	—	—	—	—
	BIST #xx:3, @aa:8	B						4				¬ C → (#xx:3 of @aa:8)	—	—	—	—	—
BAND	BAND #xx:3, Rd	B		2								C∧(#xx:3 of Rd8) → C	—	—	—	—	—
	BAND #xx:3, @ERd	B			4							C∧(#xx:3 of @ERd24) → C	—	—	—	—	—
	BAND #xx:3, @aa:8	B						4				C∧(#xx:3 of @aa:8) → C	—	—	—	—	—
BIAND	BIAND #xx:3, Rd	B		2								C∧ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—
	BIAND #xx:3, @ERd	B			4							C∧ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—
	BIAND #xx:3, @aa:8	B						4				C∧ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—
BOR	BOR #xx:3, Rd	B		2								C∨(#xx:3 of Rd8) → C	—	—	—	—	—
	BOR #xx:3, @ERd	B			4							C∨(#xx:3 of @ERd24) → C	—	—	—	—	—
	BOR #xx:3, @aa:8	B						4				C∨(#xx:3 of @aa:8) → C	—	—	—	—	—
BIOR	BIOR #xx:3, Rd	B		2								C∨ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—
	BIOR #xx:3, @ERd	B			4							C∨ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—
	BIOR #xx:3, @aa:8	B						4				C∨ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—
BXOR	BXOR #xx:3, Rd	B		2								C⊕(#xx:3 of Rd8) → C	—	—	—	—	—
	BXOR #xx:3, @ERd	B			4							C⊕(#xx:3 of @ERd24) → C	—	—	—	—	—
	BXOR #xx:3, @aa:8	B						4				C⊕(#xx:3 of @aa:8) → C	—	—	—	—	—
BIXOR	BIXOR #xx:3, Rd	B		2								C⊕ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—
	BIXOR #xx:3, @ERd	B			4							C⊕ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—
	BIXOR #xx:3, @aa:8	B						4				C⊕ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—

	BHI d:8	—							2			C∨ Z = 0	—	—	—	—	—	—
	BHI d:16	—							4				—	—	—	—	—	—
	BLS d:8	—							2			C∨ Z = 1	—	—	—	—	—	—
	BLS d:16	—							4				—	—	—	—	—	—
	BCC d:8 (BHS d:8)	—							2			C = 0	—	—	—	—	—	—
	BCC d:16 (BHS d:16)	—							4				—	—	—	—	—	—
	BCS d:8 (BLO d:8)	—							2			C = 1	—	—	—	—	—	—
	BCS d:16 (BLO d:16)	—							4				—	—	—	—	—	—
	BNE d:8	—							2			Z = 0	—	—	—	—	—	—
	BNE d:16	—							4				—	—	—	—	—	—
	BEQ d:8	—							2			Z = 1	—	—	—	—	—	—
	BEQ d:16	—							4				—	—	—	—	—	—
	BVC d:8	—							2			V = 0	—	—	—	—	—	—
	BVC d:16	—							4				—	—	—	—	—	—
	BVS d:8	—							2			V = 1	—	—	—	—	—	—
	BVS d:16	—							4				—	—	—	—	—	—
	BPL d:8	—							2			N = 0	—	—	—	—	—	—
	BPL d:16	—							4				—	—	—	—	—	—
	BMI d:8	—							2			N = 1	—	—	—	—	—	—
	BMI d:16	—							4				—	—	—	—	—	—
	BGE d:8	—							2			N⊕V = 0	—	—	—	—	—	—
	BGE d:16	—							4				—	—	—	—	—	—
	BLT d:8	—							2			N⊕V = 1	—	—	—	—	—	—
	BLT d:16	—							4				—	—	—	—	—	—
	BGT d:8	—							2			Z∨ (N⊕V) = 0	—	—	—	—	—	—
	BGT d:16	—							4				—	—	—	—	—	—
	BLE d:8	—							2			Z∨ (N⊕V) = 1	—	—	—	—	—	—
	BLE d:16	—							4				—	—	—	—	—	—

	BSR d:16	—						4			PC → @–SP PC ← PC+d:16	—	—	—	—	—	
JSR	JSR @ERn	—			2						PC → @–SP PC ← ERn	—	—	—	—	—	
	JSR @aa:24	—						4			PC → @–SP PC ← aa:24	—	—	—	—	—	
	JSR @@aa:8	—							2		PC → @–SP PC ← @aa:8	—	—	—	—	—	
RTS	RTS	—								2	PC ← @SP+	—	—	—	—	—	

RTE	RTE	—										CCR ← @SP+ PC ← @SP+	↕	↕	↕	↕	↕	↕
SLEEP	SLEEP	—										Transition to power-down state	—	—	—	—	—	—
LDC	LDC #xx:8, CCR	B	2									#xx:8 → CCR	↕	↕	↕	↕	↕	↕
	LDC Rs, CCR	B		2								Rs8 → CCR	↕	↕	↕	↕	↕	↕
	LDC @ERs, CCR	W			4							@ERs → CCR	↕	↕	↕	↕	↕	↕
	LDC @(d:16, ERs), CCR	W				6						@(d:16, ERs) → CCR	↕	↕	↕	↕	↕	↕
	LDC @(d:24, ERs), CCR	W				10						@(d:24, ERs) → CCR	↕	↕	↕	↕	↕	↕
	LDC @ERs+, CCR	W					4					@ERs → CCR ERs32+2 → ERs32	↕	↕	↕	↕	↕	↕
	LDC @aa:16, CCR	W						6				@aa:16 → CCR	↕	↕	↕	↕	↕	↕
	LDC @aa:24, CCR	W						8				@aa:24 → CCR	↕	↕	↕	↕	↕	↕
STC	STC CCR, Rd	B		2								CCR → Rd8	—	—	—	—	—	—
	STC CCR, @ERd	W			4							CCR → @ERd	—	—	—	—	—	—
	STC CCR, @(d:16, ERd)	W				6						CCR → @(d:16, ERd)	—	—	—	—	—	—
	STC CCR, @(d:24, ERd)	W				10						CCR → @(d:24, ERd)	—	—	—	—	—	—
	STC CCR, @–ERd	W					4					ERd32–2 → ERd32 CCR → @ERd	—	—	—	—	—	—
	STC CCR, @aa:16	W						6				CCR → @aa:16	—	—	—	—	—	—
	STC CCR, @aa:24	W						8				CCR → @aa:24	—	—	—	—	—	—
ANDC	ANDC #xx:8, CCR	B	2									CCR∧#xx:8 → CCR	↕	↕	↕	↕	↕	↕
ORC	ORC #xx:8, CCR	B	2									CCR∨#xx:8 → CCR	↕	↕	↕	↕	↕	↕
XORC	XORC #xx:8, CCR	B	2									CCR⊕#xx:8 → CCR	↕	↕	↕	↕	↕	↕
NOP	NOP	—									2	PC ← PC+2	—	—	—	—	—	—

												R4L–1 → R4L						
											until	R4L=0						
											else next							
	EEPMOV. W	—								4	if R4 ≠ 0 then		—	—	—	—	—	
											repeat	@R5 → @R6						
												R5+1 → R5						
												R6+1 → R6						
												R4–1 → R4						
											until	R4=0						
											else next							

Notes: 1. The number of states in cases where the instruction code and its operands ar
in on-chip memory is shown here. For other cases see appendix A.3, Numbe
Execution States.

2. The value n is set in register R4L or R4.
   (1) Set to 1 when a carry or borrow occurs at bit 11; otherwise cleared to 0.
   (2) Set to 1 when a carry or borrow occurs at bit 27; otherwise cleared to 0.
   (3) Retains its previous value when the result is zero; otherwise cleared to 0.
   (4) Set to 1 when the adjustment produces a carry; otherwise retains its prev
   (5) The number of states required for execution of an instruction that transfer
   synchronization with the E clock is variable.
   (6) Set to 1 when the divisor is negative; otherwise cleared to 0.
   (7) Set to 1 when the divisor is zero; otherwise cleared to 0.
   (8) Set to 1 when the quotient is negative; otherwise cleared to 0.

Instruction code:

1st byte		2nd byte	
AH	AL	BH	BL

Instruction when most significant bit of BH is 0.

Instruction when most significant bit of BH is 1.

AH \ AL	0	1	2	3	4	5	6	7	8	9	A	B	C
0	NOP	Table A.2 (2)	STC	LDC	ORC	XORC	ANDC	LDC	ADD		Table A.2 (2)	Table A.2 (2)	
1	Table A.2 (2)	Table A.2 (2)	Table A.2 (2)	Table A.2 (2)	OR.B	XOR.B	AND.B	Table A.2 (2)	SUB		Table A.2 (2)	Table A.2 (2)	
2	MOV.B												
3													
4	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGE
5	MULXU	DIVXU	MULXU	DIVXU	RTS	BSR	RTE	TRAPA	Table A.2 (2)	JMP			BSR
6	BSET	BNOT	BCLR	BTST	OR	XOR	AND	BST / BIST	MOV				
7					BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD	MOV	Table A.2 (2)	Table A.2 (2)	EEPMOV	
8	ADD												
9	ADDX												
A	CMP												
B	SUBX												
C	OR												
D	XOR												
E	AND												
F	MOV												

Instruction code:

1st byte		2nd byte	
AH	AL	BH	BL

AH AL \ BH	0	1	2	3	4	5	6	7	8	9	A	B
01	MOV				LDC/STC				SLEEP			
0A	INC								AD			
0B	ADDS					INC		INC	ADDS			
0F	DAA								MO			
10	SHLL			SHLL					SHAL			SHAL
11	SHLR			SHLR					SHAR			SHAR
12	ROTXL			ROTXL					ROTL			ROTL
13	ROTXR			ROTXR					ROTR			ROTR
17	NOT			NOT		EXTU		EXTU	NEG			NEG
1A	DEC								SU			
1B	SUBS					DEC		DEC	SUB			
1F	DAS								CM			
58	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI
79	MOV	ADD	CMP	SUB	OR	XOR	AND					

Instruction code:

1st byte		2nd byte		3rd byte		4th byte	
AH	AL	BH	BL	CH	CL	DH	DL

Instruction when most

Instruction when most

AH / ALBH / BLCH \ CL	0	1	2	3	4	5	6	7	8	9	A	B
01406										LDC / STC		LDC /
01C05	MULXS		MULXS									
01D05		DIVXS		DIVXS								
01F06					OR	XOR	AND					
7Cr06*1				BTST								
7Cr07*1				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD				
7Dr06*1	BSET	BNOT	BCLR					BST / BIST				
7Dr07*1	BSET	BNOT	BCLR									
7Eaa6*2				BTST								
7Eaa7*2				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD				
7Faa6*2	BSET	BNOT	BCLR					BST / BIST				
7Faa7*2	BSET	BNOT	BCLR									

Notes: 1. r is the register designation field.
2. aa is the absolute address field.

BSET #0, @FF00

From table A.4:

I = L = 2, J = K = M = N= 0

From table A.3:

$S_I = 2$, $S_L = 2$

Number of states required for execution = $2 \times 2 + 2 \times 2 = 8$

When instruction is fetched from on-chip ROM, branch address is read from on-chip RO
on-chip RAM is used for stack area.

JSR @@ 30

From table A.4:

I = 2, J = K = 1, L = M = N = 0

From table A.3:

$S_I = S_J = S_K = 2$

Number of states required for execution = $2 \times 2 + 1 \times 2 + 1 \times 2 = 8$

Note: * Depends on which on-chip peripheral module is accessed. For details, see sec
22.1, Register Addresses (Address Order).

ADDX	ADDX #xx:8, Rd	1		
	ADDX Rs, Rd	1		
AND	AND.B #xx:8, Rd	1		
	AND.B Rs, Rd	1		
	AND.W #xx:16, Rd	2		
	AND.W Rs, Rd	1		
	AND.L #xx:32, ERd	3		
	AND.L ERs, ERd	2		
ANDC	ANDC #xx:8, CCR	1		
BAND	BAND #xx:3, Rd	1		
	BAND #xx:3, @ERd	2		1
	BAND #xx:3, @aa:8	2		1
Bcc	BRA d:8 (BT d:8)	2		
	BRN d:8 (BF d:8)	2		
	BHI d:8	2		
	BLS d:8	2		
	BCC d:8 (BHS d:8)	2		
	BCS d:8 (BLO d:8)	2		
	BNE d:8	2		
	BEQ d:8	2		
	BVC d:8	2		
	BVS d:8	2		
	BPL d:8	2		
	BMI d:8	2		
	BGE d:8	2		

	BCC d:16(BHS d:16)	2		2
	BCS d:16(BLO d:16)	2		2
	BNE d:16	2		2
	BEQ d:16	2		2
	BVC d:16	2		2
	BVS d:16	2		2
	BPL d:16	2		2
	BMI d:16	2		2
	BGE d:16	2		2
	BLT d:16	2		2
	BGT d:16	2		2
	BLE d:16	2		2
BCLR	BCLR #xx:3, Rd	1		
	BCLR #xx:3, @ERd	2	2	
	BCLR #xx:3, @aa:8	2	2	
	BCLR Rn, Rd	1		
	BCLR Rn, @ERd	2	2	
	BCLR Rn, @aa:8	2	2	
BIAND	BIAND #xx:3, Rd	1		
	BIAND #xx:3, @ERd	2	1	
	BIAND #xx:3, @aa:8	2	1	
BILD	BILD #xx:3, Rd	1		
	BILD #xx:3, @ERd	2	1	
	BILD #xx:3, @aa:8	2	1	

	BIXOR #xx:3, @aa:8	2		1
BLD	BLD #xx:3, Rd	1		
	BLD #xx:3, @ERd	2		1
	BLD #xx:3, @aa:8	2		1
BNOT	BNOT #xx:3, Rd	1		
	BNOT #xx:3, @ERd	2		2
	BNOT #xx:3, @aa:8	2		2
	BNOT Rn, Rd	1		
	BNOT Rn, @ERd	2		2
	BNOT Rn, @aa:8	2		2
BOR	BOR #xx:3, Rd	1		
	BOR #xx:3, @ERd	2		1
	BOR #xx:3, @aa:8	2		1
BSET	BSET #xx:3, Rd	1		
	BSET #xx:3, @ERd	2		2
	BSET #xx:3, @aa:8	2		2
	BSET Rn, Rd	1		
	BSET Rn, @ERd	2		2
	BSET Rn, @aa:8	2		2
BSR	BSR d:8	2	1	
	BSR d:16	2	1	
BST	BST #xx:3, Rd	1		
	BST #xx:3, @ERd	2		2
	BST #xx:3, @aa:8	2		2

	BXOR #xx:3, @ERd	2		1
	BXOR #xx:3, @aa:8	2		1
CMP	CMP.B #xx:8, Rd	1		
	CMP.B Rs, Rd	1		
	CMP.W #xx:16, Rd	2		
	CMP.W Rs, Rd	1		
	CMP.L #xx:32, ERd	3		
	CMP.L ERs, ERd	1		
DAA	DAA Rd	1		
DAS	DAS Rd	1		
DEC	DEC.B Rd	1		
	DEC.W #1/2, Rd	1		
	DEC.L #1/2, ERd	1		
DUVXS	DIVXS.B Rs, Rd	2		
	DIVXS.W Rs, ERd	2		
DIVXU	DIVXU.B Rs, Rd	1		
	DIVXU.W Rs, ERd	1		
EEPMOV	EEPMOV.B	2		2n+2*[1]
	EEPMOV.W	2		2n+2*[1]
EXTS	EXTS.W Rd	1		
	EXTS.L ERd	1		
EXTU	EXTU.W Rd	1		
	EXTU.L ERd	1		

	JSR @aa:24	2		1			
	JSR @@aa:8	2	1	1			
LDC	LDC #xx:8, CCR	1					
	LDC Rs, CCR	1					
	LDC@ERs, CCR	2					1
	LDC@(d:16, ERs), CCR	3					1
	LDC@(d:24,ERs), CCR	5					1
	LDC@ERs+, CCR	2					1
	LDC@aa:16, CCR	3					1
	LDC@aa:24, CCR	4					1
MOV	MOV.B #xx:8, Rd	1					
	MOV.B Rs, Rd	1					
	MOV.B @ERs, Rd	1			1		
	MOV.B @(d:16, ERs), Rd	2			1		
	MOV.B @(d:24, ERs), Rd	4			1		
	MOV.B @ERs+, Rd	1			1		
	MOV.B @aa:8, Rd	1			1		
	MOV.B @aa:16, Rd	2			1		
	MOV.B @aa:24, Rd	3			1		
	MOV.B Rs, @Erd	1			1		
	MOV.B Rs, @(d:16, ERd)	2			1		
	MOV.B Rs, @(d:24, ERd)	4			1		
	MOV.B Rs, @-ERd	1			1		
	MOV.B Rs, @aa:8	1			1		

	MOV.W @aa:16, Rd	2		1
	MOV.W @aa:24, Rd	3		1
	MOV.W Rs, @ERd	1		1
	MOV.W Rs, @(d:16,ERd)	2		1
	MOV.W Rs, @(d:24,ERd)	4		1
MOV	MOV.W Rs, @-ERd	1		1
	MOV.W Rs, @aa:16	2		1
	MOV.W Rs, @aa:24	3		1
	MOV.L #xx:32, ERd	3		
	MOV.L ERs, ERd	1		
	MOV.L @ERs, ERd	2		2
	MOV.L @(d:16,ERs), ERd	3		2
	MOV.L @(d:24,ERs), ERd	5		2
	MOV.L @ERs+, ERd	2		2
	MOV.L @aa:16, ERd	3		2
	MOV.L @aa:24, ERd	4		2
	MOV.L ERs,@ERd	2		2
	MOV.L ERs, @(d:16,ERd)	3		2
	MOV.L ERs, @(d:24,ERd)	5		2
	MOV.L ERs, @-ERd	2		2
	MOV.L ERs, @aa:16	3		2
	MOV.L ERs, @aa:24	4		2
MOVFPE	MOVFPE @aa:16, Rd*[2]	2	1	
MOVTPE	MOVTPE Rs,@aa:16*[2]	2	1	

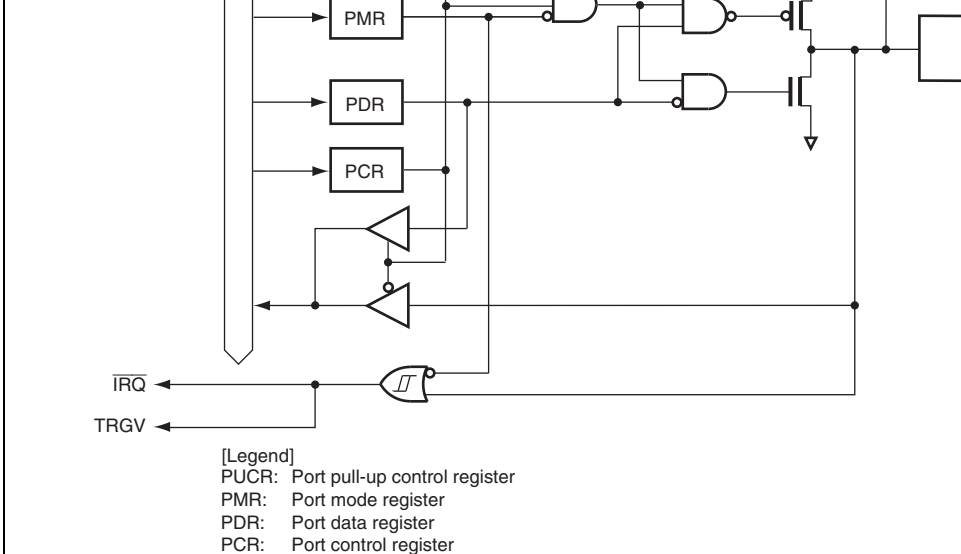
NOP	NOP	1		
NOT	NOT.B Rd	1		
	NOT.W Rd	1		
	NOT.L ERd	1		
OR	OR.B #xx:8, Rd	1		
	OR.B Rs, Rd	1		
	OR.W #xx:16, Rd	2		
	OR.W Rs, Rd	1		
	OR.L #xx:32, ERd	3		
	OR.L ERs, ERd	2		
ORC	ORC #xx:8, CCR	1		
POP	POP.W Rn	1		1
	POP.L ERn	2		2
PUSH	PUSH.W Rn	1		1
	PUSH.L ERn	2		2
ROTL	ROTL.B Rd	1		
	ROTL.W Rd	1		
	ROTL.L ERd	1		
ROTR	ROTR.B Rd	1		
	ROTR.W Rd	1		
	ROTR.L ERd	1		
ROTXL	ROTXL.B Rd	1		
	ROTXL.W Rd	1		
	ROTXL.L ERd	1		

	SHAL.L ERd	1		
SHAR	SHAR.B Rd	1		
	SHAR.W Rd	1		
	SHAR.L ERd	1		
SHLL	SHLL.B Rd	1		
	SHLL.W Rd	1		
	SHLL.L ERd	1		
SHLR	SHLR.B Rd	1		
	SHLR.W Rd	1		
	SHLR.L ERd	1		
SLEEP	SLEEP	1		
STC	STC CCR, Rd	1		
	STC CCR, @ERd	2		1
	STC CCR, @(d:16,ERd)	3		1
	STC CCR, @(d:24,ERd)	5		1
	STC CCR,@-ERd	2		1
	STC CCR, @aa:16	3		1
	STC CCR, @aa:24	4		1
SUB	SUB.B Rs, Rd	1		
	SUB.W #xx:16, Rd	2		
	SUB.W Rs, Rd	1		
	SUB.L #xx:32, ERd	3		
	SUB.L ERs, ERd	1		
SUBS	SUBS #1/2/4, ERd	1		

	XOR.L #xx:32, ERd	3
	XOR.L ERs, ERd	2
XORC	XORC #xx:8, CCR	1

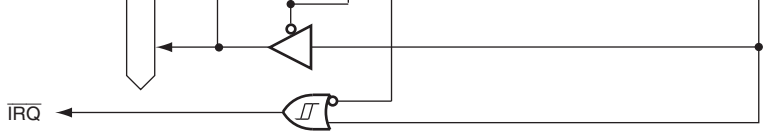
Notes: 1. n: Specified value in R4L and R4. The source and destination operands are a
n+1 times respectively.
2. Cannot be used in this LSI.

transfer instructions	POP, PUSH	—	—	—	—	—	—	—	—	—	—	—	—
	MOVFPE, MOVTPE	—	—	—	—	—	—	—	—	—	—	—	—
Arithmetic operations	ADD, CMP	BWL	BWL	—	—	—	—	—	—	—	—	—	—
	SUB	WL	BWL	—	—	—	—	—	—	—	—	—	—
	ADDX, SUBX	B	B	—	—	—	—	—	—	—	—	—	—
	ADDS, SUBS	—	L	—	—	—	—	—	—	—	—	—	—
	INC, DEC	—	BWL	—	—	—	—	—	—	—	—	—	—
	DAA, DAS	—	B	—	—	—	—	—	—	—	—	—	—
	MULXU, MULXS, DIVXU, DIVXS	—	BW	—	—	—	—	—	—	—	—	—	—
	NEG	—	BWL	—	—	—	—	—	—	—	—	—	—
	EXTU, EXTS	—	WL	—	—	—	—	—	—	—	—	—	—
Logical operations	AND, OR, XOR	—	BWL	—	—	—	—	—	—	—	—	—	—
	NOT	—	BWL	—	—	—	—	—	—	—	—	—	—
Shift operations		—	BWL	—	—	—	—	—	—	—	—	—	—
Bit manipulations		—	B	B	—	—	—	B	—	—	—	—	—
Branching instructions	BCC, BSR	—	—	—	—	—	—	—	—	—	—	—	—
	JMP, JSR	—	—	◯	—	—	—	—	—	—	◯	◯	—
	RTS	—	—	—	—	—	—	—	—	◯	—	—	◯
System control instructions	TRAPA	—	—	—	—	—	—	—	—	—	—	—	—
	RTE	—	—	—	—	—	—	—	—	—	—	—	—
	SLEEP	—	—	—	—	—	—	—	—	—	—	—	—
	LDC	B	B	W	W	W	W	—	W	W	—	—	—
	STC	—	B	W	W	W	W	—	W	W	—	—	—
	ANDC, ORC, XORC	B	—	—	—	—	—	—	—	—	—	—	—
	NOP	—	—	—	—	—	—	—	—	—	—	—	—
Block data transfer instructions		—	—	—	—	—	—	—	—	—	—	—	—



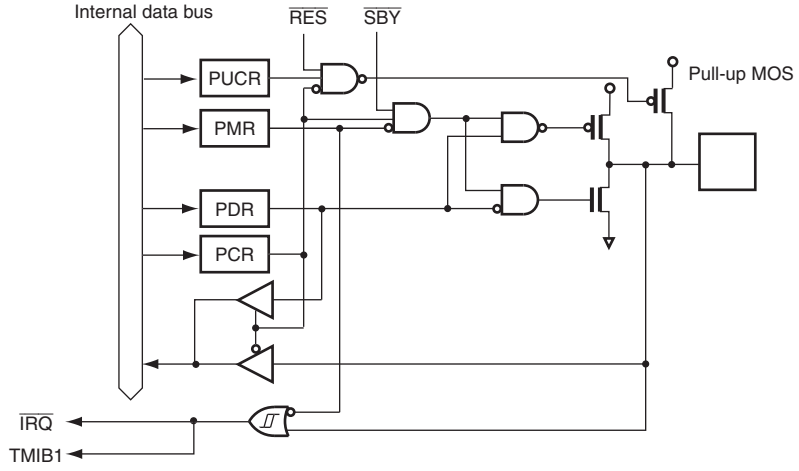
[Legend]
PUCR: Port pull-up control register
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.1 Port 1 Block Diagram (P17)



[Legend]
PUCR: Port pull-up control register
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.2 Port 1 Block Diagram (P16, P14)

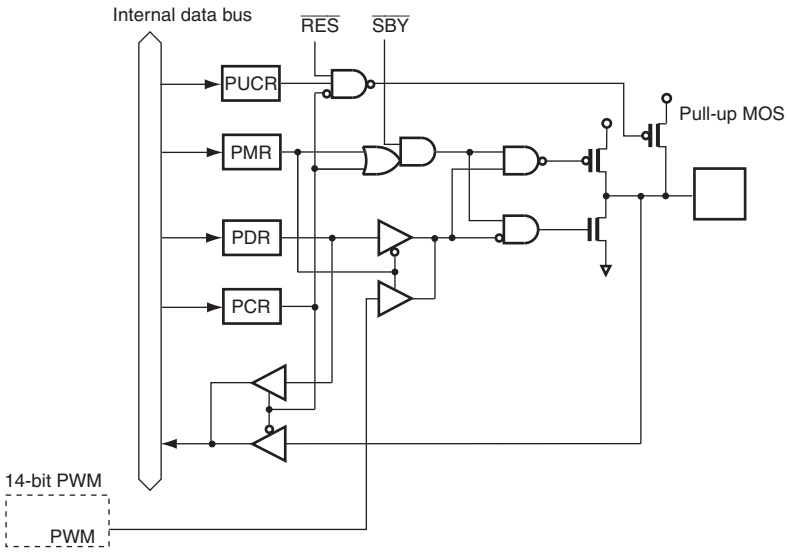


[Legend]
PUCR: Port pull-up control register
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.3 Port 1 Block Diagram (P15)

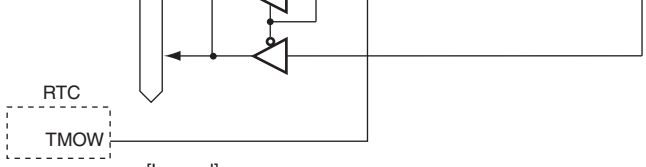
[Legend]
PUCR: Port pull-up control register
PDR: Port data register
PCR: Port control register

Figure B.4 Port 1 Block Diagram (P12)



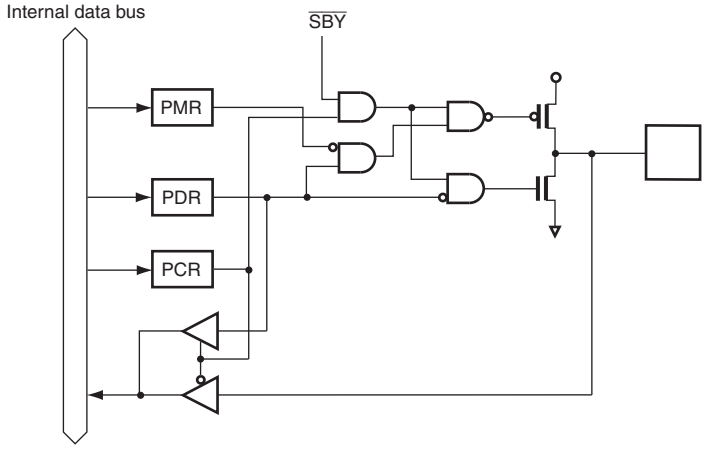
[Legend]
PUCR: Port pull-up control register
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.5 Port 1 Block Diagram (P11)



[Legend]
PUCR: Port pull-up control register
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.6 Port 1 Block Diagram (P10)



[Legend]
PUCR: Port pull-up control register
PDR: Port data register
PCR: Port control register

Figure B.7 Port 2 Block Diagram (P27, P26, P25, P24, P23)

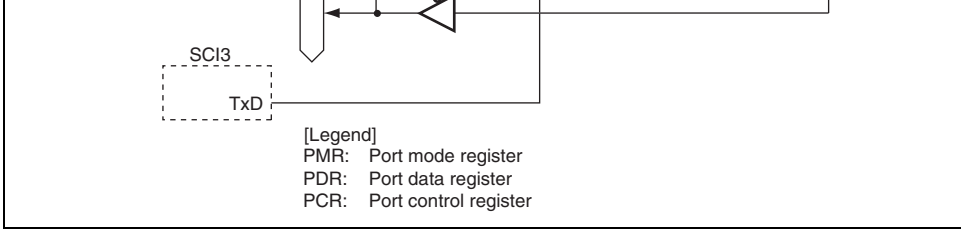


Figure B.8 Port 2 Block Diagram (P22)

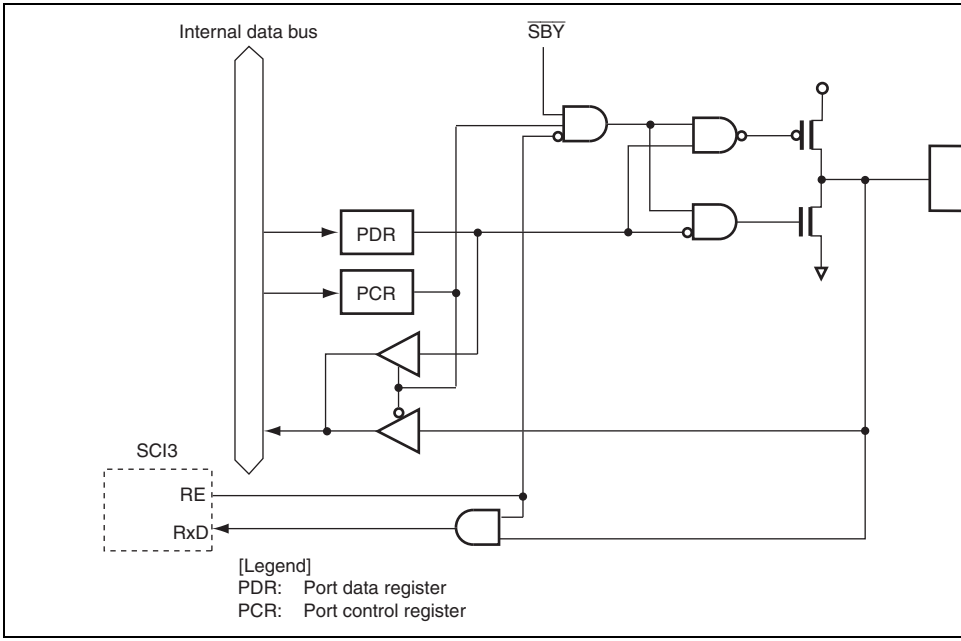


Figure B.9 Port 2 Block Diagram (P21)

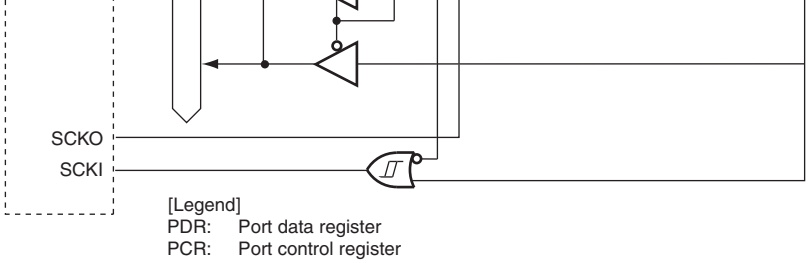


Figure B.10 Port 2 Block Diagram (P20)

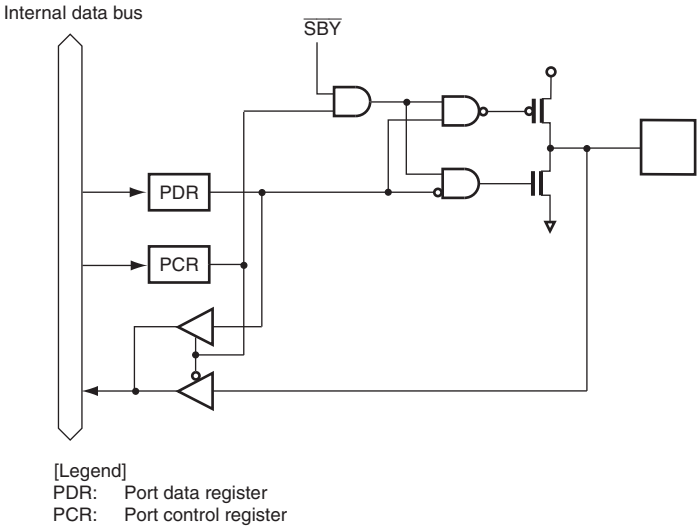
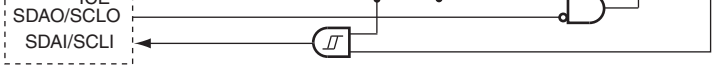
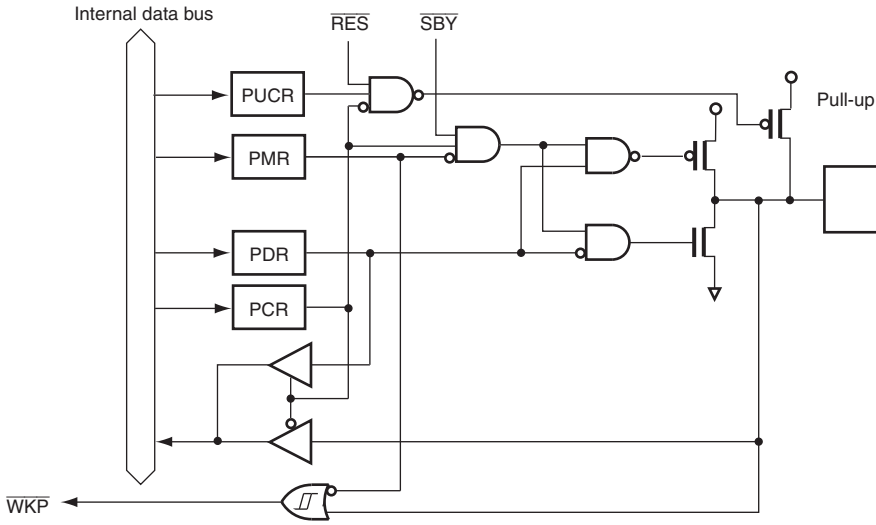


Figure B.11 Port 3 Block Diagram (P37, P36, P35, P34, P33, P32, P31, P30



[Legend]
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.12 Port5 Block Diagram (P57, P56)

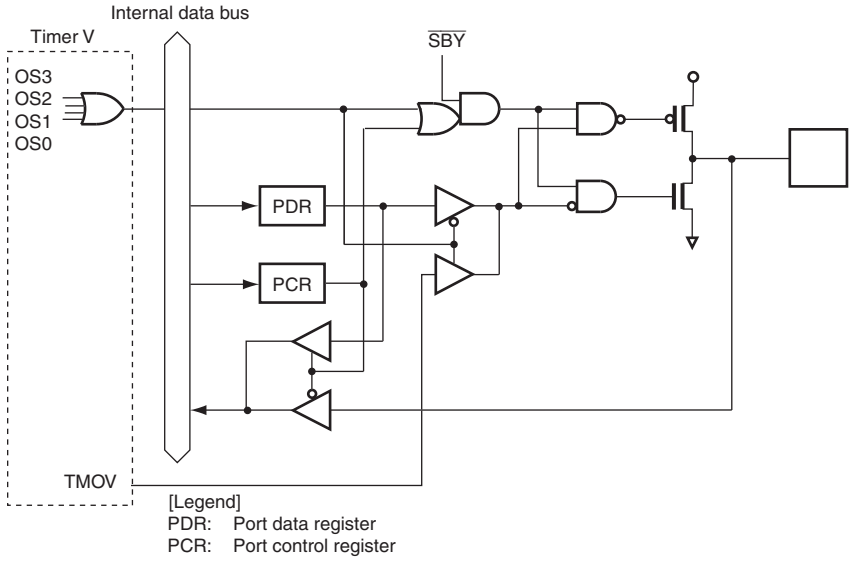


[Legend]
PUCR: Port pull-up control register
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.13 Port 5 Block Diagram (P55, P54, P53, P52, P51, P50)

[Legend]
PDR: Port data register
PCR: Port control register

Figure B.14 Port 7 Block Diagram (P77)



[Legend]
PDR: Port data register
PCR: Port control register

Figure B.15 Port 7 Block Diagram (P76)

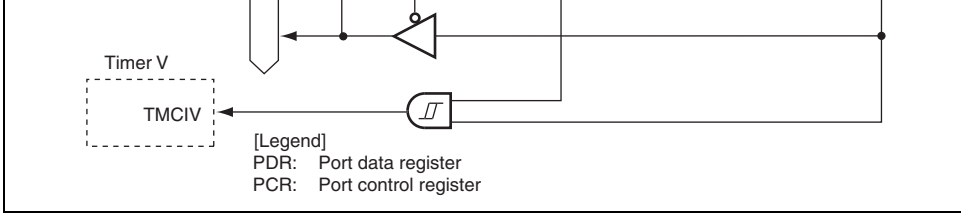


Figure B.16 Port 7 Block Diagram (P75)

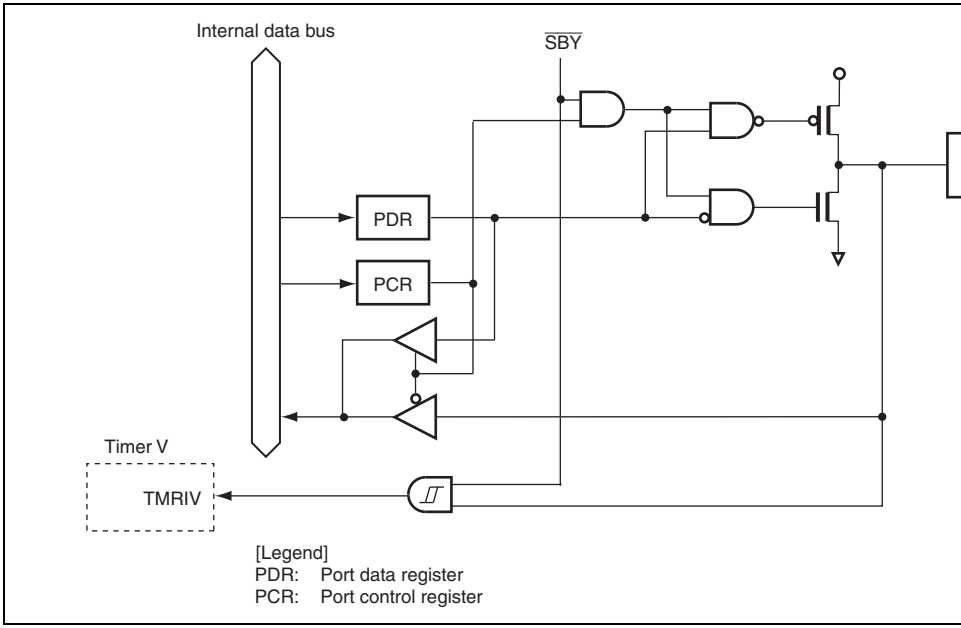
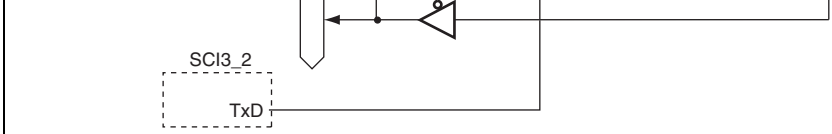
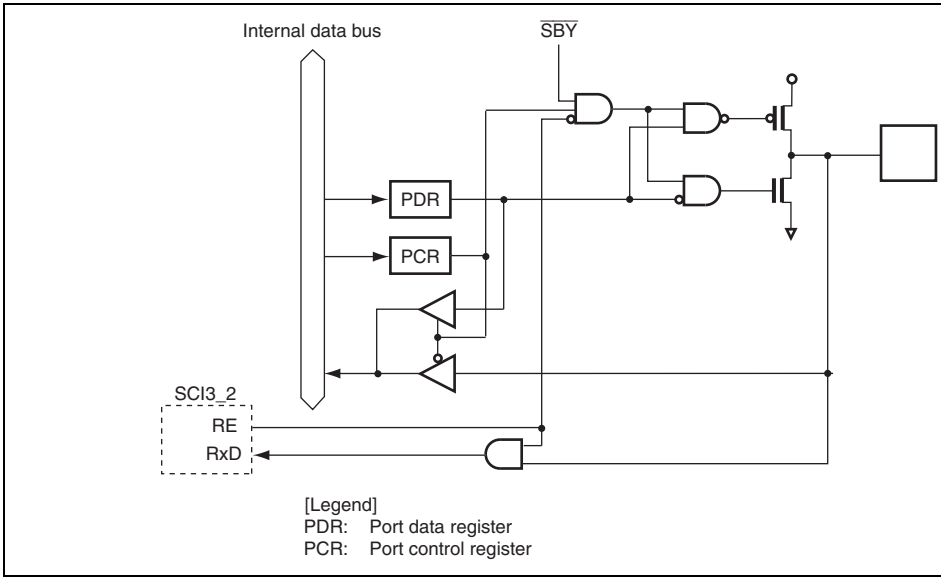


Figure B.17 Port 7 Block Diagram (P74)



[Legend]
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.18 Port 7 Block Diagram (P72)



[Legend]
PDR: Port data register
PCR: Port control register

Figure B.19 Port 7 Block Diagram (P71)

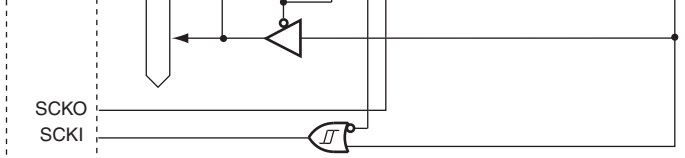


Figure B.20 Port 7 Block Diagram (P70)

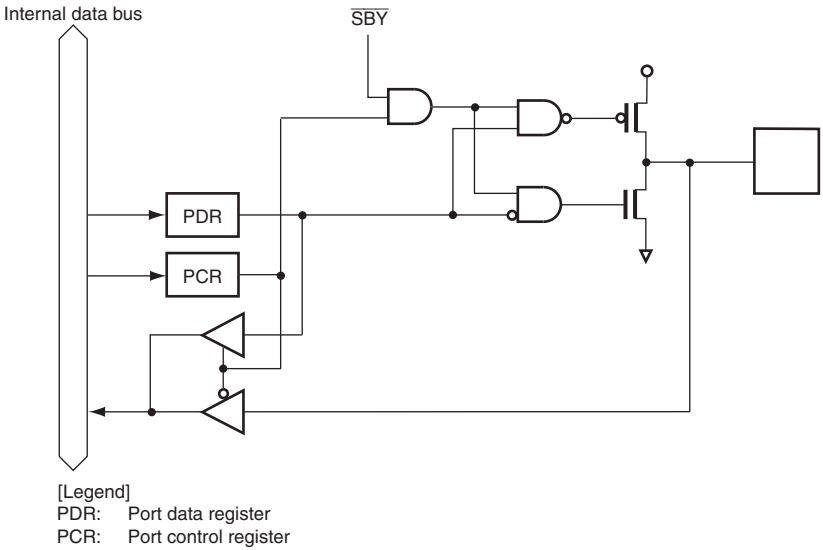
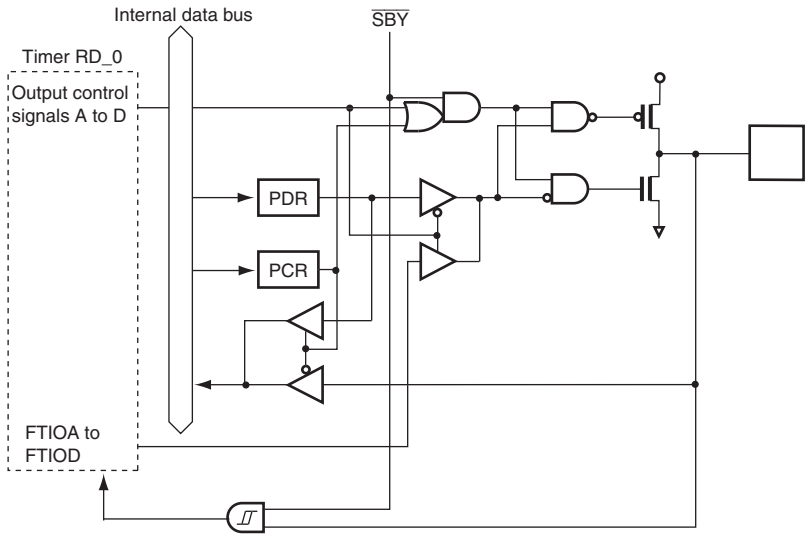


Figure B.21 Port 8 Block Diagram (P87, P86, P85)

[Legend]
PDR: Port data register
PCR: Port control register

Figure B.22 Port C Block Diagram (PC3, PC2, PC1, PC0)



[Legend]
PDR: Port data register
PCR: Port control register

Figure B.23 Port D Block Diagram (PD7, PD6, PD5, PD4, PD3, PD2, PD1, PI

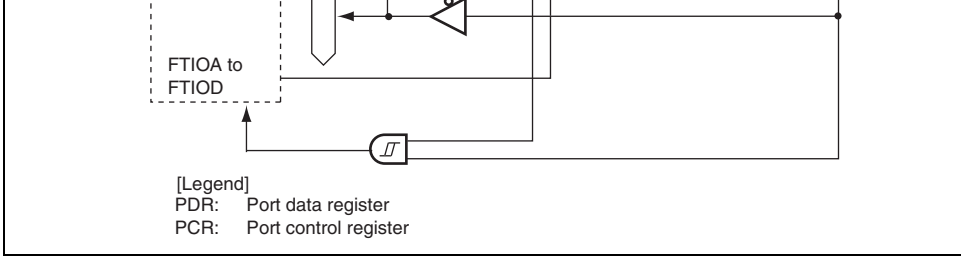


Figure B.24 Port E Block Diagram (PE7, PE6, PE5, PE4, PE3, PE2, PE1, P

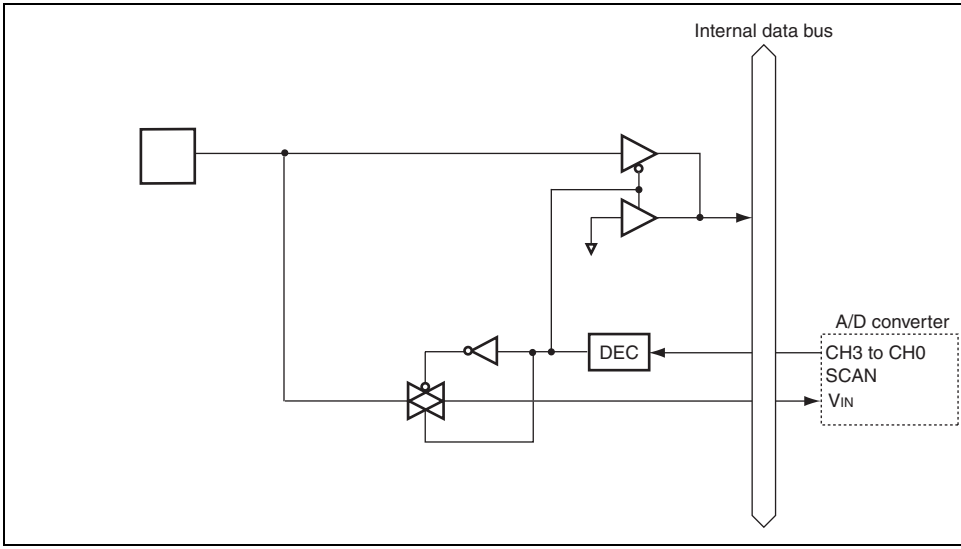
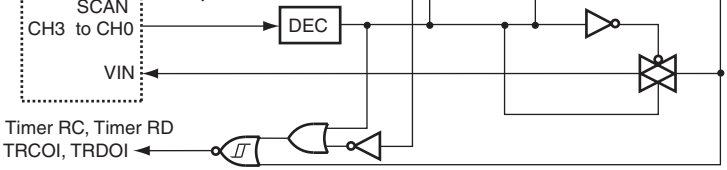
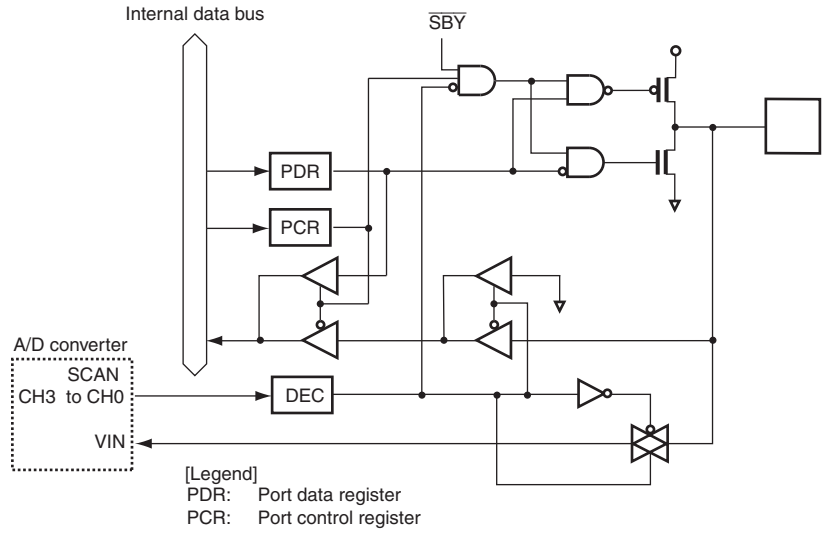


Figure B.25 Port F Block Diagram (PF7, PF6, PF5, PF4, PF3, PF2, PF1, P



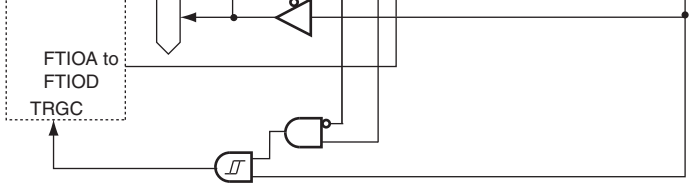
[Legend]
PDR: Port data register
PCR: Port control register
PMR: Port mode register

Figure B.26 Port G Block Diagram (PG7, PG6, PG5)



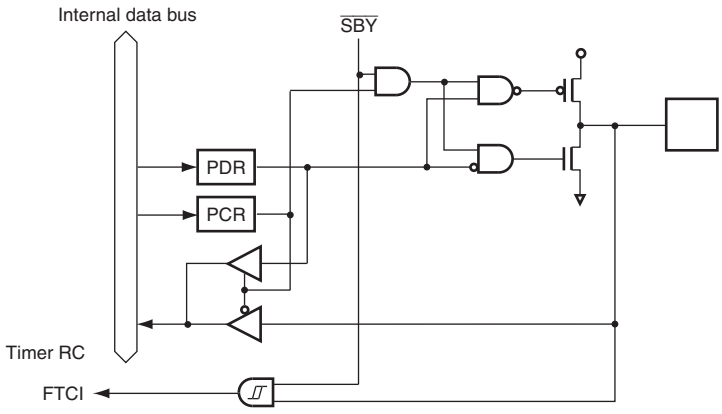
[Legend]
PDR: Port data register
PCR: Port control register

Figure B.27 Port G Block Diagram (PG4, PG3, PG2, PG1, PG0)



[Legend]
PDR: Port data register
PCR: Port control register

Figure B.28 Port H Block Diagram (PH7, PH6, PH5, PH4)

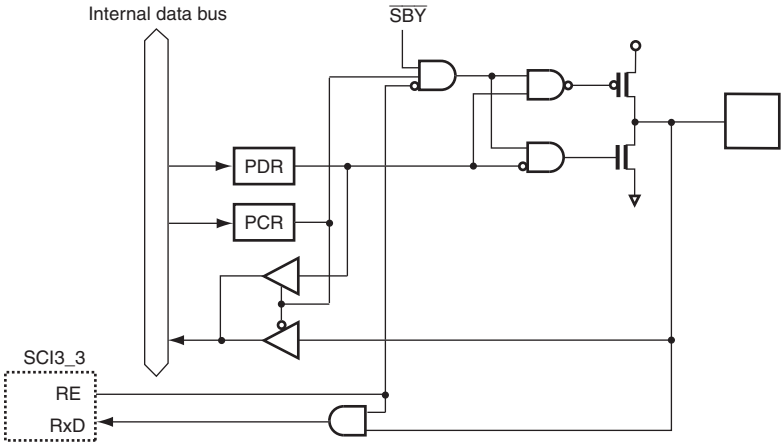


[Legend]
PDR: Port data register
PCR: Port control register

Figure B.29 Port H Block Diagram (PH3)

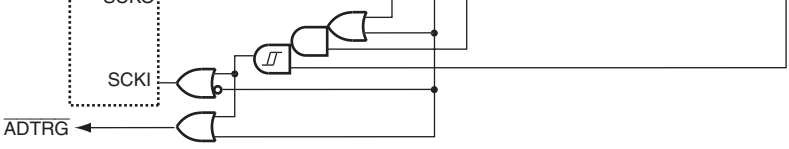
[Legend]
SMCR3: Serial module control register 3
PDR: Port data register
PCR: Port control register

Figure B.30 Port H Block Diagram (PH2)



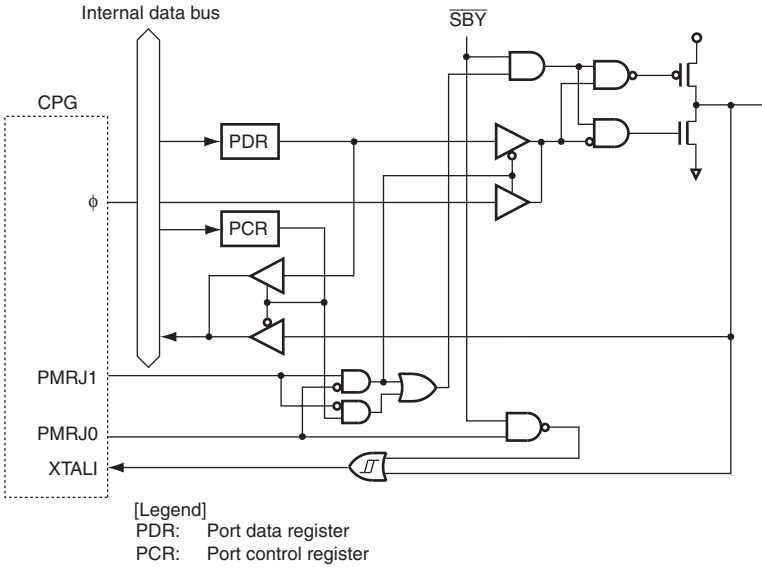
[Legend]
PDR: Port data register
PCR: Port control register

Figure B.31 Port H Block Diagram (PH1)



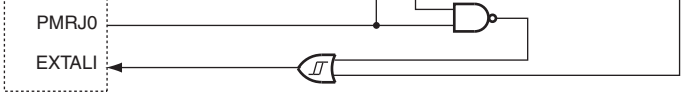
[Legend]
PMRG: Port mode register G
PDR: Port data register
PCR: Port control register

Figure B.32 Port H Block Diagram (PH0)



[Legend]
PDR: Port data register
PCR: Port control register

Figure B.33 Port J Block Diagram (PJ1)



[Legend]
PDR: Port data register
PCR: Port control register

Figure B.34 Port J Block Diagram (PJ0)

	impedance			impedance*		
P77 to P74, P72 to P70	High impedance	Retained	Retained	High impedance	Functioning	Fur
P87 to P85	High impedance	Retained	Retained	High impedance	Functioning	Fur
PC3 to PC0	High impedance	Retained	Retained	High impedance	Functioning	Fur
PD7 to PD0	High impedance	Retained	Retained	High impedance	Functioning	Fur
PE7 to PE0	High impedance	Retained	Retained	High impedance	Functioning	Fur
PF7 to PF0	High impedance	High impedance	High impedance	High impedance	High impedance	Hig imp
PG7 to PG0	High impedance	Retained	Retained	High impedance	Functioning	Fur
PH7 to PH0	High impedance	Retained	Retained	High impedance	Functioning	Fur

Note: * High level output when the pull-up MOS is in on state.

D. Package Dimensions

The package dimensions that are shown in the Renesas Semiconductor Packages Data Bo
priority.

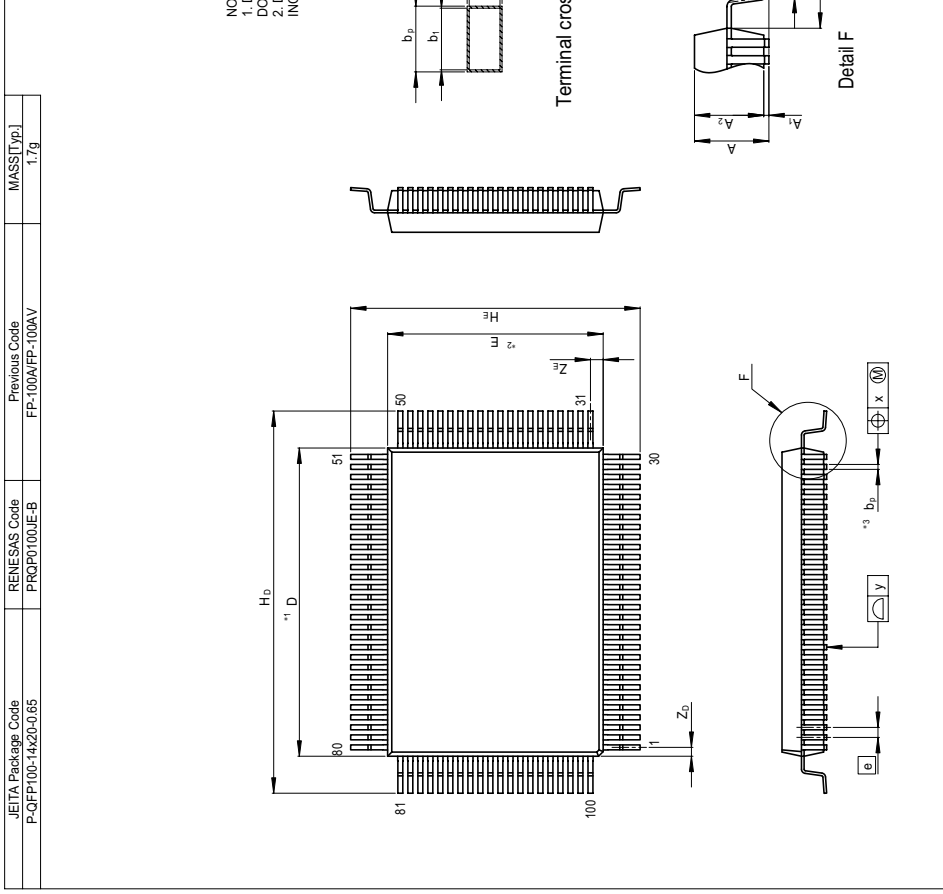


Figure D.1 FP-100A Package Dimensions

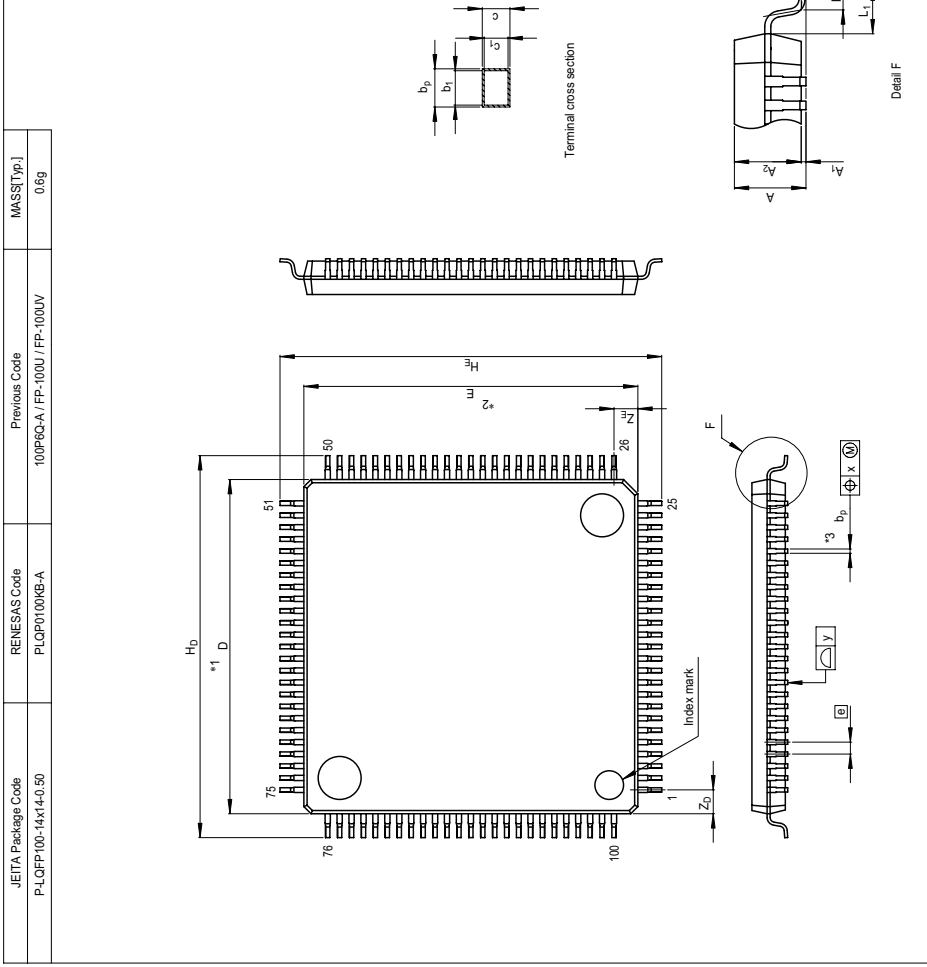
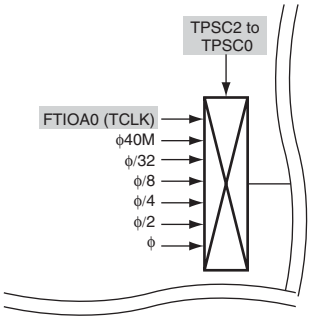


Figure D.2 FP-100U Package Dimensions

		0	1	Hi-Z	OSC1 (externa
		1	1	OSC2	OSC1

Section 14 Timer RD Figure 14.54 Block Diagram of Digital Filter	346	Amended 
Section 17 Serial Communication Interface 3 (SCI3) 17.8.2 Mark State and Break Sending	404	Amended When the TXD or TXD2 bit in PMR1 or the TX SMCR is 1, the TXD pin is used as an I/O por direction (input or output) and level are determ PCR and PDR. This can be used to set the TX mark state (high level) or send a break during data transmission. To maintain the communic at mark state until TE is set to 1, set both PCR to 1 and also set the TXD bit to 1. Then, the T becomes an I/O port, and 1 is output from the To send a break during serial transmission, fi PCR to 1 and clear PDR to 0, and then set th to 1. At this time, regardless of the current tra state, the TXD pin becomes an I/O port, and 0 from the TXD pin.

Section 23 Electrical Characteristics	497 to 520	Amended The wide temperature range of T_a = –40 to +85 added to the conditions.

	f_{osc} = 20 MHz				
	Active mode 2 V_{cc} = 3.0 V, f_{osc} = 10 MHz	—	4.5	—	
Sleep mode supply current	Sleep mode 1 V_{cc} = 5.0 V, f_{osc} = 20 MHz	—	22.0	30.0	mA
	Sleep mode 1 V_{cc} = 3.0 V, f_{osc} = 10 MHz	—	12.0	—	
	Sleep mode 2 V_{cc} = 5.0 V, f_{osc} = 20 MHz	—	5.0	6.5	mA
	Sleep mode 2 V_{cc} = 3.0 V, f_{osc} = 10 MHz	—	4.5	—	
Subactive mode supply current	V_{cc} = 3.0 V 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	130	150	µA
		—	50	70	
	V_{cc} = 3.0 V 32-kHz crystal resonator not used ($\phi_{SUB} = \phi_W/8$)	—	100	—	
		—	40	—	
Subsleep mode supply current	Subsleep mode 1 V_{cc} = 3.0 V 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	110	140	µA
		—	40	50	
	Subsleep mode 2 V_{cc} = 3.0 V 32-kHz crystal resonator not used	—	110	135	
		—	—	6.0	
Standby mode supply current	32-kHz crystal resonator not used	—	—	135	µA
		—	—	5.0	

Allowable output high current (total)	Ports 3, 5			mA

FSEL = 1 VCLSEL = 0			
V_{cc} = 4.0 to 5.5V Ta = -40°C to +85°C FSEL = 1 VCLSEL = 0	38.40	40.00	41
Ta = -20°C to +75°C FSEL = 1 VCLSEL = 0	38.40	40.00	41
Ta = -40°C to +85°C FSEL = 1 VCLSEL = 0	38.00	40.00	42
V_{cc} = 4.0 to 5.5V Ta = 25°C FSEL = 0 VCLSEL = 0	31.52	32.00	32
Ta = 25°C FSEL = 0 VCLSEL = 0	31.36	32.00	32
V_{cc} = 4.0 to 5.5V Ta = -20°C to +75°C FSEL = 0 VCLSEL = 0	31.04	32.00	32
V_{cc} = 4.0 to 5.5V Ta = -40°C to +85°C FSEL = 0 VCLSEL = 0	30.72	32.00	33
Ta = -20°C to +75°C FSEL = 0 VCLSEL = 0	30.72	32.00	33
Ta = -40°C to +85°C FSEL = 0 VCLSEL = 0	30.40	32.00	33

voltage 1*1					
Reset detection voltage 2*2	Vreset2	LVDSEL = 1	3.3	3.6	3.
Lower-limit voltage of LVDR operation	$V_{LVDRmin}$		1.0	—	—

Notes: 1. This voltage should be used when the falling and rising volta function is used.

2. Select the low-voltage reset 2 when only the low-voltage det is used.

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H8/36109 Group

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