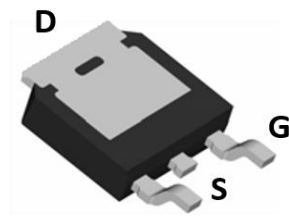
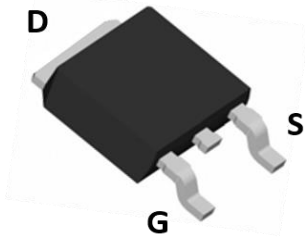
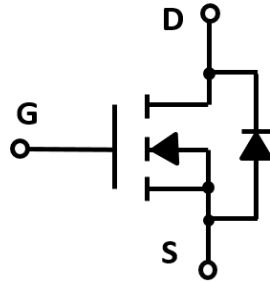


N-Channel Enhancement Mode Field Effect Transistor



TO-252



Product Summary

- V_{DS} 100V
- I_D 15A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <110 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <120 mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	100	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_C=25^\circ C$	15
		$T_C=100^\circ C$	10.5
Pulsed Drain Current ^A	I_{DM}	60	A
Single Pulse Avalanche Energy	E_{AS}	9	mJ
Total Power Dissipation	P_D	$T_C=25^\circ C$	45
		$T_C=100^\circ C$	22.5
Thermal Resistance Junction-to-Case ^B	$R_{\theta JC}$	3.3	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+175	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD15N10A	F1	YJD15N10A	2500	2500	25000	13" reel



YJD15N10A

■ Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	$T_J=25^\circ\text{C}$		1	μA
			$T_J=55^\circ\text{C}$		5	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.8	3.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$		95	110	m Ω
		$V_{GS}=4.5V, I_D=8A$		100	120	
Diode Forward Voltage	V_{SD}	$I_S=15A, V_{GS}=0V$		0.8	1.2	V
Maximum Body-Diode Continuous Current	I_S				15	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V, f=1\text{MHZ}$		785		μF
Output Capacitance	C_{oss}			38		
Reverse Transfer Capacitance	C_{rss}			30		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=50V, I_D=10A$		16		nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.6		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=50V, R_L=6.4\Omega$ $R_{GEN}=3\Omega$		5		ns
Turn-on Rise Time	t_r			40		
Turn-off Delay Time	$t_{D(off)}$			20		
Turn-off fall Time	t_f			7		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



YJD15N10A

■ Typical Performance Characteristics

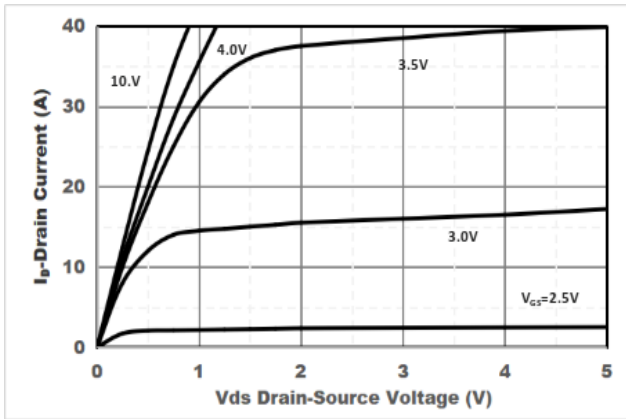


Figure1. Output Characteristics

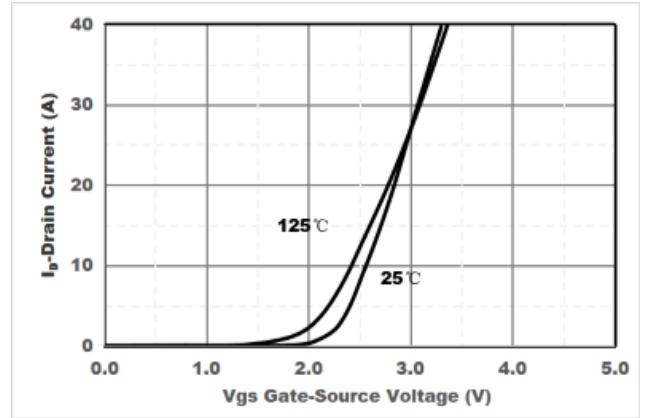


Figure2. Transfer Characteristics

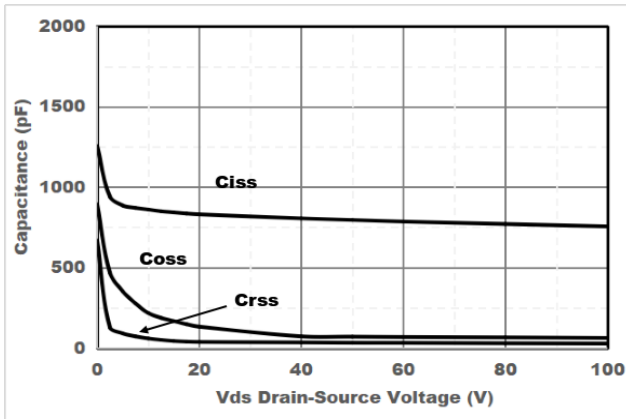


Figure3. Capacitance Characteristics

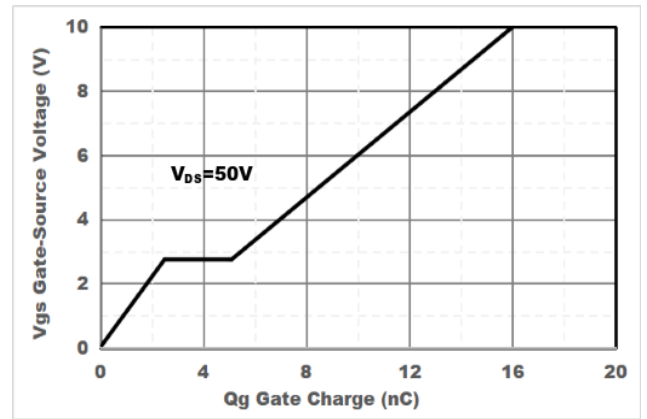


Figure4. Gate Charge

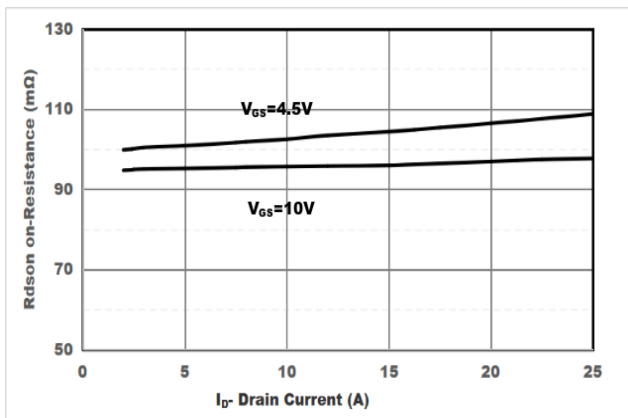


Figure5. Drain-Source on Resistance

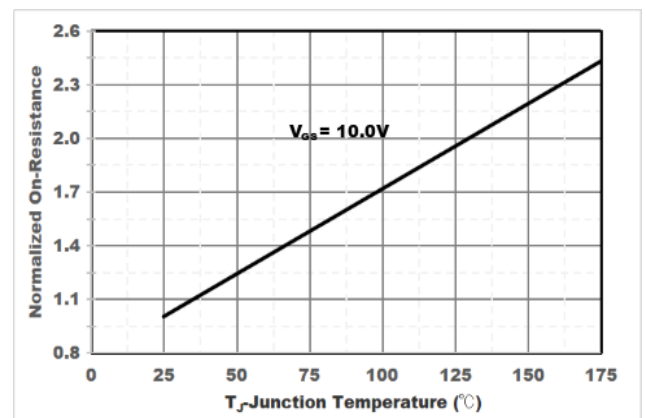


Figure6. Drain-Source on Resistance



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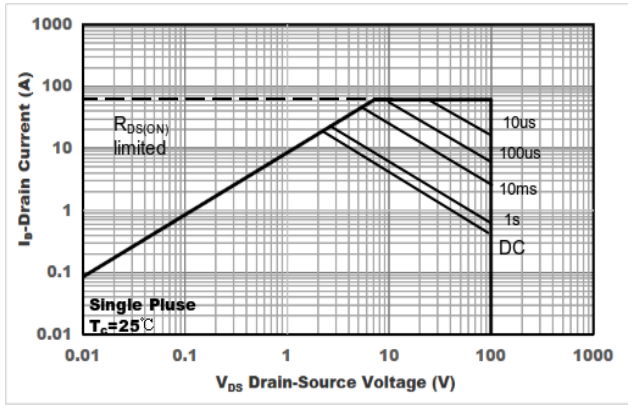


Figure7. Safe Operation Area

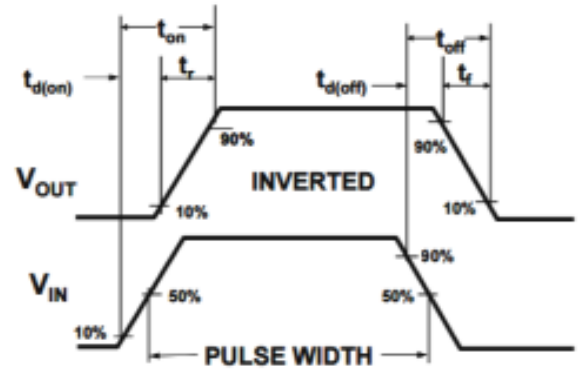
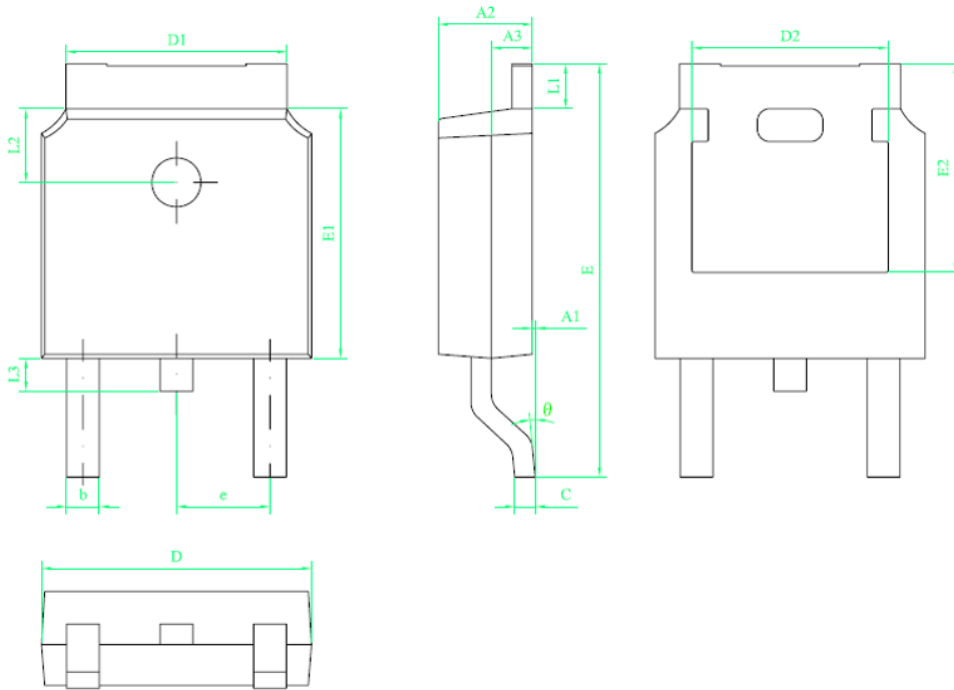


Figure8. Switching wave



YJD15N10A

■ TO-252 Package information



符号	尺寸		
	min	nom	max
A1	0	----	0.10
A2	2.20	2.30	2.40
A3	0.90	1.00	1.10
b	0.75	----	0.85
c	0.50	----	0.60
D	6.50	6.60	6.70
D1	5.30	5.40	5.50
D2	4.70	4.80	4.90
E	9.90	10.10	10.30
E1	6.00	6.10	6.20
E2	5.20	5.30	5.40
e	2.20	2.286	2.40
L1	0.90	----	1.25
L2	1.70	1.80	1.90
L3	0.60	0.80	1.00
θ	0°	----	8°

技术要求:

1. 树脂体不应有崩裂、缺损等缺陷;
2. 树脂上下部X、Y方向偏差不得超过0.20;
3. 胶体两端留废胶总和宽度不得超过0.50;
4. 所有单位为mm;



YJD15N10A

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