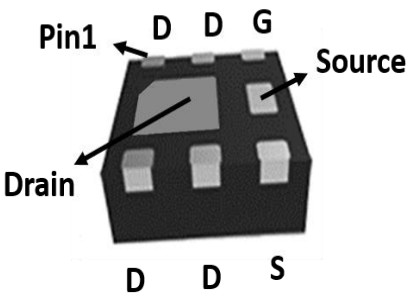
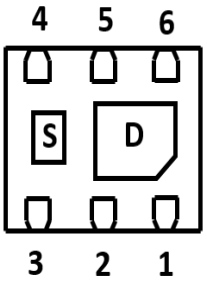
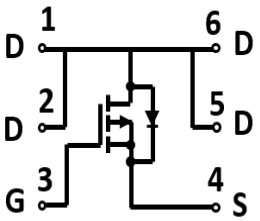
P-Channel Enhancement Mode Field Effect Transistor





DFN2020-6L



Product Summary

- V_{DS} -20V
- I_D -7A
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜26 mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜34 mohm
- $R_{DS(ON)}$(at V_{GS}=-1.8V) ＜55 mohm

General Description

- Trench Power LV MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge

Applications

- Battery charge
- Load switching in Cellular handset
- Ultraportable applications

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±10	V
Drain Current	T_A=25℃	I_D	-7	A
	T_A=70℃		-5.6	
Pulsed Drain Current [A]		I_{DM}	-28	A
Total Power Dissipation @ T_A=25℃		P_D	2.5	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	50	℃/ W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	15	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ4666A	F2	..G66A	3000	15000	60000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D=-7A		22	26	mΩ
		V_{GS}= -2.5V, I_D=-5.6A		28	34	
		V_{GS}= -1.8V, I_D=-2A		37	55	
Diode Forward Voltage	V_{SD}	I_S=-7A,V_{GS}=0V		-0.7	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-7	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHZ		990		pF
Output Capacitance	C_{oss}			168		
Reverse Transfer Capacitance	C_{rss}			107		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-7A		8.6		nC
Gate Source Charge	Q_{gs}			1.6		
Gate Drain Charge	Q_{gd}			2.2		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, I_D=-1A, R_{GEN}=2.5Ω		12		ns
Turn-on Rise Time	t_r			54		
Turn-off Delay Time	$t_{D(off)}$			15		
Turn-off Fall Time	t_f			9		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

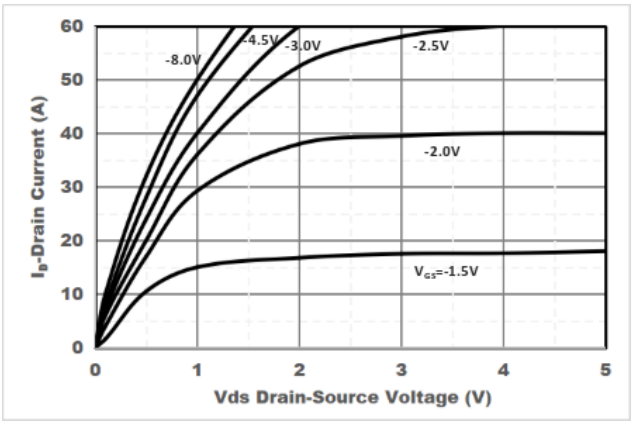


Figure1. Output Characteristics

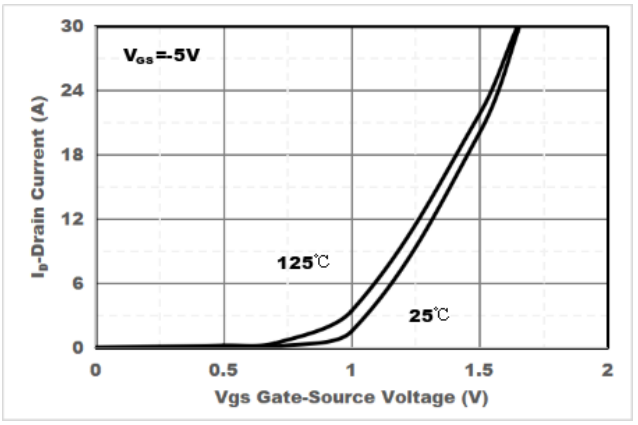


Figure2. Transfer Characteristics

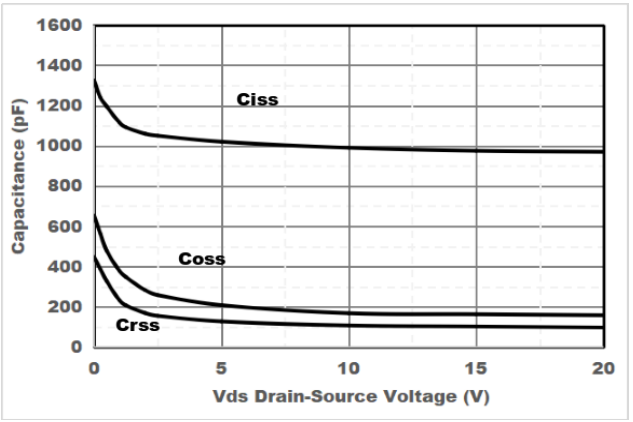


Figure3. Capacitance Characteristics

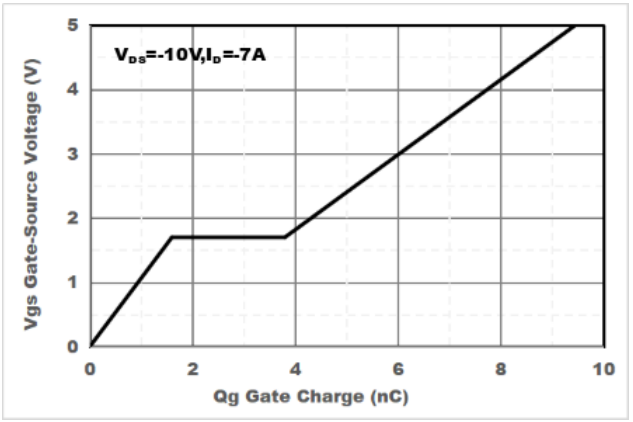


Figure4. Gate Charge

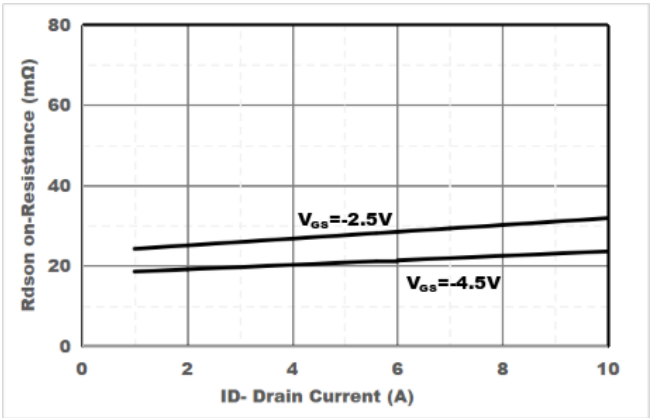


Figure5. Drain-Source on Resistance

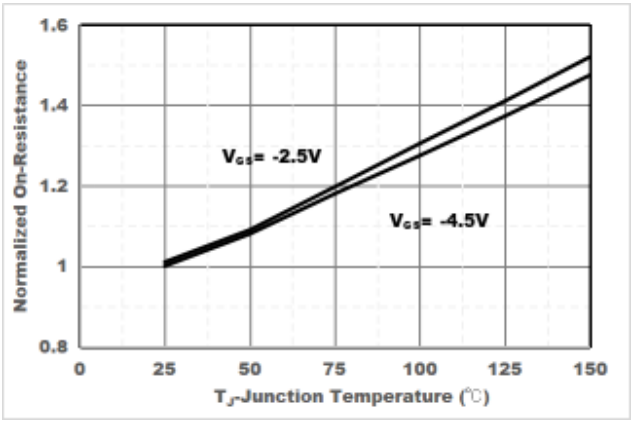


Figure6. Drain-Source on Resistance

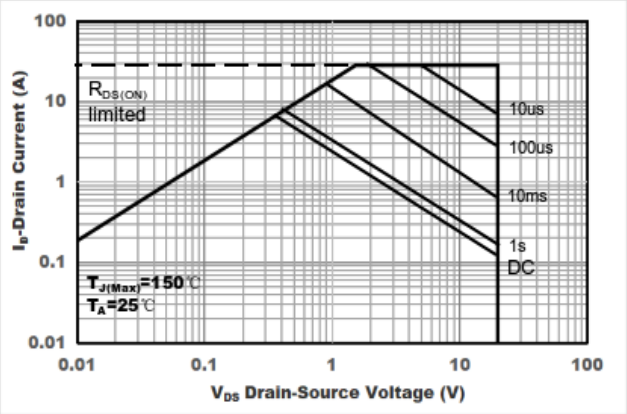


Figure7. Safe Operation Area

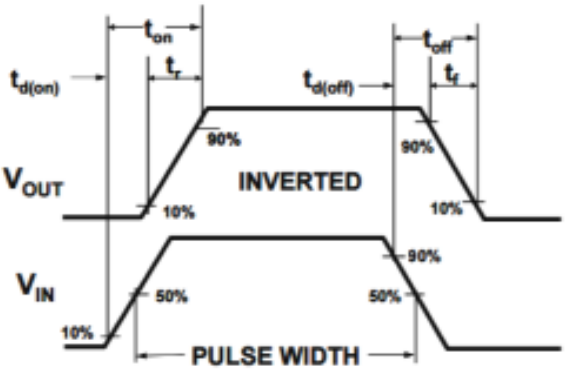
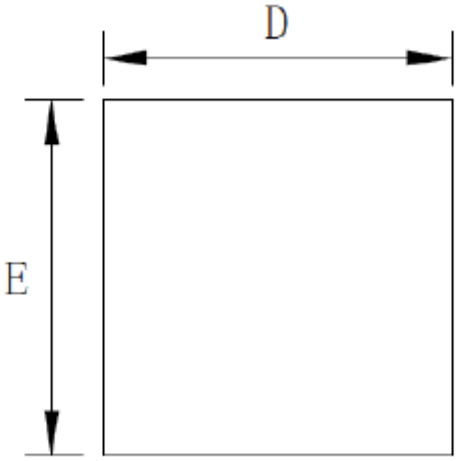
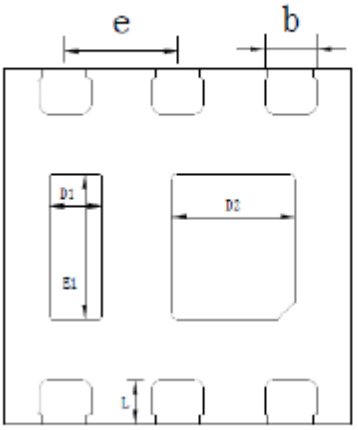


Figure8. Switching wave

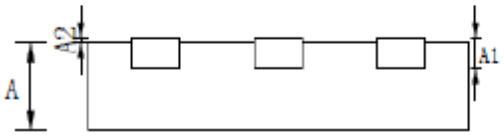
■ DFN2020-6L Package information



Top View
【顶视图】



Bottom View
【背视图】



Side View
【侧视图】

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.15REF	
A2	0.00	0.02	0.05
L	0.20	0.25	0.30
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e		0.65BSC	
D2	0.61	0.71	0.81
D1	0.20	0.30	0.40
E1	0.71	0.81	0.91

备注： A1/e 不监控

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