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User's Manual

32

SH7125 Group, SH7124 Group

Hardware Manual

Renesas 32-Bit RISC Microcomputer

SuperH™ RISC engine Family

SH7125	R5F7125
SH7124	R5F7124

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Rev.5.00 2009.03

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are in their open states, intermediate levels are induced by noise in the vicinity, a
through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied througho
chip and a low level is input on the reset pin. During the period where the states
undefined, the register settings and the output state of each pin are also undefine
your system so that it does not malfunction because of processing while it is in t
undefined state. For those products which have a reset function, reset the LSI im
after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test re
may have been be allocated to these addresses. Do not access these registers; the
operation is not guaranteed if they are accessed.

- CPU and System-Control Modules
- On-Chip Peripheral Modules

  The configuration of the functional description of each module differs according t module. However, the generic style includes the following items:

  i) Feature

  ii) Input/Output Pin

  iii) Register Description

  iv) Operation

  v) Usage Note

When designing an application system that includes this LSI, take notes into account. Eac includes notes in relation to the descriptions given, and usage notes are given, as required final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier vers This does not include all of the revised contents. For details, see the actual locations in th manual.

11. Index

Objective: This manual was written to explain the hardware functions and electrical characteristics of the SH7125 Group and SH7124 Group to the target user Refer to the SH-1/SH-2/SH-DSP Software Manual for a detailed descripti instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip

  Read the manual according to the contents. This manual can be roughly categorized on the CPU, system control functions, peripheral functions and electrical characteris

- In order to understand the details of the CPU's functions

  Read the SH-1/SH-2/SH-DSP Software Manual.

- In order to understand the details of a register when its name is known

  Read the index that is the final part of the manual to find the page number of the entr register. The addresses, bits, and initial values of the registers are summarized in sec List of Registers.

  Examples: Register name: The following notation is used for cases when th similar function, e.g. serial communication interf implemented on more than one channel: XXX_N (XXX is the register name and N is the number)

  Bit order: The MSB is on the left and the LSB is on the rig

  Number notation: Binary is B'xxxx, hexadecimal is H'xxxx, decima

  Signal notation: An overbar is added to a low-active signal: $\overline{\text{xxxx}}$

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SuperH$^{\text{TM}}$ RISC engine High-performance Embedded Workshop 3 User's Manual	REJ10B0025
SuperH RISC engine High-Performance Embedded Workshop 3 Tutorial	REJ10B0023

Application note:

Document Title	**Document N**
SuperH RISC engine C/C++ Compiler Package Application Note	REJ05B0463

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Section 8 Bus State Controller (BSC) ....

Section 9 Multi-Function Timer Pulse Unit 2 (MTU2)..............................

Section 15 Pin Function Controller (PFC)..

Section 16 I/O Ports..

the 32-bit internal-bus architecture enhances data processing power. With this CPU, it ha possible to assemble low-cost, high-performance, and high-functioning systems, even fo applications that were previously impossible with microcomputers, such as real-time co which demands high speeds.

In addition, this LSI includes on-chip peripheral functions necessary for system configu such as a ROM, a RAM, timers, a serial communication interface (SCI), an A/D convert interrupt controller (INTC), and I/O ports.

The version of the on-chip ROM is F-ZTAT™ (Flexible Zero Turn Around Time)* that flash memory. The flash memory can be programmed with a programmer that supports programming of this LSI, and can also be programmed and erased by software. This ena chip to be re-programmed at a user-site while mounted on a board.

The features of this LSI are listed in table 1.1.

Note: * F-ZTAT™ is a trademark of Renesas Technology Corp.

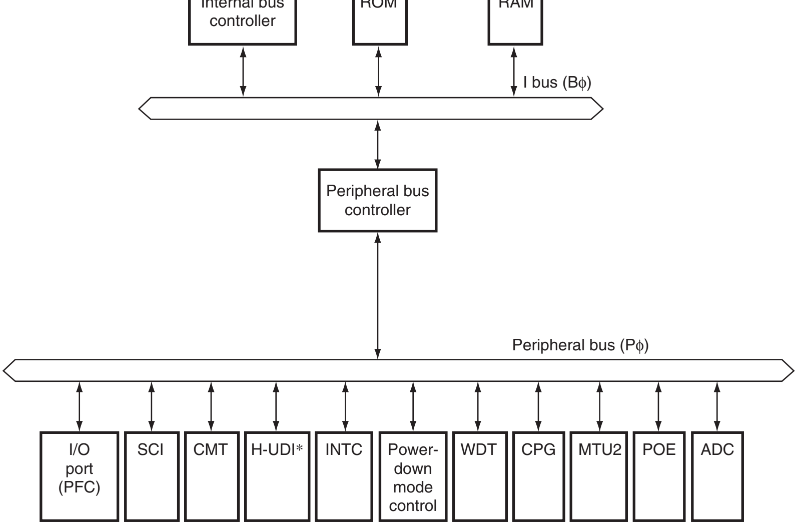
	- On-chip multiplier: Multiplication operations (32 bits × 32 bits → executed in two to five cycles - C language-oriented 62 basic instructions Note: Some specifications on slot illegal instruction exception ha this LSI differ from those of the conventional SH-2. For de section 5.8.4, Notes on Slot Illegal Instruction Exception H
Operating modes	- Operating modes — Single chip mode - Operating states — Program execution state — Exception handling state - Power-down modes — Sleep mode — Software standby mode — Module standby mode
User break controller (UBC)*	- Addresses, data values, type of access, and data size can all b break conditions - Supports a sequential break function - Two break channels
On-chip ROM	- 128 kbytes (SH71253, SH71243) - 64 kbytes (SH71252, SH71242) - 32 kbytes (SH71251A, SH71241A) - 16 kbytes (SH71250A, SH71240A)
On-chip RAM	- 8 kbytes (SH71253, SH71243, SH71252, SH71242, SH71251A SH71241A) - 4 kbytes (SH71250A, SH71240A)

generator (CPG)	resonator • Four types of clocks generated: — CPU clock: Maximum 50 MHz — Bus clock: Maximum 40 MHz — Peripheral clock: Maximum 40 MHz — MTU2 clock: Maximum 40 MHz
Watchdog timer (WDT)	• On-chip one-channel watchdog timer • Interrupt generation is supported.

	Toggle, PWM, complementary PWM, and reset-synchronized modes • Synchronization of multiple counters • Complementary PWM output mode — Non-overlapping waveforms output for 6-phase inverter co — Automatic dead time setting — 0% to 100% PWM duty cycle specifiable — Output suppression — A/D conversion delaying function — Dead time compensation — Interrupt skipping at crest or trough • Reset-synchronized PWM mode Three-phase PWM waveforms in positive and negative phase output with a required duty cycle • Phase counting mode Two-phase encoder pulse counting available
Port output enable (POE)	• High-impedance control of waveform output pins and channel MTU2
Compare match timer (CMT)	• 16-bit counters • Compare match interrupts can be generated • Two channels
Serial communication interface (SCI)	• Clock synchronous or asynchronous mode • Three channels

	• LQFP-64 (0.5 pitch) (SH7125) • LQFP-48 (0.65 pitch) (SH7124) • VQFN-64 (0.4 pitch) (SH7125) • VQFN-52 (0.4 pitch) (SH7124)
Power supply voltage	• Vcc: 4.0 to 5.5 V • AVcc: 4.0 to 5.5 V

Note: * The 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH versions are not supported.

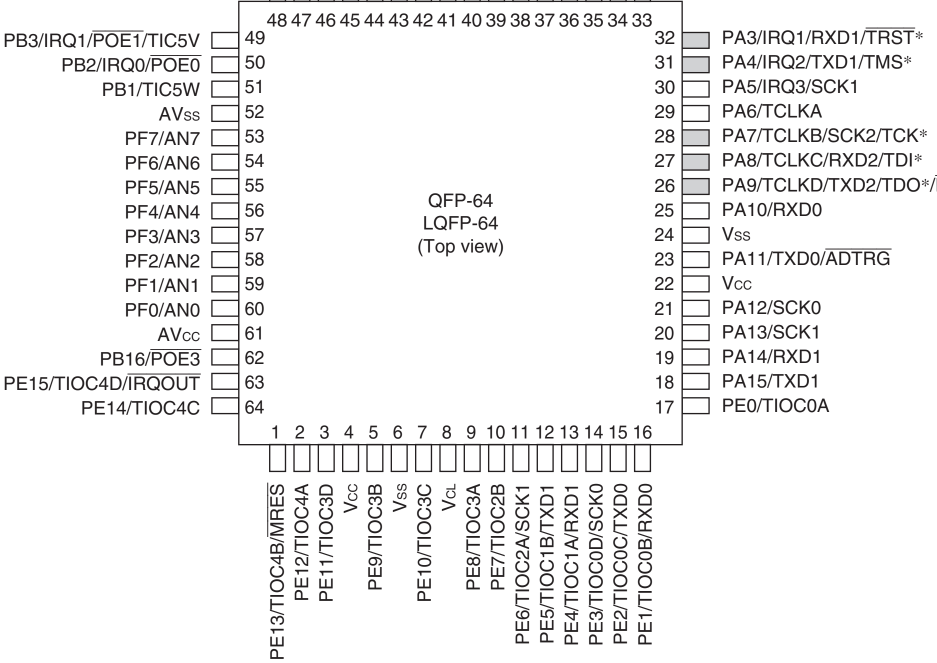


[Legend]

ROM:	On-chip ROM	PFC:	Pin function controller
RAM:	On-chip RAM	MTU2:	Multi-function timer pulse unit 2
UBC*:	User break controller	POE:	Port output enable
H-UDI*:	User debugging interface	SCI:	Serial communication interface
INTC:	Interrupt controller	CMT:	Compare match timer
CPG:	Clock pulse generator	ADC:	A/D converter
WDT:	Watchdog timer		
CPU:	Central processing unit		

Note: * The 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions are not supporte

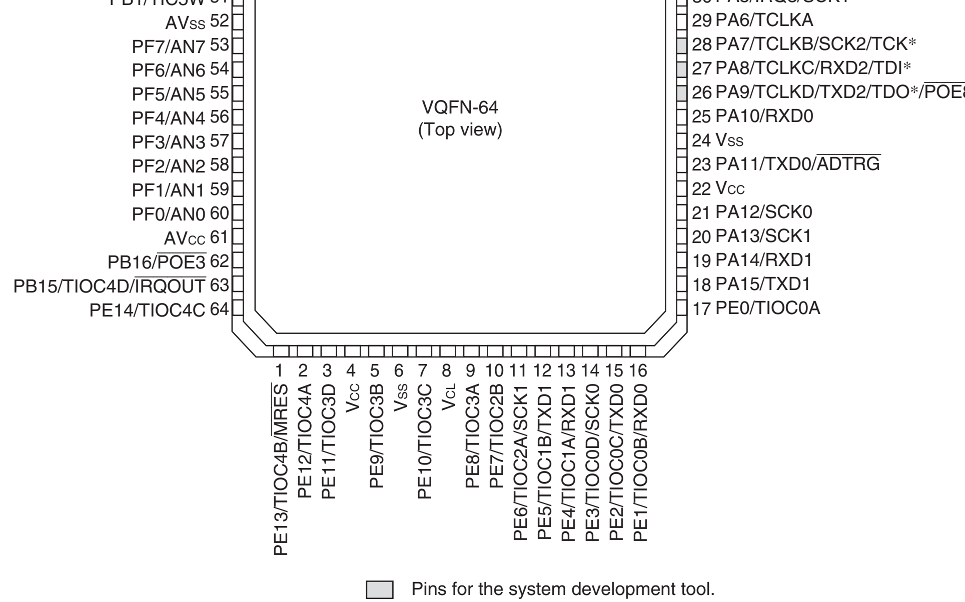
Figure 1.1 Block Diagram



▨ Pins for the system development tool.
When these pins are used for an on-chip debugger, they are not available.

Note: * Pins $\overline{\text{ASEBRK}}$, $\overline{\text{ASEBRKAK}}$, $\overline{\text{TRST}}$, TMS, TCK, TDI, and IDO are n
on the 32 Kbyte version (SH71251A) and 16 Kbyte version (SH712

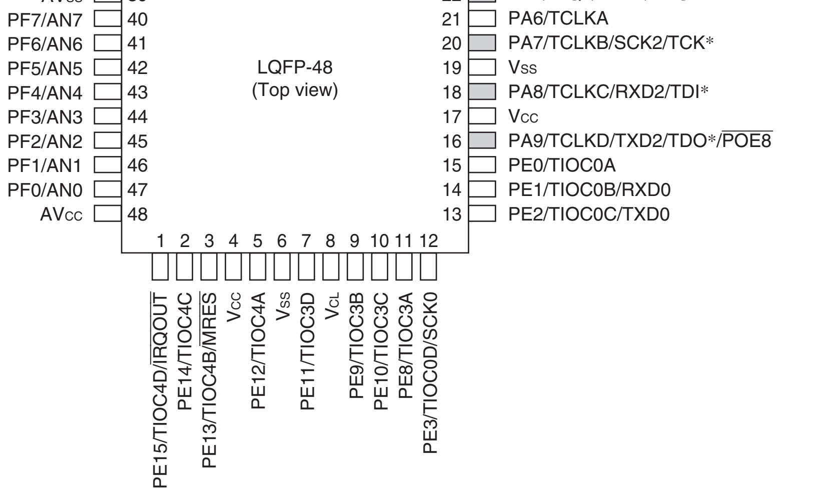
Figure 1.2 (1) Pin Assignments of SH7125



▨ Pins for the system development tool. When these pins are used for an on-chip debugger, they are not available.

Note: * Pins $\overline{\text{ASEBRK}}$, $\overline{\text{ASEBRKAK}}$, $\overline{\text{TRST}}$, TMS, TCK, TDI, and IDO are no on the 32 Kbyte version (SH71251A) and 16 Kbyte version (SH7125

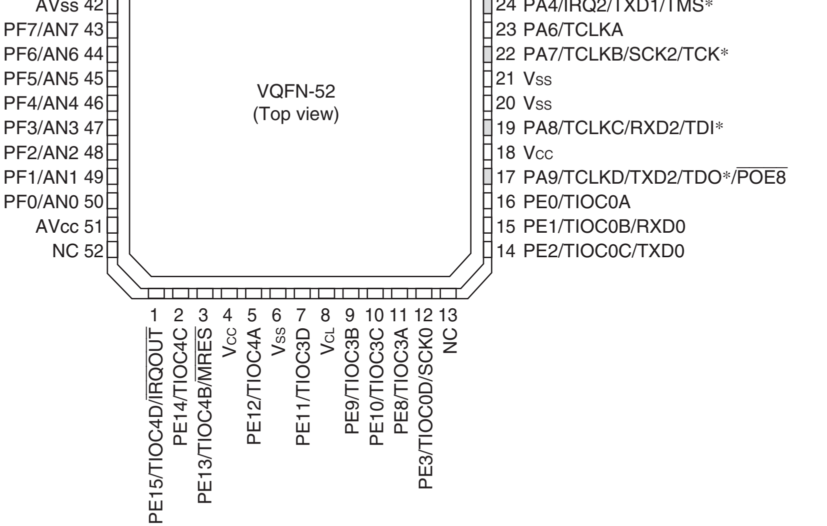
Figure 1.2 (2) Pin Assignments of SH7125



▨ Pins for the system development tool.
When these pins are used for an on-chip
debugger, they are not available.

Note: * Pins ASEBRK, ASEBRKAK, TRST, TMS, TCK, TDI, and IDO are n
on the 32 Kbyte version (SH71241A) and 16 Kbyte version (SH712

Figure 1.3 (1) Pin Assignments of SH7124



▨ Pins for the system development tool. When these pins are used for an on-chip debugger, they are not available.

Note: * Pins $\overline{\text{ASEBRK}}$, $\overline{\text{ASEBRKAK}}$, $\overline{\text{TRST}}$, TMS, TCK, TDI, and IDO are not on the 32 Kbyte version (SH71241A) and 16 Kbyte version (SH7124

Figure 1.3 (2) Pin Assignments of SH7124

	Vss	I	Ground	Ground pin Connect all Vss pins to the power supply (0V). There v operation if any pins are op
	VCL	O	Power supply for internal power-down	External capacitance pins power-down power supply Connect these pins to Vss to 0.47 μF capacitor (place the pins).
Clock	PLLVss	I	PLL ground	Ground pin for the on-chip oscillator
	EXTAL	I	External clock	Connected to a crystal reso An external clock signal ma input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal reso
Operating mode control	MD1	I	Mode set	Sets the operating mode. D change values on this pin d operation.
	FWE	I	Flash memory write enable	Pin for flash memory Flash memory can be prot against programming or er through this pin.

			interrupt	Fix to high or low level whe use.
	IRQ3 to IRQ0 (SH7125) IRQ3 to IRQ1 (SH7124)	I	Interrupt requests 3 to 0	Maskable interrupt request Selectable as level input or input. The rising edge, fallin and both edges are selecta edges.
	$\overline{\text{IRQOUT}}$	O	Interrupt request output	Shows that an interrupt cau occurred. The interrupt cau recognized even in the bus state.
Multi function timer-pulse unit 2 (MTU2)	TCLKA, TCLKB, TCLKC, TCLKD	I	MTU2 timer clock input	External clock input pins fo
	TIOC0A, TIOC0B, TIOC0C, TIOC0D	I/O	MTU2 input capture/output compare (channel 0)	The TGRA_0 to TGRD_0 in capture input/output compa output/PWM output pins
	TIOC1A, TIOC1B (only in SH7125)	I/O	MTU2 input capture/output compare (channel 1)	The TGRA_1 to TGRB_1 in capture input/output compa output/PWM output pins
	TIOC2A, TIOC2B (only in SH7125)	I/O	MTU2 input capture/output compare (channel 2)	The TGRA_2 to TGRB_2 in capture input/output compa output/PWM output pins

	TIOC3W		(channel 3)	
Port output enable (POE)	$\overline{\text{POE8}}$, $\overline{\text{POE3}}$, $\overline{\text{POE1}}$, $\overline{\text{POE0}}$ (SH7125) $\overline{\text{POE8}}$, $\overline{\text{POE1}}$, $\overline{\text{POE0}}$ (SH7124)	I	Port output enable	Request signal input to pla waveform output pins and pins of MTU2 in high impe state. In the SH7125, while $\overline{\text{POE}}$ is selected in the PFC, the pulled up inside this LSI if are input to them.
Serial communication interface (SCI)	TXD2 to TXD0	O	Transmit data	Transmit data output pins
	RXD2 to RXD0	I	Receive data	Receive data input pins
	SCK2 to SCK0 (SH7125) SCK2, SCK0 (SH7124)	I/O	Serial clock	Clock input/output pins
A/D converter (ADC)	AN7 to AN0	I	Analog input pins	Analog input pins
	$\overline{\text{ADTRG}}$ (only in SH7125)	I	A/D conversion trigger input	External trigger input pin fo A/D conversion
	AVcc	I	Analog power supply	Power supply pin for the A converter Connect all AVcc pins to th power supply (Vcc) when t converter is not used.

	(SH7124)			
	PB16, PB5, PB3 to PB1 (SH7125)	I/O	General port	5-bit input/output port pins
	PB5, PB3, PB1 (SH7124)			3-bit input/output port pins
	PE15 to PE0 (SH7125)	I/O	General port	16-bit input/output port pins
	PE15 to PE8, PE3 to PE0 (SH7124)			12-bit input/output port pins
	PF7 to PF0	I	General port	8-bit input port pins
User debugging interface (H-UDI)*[1]	TCK	I	Test clock	Test-clock input pin
	TMS	I	Test mode select	Inputs the test-mode select
	TDI	I	Test data input	Serial input pin for instructio data
	TDO	O	Test data output	Serial output pin for instruct data
	$\overline{\text{TRST}}$	I	Test reset	Initialization-signal input pin

			If only normal mode will be up the pin by connecting a
$\overline{\text{ASEBRK}}$[*2]	I	Break request	E10A emulator break input
$\overline{\text{ASEBRKAK}}$[*2]	O	Break mode acknowledge	Indicates that the E10A em entered its break mode.

[Legend]: The $\overline{\text{WDTOVF}}$ pin should not be pulled down. When absolutely necessary, pu through a resistor of 1 MΩ or larger.

Notes: *1 This pin function is not supported on the 32 Kbyte (SH71251A and SH71241 Kbyte (SH71250A and SH71240A) versions.

*2 On 32 Kbyte versions (SH71251A, SH71241A) and 16 Kbyte versions (SH71 SH71240A), connect $\overline{\text{ASEMD0}}$ to V_{cc} via a resistor and fix it high. Note that th versions do not support $\overline{\text{ASEBRK}}$ and $\overline{\text{ASEBRKAK}}$.

Post-increment register indirect (@Rn+)

Pre-decrement register indirect (@-Rn)

Register indirect with displacement (@disp:4, Rn)

Index register indirect (@R0, Rn)

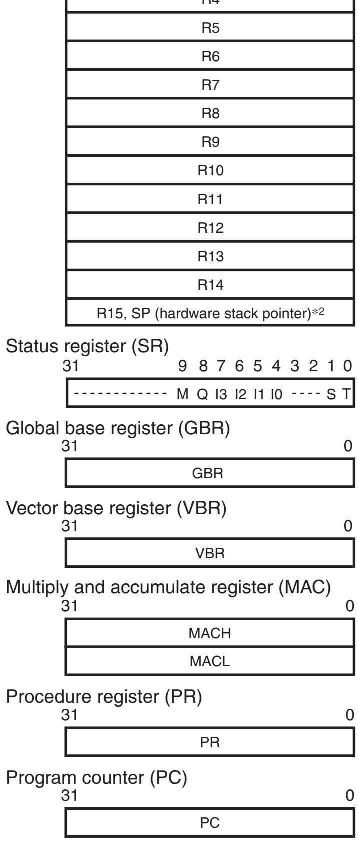
GBR indirect with displacement (@disp:8, GBR)

Index GBR indirect (@R0, GBR)

PC relative with displacement (@disp:8, PC)

PC relative (disp:8/disp:12/Rn)

Immediate (#imm:8)


R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15, SP (hardware stack pointer)*2
Status register (SR)
31 9 8 7 6 5 4 3 2 1 0
- - - - - - - - - - - - M Q I3 I2 I1 I0 - - - - S T
Global base register (GBR)
31 0
GBR
Vector base register (VBR)
31 0
VBR
Multiply and accumulate register (MAC)
31 0
MACH
MACL
Procedure register (PR)
31 0
PR
Program counter (PC)
31 0
PC

Notes: 1. R0 can be used as an index register in index register indirect or index GBR indirect addressing mode. For some instructions, only R0 is used as the source or destination register.
2. R15 is used as a hardware stack pointer during exception handling.

Figure 2.1 CPU Internal Register Configuration

There are three 32-bit control registers, designated status register (SR), global base regis (GBR), and vector base register (VBR). SR indicates a processing state. GBR is used as address in GBR indirect addressing mode for data transfer of on-chip peripheral module VBR is used as a base address of the exception handling (including interrupts) vector ta

- Status register (SR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	M	Q	I[3:0]				-	-
Initial value:	0	0	0	0	0	0	-	-	1	1	1	1	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit name	Default	Read/ Write	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.
9	M	Undefined	R/W	Used by the DIV0U, DIV0S, and DIV1 instru
8	Q	Undefined	R/W	Used by the DIV0U, DIV0S, and DIV1 instru
7 to 4	I[3:0]	1111	R/W	Interrupt Mask
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.

- Global-base register (GBR)

  This register indicates a base address in GBR indirect addressing mode. The GBR ind addressing mode is used for data transfer of the on-chip peripheral module registers ar operations.

- Vector-base register (VBR)

  This register indicates the base address of the exception handling vector table.

The PC indicates the point which is four bytes (two instructions) after the current ex instruction.

2.2.4 Initial Values of Registers

Table 2.1 lists the initial values of registers after a reset.

Table 2.1 Initial Values of Registers

Type of register	Register	Default
General register	R0 to R14	Undefined
	R15 (SP)	SP value set in the exception handling vect
Control register	SR	I3 to I0: 1111 (H'F) Reserved bits: 0 Other bits: Undefined
	GBR	Undefined
	VBR	H'00000000
System register	MACH, MACL, PR	Undefined
	PC	PC value set in the exception handling vect

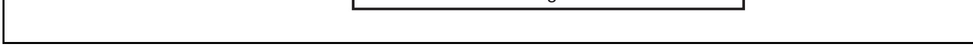


Figure 2.2 Register Data Format

2.3.2 Memory Data Formats

Memory data formats are classified into bytes, words, and longwords. Byte data can be ac from any address. Locate, however, word data at an address 2n, longword data at 4n. Oth an address error will occur if an attempt is made to access word data starting from an add than 2n or longword data starting from an address other than 4n. In such cases, the data ac cannot be guaranteed. The hardware stack area, pointed by the hardware stack pointer (SI uses only longword data starting from address 4n because this area holds the program cou status register.

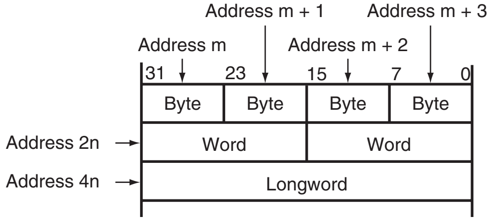


Figure 2.3 Memory Data Format

relative addressing mode with displacement.

2.4 Features of Instructions

2.4.1 RISC Type

The instructions are RISC-type instructions with the following features:

Fixed 16-Bit Length: All instructions have a fixed length of 16 bits. This improves prog efficiency.

One Instruction per Cycle: Since pipelining is used, basic instructions can be executed cycle.

Data Size: The basic data size for operations is longword. Byte, word, or longword can selected as the memory access size. Byte or word data in memory is sign-extended to lo and then calculated. Immediate data is sign-extended to longword for arithmetic operati zero-extended to longword size for logical operations.

Table 2.2 Word Data Sign Extension

CPU in this LSI		Description	Example of Other C
MOV.W	@(disp,PC),R1	Sign-extended to 32 bits, R1 becomes H'00001234, and is then operated on by the ADD instruction.	ADD.W #H'1234,R0
ADD	R1,R0		
	....		
.DATA.W	H'1234		

Note: * Immediate data is accessed by @(disp,PC).

CPU in this LSI		Description	Example of Oth	
BRA	TRGET	ADD is executed before branch to TRGET.	ADD.W	R1,R0
ADD	R1,R0		BRA	TRGE

Multiply/Multiply-and-Accumulate Operations: A 16 × 16 → 32 multiply operation is executed in one to two cycles, and a 16 × 16 + 64 → 64 multiply-and-accumulate operati to three cycles. A 32 × 32 → 64 multiply operation and a 32 × 32 + 64 → 64 multiply-an accumulate operation are each executed in two to four cycles.

T Bit: The result of a comparison is indicated by the T bit in SR, and a conditional branc performed according to whether the result is True or False. Processing speed has been im by keeping the number of instructions that modify the T bit to a minimum.

Table 2.4 T Bit

CPU in this LSI		Description	Example of Oth	
CMP/GE	R1,R0	When R0 ≥ R1, the T bit is set.	CMP.W	R1,R0
BT	TRGET0	When R0 ≥ R1, a branch is made to TRGET0.	BGE	TRGET
BF	TRGET1	When R0 < R1, a branch is made to TRGET1.	BLT	TRGET
ADD	#̃1,R0	The T bit is not changed by ADD.	SUB.W	#1,R0
CMP/EQ	#0,R0	When R0 = 0, the T bit is set.	BEQ	TRGET
BT	TRGET	A branch is made when R0 = 0.		

Immediate Data: 8-bit immediate data is placed in the instruction code. Word and longw immediate data is not placed in the instruction code. It is placed in a table in memory. Th memory is accessed with the MOV immediate data instruction using PC relative addressi with displacement.

Note: * Immediate data is accessed by @(disp,PC).

Absolute Addresses: When data is accessed by absolute address, place the absolute add in a table in memory beforehand. The absolute address value is transferred to a register u method whereby immediate data is loaded when an instruction is executed, and the data accessed using the register indirect addressing mode.

Table 2.6 Access to Absolute Address

Type	CPU in this LSI	Example of Oth
Absolute address	MOV.L @(disp,PC),R1	MOV.B @H'123
	MOV.B @R1,R0	
	....	
	.DATA.L H'12345678	

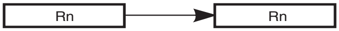
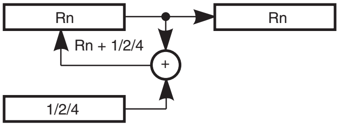
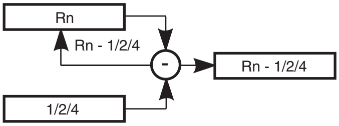
Note: * Immediate data is referenced by @(disp,PC).

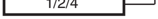
16-Bit/32-Bit Displacement: When data is accessed using the 16- or 32-bit displacemen addressing mode, the displacement value is placed in a table in memory beforehand. Usi method whereby immediate data is loaded when an instruction is executed, this value is transferred to a register and the data is accessed using index register indirect addressing

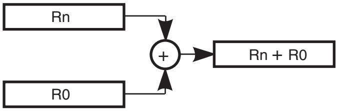
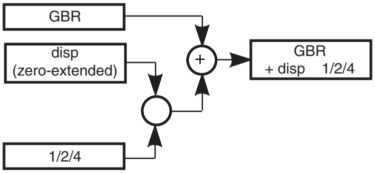
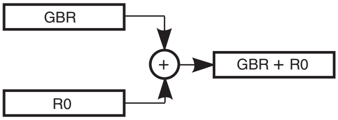
2.4.2 Addressing Modes

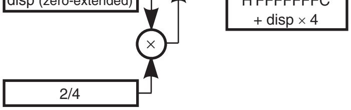
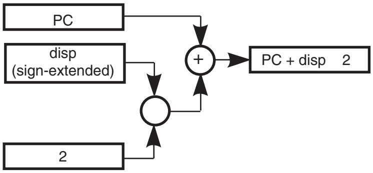
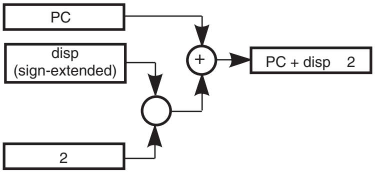
Table 2.8 lists addressing modes and effective address calculation methods.

Table 2.8 Addressing Modes and Effective Addresses

Addressing Mode	Instruction Format	Effective Address Calculation Method	Calculati Formula
Register direct	Rn	Effective address is register Rn. (Operand is register Rn contents.)	—
Register indirect	@Rn	Effective address is register Rn contents. 	Rn
Register indirect with post-increment	@Rn+	Effective address is register Rn contents. A constant is added to Rn after instruction execution: 1 for a byte operand, 2 for a word operand, 4 for a longword operand. 	Rn After inst executior Byte: Rn Word: Rr Longword → Rn
Register indirect with pre-decrement	@–Rn	Effective address is register Rn contents, decremented by a constant beforehand: 1 for a byte operand, 2 for a word operand, 4 for a longword operand. 	Byte: Rn Word: Rr Longword → Rn (Instructio executed after calc



Index register indirect	@(R0, Rn)	Effective address is sum of register Rn and R0 contents.  	Rn + R0
GBR indirect with displacement	@(disp:8, GBR)	Effective address is register GBR contents with 8-bit displacement disp added. After disp is zero-extended, it is multiplied by 1 (byte), 2 (word), or 4 (longword), according to the operand size.  GBR disp (zero-extended) + GBR + disp 1/2/4 1/2/4	Byte: G Word: G 2 Longwo disp × 4
Index GBR indirect	@(R0, GBR)	Effective address is sum of register GBR and R0 contents.  	GBR +

		 disp (zero-extended) × 2/4 H'FFFFFFFC + disp × 4	
PC relative	disp:8	Effective address is PC with 8-bit displacement disp added after being sign-extended and multiplied by 2. 	PC + disp
	disp:12	Effective address is PC with 12-bit displacement disp added after being sign-extended and multiplied by 2. 	PC + disp

#imm:8	8-bit immediate data imm of TRAPA instruction is zero-extended and multiplied by 4.	—

2.4.3 Instruction Formats

This section describes the instruction formats, and the meaning of the source and destina operands. The meaning of the operands depends on the instruction code. The following are used in the table.

`xxxx`: Instruction code

`mmmm`: Source register

`nnnn`: Destination register

`iiii`: Immediate data

`dddd`: Displacement

	Control register or system register	nnnn: pre-decrement register indirect	STC.L SR,@-R
m type 15 0 xxxx mmmm xxxx xxxx	mmmm: register direct	Control register or system register	LDC Rm,SR
	mmmm: post-increment register indirect	Control register or system register	LDC.L @Rm+,S
	mmmm: register indirect	—	JMP @Rm
	PC relative using Rm	—	BRAF Rm

	nnnn: * post-increment register indirect (multiply-and-accumulate operation)		
	mmmm: post-increment register indirect	nnnn: register direct	MOV.L @Rm-
	mmmm: register direct	nnnn: pre-decrement register indirect	MOV.L Rm,@
	mmmm: register direct	nnnn: index register indirect	MOV.L Rm,@
md type 15 0 xxxx xxxx | mmmm | dddd	mmmmdddd: register indirect with displacement	R0 (register direct)	MOV.B @(dis
nd4 type 15 0 xxxx xxxx | nnnn | dddd	R0 (register direct)	nnnndddd: register indirect with displacement	MOV.B R0,@
nmd type 15 0 xxxx | nnnn | mmmm | dddd	mmmm: register direct	nnnndddd: register indirect with displacement	MOV.L Rm,@
	mmmmdddd: register indirect with displacement	nnnn: register direct	MOV.L @(dis

	—	dddddddd: PC relative	BF label
d12 type 15 0 xxxx dddd dddd dddd	—	dddddddddddd: PC relative	BRA label (label=disp+PC
nd8 type 15 0 xxxx nnnn dddd dddd	dddddddd: PC relative with displacement	nnnn: register direct	MOV.L @(disp,
i type 15 0 xxxx xxxx iiii iiii	iiiiiiii: immediate	Index GBR indirect	AND.B #imm,@
	iiiiiiii: immediate	R0 (register direct)	AND #imm,R0
	iiiiiiii: immediate	—	TRAPA #imm
ni type 15 0 xxxx nnnn iiii iiii	iiiiiiii: immediate	nnnn: register direct	ADD #imm,Rn

Note: * In multiply and accumulate instructions, nnnn is the source register.

instructions			Immediate data transfer Peripheral module data transfer Structure data transfer	
		MOVA	Effective address transfer	
		MOVT	T bit transfer	
		SWAP	Upper/lower swap	
		XTRCT	Extraction of middle of linked registers	
Arithmetic operation instructions	21	ADD	Binary addition	33
		ADDC	Binary addition with carry	
		ADDV	Binary addition with overflow	
		CMP/cond	Comparison	
		DIV1	Division	
		DIV0S	Signed division initialization	
		DIV0U	Unsigned division initialization	
		DMULS	Signed double-precision multiplication	
		DMULU	Unsigned double-precision multiplication	
		DT	Decrement and test	
		EXTS	Sign extension	
		EXTU	Zero extension	
		MAC	Multiply-and-accumulate, double-precision multiply-and-accumulate	
		MUL	Double-precision multiplication	

Logic operation instructions	6	AND	Logical AND	14
		NOT	Bit inversion	
		OR	Logical OR	
		TAS	Memory test and bit setting	
		TST	T bit setting for logical AND	
		XOR	Exclusive logical OR	
Shift instructions	10	ROTL	1-bit left shift	14
		ROTR	1-bit right shift	
		ROTCL	1-bit left shift with T bit	
		ROTCR	1-bit right shift with T bit	
		SHAL	Arithmetic 1-bit left shift	
		SHAR	Arithmetic 1-bit right shift	
		SHLL	Logical 1-bit left shift	
		SHLLn	Logical n-bit left shift	
		SHLR	Logical 1-bit right shift	
		SHLRn	Logical n-bit right shift	

		JMP	Unconditional branch	
		JSR	Branch to subroutine procedure	
		RTS	Return from subroutine procedure	
System control instructions	11	CLRT	T bit clear	31
		CLRMAC	MAC register clear	
		LDC	Load into control register	
		LDS	Load into system register	
		NOP	No operation	
		RTE	Return from exception handling	
		SETT	T bit setting	
		SLEEP	Transition to power-down mode	
		STC	Store from control register	
		STS	Store from system register	
		TRAPA	Trap exception handling	
Total:	62			14

OP: Operation code Sz: Size SRC: Source DEST: Destination Rm: Source register Rn: Destination register imm: Immediate data disp: Displacement*2	nnnn: Destination register 0000: R0 0001: R1 ········· 1111: R15 iiii: Immediate data dddd: Displacement	(xx): Memory operand M/Q/T: Flag bits in SR &: Logical AND of each bit |: Logical OR of each bit ^: Exclusive logical OR of each bit –: Logical NOT of each bit <<n: n-bit left shift >>n: n-bit right shift

Notes: 1. The table shows the minimum number of execution states. In practice, the nun instruction execution states will be increased in cases such as the following:

- When there is contention between an instruction fetch and a data access
- When the destination register of a load instruction (memory → register) is by the following instruction

2. Scaled (×1, ×2, or ×4) according to the instruction operand size, etc. For details, see SH-1/SH-2/SH-DSP Software Manual.

MOV	Rm,Rn	Rm → Rn	0110nnnnmmmm0011	1
MOV.B	Rm,@Rn	Rm → (Rn)	0010nnnnmmmm0000	1
MOV.W	Rm,@Rn	Rm → (Rn)	0010nnnnmmmm0001	1
MOV.L	Rm,@Rn	Rm → (Rn)	0010nnnnmmmm0010	1
MOV.B	@Rm,Rn	(Rm) → Sign extension → Rn	0110nnnnmmmm0000	1
MOV.W	@Rm,Rn	(Rm) → Sign extension → Rn	0110nnnnmmmm0001	1
MOV.L	@Rm,Rn	(Rm) → Rn	0110nnnnmmmm0010	1
MOV.B	Rm,@–Rn	Rn–1 → Rn, Rm → (Rn)	0010nnnnmmmm0100	1
MOV.W	Rm,@–Rn	Rn–2 → Rn, Rm → (Rn)	0010nnnnmmmm0101	1
MOV.L	Rm,@–Rn	Rn–4 → Rn, Rm → (Rn)	0010nnnnmmmm0110	1
MOV.B	@Rm+,Rn	(Rm) → Sign extension → Rn, Rm + 1 → Rm	0110nnnnmmmm0100	1
MOV.W	@Rm+,Rn	(Rm) → Sign extension → Rn, Rm + 2 → Rm	0110nnnnmmmm0101	1
MOV.L	@Rm+,Rn	(Rm) → Rn,Rm + 4 → Rm	0110nnnnmmmm0110	1
MOV.B	R0,@(disp,Rn)	R0 → (disp + Rn)	10000000nnnndddd	1
MOV.W	R0,@(disp,Rn)	R0 → (disp × 2 + Rn)	10000001nnnndddd	1
MOV.L	Rm,@(disp,Rn)	Rm → (disp × 4 + Rn)	0001nnnnmmmmdddd	1
MOV.B	@(disp,Rm),R0	(disp + Rm) → Sign extension → R0	10000100mmmmdddd	1
MOV.W	@(disp,Rm),R0	(disp × 2 + Rm) → Sign extension → R0	10000101mmmmdddd	1
MOV.L	@(disp,Rm),Rn	(disp × 4 + Rm) → Rn	0101nnnnmmmmdddd	1

MOV.B	R0,@(disp,GBR)	R0 → (disp + GBR)	11000000dddddddd	1	-
MOV.W	R0,@(disp,GBR)	R0 → (disp × 2 + GBR)	11000001dddddddd	1	-
MOV.L	R0,@(disp,GBR)	R0 → (disp × 4 + GBR)	11000010dddddddd	1	-
MOV.B	@(disp,GBR),R0	(disp + GBR) → Sign extension → R0	11000100dddddddd	1	-
MOV.W	@(disp,GBR),R0	(disp × 2 + GBR) → Sign extension → R0	11000101dddddddd	1	-
MOV.L	@(disp,GBR),R0	(disp × 4 + GBR) → R0	11000110dddddddd	1	-
MOVA	@(disp,PC),R0	disp × 4 + PC → R0	11000111dddddddd	1	-
MOVT	Rn	T → Rn	0000nnnn00101001	1	-
SWAP.B	Rm,Rn	Rm → Swap lowest two bytes → Rn	0110nnnnmmmm1000	1	-
SWAP.W	Rm,Rn	Rm → Swap two consecutive words → Rn	0110nnnnmmmm1001	1	-
XTRCT	Rm,Rn	Rm: Middle 32 bits of Rn → Rn	0010nnnnmmmm1101	1	-

		Overflow → T		
CMP/EQ	#imm,R0	If R0 = imm, 1 → T	10001000iiiiiiii	1
CMP/EQ	Rm,Rn	If Rn = Rm, 1 → T	0011nnnnmmmm0000	1
CMP/HS	Rm,Rn	If Rn ≥ Rm with unsigned data, 1 → T	0011nnnnmmmm0010	1
CMP/GE	Rm,Rn	If Rn ≥ Rm with signed data, 1 → T	0011nnnnmmmm0011	1
CMP/HI	Rm,Rn	If Rn > Rm with unsigned data, 1 → T	0011nnnnmmmm0110	1
CMP/GT	Rm,Rn	If Rn > Rm with signed data, 1 → T	0011nnnnmmmm0111	1
CMP/PZ	Rn	If Rn ≥ 0, 1 → T	0100nnnn00010001	1
CMP/PL	Rn	If Rn > 0, 1 → T	0100nnnn00010101	1
CMP/STR	Rm,Rn	If Rn and Rm have an equivalent byte, 1 → T	0010nnnnmmmm1100	1
DIV1	Rm,Rn	Single-step division (Rn/Rm)	0011nnnnmmmm0100	1
DIV0S	Rm,Rn	MSB of Rn → Q, MSB of Rm → M, M^ Q → T	0010nnnnmmmm0111	1
DIV0U		0 → M/Q/T	0000000000011001	1
DMULS.L	Rm,Rn	Signed operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bits	0011nnnnmmmm1101	2 to 5*

EXTU.B	Rm,Rn	A byte in Rm is zero-extended → Rn	0110nnnnmmmm1100	1	-
EXTU.W	Rm,Rn	A word in Rm is zero-extended → Rn	0110nnnnmmmm1101	1	-
MAC.L	@Rm+,@Rn+	Signed operation of (Rn) × (Rm) + MAC → MAC, 32 × 32 + 64 → 64 bits	0000nnnnmmmm1111	2 to 5*	-
MAC.W	@Rm+,@Rn+	Signed operation of (Rn) × (Rm) + MAC → MAC, 16 × 16 + 64 → 64 bits	0100nnnnmmmm1111	2 to 4*	-
MUL.L	Rm,Rn	Rn × Rm → MACL 32 × 32 → 32 bits	0000nnnnmmmm0111	2 to 5*	-
MULS.W	Rm,Rn	Signed operation of Rn × Rm → MAC 16 × 16 → 32 bits	0010nnnnmmmm1111	1 to 3*	-
MULU.W	Rm,Rn	Unsigned operation of Rn × Rm → MAC 16 × 16 → 32 bits	0010nnnnmmmm1110	1 to 3*	-
NEG	Rm,Rn	0-Rm → Rn	0110nnnnmmmm1011	1	-
NEGC	Rm,Rn	0-Rm-T → Rn, Borrow → T	0110nnnnmmmm1010	1	
SUB	Rm,Rn	Rn-Rm → Rn	0011nnnnmmmm1000	1	-
SUBC	Rm,Rn	Rn-Rm–T → Rn, Borrow → T	0011nnnnmmmm1010	1	
SUBV	Rm,Rn	Rn-Rm → Rn, Underflow → T	0011nnnnmmmm1011	1	

Note: * Indicates the number of execution cycles for normal operation.

NOT	Rm,Rn	~Rm → Rn	0110nnnnmmmm0111	1
OR	Rm,Rn	Rn | Rm → Rn	0010nnnnmmmm1011	1
OR	#imm,R0	R0 | imm → R0	11001011iiiiiiii	1
OR.B	#imm,@(R0,GBR)	(R0 + GBR) | imm → (R0 + GBR)	11001111iiiiiiii	3
TAS.B	@Rn	If (Rn) is 0, 1 → T; 1 → MSB of (Rn)	0100nnnn00011011	4
TST	Rm,Rn	Rn & Rm; if the result is 0, 1 → T	0010nnnnmmmm1000	1
TST	#imm,R0	R0 & imm; if the result is 0, 1 → T	11001000iiiiiiii	1
TST.B	#imm,@(R0,GBR)	(R0 + GBR) & imm; if the result is 0, 1 → T	11001100iiiiiiii	3
XOR	Rm,Rn	Rn ^ Rm → Rn	0010nnnnmmmm1010	1
XOR	#imm,R0	R0 ^ imm → R0	11001010iiiiiiii	1
XOR.B	#imm,@(R0,GBR)	(R0 + GBR) ^ imm → (R0 + GBR)	11001110iiiiiiii	3

SHAL	Rn	T ← Rn ← 0	0100nnnn00100000	1	
SHAR	Rn	MSB → Rn → T	0100nnnn00100001	1	
SHLL	Rn	T ← Rn ← 0	0100nnnn00000000	1	
SHLR	Rn	0 → Rn → T	0100nnnn00000001	1	
SHLL2	Rn	Rn << 2 → Rn	0100nnnn00001000	1	-
SHLR2	Rn	Rn >> 2 → Rn	0100nnnn00001001	1	-
SHLL8	Rn	Rn << 8 → Rn	0100nnnn00011000	1	-
SHLR8	Rn	Rn >> 8 → Rn	0100nnnn00011001	1	-
SHLL16	Rn	Rn << 16 → Rn	0100nnnn00101000	1	-
SHLR16	Rn	Rn >> 16 → Rn	0100nnnn00101001	1	-

BT	label	If T = 1, disp × 2 + PC → PC;
		if T = 0, nop
			10001001dddddddd	3/1*

BT/S	label	Delayed branch, if T = 1, disp × 2 + PC → PC;
		if T = 0, nop
			10001101dddddddd	2/1*

BRA	label	Delayed branch, disp × 2 + PC → PC	1010dddddddddddd	2
BRAF	Rm	Delayed branch, Rm + PC → PC	0000mmmm00100011	2
BSR	label	Delayed branch, PC → PR, disp × 2 + PC → PC	1011dddddddddddd	2
BSRF	Rm	Delayed branch, PC → PR, Rm + PC → PC	0000mmmm00000011	2
JMP	@Rm	Delayed branch, Rm → PC	0100mmmm00101011	2
JSR	@Rm	Delayed branch, PC → PR, Rm → PC	0100mmmm00001011	2
RTS		Delayed branch, PR → PC	0000000000001011	2

Note: * One cycle when the branch is not executed.

LDC Rm,VBR	Rm → VBR	0100mmmm00101110	1
LDC.L @Rm+,SR	(Rm) → SR, Rm + 4 → Rm	0100mmmm00000111	3
LDC.L @Rm+,GBR	(Rm) → GBR, Rm + 4 → Rm	0100mmmm00010111	3
LDC.L @Rm+,VBR	(Rm) → VBR, Rm + 4 → Rm	0100mmmm00100111	3
LDS Rm,MACH	Rm → MACH	0100mmmm00001010	1
LDS Rm,MACL	Rm → MACL	0100mmmm00011010	1
LDS Rm,PR	Rm → PR	0100mmmm00101010	1
LDS.L @Rm+,MACH	(Rm) → MACH, Rm + 4 → Rm	0100mmmm00000110	1
LDS.L @Rm+,MACL	(Rm) → MACL, Rm + 4 → Rm	0100mmmm00010110	1
LDS.L @Rm+,PR	(Rm) → PR, Rm + 4 → Rm	0100mmmm00100110	1
NOP	No operation	0000000000001001	1
RTE	Delayed branch, Stack area → PC/SR	0000000000101011	5
SETT	1 → T	0000000000011000	1
SLEEP	Sleep	0000000000011011	4*
STC SR,Rn	SR → Rn	0000nnnn00000010	1
STC GBR,Rn	GBR → Rn	0000nnnn00010010	1
STC VBR,Rn	VBR → Rn	0000nnnn00100010	1
STC.L SR,@–Rn	Rn–4 → Rn, SR → (Rn)	0100nnnn00000011	1
STC.L GBR,@–Rn	Rn–4 → Rn, GBR → (Rn)	0100nnnn00010011	1
STC.L VBR,@–Rn	Rn–4 → Rn, VBR → (Rn)	0100nnnn00100011	1

Note: * Number of execution cycles until this LSI enters sleep mode.

About the number of execution cycles:

The table lists the minimum number of execution cycles. In practice, the numb execution cycles will be increased depending on the conditions such as:

- When there is a conflict between instruction fetch and data access
- When the destination register of a load instruction (memory → register) is a by the instruction immediately after the load instruction.

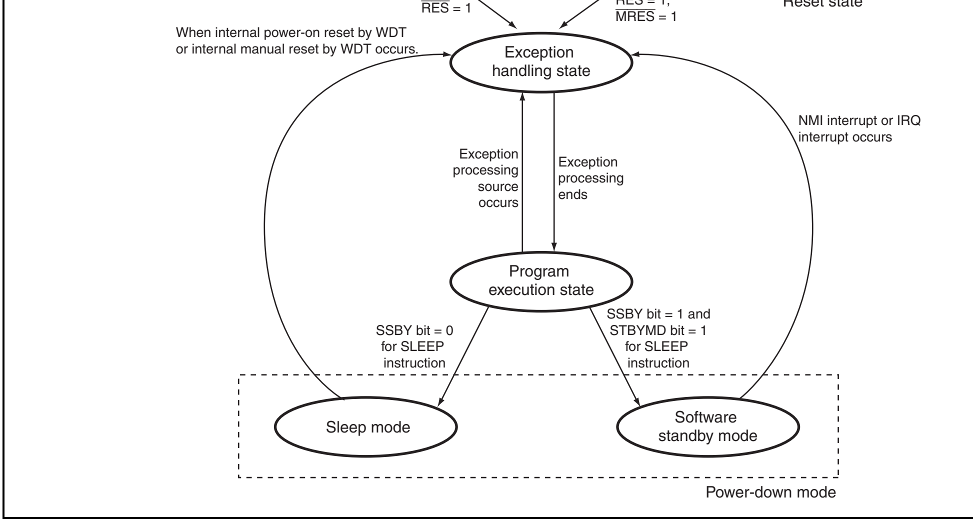


Figure 2.4 Transitions between Processing States

by SP. The start address of an exception handling routine is fetched from the excepti
handling vector table and a branch to the address is made to execute a program.

Then the processing state enters the program execution state.

- Program execution state

  The CPU executes programs sequentially.

- Power-down state

  The CPU stops to reduce power consumption. The SLEEP instruction makes the CP
  sleep mode or software standby mode.

The MCU operating mode can be selected from MCU extension modes 0 to 2 and single mode. For the on-chip flash memory programming mode, boot mode, user boot mode, a program mode, which are on-chip programming modes are available.

Table 3.1 Selection of Operating Modes

	Pin Setting			On-Chip ROM
Mode No.	**FWE**	**MD1**	**Mode Name**	(Flash memory)
Mode 3	0	1	Single chip mode	Active
Mode 4*[1]	1	0	Boot mode	Active
Mode 6*[2]	1	1	User program mode	Active

Notes: 1. Flash memory programming mode.

2. Prohibited in SH71251A, SH71250A, SH71241A and SH71240A.

3.3 Operating Modes

3.3.1 Mode 3 (Single Chip Mode)

All ports can be used in this mode, however the external address cannot be used.

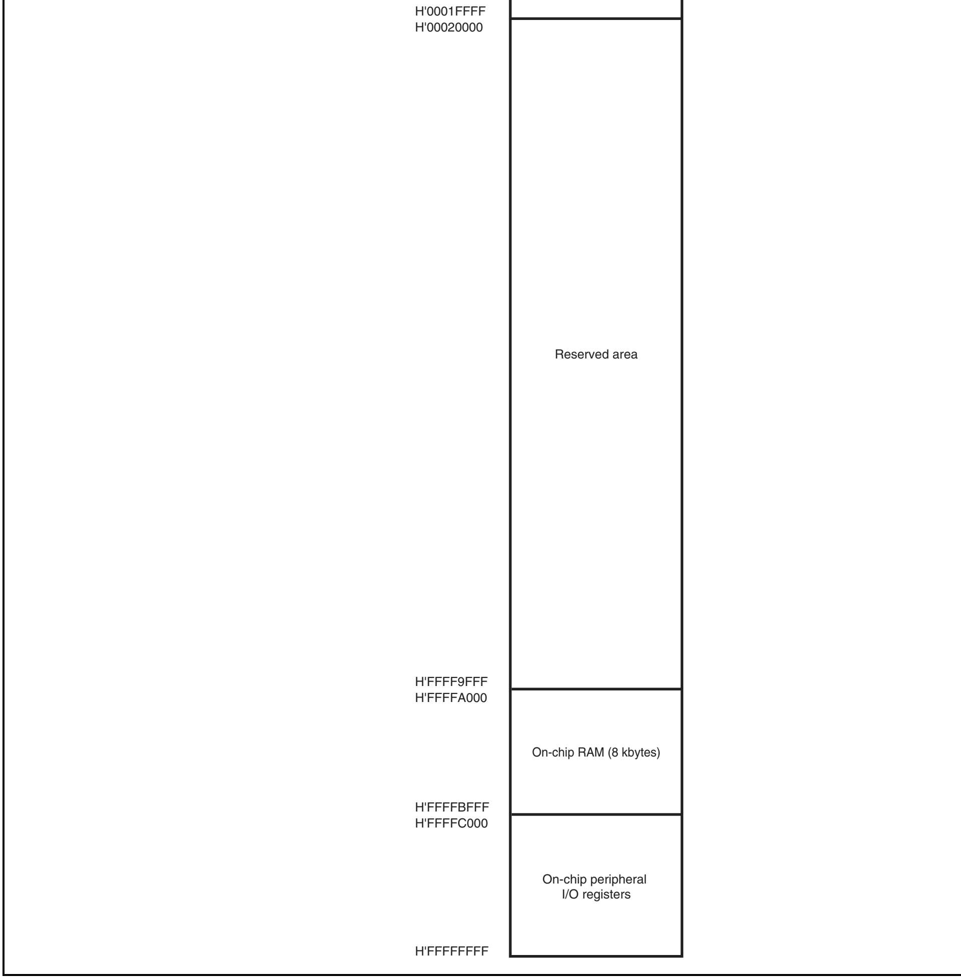


Figure 3.1 Address Map in SH7125, SH7124 (128 Kbytes Flash Memory Ver

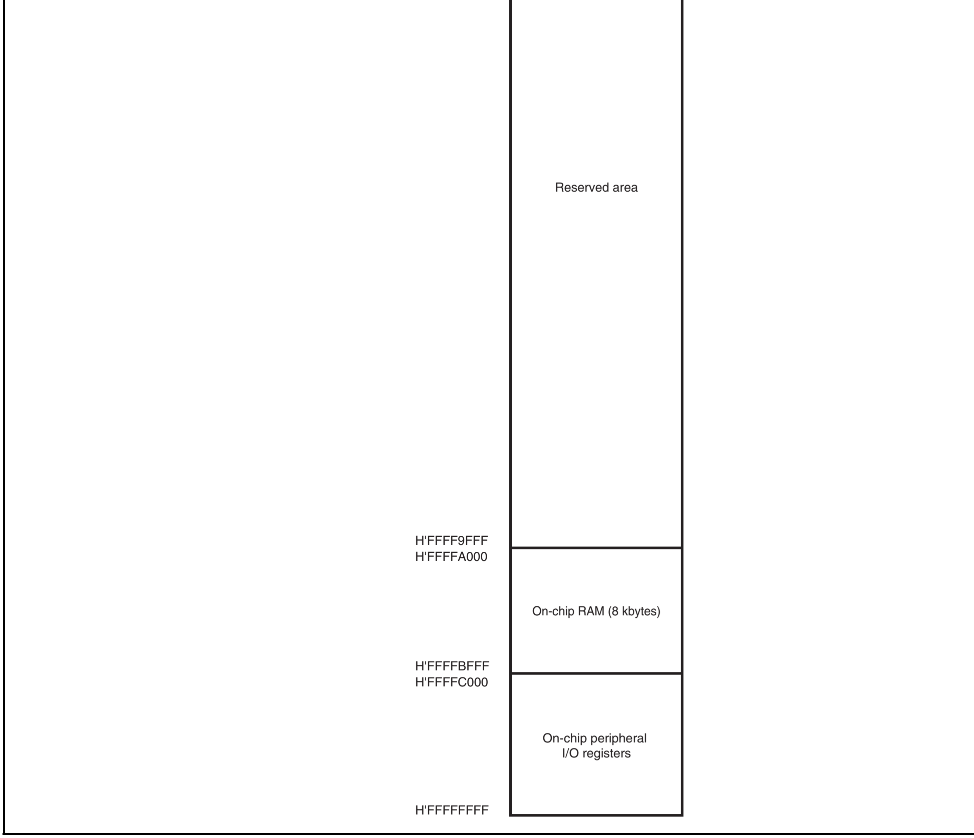


Figure 3.2 Address Map in SH7125, SH7124 (64 Kbytes Flash Memory Versi

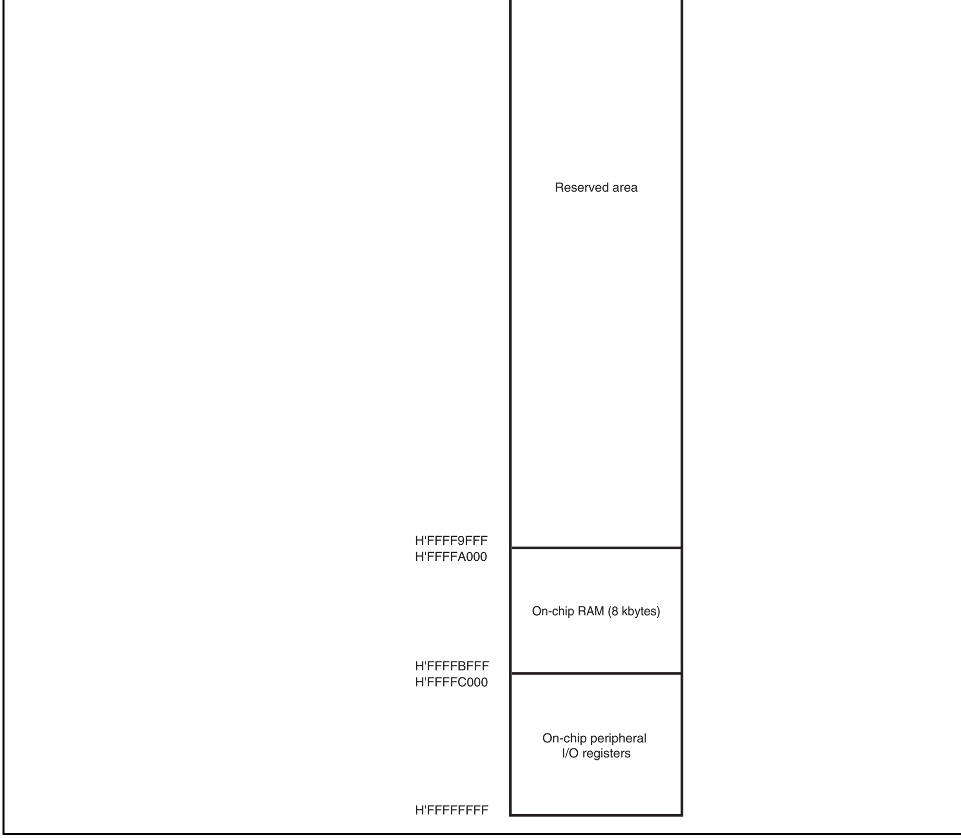


Figure 3.3 Address Map in SH71251A and SH71241A (32 Kbytes Flash Memory

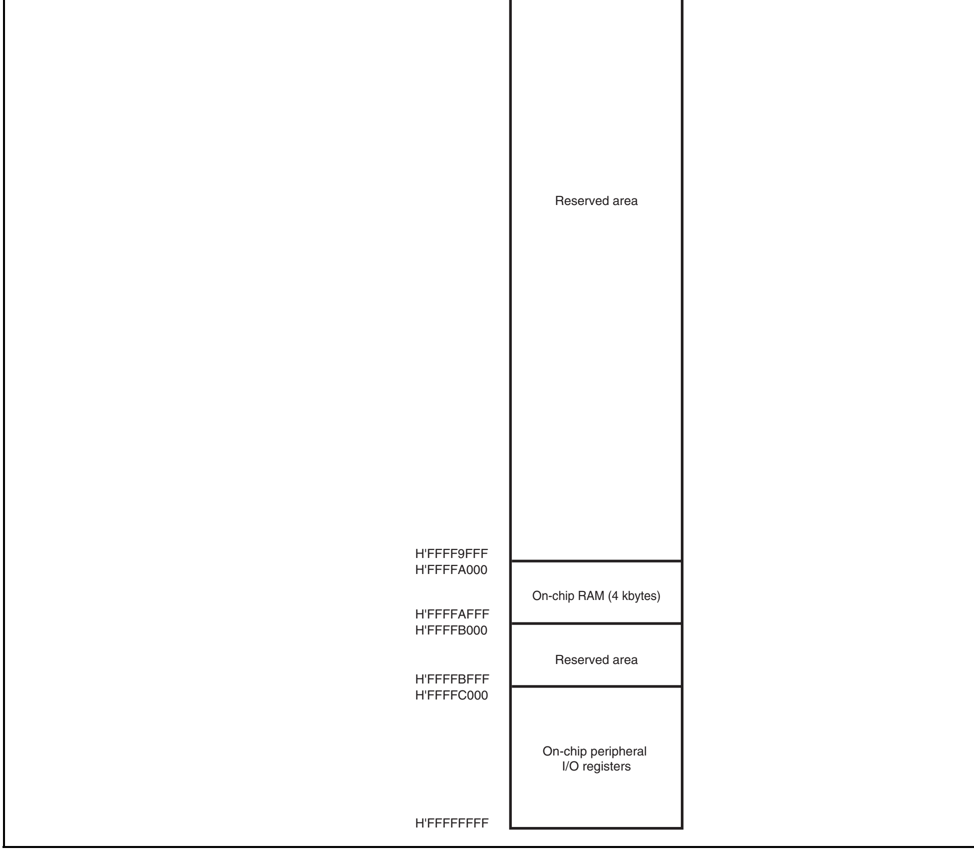
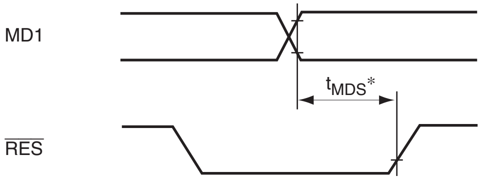


Figure 3.4 Address Map in SH71250A and SH71240A (16 Kbytes Flash Memory V



Note: * See section 21.3.2, Control Signal Timing.

Figure 3.5 Reset Input Timing when Changing Operating Mode

a bus clock (Bϕ = CK) for the external bus interface; and a MTU2 clock (MPϕ) for t
MTU2 module.

- Frequency change function

  Frequencies of the internal clock (Iϕ), bus clock (Bϕ), peripheral clock (Pϕ), and MT (MPϕ) can be changed independently using the divider circuit within the CPG. Frequ changed by software using the frequency control register (FRQCR) setting.

- Power-down mode control

  The clock can be stopped in sleep mode and standby mode and specific modules can stopped using the module standby function.

- Oscillation stop detection

  If the clock supplied through the clock input pin stops for any reason, the timer pins automatically placed in the high-impedance state.

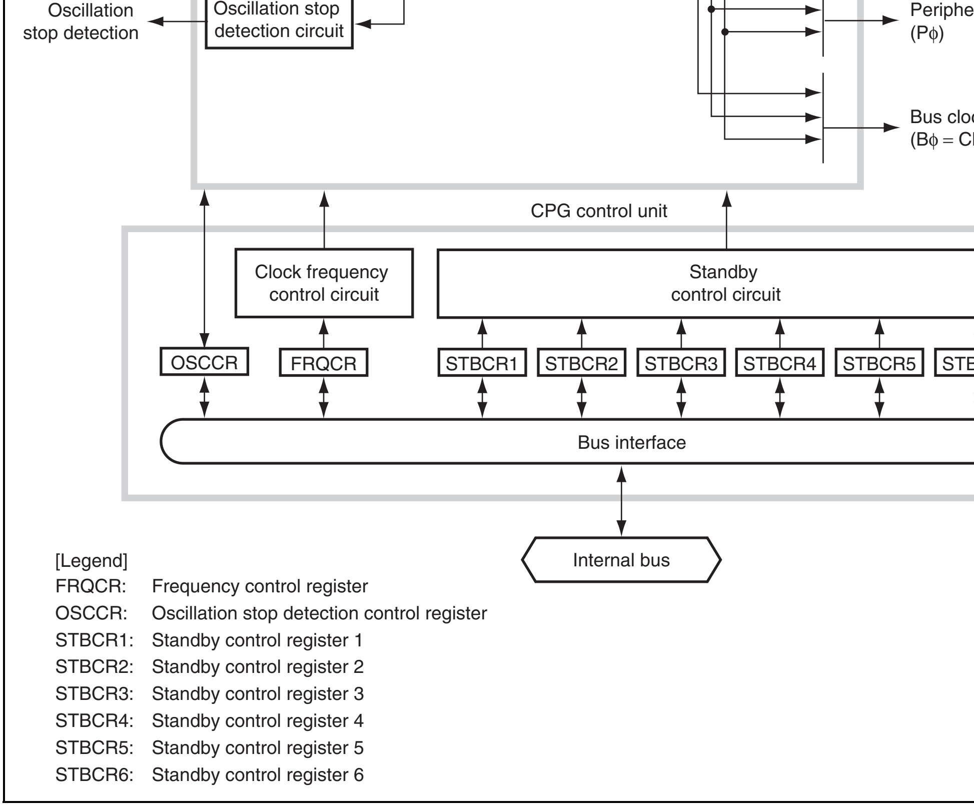

Oscillation
stop detection
Oscillation stop
detection circuit
Periphe
(Pϕ)
Bus cloc
(Bϕ = Cl
CPG control unit
Clock frequency
control circuit
Standby
control circuit
OSCCR
FRQCR
STBCR1
STBCR2
STBCR3
STBCR4
STBCR5
STB
Bus interface
Internal bus
[Legend]
FRQCR: Frequency control register
OSCCR: Oscillation stop detection control register
STBCR1: Standby control register 1
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4
STBCR5: Standby control register 5
STBCR6: Standby control register 6

Figure 4.1 Block Diagram of CPG

from the PLL circuit. The division ratio should be specified in the frequency control reg
(FRQCR).

Oscillation Stop Detection Circuit: This circuit detects an abnormal condition in the cr
oscillator.

Clock Frequency Control Circuit: The clock frequency control circuit controls the clo
frequency according to the setting in the frequency control register (FRQCR).

Standby Control Circuit: The standby control circuit controls the state of the on-chip c
circuit and other modules in sleep or standby mode.

Frequency Control Register (FRQCR): The frequency control register (FRQCR) has c
bits for the frequency division ratios of the internal clock (Iϕ), bus clock (Bϕ), periphera
(Pϕ), and MTU2 clock (MPϕ).

Oscillation Stop Detection Control Register (OSCCR): The oscillation stop detection
register (OSCCR) has an oscillation stop detection flag and a bit for selecting flag status
through an external pin.

Standby Control Registers 1 to 6 (STBCR1 to STBCR6): The standby control registe
(STBCR) has bits for controlling the power-down modes. For details, see section 19, Po
Modes.

Bus clock (Bφ)	MTU2 clock (MPφ)	MTU2

Note: * The UBC is not supported on 32 Kbyte versions (SH71251A, SH71241A) and versions (SH71250A, SH71240A).

4.2 Input/Output Pins

Table 4.2 shows the CPG pin configuration.

Table 4.2 Pin Configuration

Pin Name	Abbr.	I/O	Description
Crystal input/output pins (clock input pins)	XTAL	Output	Connects a crystal resonator.
	EXTAL	Input	Connects a crystal resonator or an external c

circuit before being supplied to the on-chip modules in this LSI, which eliminates the ne generate a high-frequency clock outside the LSI. Since the input clock frequency rangin MHz to 12.5 MHz can be used, the internal clock (Iϕ) frequency ranges from 10 MHz to

Maximum operating frequencies:
Iϕ = 50 MHz, Bϕ = 40 MHz, Pϕ = 40 MHz, and MPϕ = 40 MHz

Table 4.4 shows the frequency division ratios that can be specified with FRQCR.

1/2	1/2	1/2	1/2	4	4	4	4	10	40	40	40
1/8	1/8	1/8	1/8	1	1	1	1	12.5	12.5	12.5	12.
1/4	1/8	1/8	1/8	2	1	1	1	12.5	25	12.5	12.
1/4	1/4	1/4	1/4	2	2	2	2	12.5	25	25	25
1/2	1/4	1/4	1/4	4	2	2	2	12.5	50	25	25

Notes: * Clock frequencies when the input clock frequency is assumed to be the shown The internal clock (Iϕ) frequency must be 10 to 50 MHz and the peripheral cloc frequency must be 10 to 40 MHz. The bus clock (Bϕ) frequency must be equal peripheral clock (Pϕ) frequency.

1. The PLL multiplication ratio is fixed at ×8. The division ratio can be selected fro ×1/4, and ×1/8 for each clock by the setting in the frequency control register.
2. The output frequency of the PLL circuit is the product of the frequency of the ir the crystal resonator or EXTAL pin and the multiplication ratio (×8) of the PLL c
3. The input to the divider is always the output from the PLL circuit.
4. The internal clock (Iϕ) frequency is the product of the frequency of the input fro crystal resonator or EXTAL pin, the multiplication ratio (×8) of the PLL circuit, a division ratio of the divider. The resultant frequency must be a maximum of 50 (maximum operating frequency).
5. The peripheral clock (Pϕ) frequency is the product of the frequency of the input crystal resonator or EXTAL pin, the multiplication ratio (×8) of the PLL circuit, a division ratio of the divider. The resultant frequency must be a maximum of 40
6. When using the MTU2, the MTU2 clock (MPϕ) frequency must be equal to or h than the peripheral clock frequency (Pϕ). The MTU2 clock (MPϕ) frequency are product of the frequency of the input from the crystal resonator or EXTAL pin, t multiplication ratio (×8) of the PLL circuit, and the division ratio of the divider.
7. The frequency of the CK pin is always be equal to the bus clock (Bϕ) frequency
8. The bus clock (Bϕ) frequency must be equal to the peripheral clock (Pϕ) freque

Oscillation stop detection control register	OSCCR	R/W	H'00	H'FFFFE814	8

4.4.1 Frequency Control Register (FRQCR)

FRQCR is a 16-bit readable/writable register that specifies the frequency division ratios internal clock (Iϕ), bus clock (Bϕ), peripheral clock (Pϕ), and MTU2 clock (MPϕ). FRQ accessed only in words.

FRQCR is initialized to H'36DB only by a power-on reset (except a power-on reset due overflow).

Before making changes to FRQCR, stop clock supply to each module except the CPU, c ROM, and on-chip-RAM.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	IFC[2:0]			BFC[2:0]			PFC[2:0]			-	-	-	M
Initial value:	0	0	1	1	0	1	1	0	1	1	0	1	1	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

				001: ×1/2 010: Setting prohibited 011: ×1/4 (initial value) 100: ×1/8 Other than above: Setting prohibited
11 to 9	BFC[2:0]	011	R/W	Bus Clock (Bϕ) Frequency Division Ratio Specify the division ratio of the bus clock (Bϕ) frequency with respect to the output frequency circuit. If a prohibited value is specified, subsec operation is not guaranteed. 000: Setting prohibited 001: ×1/2 010: Setting prohibited 011: ×1/4 (initial value) 100: ×1/8 Other than above: Setting prohibited

				011: ×1/4 (initial value) 100: ×1/8 Other than above: Setting prohibited
5 to 3	—	011	R/W	Reserved These bits are always read as B'011. The wri should always be B'011.
2 to 0	MPFC[2:0]	011	R/W	MTU2 Clock (MPϕ) Frequency Division Ratio Specify the division ratio of the MTU2 clock (M frequency with respect to the output frequenc circuit. If a prohibited value is specified, subse operation is not guaranteed. 000: Setting prohibited 001: ×1/2 010: Setting prohibited 011: ×1/4 (initial value) 100: ×1/8 Other than above: Setting prohibited

Bit	Bit Name	Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
2	OSCSTOP	0	R	Oscillation Stop Detection Flag [Setting condition] • When a stop in the clock input is detected d normal operation [Clearing condition] • By a power-on reset input through the $\overline{\text{RES}}$
1	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
0	OSCERS	0	R/W	Oscillation Stop Detection Flag Output Select Selects whether to output the oscillation stop d flag signal through the $\overline{\text{WDTOVF}}$ pin. 0: Outputs only the WDT overflow signal throug $\overline{\text{WDTOVF}}$ pin 1: Outputs the WDT overflow signal and the os stop detection flag signal through the $\overline{\text{WDTO}}$

3. Set the desired values in bits IFC2 to IFC0, BFC2 to BFC0, PFC2 to PFC0, and MP
MPFC0 bits. Since the frequency multiplication ratio in the PLL circuit is fixed at ×8
frequencies are determined only be selecting division ratios. When specifying the fre
satisfy the following condition: internal clock (Iϕ) ≥ bus clock (Bϕ) = peripheral cloc
When using the MTU2 clock, specify the frequencies to satisfy the following conditi
internal clock (Iϕ) ≥ MTU2 clock (MPϕ) ≥ peripheral clock (Pϕ).

4. After an instruction to rewrite FRQCR has been issued, the actual clock frequencies
change after (1 to 24n) cyc + 11Bϕ + 7Pϕ.
n: Division ratio specified by the BFC bit in FRQCR (1/2, 1/4, or 1/8)
cyc: Clock obtained by dividing EXTAL by 8 with the PLL.

Note: (1 to 24n) depends on the internal state.

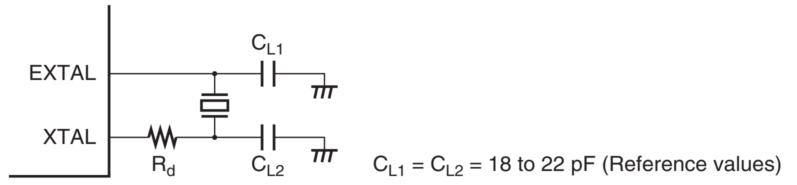


Figure 4.2 Connection of Crystal Resonator (Example)

Table 4.6 Damping Resistance Values (Reference Values)

Frequency (MHz)	10	12.5
Rd (Ω) (Reference Values)	0	0

Figure 4.3 shows an equivalent circuit of the crystal resonator. Use a crystal resonator wit characteristics listed in table 4.7.

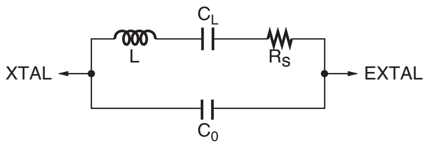


Figure 4.3 Crystal Resonator Equivalent Circuit

input clock frequency 10 to 12.5 MHz.

When leaving the XTAL pin open, make sure the parasitic capacitance is less than 10 pF

Even when inputting an external clock, be sure to wait at least the oscillation stabilizatio power-on sequence or in releasing software standby mode, in order to ensure the PLL st time.

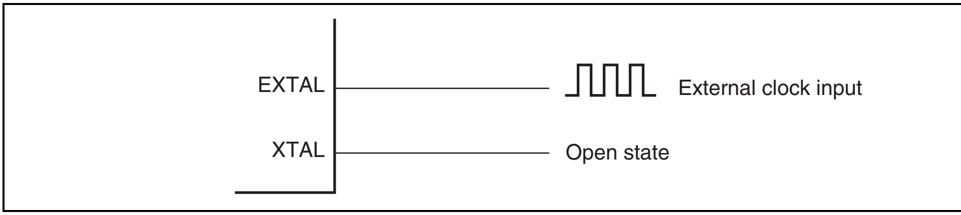


Figure 4.4 Example of External Clock Connection

Even in software standby mode, these pins are always placed in high-impedance state. Fo refer to appendix A, Pin States. These pins enter the normal state after software standby r canceled. Under an abnormal condition where oscillation stops while the LSI is not in sof standby mode, LSI operations other than the oscillation stop detection function become unpredictable. In this case, even after oscillation is restarted, LSI operations including the high-current pins become unpredictable.

Even while no change is detected in the EXTAL input, the PLL circuit in this LSI continu oscillating at a frequency range from 100 kHz to 10 MHz (depending on the temperature operating voltage).

to the oscillator pin.

4.8.2 Notes on Board Design

Measures against radiation noise are taken in this LSI. If further reduction in radiation n
needed, it is recommended to use a multiple layer board and provide a layer exclusive to
system ground.

When using a crystal resonator, place the crystal resonator and its load capacitors as clos
possible to the XTAL and EXTAL pins. Do not route any signal lines near the oscillator
as shown in figure 4.5. Otherwise, correct oscillation can be interfered by induction.

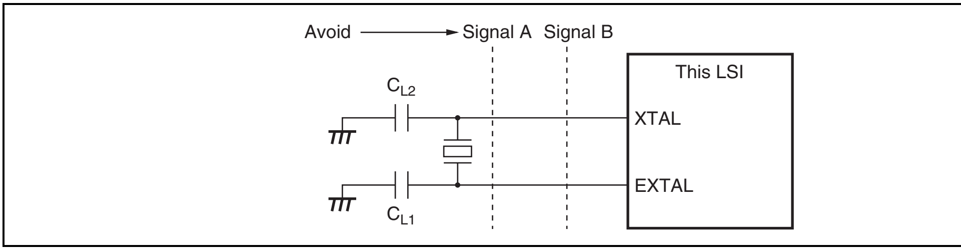
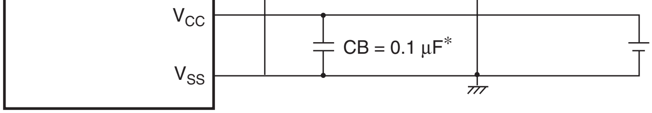


Figure 4.5 Cautions for Oscillator Circuit Board Design



(Recommended values are shown.)

Note: * CB and CPB are laminated ceramic type.

Figure 4.6 Recommended External Circuitry around PLL

Table 5.1 Types of Exceptions and Priority

Exception	Exception Source
Reset	Power-on reset
	Manual reset
Interrupt	User break (break before instruction execution)*3
Address error	CPU address error (instruction fetch)
Instruction	General illegal instructions (undefined code)
	Illegal slot instruction (undefined code placed immediately after a delayed branch instruction*1 or instruction that changes the PC value*
	Trap instruction (TRAPA instruction)
Address error	CPU address error (data access)
Interrupt	User break (break after instruction execution or operand break)*3
	NMI
	IRQ
	On-chip peripheral modules

Notes: 1. Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BRAF.

2. Instructions that change the PC value: JMP, JSR, BRA, BSR, RTS, RTE, BT, TRAPA, BF/S, BT/S, BSRF, BRAF, LDC Rm,SR, LDC.L @Rm+,SR.

3. The user break interrupt is not generated on the 32 Kbyte (SH71251A and S and 16 Kbyte (SH71250A and SH71240A) versions.

		WDT overflows.
Address error		Detected during the instruction decode stage and started execution of the current instruction is completed.
Interrupt		
Instruction	Trap instruction	Started by the execution of the TRAPA instruction.
	General illegal instructions	Started when an undefined code placed at other than a d (immediately after a delayed branch instruction) is decode
	Illegal slot instructions	Started when an undefined code placed at a delay slot (immediately after a delayed branch instruction) or an ins that changes the PC value is detected.

When exception handling starts, the CPU operates

Exception Handling Triggered by Reset: The initial values of the program counter (PC stack pointer (SP) are fetched from the exception handling vector table (PC from the addr H'00000000 and SP from the address H'00000004 when a power-on reset. PC from the ad H'00000008 and SP from the address H'0000000C when a manual reset.). For details, see 5.1.3, Exception Handling Vector Table. H'00000000 is then written to the vector base re (VBR), and H'F (B'1111) is written to the interrupt mask bits (I3 to I0) in the status regist The program starts from the PC address fetched from the exception handling vector table

Exception Handling Triggered by Address Error, Interrupt, and Instruction: SR and saved to the stack indicated by R15. For interrupt exception handling, the interrupt priorit written to the interrupt mask bits (I3 to I0) in SR. For address error and instruction excep handling, bits I3 to I0 are not affected. The start address is then fetched from the exceptio handling vector table and the program starts from that address.

Table 5.3 shows the vector numbers and vector table address offsets. Table 5.4 shows ho table addresses are calculated.

Table 5.3 Vector Numbers and Vector Table Address Offsets

Exception Handling Source		Vector Number	Vector Table Address Of
Power-on reset	PC	0	H'00000000 to H'0000000
	SP	1	H'00000004 to H'0000000
Manual reset	PC	2	H'00000008 to H'0000000
	SP	3	H'0000000C to H'0000000
General illegal instruction		4	H'00000010 to H'0000001
(Reserved for system use)		5	H'00000014 to H'0000001
Illegal slot instruction		6	H'00000018 to H'0000001
(Reserved for system use)		7	H'0000001C to H'0000001
		8	H'00000020 to H'0000002
CPU address error		9	H'00000024 to H'0000002
(Reserved for system use)		10	H'00000028 to H'0000002
Interrupt	NMI	11	H'0000002C to H'0000002
	User break*1	12	H'00000030 to H'0000003
(Reserved for system use)		13	H'00000034 to H'0000003
		:	:
		31	H'0000007C to H'0000007
Trap instruction (user vector)		32	H'00000080 to H'0000008
		:	:
		63	H'000000FC to H'000000F

:	:
255	H'000003FC to H'000003FF

Notes: 1. Reserved on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH7125 SH71240A) versions.

2. For details on the vector numbers and vector table address offsets of on-chip p module interrupts, see table 6.3 in section 6, Interrupt Controller (INTC).

Table 5.4 Calculating Exception Handling Vector Table Addresses

Exception Source	Vector Table Address Calculation
Resets	Vector table address = (vector table address offset) = (vector number) × 4
Address errors, interrupts, instructions	Vector table address = VBR + (vector table address offse = VBR + (vector number) × 4

Notes: 1. VBR: Vector base register

2. Vector table address offset: See table 5.3.

3. Vector number: See table 5.3.

	Conditions for Transition to Reset State			Internal State		
Type	$\overline{\text{RES}}$	WDT Overflow	$\overline{\text{MRES}}$	CPU, INTC	On-Chip Peripheral Module	POI I/O
Power-on reset	Low	—	—	Initialized	Initialized	Initi
	High	Overflow	High	Initialized	Initialized	Initi
Manual reset	High	Not overflowed	Low	Initialized	Not initialized	Not
	High	Overflow	High	Initialized	Not initialized	Not

5.2.2 Power-On Reset

Power-On Reset by $\overline{\text{RES}}$ Pin: When the $\overline{\text{RES}}$ pin is driven low, this LSI enters the pow reset state. To reliably reset this LSI, the $\overline{\text{RES}}$ pin should be kept low for at least the osc settling time when applying the power or when in standby mode (when the clock is halt least 20 tcyc when the clock is operating. During the power-on reset state, CPU internal all registers of on-chip peripheral modules are initialized. See appendix A, Pin States, fo status of individual pins during power-on reset mode.

In the power-on reset state, power-on reset exception handling starts when driving the $\overline{\text{R}}$ high after driving the pin low for the given time. The CPU operates as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched fro exception handling vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception handling vec
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits of the status register (SR) are set to H'F (B'1111).

initialized by a power-on reset from the RES pin).

If a reset caused by the signal input on the $\overline{\text{RES}}$ pin and a reset caused by a WDT overflo simultaneously, the $\overline{\text{RES}}$ pin reset has priority, and the WOVF bit in RSTCSR is cleared When the power-on reset exception handling caused by the WDT is started, the CPU ope follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from exception handling vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception handling vect
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits (of the status register (SR) are set to H'F (B'1111).
4. The values fetched from the exception handling vector table are set in the PC and SP, program starts.

5.2.3 Manual Reset

When the $\overline{\text{RES}}$ pin is high and the $\overline{\text{MRES}}$ pin is driven low, the LSI becomes to be a man state. To reliably reset the LSI, the $\overline{\text{MRES}}$ pin should be kept at low for at least the durati oscillation settling time that is set in WDT when in software standby mode (when the clo halted) or at least 20 t_{cyc} when the clock is operating. During manual reset, the CPU inter is initialized. Registers of on-chip peripheral modules are not initialized. See appendix A States, for the status of individual pins during manual reset mode.

In the manual reset status, manual reset exception processing starts when the $\overline{\text{MRES}}$ pin i kept low for a set period of time and then returned to high. The CPU will then operate in procedures as described for power-on resets.

Instruction fetch	CPU	Instruction fetched from even address	None (norma
		Instruction fetched from odd address	Address erro
		Instruction fetched from a space other than on-chip peripheral module space	None (norma
		Instruction fetched from on-chip peripheral module space	Address erro
Data read/write	CPU	Word data accessed from even address	None (norma
		Word data accessed from odd address	Address erro
		Longword data accessed from a longword boundary	None (norma
		Longword data accessed from other than a long-word boundary	Address erro
		Byte or word data accessed in on-chip peripheral module space	None (norma
		Longword data accessed in 16-bit on-chip peripheral module space	None (norma
		Longword data accessed in 8-bit on-chip peripheral module space	None (norma

3. The start address of the exception handling routine is fetched from the exception hanc vector table that corresponds to the generated address error, and the program starts exc from that address. This branch is not a delayed branch.

NMI	NMI pin (external input)	1
User break*	User break controller (UBC)	1
IRQ	IRQ0 to IRQ3 pins (external input)	4 (SH 3 (SH
On-chip peripheral module	Multi-function timer pulse unit 2 (MTU2)	28
	Watchdog timer (WDT)	1
	A/D converter (A/D_0 and A/D_1)	2
	Compare match timer (CMT_0 and CMT_1)	2
	Serial communication interface (SCI_0, SCI_1, and SCI_2)	12
	Port output enable (POE)	2

Note: * The user break interrupt is not generated on the 32 Kbyte (SH71251A and SH and 16 Kbyte (SH71250A and SH71240A) versions.

All interrupt sources are given different vector numbers and vector table address offsets details on vector numbers and vector table address offsets, see table 6.3 in section 6, Inte Controller (INTC).

that can be set are 0 to 15. Level 16 cannot be set. For details on IPRA to IPRF, see sectio
Interrupt Priority Registers A to F and H to M (IPRA to IPRF and IPRH to IPRM).

Table 5.8 Interrupt Priority

Type	Priority Level	Comment
NMI	16	Fixed priority level. Cannot be maskec
User break*	15	Fixed priority level. Can be masked.
IRQ	0 to 15	Set with interrupt priority registers A to to M (IPRA to IPRF and IPRH to IPRM
On-chip peripheral module		

Note: * The user break interrupt is not generated on the 32 Kbyte (SH71251A and SH and 16 Kbyte (SH71250A and SH71240A) versions.

5.4.3 Interrupt Exception Handling

When an interrupt occurs, the interrupt controller (INTC) ascertains its priority level. NM always accepted, but other interrupts are only accepted if they have a priority level highe priority level set in the interrupt mask bits (I3 to I0) of the status register (SR).

When an interrupt is accepted, exception handling begins. In interrupt exception handlin CPU saves SR and the program counter (PC) to the stack. The priority level of the accept interrupt is written to bits I3 to I0 in SR. Although the priority level of the NMI is 16, the in bits I3 to I0 is H'F (level 15). Next, the start address of the exception handling routine from the exception handling vector table for the accepted interrupt, and program executio branches to that address and the program starts. For details on the interrupt exception han section 6.6, Interrupt Operation.

Illegal slot instructions*	Undefined code placed immediately after a delayed branch instruction (delay slot) or instructions that changes the PC value	Delayed branch instructions: JMP, BRA, BSR, RTS, RTE, BF/S, BT/S BRAF Instructions that changes the PC v JSR, BRA, BSR, RTS, RTE, BT, B BF/S, BT/S, BSRF, BRAF, LDC R LDC.L @Rm+,SR
General illegal instructions*	Undefined code anywhere besides in a delay slot	—

Note: * The operation is not guaranteed when undefined instructions other than H'F0 H'FFFF are decoded.

5.5.2 Trap Instructions

When a TRAPA instruction is executed, the trap instruction exception handling starts. T operates as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the start addr instruction to be executed after the TRAPA instruction.
3. The CPU reads the start address of the exception handling routine from the exceptio vector table that corresponds to the vector number specified in the TRAPA instructi program execution branches to that address, and then the program starts. This branch delayed branch.

rewrites the PC.

3. The start address of the exception handling routine is fetched from the exception hand vector table that corresponds to the exception that occurred. Program execution branc that address and the program starts. This branch is not a delayed branch.

5.5.4 General Illegal Instructions

When an undefined code placed anywhere other than immediately after a delayed branch instruction (i.e., in a delay slot) is decoded, general illegal instruction exception handling The CPU handles the general illegal instructions in the same procedures as in the illegal s instructions. Unlike processing of illegal slot instructions, however, the program counter is stacked is the start address of the undefined code.

Occurrence Timing	Address Error	Illegal Instruction	Slot Illegal Instruction	Trap Instruction	I
Instruction in delay slot	×*2	—	×*2	—	×
Immediately after interrupt disabled instruction*1	√	√	√	√	×

[Legend]

√: Accepted

×: Not accepted

—: Does not occur

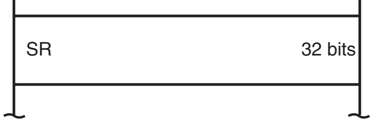
Notes: 1. Interrupt disabled instructions: LDC, LDC.L, STC, STC.L, LDS, LDS.L, STS, a

2. An exception is accepted before the execution of a delayed branch instructio However, when an address error or a slot illegal instruction exception occurs delay slot of the RTE instruction, correct operation is not guaranteed.

3. An exception is accepted after a delayed branch (between instructions in the and the branch destination).

4. An exception is accepted after the execution of the next instruction of an inte disabled instruction (before the execution two instructions after an interrupt d instruction).

		SR	32 bits
Address error (other than above)	SP →	Address of instruction that caused exception	32 bits
		SR	32 bits
Interrupt	SP →	Address of instruction after executed instruction	32 bits
		SR	32 bits
Trap instruction	SP →	Address of instruction after TRAPA instruction	32 bits
		SR	32 bits


SR
32 bits

stack is accessed during exception handling.

5.8.3 Address Errors Caused by Stacking for Address Error Exception Handlin

When the SP value is not a multiple of 4, an address error will occur when stacking for ex
handling (interrupts, etc.) and address error exception handling will start after the first exc
handling is ended. Address errors will also occur in the stacking for this address error exc
handling. To ensure that address error exception handling does not go into an endless loo
address errors are accepted at that point. This allows program control to be passed to the
routine for address error exception and enables error processing.

When an address error occurs during exception handling stacking, the stacking bus cycle
executed. When stacking the SR and PC values, the SP values for both are subtracted by
therefore, the SP value is still not a multiple of 4 after the stacking. The address value out
during stacking is the SP value whose lower two bits are cleared to 0. So the write data st
undefined.

Compiler

This instruction is not allocated in the delay slot in the compiler V.4 and its subsequent v

Real-time OS for μITRON specifications

1. HI7000/4, HI-SH7

   This instruction does not exist in the delay slot within the OS.

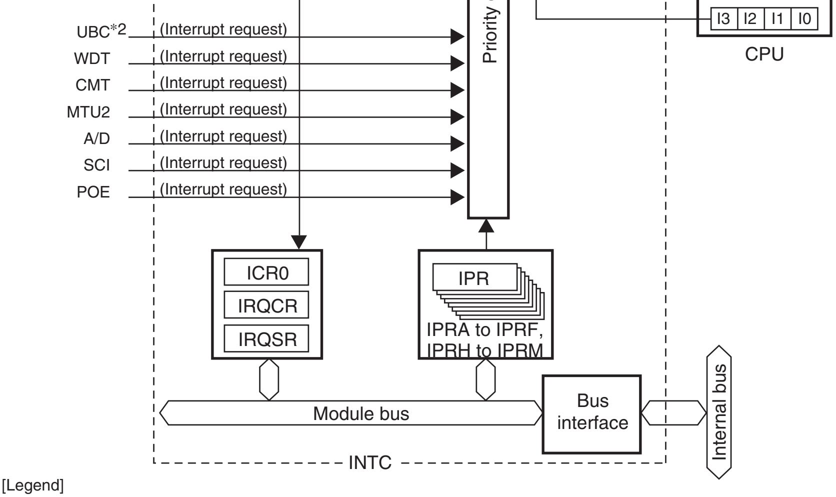
2. HI7000

   This instruction is in part allocated to the delay slot within the OS, which may cause illegal instruction exception handling in this LSI.

3. Others

   The slot illegal instruction exception handling may be generated in this LSI in a case instruction is described in assembler or when the middleware of the object is introdu

Note that a check-up program (checker) to pick up this instruction is available on our w Download and utilize this checker as needed.



[Legend]

UBC:	User break controller	ICR0:	Interrupt control register 0
WDT:	Watchdog timer	IRQCR:	IRQ control register
CMT:	Compare match timer	IRQSR:	IRQ status register
SCI:	Serial communication interface	IPRA to IPRF,	
MTU2:	Multi-function timer pulse unit 2	IPRH to IPRM:	Interrupt priority registers A to F and H to M
A/D:	A/D converter	SR:	Status register
POE:	Port output enable		

Note: *1 Supported only by the SH7125.

*2 The 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions are not supporte

Figure 6.1 Block Diagram of INTC

Interrupt request output pin	IRQOUT	Output	Output of notification signal wh interrupt has occurred

IRQ status register	IRQSR	R/W	H'Fx00	H'FFFFE904	8, 1
Interrupt priority register A	IPRA	R/W	H'0000	H'FFFFE906	8, 1
Interrupt priority register B	IPRB	R/W	H'0000	H'FFFFE908	8, 1
Interrupt priority register C	IPRC	R/W	H'0000	H'FFFFE980	16
Interrupt priority register D	IPRD	R/W	H'0000	H'FFFFE982	16
Interrupt priority register E	IPRE	R/W	H'0000	H'FFFFE984	16
Interrupt priority register F	IPRF	R/W	H'0000	H'FFFFE986	16
Interrupt priority register H	IPRH	R/W	H'0000	H'FFFFE98A	16
Interrupt priority register I	IPRI	R/W	H'0000	H'FFFFE98C	16
Interrupt priority register J	IPRJ	R/W	H'0000	H'FFFFE98E	16
Interrupt priority register K	IPRK	R/W	H'0000	H'FFFFE990	16
Interrupt priority register L	IPRL	R/W	H'0000	H'FFFFE992	16
Interrupt priority register M	IPRM	R/W	H'0000	H'FFFFE994	16

Bit	Bit Name	Initial Value	R/W	Description
15	NMIL	*	R	NMI Input Level Indicates the state of the signal input to the N This bit can be read to determine the NMI pin bit cannot be modified. 0: State of the NMI input is low 1: State of the NMI input is high
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
8	NMIE	0	R/W	NMI Edge Select 0: Interrupt request is detected on the falling e NMI input 1: Interrupt request is detected on the rising e NMI input
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.

Bit	Bit Name	Value	R/W	Description
15 to 8	—	All 0	R/W	Reserved These bits are always read as 0. The write va should always be 0.
7	IRQ31S	0	R/W	IRQ3 Sense Select
6	IRQ30S	0	R/W	Set the interrupt request detection mode for p 00: Interrupt request is detected at the low lev IRQ3 01: Interrupt request is detected at the falling pin IRQ3 10: Interrupt request is detected at the rising e pin IRQ3 11: Interrupt request is detected at both the fa rising edges of pin IRQ3
5	IRQ21S	0	R/W	IRQ2 Sense Select
4	IRQ20S	0	R/W	Set the interrupt request detection mode for p 00: Interrupt request is detected at the low lev IRQ2 01: Interrupt request is detected at the falling pin IRQ2 10: Interrupt request is detected at the rising e pin IRQ2 11: Interrupt request is detected at both the fa rising edges of pin IRQ2

				11: Interrupt request is detected at both the rising edges of pin IRQ1
1	IRQ01S	0	R/W	IRQ0 Sense Select (SH7125)
0	IRQ00S	0	R/W	Set the interrupt request detection mode for 00: Interrupt request is detected at the low le IRQ0 01: Interrupt request is detected at the fallin pin IRQ0 10: Interrupt request is detected at the rising pin IRQ0 11: Interrupt request is detected at both the rising edges of pin IRQ0 Reserved (SH7124) These bits are always read as 0. The write v should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 1	R	Reserved These bits are always read as 1.
11	IRQ3L	*	R	Indicates the state of pin IRQ3. 0: State of pin IRQ3 is low 1: State of pin IRQ3 is high
10	IRQ2L	*	R	Indicates the state of pin IRQ2. 0: State of pin IRQ2 is low 1: State of pin IRQ2 is high
9	IRQ1L	*	R	Indicates the state of pin IRQ1. 0: State of pin IRQ1 is low 1: State of pin IRQ1 is high
8	IRQ0L	*	R	Indicates the state of pin IRQ0. 0: State of pin IRQ0 is low 1: State of pin IRQ0 is high
7to 4	—	All 0	—	Reserved These bits are always read as 0. The write va should always be 0.

- When edge detection mode is selected

0: An IRQ3 interrupt has not been detected

[Clearing conditions]

— Writing 0 after reading IRQ3F = 1

— Accepting an IRQ3 interrupt

1: An IRQ3 interrupt request has been detec

[Setting condition]

Detecting the specified edge of pin IRQ3

				• When edge detection mode is selected 0: An IRQ2 interrupt has not been detected [Clearing conditions] — Writing 0 after reading IRQ2F = 1 — Accepting an IRQ2 interrupt 1: An IRQ2 interrupt request has been detect [Setting condition] Detecting the specified edge of pin IRQ2
1	IRQ1F	0	R/W	Indicates the status of an IRQ1 interrupt requ • When level detection mode is selected 0: An IRQ1 interrupt has not been detected [Clearing condition] Driving pin IRQ1 high 1: An IRQ1 interrupt has been detected [Setting condition] Driving pin IRQ1 low • When edge detection mode is selected 0: An IRQ1 interrupt has not been detected [Clearing conditions] — Writing 0 after reading IRQ1F = 1 — Accepting an IRQ1 interrupt 1: An IRQ1 interrupt request has been detect [Setting condition] Detecting the specified edge of pin IRQ1

- When edge detection mode is selected

0: An IRQ0 interrupt has not been detected

[Clearing conditions]

— Writing 0 after reading IRQ0F = 1

— Accepting an IRQ0 interrupt

1: An IRQ0 interrupt request has been detec

[Setting condition]

Detecting the specified edge of pin IRQ0

Note: * The initial value is 1 when the level on the corresponding IRQ pin is high, and the level on the pin is low.

6.3.4 Interrupt Priority Registers A to F and H to M (IPRA to IPRF and IPRH IPRM)

Interrupt priority registers are twelve 16-bit readable/writable registers that set priority l 0 to 15 for interrupts except NMI. For the correspondence between interrupt request sou IPR, refer to table 6.3. Each of the corresponding interrupt priority ranks are established a value from H'0 to H'F in each of the four-bit groups 15 to 12, 11 to 8, 7 to 4 and 3 to 0 bits that are not assigned should be set H'0 (B'0000).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	IPR[15:12]				IPR[11:8]				IPR[7:4]				IPR[3	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

				0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
11 to 8	IPR[11:8]	0000	R/W	Set priority levels for the corresponding inter source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)

				0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
3 to 0	IPR[3:0]	0000	R/W	Set priority levels for the corresponding inte source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)

Note: Name in the tables above is represented by a general name. Name in the list of r on the other hand, represented by a module name.

handler, the interrupt mask level bits (I3 to I0) in the status register (SR) are set to level 1

IRQ3 to IRQ0 Interrupts: IRQ interrupts are requested by input from pins IRQ0 to IRQ the IRQ sense select bits (IRQ31S, IRQ30S to IRQ01S, and IRQ00S) in the IRQ control (IRQCR) to select the detection mode from low level detection, falling edge detection, ris detection, and both edge detection for each pin. The priority level can be set from 0 to 15 pin using the interrupt priority register A (IPRA).

In the case that the low level detection is selected, an interrupt request signal is sent to the while the IRQ pin is driven low. The interrupt request signal stops to be sent to the INTC IRQ pin becomes high. It is possible to confirm that an interrupt is requested by reading t flags (IRQ3F to IRQ0F) in the IRQ status register (IRQSR).

In the case that the edge detection is selected, an interrupt request signal is sent to the INT the following change on the IRQ pin is detected: from high to low in falling edge detectio from low to high in rising edge detection mode, and from low to high or from high to low edge detection mode. The IRQ interrupt request by detecting the change on the pin is held interrupt request is accepted. It is possible to confirm that an IRQ interrupt request has be detected by reading the IRQ flags (IRQ3F to IRQ0F) in the IRQ status register (IRQSR). interrupt request by detecting the change on the pin can be withdrawn by writing 0 to an I after reading 1.

In the IRQ interrupt exception handling, the interrupt mask bits (I3 to I0) in the status reg (SR) are set to the priority level value of the accepted IRQ interrupt. Figure 6.2 shows the diagram of the IRQ3 to IRQ0 interrupts.

Figure 6.2 Block Diagram of IRQ3 to IRQ0 Interrupts Control

6.4.2 On-Chip Peripheral Module Interrupts

On-chip peripheral module interrupts are interrupts generated by the following on-chip p modules.

Since a different interrupt vector is allocated to each interrupt source, the exception hand routine does not have to decide which interrupt has occurred. Priority levels between 0 a be allocated to individual on-chip peripheral modules in interrupt priority registers C to M (IPRC to IPRF and IPRH to IPRM). On-chip peripheral module interrupt exception h sets the interrupt mask level bits (I3 to I0) in the status register (SR) to the priority level the on-chip peripheral module interrupt that was accepted.

6.4.3 User Break Interrupt*

A user break interrupt has a priority level of 15, and occurs when the break condition set user break controller (UBC) is satisfied. User break interrupt requests are detected by ed held until accepted. User break interrupt exception handling sets the interrupt mask leve to I0) in the status register (SR) to level 15. For more details on the user break interrupt, section 7, User Break Controller (UBC).

Note: * The user break interrupt is not generated on the 32 Kbyte (SH71251A and SH and 16 Kbyte (SH71250A and SH71240A) versions.

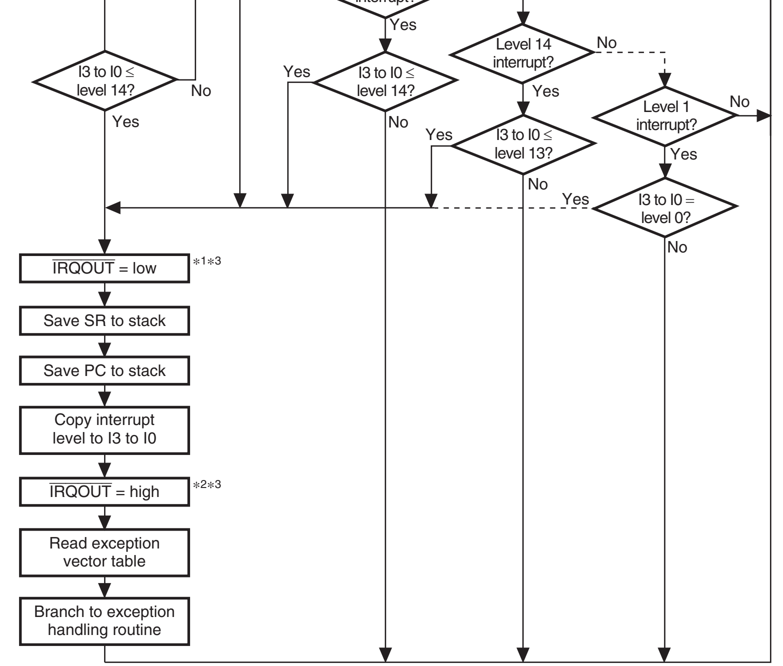
IRQ interrupts and on-chip peripheral module interrupt priorities can be set freely betwee
and 15 for each pin or module by setting interrupt priority registers A to F and H to M (IP
IPRF and IPRH to IPRM). However, when interrupt sources whose priority levels are allo
with the same IPR are requested, the interrupt of the smaller vector number has priority. T
priority cannot be changed. Priority levels of IRQ interrupts and on-chip peripheral modu
interrupts are initialized to level 0 at a power-on reset. If the same priority level is allocat
or more interrupt sources and interrupts from those sources occur simultaneously, they ar
processed by the default priority order shown in table 6.3.

MTU2_0	TGIA_0	88	H'00000160	IPRD15 to IPRD12
	TGIB_0	89	H'00000164	
	TGIC_0	90	H'00000168	
	TGID_0	91	H'0000016C	
	TCIV_0	92	H'00000170	IPRD11 to IPRD8
	TGIE_0	93	H'00000174	
	TGIF_0	94	H'00000178	
MTU2_1	TGIA_1	96	H'00000180	IPRD7 to IPRD4
	TGIB_1	97	H'00000184	
	TCIV_1	100	H'00000190	IPRD3 to IPRD0
	TCIU_1	101	H'00000194	
MTU2_2	TGIA_2	104	H'000001A0	IPRE15 to IPRE12
	TGIB_2	105	H'000001A4	
	TCIV_2	108	H'000001B0	IPRE11 to IPRE8
	TCIU_2	109	H'000001B4	
MTU2_3	TGIA_3	112	H'000001C0	IPRE7 to IPRE4
	TGIB_3	113	H'000001C4	
	TGIC_3	114	H'000001C8	
	TGID_3	115	H'000001CC	
	TCIV_3	116	H'000001D0	IPRE3 to IPRE0

	TGIW_5	130	H'00000208	
POE (MTU2)	OEI1	132	H'00000210	IPRF3 to IPRF0
	OEI3	133	H'00000214	
CMT_0	CMI_0	184	H'000002E0	IPRJ15 to IPRJ12
CMT_1	CMI_1	188	H'000002F0	IPRJ11 to IPRJ8
WDT	ITI	196	H'00000310	IPRJ3 to IPRJ0
A/D_0 and A/D_1	ADI_0	200	H'00000320	IPRK15 to IPRK12
	ADI_1	201	H'00000324	
SCI_0	ERI_0	216	H'00000360	IPRL15 to IPRL12
	RXI_0	217	H'00000364	
	TXI_0	218	H'00000368	
	TEI_0	219	H'0000036C	
SCI_1	ERI_1	220	H'00000370	IPRL11 to IPRL8
	RXI_1	221	H'00000374	
	TXI_1	222	H'00000378	
	TEI_1	223	H'0000037C	
SCI_2	ERI_2	224	H'00000380	IPRL7 to IPRL4
	RXI_2	225	H'00000384	
	TXI_2	226	H'00000388	
	TEI_2	227	H'0000038C	

are ignored*. If interrupts that have the same priority level or interrupts within a sam occur simultaneously, the interrupt with the highest priority is selected according to priority shown in table 6.3.

3. The interrupt controller compares the priority level of the selected interrupt request interrupt mask bits (I3 to I0) in the status register (SR) of the CPU. If the priority lev selected request is equal to or less than the level set in bits I3 to I0, the request is ign the priority level of the selected request is higher than the level in bits I3 to I0, the in controller accepts the request and sends an interrupt request signal to the CPU.
4. When the interrupt controller accepts an interrupt, a low level is output from the $\overline{\text{IRQ}}$
5. The CPU detects the interrupt request sent from the interrupt controller in the decod an instruction to be executed. Instead of executing the decoded instruction, the CPU interrupt exception handling.
6. SR and PC are saved onto the stack.
7. The priority level of the accepted interrupt is copied to bits (I3 to I0) in SR.
8. When the accepted interrupt is sensed by level or is from an on-chip peripheral mod level is output from the $\overline{\text{IRQOUT}}$ pin. When the accepted interrupt is sensed by edge level is output from the $\overline{\text{IRQOUT}}$ pin at the moment when the CPU starts interrupt e processing instead of instruction execution as noted in 5. above. However, if the inte controller accepts an interrupt with a higher priority than the interrupt just to be acce $\overline{\text{IRQOUT}}$ pin holds low level.
9. The CPU reads the start address of the exception handling routine from the exceptio table for the accepted interrupt, branches to that address, and starts executing the pro This branch is not a delayed branch.



Notes: I3 to I0 are interrupt mask bits in the status register (SR) of the CPU

1. $\overline{\text{IRQOUT}}$ is the same signal as the interrupt request signal to the CPU (see figure 6.1). Therefore, $\overline{\text{IRQOUT}}$ is output when the request priority level is higher than the level in bits I3–I0 of SR.
2. When the accepted interrupt is sensed by edge, a high level is output from the $\overline{\text{IRQOUT}}$ pin at the moment wh the CPU starts interrupt exception processing instead of instruction execution (namely, before saving SR to sta However, if the interrupt controller accepts an interrupt with a higher priority than the interrupt just to be accept and has output an interrupt request to the CPU, the $\overline{\text{IRQOUT}}$ pin holds low level.
3. The $\overline{\text{IRQOUT}}$ pin change timing depends on a frequency dividing ratio between the internal (Iϕ) and bus (Bϕ) clocks. This flowchart shows that the frequency dividing ratios of the internal (Iϕ) and bus (Bϕ) clocks are the s

Figure 6.3 Interrupt Sequence Flowchart

Notes: 1. PC is the start address of the next instruction (instruction at the return address) after the e
instruction.
2. Always make sure that SP is a multiple of 4

Figure 6.4 Stack after Interrupt Exception Handling

6.7 Interrupt Response Time

Table 6.4 lists the interrupt response time, which is the time from the occurrence of an int request until the interrupt exception handling starts and fetching of the first instruction of interrupt handling routine begins.

					(X = 7 × Icyc + m3 + m4). interrupt-mas instruction fo however, the be even long
Time from start of interrupt exception handling until fetch of first instruction of exception handling routine starts		8 × Icyc + m1 + m2 + m3	8 × Icyc + m1 + m2 + m3	8 × Icyc + m1 + m2 + m3	Performs the and SR, and address fetch
Interrupt response time	Total:	9 × Icyc + 2 × Pcyc + m1 + m2 + m3 + X	9 × Icyc + 1 × Pcyc + m1 + m2 + m3 + X	9 × Icyc + 2 × Pcyc + m1 + m2 + m3 + X	
	Minimum*:	12 × Icyc + 2 × Pcyc	12 × Icyc + 1 × Pcyc	12 × Icyc + 2 × Pcyc	SR, PC, and are all in on-c
	Maximum:	16 × Icyc + 2 × Pcyc + 2 × (m1 + m2 + m3) + m4	16 × Icyc + 1 × Pcyc + 2 (m1 + m2 + m3) + m4	16 × Icyc + 2 × Pcyc + 2 (m1 + m2 + m3) + m4	

Notes: * In the case that m1 = m2 = m3 = m4 = 1 × Icyc.

m1 to m4 are the number of cycles needed for the following memory accesse

m1: SR save (longword write)

m2: PC save (longword write)

m3: Vector address read (longword read)

m4: Fetch first instruction of interrupt service routine

If NMI is not used, connect it to V_{CC} via a resistor and fix it high.

The UBC has the following features:

1. The following break comparison conditions can be set.

   Number of break channels: two channels (channels A and B)

   User break can be requested as either the independent or sequential condition on cha and B (sequential break setting: channel A and then channel B match with break con but not in the same bus cycle).

- Address

  Comparison bits are maskable in 1-bit units.

  One of the two address buses (L-bus address (LAB) and I-bus address (IAB)) can be

- Data

  32-bit maskable.

  One of the two data buses (L-bus data (LDB) and I-bus data (IDB)) can be selected.

- Bus cycle

  Instruction fetch or data access

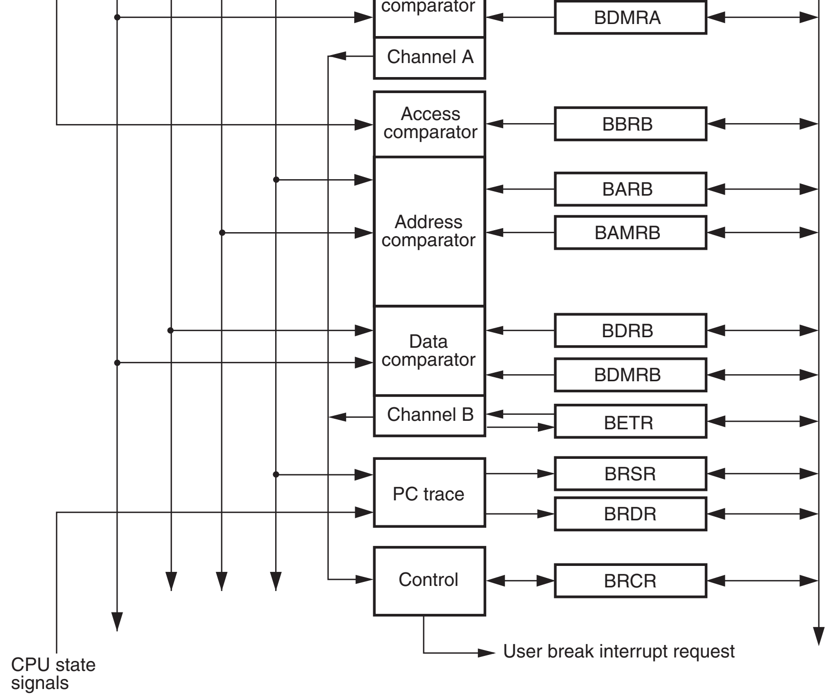
- Read/write

- Operand size

  Byte, word, and longword

2. A user-designed user-break condition interrupt exception processing routine can be r
3. In an instruction fetch cycle, it can be selected that a user-break is set before or after instruction is executed.
4. Maximum repeat times for the break condition (only for channel B): 2^{12} – 1 times.
5. Four pairs of branch source/destination buffers.

Note: * The user break controller is not supported on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.



[Legend]

BBRA:	Break bus cycle register A
BARA:	Break address register A
BAMRA:	Break address mask register A
BDRA:	Break data register A
BDMRA:	Break data mask register A
BBRB:	Break bus cycle register B
BARB:	Break address register B
BAMRB:	Break address mask register B
BDRB:	Break data register B
BDMRB:	Break data mask register B
BETR:	Execution times break register
BRSR:	Branch source register
BRDR:	Branch destination register
BRCR:	Break control register

Figure 7.1 Block Diagram of UBC

Break bus cycle register A	BBRA	R/W	H'0000	H'FFFFF308	16
Break data register A	BDRA	R/W	H'00000000	H'FFFFF310	32
Break data mask register A	BDMRA	R/W	H'00000000	H'FFFFF314	32
Break address register B	BARB	R/W	H'00000000	H'FFFFF320	32
Break address mask register B	BAMRB	R/W	H'00000000	H'FFFFF324	32
Break bus cycle register B	BBRB	R/W	H'0000	H'FFFFF328	16
Break data register B	BDRB	R/W	H'00000000	H'FFFFF330	32
Break data mask register B	BDMRB	R/W	H'00000000	H'FFFFF334	32
Break control register	BRCR	R/W	H'00000000	H'FFFFF3C0	32
Branch source register	BRSR	R	H'0xxxxxxx	H'FFFFF3D0	32
Branch destination register	BRDR	R	H'0xxxxxxx	H'FFFFF3D4	32
Execution times break register	BETR	R/W	H'0000	H'FFFFF3DC	16

Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BAA31 to BAA 0	All 0	R/W	Break Address A Store the address on the LAB or IAB specifying conditions of channel A.

7.2.2 Break Address Mask Register A (BAMRA)

BAMRA is a 32-bit readable/writable register. BAMRA specifies bits masked in the brea specified by BARA.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	BAMA31	BAMA30	BAMA29	BAMA28	BAMA27	BAMA26	BAMA25	BAMA24	BAMA23	BAMA22	BAMA21	BAMA20	BAMA19	BAMA18
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	BAMA15	BAMA14	BAMA13	BAMA12	BAMA11	BAMA10	BAMA9	BAMA8	BAMA7	BAMA6	BAMA5	BAMA4	BAMA3	BAMA2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7.2.3 Break Bus Cycle Register A (BBRA)

BBRA is a 16-bit readable/writable register, which specifies (1) bus master for I bus cyc bus cycle or I bus cycle, (3) instruction fetch or data access, (4) read or write, and (5) op in the break conditions of channel A.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	CPA[2:0]			CDA[1:0]		IDA[1:0]		RWA[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write val always be 0.
10 to 8	CPA[2:0]	000	R/W	Bus Master Select A for I Bus Select the bus master when the I bus is select bus cycle of the channel A break condition. Ho when the L bus is selected as the bus cycle, th of the CPA2 to CPA0 bits is disabled. 000: Condition comparison is not performed xx1: The CPU cycle is included in the break co x1x: Setting prohibited 1xx: Setting prohibited

				Select the instruction fetch cycle or data access the bus cycle of the channel A break condition. 00: Condition comparison is not performed 01: The break condition is the instruction fetch c 10: The break condition is the data access cycl 11: The break condition is the instruction fetch c data access cycle
3, 2	RWA[1:0]	00	R/W	Read/Write Select A Select the read cycle or write cycle as the bus c the channel A break condition. 00: Condition comparison is not performed 01: The break condition is the read cycle 10: The break condition is the write cycle 11: The break condition is the read cycle or wri
1, 0	SZA[1:0]	00	R/W	Operand Size Select A Select the operand size of the bus cycle for the A break condition. 00: The break condition does not include opera 01: The break condition is byte access 10: The break condition is word access 11: The break condition is longword access Note: When specifying the operand size, spe size which matches the address boun

[Legend]

x: Don't care.

Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BDA31 to BDA0	All 0	R/W	Break Data Bit A Stores data, which specifies a break condition channel A. If the I bus is selected in BBRA, the break dat set in BDA31 to BDA0. If the L bus is selected in BBRA, the break dat is set in BDA31 to BDA0.

Notes: 1. Specify an operand size when including the value of the data bus in the breal

2. When the byte size is selected as a break condition, the same byte data mus bits 15 to 8 and 7 to 0 in BDRA as the break data.

Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BDMA31 to BDMA 0	All 0	R/W	Break Data Mask A Specifies bits masked in the break data of char specified by BDRA (BDA31 to BDA0). 0: Break data BDAn of channel A is included in break condition 1: Break data BDAn of channel A is masked an included in the break condition Note: n = 31 to 0

Notes: 1. Specify an operand size when including the value of the data bus in the break

2. When the byte size is selected as a break condition, the same byte data must bits 15 to 8 and 7 to 0 in BDMRA as the break mask data in BDRA.

	BAB15	BAB14	BAB13	BAB12	BAB11	BAB10	BAB9	BAB8	BAB7	BAB6	BAB5	BAB4	BAB3	BAB2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BAB31 to BAB 0	All 0	R/W	Break Address B Stores an address, which specifies a break co channel B. If the I bus or L bus is selected in BBRB, an IA address is set in BAB31 to BAB0.

Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BAMB31 to BAMB 0	All 0	R/W	Break Address Mask B Specifies bits masked in the break address of c specified by BARB (BAB31 to BAB0). 0: Break address BABn of channel B is include break condition 1: Break address BABn of channel B is masked not included in the break condition Note: n = 31 to 0

Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BDB31 to BDB0	All 0	R/W	Break Data Bit B Stores data which specifies a break condition B. If the I bus is selected in BBRB, the break data set in BDB31 to BDB0. If the L bus is selected in BBRB, the break dat is set in BDB31 to BDB0.

Notes: 1. Specify an operand size when including the value of the data bus in the break

2. When the byte size is selected as a break condition, the same byte data mus bits 15 to 8 and 7 to 0 in BDRB as the break data.

Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BDMB31 to BDMB 0	All 0	R/W	Break Data Mask B Specifies bits masked in the break data of char specified by BDRB (BDB31 to BDB0). 0: Break data BDBn of channel B is included in break condition 1: Break data BDBn of channel B is masked an included in the break condition Note: n = 31 to 0

Notes: 1. Specify an operand size when including the value of the data bus in the break

2. When the byte size is selected as a break condition, the same byte data must bits 15 to 8 and 7 to 0 in BDMRB as the break mask data in BDRB.

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
10 to 8	CPB[2:0]	000	R/W	Bus Master Select B for I Bus Select the bus master when the I bus is selec the bus cycle of the channel B break conditio However, when the L bus is selected as the the setting of the CPB2 to CPB0 bits is disab 000: Condition comparison is not performed xx1: The CPU cycle is included in the break c x1x: Setting prohibited 1xx: Setting prohibited
7, 6	CDB[1:0]	00	R/W	L Bus Cycle/I Bus Cycle Select B Select the L bus cycle or I bus cycle as the b of the channel B break condition. 00: Condition comparison is not performed 01: The break condition is the L bus cycle 10: The break condition is the I bus cycle 11: The break condition is the L bus cycle

3, 2	RWB[1:0]	00	R/W	Read/Write Select B Select the read cycle or write cycle as the bus the channel B break condition. 00: Condition comparison is not performed 01: The break condition is the read cycle 10: The break condition is the write cycle 11: The break condition is the read cycle or w
1, 0	SZB[1:0]	0	R/W	Operand Size Select B Select the operand size of the bus cycle for th channel B break condition. 00: The break condition does not include oper 01: The break condition is byte access 10: The break condition is word access 11: The break condition is longword access Note: When specifying the operand size, sp size which matches the address bour

[Legend]

x: Don't care.

5. Enable PC trace.
6. Specify whether to request the user break interrupt when channels A and B match wi comparison conditions.

BRCR is a 32-bit readable/writable register that has break conditions match flags and bi setting a variety of break conditions.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	-	-	-	-	-	-	-	-	-	-	-	-	UBIDB	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	SCM FCA	SCM FCB	SCM FDA	SCM FDB	PCTE	PCBA	-	-	DBEA	PCBB	DBEB	-	SEQ	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
19	UBIDB	0	R/W	User Break Disable B Enables or disables the user break interrupt when the channel B break conditions are sat 0: User break interrupt request is enabled wh conditions are satisfied 1: User break interrupt request is disabled wh conditions are satisfied

				1: User break interrupt request is disabled wh conditions are satisfied
16	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
15	SCMFCA	0	R/W	L Bus Cycle Condition Match Flag A When the L bus cycle condition in the break c set for channel A is satisfied, this flag is set to order to clear this flag, write 0 into this bit. 0: The L bus cycle condition for channel A do match 1: The L bus cycle condition for channel A ma
14	SCMFCB	0	R/W	L Bus Cycle Condition Match Flag B When the L bus cycle condition in the break c set for channel B is satisfied, this flag is set to order to clear this flag, write 0 into this bit. 0: The L bus cycle condition for channel B do match 1: The L bus cycle condition for channel B ma
13	SCMFDA	0	R/W	I Bus Cycle Condition Match Flag A When the I bus cycle condition in the break c set for channel A is satisfied, this flag is set to order to clear this flag, write 0 into this bit. 0: The I bus cycle condition for channel A doe match 1: The I bus cycle condition for channel A mat

				0: Disables PC trace 1: Enables PC trace
10	PCBA	0	R/W	PC Break Select A Selects the break timing of the instruction fet for channel A as before or after instruction ex 0: PC break of channel A is set before instruc execution 1: PC break of channel A is set after instructi execution
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
7	DBEA	0	R/W	Data Break Enable A Selects whether or not the data bus conditior included in the break condition of channel A. 0: No data bus condition is included in the co channel A 1: The data bus condition is included in the c channel A
6	PCBB	0	R/W	PC Break Select B Selects the break timing of the instruction fet for channel B as before or after instruction ex 0: PC break of channel B is set before instruc execution 1: PC break of channel B is set after instructi execution

				This bit is always read as 0. The write value s always be 0.
3	SEQ	0	R/W	Sequence Condition Select Selects two conditions of channels A and B as independent or sequential conditions. 0: Channels A and B are compared under inde conditions 1: Channels A and B are compared under sec conditions (channel A, then channel B)
2, 1	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
0	ETBE	0	R/W	Number of Execution Times Break Enable Enables the execution-times break condition c channel B. If this bit is 1 (break enable), a use requested when the number of break conditio matches with the number of execution times t specified by BETR. 0: The execution-times break condition is disa channel B 1: The execution-times break condition is ena channel B

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
11 to 0	BET[11:0]	All 0	R/W	Number of Execution Times

R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	BSA15	BSA14	BSA13	BSA12	BSA11	BSA10	BSA9	BSA8	BSA7	BSA6	BSA5	BSA4	BSA3	BSA2
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SVF	0	R	BRSR Valid Flag Indicates whether the branch source address This flag bit is set to 1 when a branch occurs. is cleared to 0 when BRSR is read, the setting enable PC trace is made, or BRSR is initialize power-on reset. 0: The value of BRSR register is invalid 1: The value of BRSR register is valid
30 to 28	—	All 0	R	Reserved These bits are always read as 0. The write val should always be 0.
27 to 0	BSA27 to BSA0	Undefined	R	Branch Source Address Store bits 27 to 0 of the branch source addres

R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	BDA15	BDA14	BDA13	BDA12	BDA11	BDA10	BDA9	BDA8	BDA7	BDA6	BDA5	BDA4	BDA3	BDA2
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	DVF	0	R	BRDR Valid Flag Indicates whether a branch destination addre stored. This flag bit is set to 1 when a branch This flag is cleared to 0 when BRDR is read, setting to enable PC trace is made, or BRDF initialized by a power-on reset. 0: The value of BRDR register is invalid 1: The value of BRDR register is valid
30 to 28	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
27 to 0	BDA27 to BDA0	Undefined	R	Branch Destination Address Store bits 27 to 0 of the branch destination a

registers (BBRA or BBRB). Three groups of BBRA or BBRB (L bus cycle/I bus cycl instruction fetch/data access select, and read/write select) are each set. No user break generated if even one of these groups is set with B'00. The respective conditions are s bits of the break control register (BRCR). Make sure to set all registers related to brea setting BBRA or BBRB.

2. When the break conditions are satisfied, the UBC sends a user break interrupt request CPU and sets the L bus condition match flag (SCMFCA or SCMFCB) and the I bus c match flag (SCMFDA or SCMFDB) for the appropriate channel.
3. The appropriate condition match flags (SCMFCA, SCMFDA, SCMFCB, and SCMFI be used to check if the set conditions match or not. The matching of the conditions se but they are not reset. Before using them again, 0 must first be written to them and the flags.
4. There may be an occasion when a break condition match occurs both in channels A a around the same time. In this case, the flags for both conditions matches will be set e though only one user-break interrupt request is issued to the CPU.
5. When selecting the I bus as the break condition, note the following:
   - The CPU is connected to the I bus. The UBC monitors bus cycles generated by al masters that are selected by the CPA2 to CPA0 bits in BBRA or the CPB2 to CPB BBRB, and compares the condition match.
   - I bus cycles (including read fill cycles) resulting from instruction fetches on the L the CPU are defined as instruction fetch cycles on the I bus, while other bus cycle defined as data access cycles.
   - If a break condition is specified for the I bus, even when the condition matches in cycle resulting from an instruction executed by the CPU, at which instruction the break is to be accepted cannot be clearly defined.

has been fetched and will be executed. This means this feature cannot be used on ins fetched by overrun (instructions fetched at a branch or during an interrupt transition, be executed). When this kind of break is set for the delay slot of a delayed branch ins the break is generated prior to execution of the delayed branch instruction.

Note: If a branch does not occur at a delay condition branch instruction, the subsec instruction is not recognized as a delay slot.

3. When the condition is specified to be occur after execution, the instruction set with t condition is executed and then the break is generated prior to the execution of the ne instruction. As with pre-execution breaks, this cannot be used with overrun fetch ins When this kind of break is set for a delayed branch instruction and its delay slot, a br generated until the first instruction at the branch destination.
4. When an instruction fetch cycle is set, the break data register (BDRA or BDRB) is ig Therefore, break data cannot be set for the break of the instruction fetch cycle.
5. If the I bus is set for a break of an instruction fetch cycle, the condition is determinec instruction fetch cycles on the I bus. For details, see 5 in section 7.3.1, Flow of the U Operation.

7.3.3 Break on Data Access Cycle

1. If the L bus is specified as a break condition for data access break, condition compar performed for the address (and data) accessed by the executed instructions, and a bre if the condition is satisfied. If the I bus is specified as a break condition, condition co is performed for the addresses (and data) of the data access cycles that are issued on by all bus masters including the CPU, and a break occurs if the condition is satisfied details on the CPU bus cycles issued on the I bus, see 5 in section 7.3.1, Flow of the Break Operation.
2. The relationship between the data access cycle address and the comparison conditior operand size is listed in table 7.2.

Longword access at H'00001000

Word access at H'00001002

Byte access at H'00001003

3. When the data value is included in the break conditions:

   When the data value is included in the break conditions, either longword, word, or by specified as the operand size of the break bus cycle register (BBRA or BBRB). When values are included in break conditions, a break is generated when the address conditi data conditions both match. To specify byte data for this case, set the same data in two bits 15 to 8 and bits 7 to 0 of the break data register (BDRA or BDRB) and break data register (BDMRA or BDMRB). When word or byte is set, bits 31 to 16 of BDRA or B and BDMRA or BDMRB are ignored.

4. If the L bus is selected, a break occurs on ending execution of the instruction that mat break condition, and immediately before the next instruction is executed. However, w is also specified as the break condition, the break may occur on ending execution of th instruction following the instruction that matches the break condition. If the I bus is se the instruction at which the break will occur cannot be determined. When this kind of occurs at a delayed branch instruction or its delay slot, the break may not actually take until the first instruction at the branch destination.

condition can be also specified. For example, when the execution times break condit
specified, the break condition is satisfied when a channel B condition matches with
H'0001 after a channel A condition has matched.

7.3.5 Value of Saved Program Counter

When a break occurs, the address of the instruction from where execution is to be resum saved in the stack, and the exception handling state is entered. If the L bus is specified a condition, the instruction at which the break should occur can be clearly determined (ex when data is included in the break condition). If the I bus is specified as a break conditio instruction at which the break should occur cannot be clearly determined.

1. When instruction fetch (before instruction execution) is specified as a break conditio

   The address of the instruction that matched the break condition is saved in the stack. instruction that matched the condition is not executed, and the break occurs before it when a delay slot instruction matches the condition, the address of the delayed branc instruction is saved in the stack.
2. When instruction fetch (after instruction execution) is specified as a break condition

   The address of the instruction following the instruction that matched the break condi saved in the stack. The instruction that matches the condition is executed, and the br before the next instruction is executed. However, when a delayed branch instruction slot matches the condition, these instructions are executed, and the branch destinatio is saved in the stack.
3. When data access (address only) is specified as a break condition:

   The address of the instruction immediately after the instruction that matched the brea condition is saved in the stack. The instruction that matches the condition is execute break occurs before the next instruction is executed. However when a delay slot instr matches the condition, the branch destination address is saved in the stack.

1. Setting PCTE in BRCR to 1 enables PC traces. When branch (branch instruction, and exception) is generated, the branch source address and branch destination address are BRSR and BRDR, respectively.
2. The values stored in BRSR and BRDR are as given below due to the kind of branch.
   — If a branch occurs due to a branch instruction, the address of the branch instructio in BRSR and the address of the branch destination instruction is saved in BRDR.
   — If a branch occurs due to an interrupt or exception, the value saved in stack due to exception occurrence is saved in BRSR and the start address of the exception hand routine is saved in BRDR.
3. BRSR and BRDR have four pairs of queue structures. The top of queues is read first v address stored in the PC trace register is read. BRSR and BRDR share the read pointe BRSR and BRDR in order, the queue only shifts after BRDR is read. After switching PCTE bit (in BRCR) off and on, the values in the queues are invalid.

Specified conditions: Channel A/channel B independent mode

<Channel A>

Address: H'00000404, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (after instruction execution)/read (operand size is
included in the condition)

<Channel B>

Address: H'00008010, Address mask: H'00000006

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read (operand size
included in the condition)

A user break occurs after an instruction of address H'00000404 is executed or before
instructions of addresses H'00008010 to H'00008016 are executed.

(Example 1-2)

- Register specifications

  BARA = H'00037226, BAMRA = H'00000000, BBRA = H'0056, BDRA = H'00000
  BDMRA = H'00000000, BARB = H'0003722E, BAMRB = H'00000000, BBRB = H
  BDRB = H'00000000, BDMRB = H'00000000, BRCR = H'00000008

  Specified conditions: Channel A/channel B sequential mode

  <Channel A>

  Address: H'00037226, Address mask: H'00000000

  Data: H'00000000, Data mask: H'00000000

  Bus cycle: L bus/instruction fetch (before instruction execution)/read/word

BARA = H'00027128, BAMRA = H'00000000, BBRA = H'005A, BDRA = H'00000
BDMRA = H'00000000, BARB = H'00031415, BAMRB = H'00000000, BBRB = H'0
BDRB = H'00000000, BDMRB = H'00000000, BRCR = H'00000000

Specified conditions: Channel A/channel B independent mode

<Channel A>

Address: H'00027128, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/write/word

<Channel B>

Address: H'00031415, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read (operand size i included in the condition)

On channel A, no user break occurs since instruction fetch is not a write cycle. On cha no user break occurs since instruction fetch is performed for an even address.

(Example 1-4)

- Register specifications

  BARA = H'00037226, BAMRA = H'00000000, BBRA = H'005A, BDRA = H'00000
  BDMRA = H'00000000, BARB = H'0003722E, BAMRB = H'00000000, BBRB = H'0
  BDRB = H'00000000, BDMRB = H'00000000, BRCR = H'00000008

  Specified conditions: Channel A/channel B sequential mode

  <Channel A>

  Address: H'00037226, Address mask: H'00000000

  Data: H'00000000, Data mask: H'00000000

  Bus cycle: L bus/instruction fetch (before instruction execution)/write/word

BARA = H'00000500, BAMRA = H'00000000, BBRA = H'0057, BDRA = H'0000
BDMRA = H'00000000, BARB = H'00001000, BAMRB = H'00000000, BBRB = H
BDRB = H'00000000, BDMRB = H'00000000, BRCR = H'00000001, BETR = H'00

Specified conditions: Channel A/channel B independent mode

<Channel A>

Address: H'00000500, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read/longword

The number of execution-times break enable (5 times)

<Channel B>

Address: H'00001000, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read/longword

On channel A, a user break occurs after the instruction of address H'00000500 is exe
times and before the fifth time.

On channel B, a user break occurs before an instruction of address H'00001000 is ex

(Example 1-6)

- Register specifications

  BARA = H'00008404, BAMRA = H'00000FFF, BBRA = H'0054, BDRA = H'0000
  BDMRA = H'00000000, BARB = H'00008010, BAMRB = H'00000006, BBRB = H
  BDRB = H'00000000, BDMRB = H'00000000, BRCR = H'00000400

  Specified conditions: Channel A/channel B independent mode

  <Channel A>

  Address: H'00008404, Address mask: H'00000FFF

  Data: H'00000000, Data mask: H'00000000

Break Condition Specified for L Bus Data Access Cycle:

(Example 2-1)

- Register specifications

  BARA = H'00123456, BAMRA = H'00000000, BBRA = H'0064, BDRA = H'123456
  BDMRA = H'FFFFFFFF, BARB = H'000ABCDE, BAMRB = H'000000FF, BBRB =
  BDRB = H'0000A512, BDMRB = H'00000000, BRCR = H'00000080

  Specified conditions: Channel A/channel B independent mode

  <Channel A>

  Address: H'00123456, Address mask: H'00000000

  Data: H'12345678, Data mask: H'FFFFFFFF

  Bus cycle: L bus/data access/read (operand size is not included in the condition)

  <Channel B>

  Address: H'000ABCDE, Address mask: H'000000FF

  Data: H'0000A512, Data mask: H'00000000

  Bus cycle: L bus/data access/write/word

  On channel A, a user break occurs with longword read from address H'00123454, wor from address H'00123456, or byte read from address H'00123456. On channel B, a us occurs when word H'A512 is written in addresses H'000ABC00 to H'000ABCFE.

Data: H'12345678, Data mask: H'FFFFFFFF

Bus cycle: I bus (CPU cycle)/instruction fetch/read (operand size is not included in condition)

<Channel B>

Address: H'00055555, Address mask: H'00000000

Data: H'00000078, Data mask: H'0000000F

Bus cycle: I bus (CPU cycle)/data access/write/byte

On channel A, a user break occurs when instruction fetch is performed for address H in the external memory space.

On channel B, a user break occurs when byte data H'7x is written in address H'0005 external memory space by the CPU.

match occurs in another bus cycle in sequential break setting. Therefore, no break occ
if a bus cycle, in which an A-channel match and a channel B match occur simultaneou
set.

4. When a user break and another exception occur at the same instruction, which has hig priority is determined according to the priority levels defined in table 5.1 in section 5, Exception Handling. If an exception with higher priority occurs, the user break is not generated.
   - Pre-execution break has the highest priority.
   - When a post-execution break or data access break occurs simultaneously with a re execution-type exception (including pre-execution break) that has higher priority, execution-type exception is accepted, and the condition match flag is not set (see t exception in the following note). The break will occur and the condition match fla set only after the exception source of the re-execution-type exception has been cle the exception handling routine and re-execution of the same instruction has ended
   - When a post-execution break or data access break occurs simultaneously with a completion-type exception (TRAPA) that has higher priority, though a break does occur, the condition match flag is set.
5. Note the following exception for the above note.

   If a post-execution break or data access break is satisfied by an instruction that genera CPU address error by data access, the CPU address error is given priority to the break that the UBC condition match flag is set in this case.
6. Note the following when a break occurs in a delay slot.

   If a pre-execution break is set at the delay slot instruction of the RTE instruction, the b does not occur until the branch destination of the RTE instruction.
7. User breaks are disabled during UBC module standby mode. Do not read from or writ UBC registers during UBC module standby mode; the values are not guaranteed.

8.2 Address Map

The address map is listed in table 8.1.

Table 8.1 Address Map

Address	Type of Memory	Size			
		128 Kbytes Version	**64 Kbytes Version**	**32 Kbytes Version**	**16 Kby Versic**
H'00000000 to H'00003FFF	On-chip FLASH	128 Kbytes	64 Kbytes	32 Kbytes	16 Kby
H'00004000 to H'00007FFF					Reserv
H'00008000 to H'0000FFFF				Reserved	
H'00010000 to H'0001FFFF			Reserved		
H'00020000 to H'FFFF9FFF	Reserved	—	—	—	—
H'FFFFA000 to H'FFFFAFFF	On-chip RAM	8 Kbytes	8 Kbytes	8 Kbytes	8 Kbyt
H'FFFFB000 to H'FFFFBFFF					Reserv
H'FFFFC000 to H'FFFFFFFF	On-chip peripheral I/O	128 Kbytes	64 Kbytes	64 Kbytes	64 Kby

8.3 Access to on-chip FLASH and on-chip RAM

Access to the on-chip FLASH for read is synchronized with I ϕ clock and is executed in cycle. For details on programming and erasing, see section 17, Flash Memory.

Access to the on-chip RAM for read/write is synchronized with I ϕ clock and is execute clock cycle. For details, see section 18, RAM.

Number of Access Cycles	Write	(3 + n) × Iclk + (1 + m) × Bclk + 2 × Pclk
	Read	(3 + n) × Iclk + (1 + m) × Bclk + 2 × Pclk + 2 × Iclk

Note: When m = 0 to 3, Bclk:Pclk = 4:1
When n = 0 to 3, Iclk:Bclk = 4:1
When m = 0, 1, Bclk:Pclk = 2:1
When n = 0, 1, Iclk:Bclk = 2:1
When m = 0, Bclk:Pclk = 1:1
When n = 0, Iclk:Bclk = 1:1

This LSI adopts synchronous logic, and data of each bus is input and output in synchroni
with the rising edge of the corresponding clock. The L bus access takes one Iclk cycle, I b
access takes one Bclk cycle, and peripheral bus access takes two Pclk cycles. When the o
peripheral I/O register is accessed by the CPU, the period required for preparation for dat
to the I bus is a period of 3 Iclk cycles.

Figure 8.1 shows an example of timing of write access to the peripheral bus when Iclk:Bc
4:1:1. From the L bus, to which the CPU is connected, data is output in synchronization v
Since there are four Iclk cycles in a single Bclk cycle when Iclk:Bclk = 4:1, data can be o
onto the L bus in four possible timings within one Bclk cycle. Accordingly, a maximum c
Iclk cycles of period (four Iclk cycles in the example shown in the figure) is required befo
rising edge of Bclk, on which data is transferred from the L bus to the I bus. Because of th
is transferred from the L bus to the I bus in a period of (3 + n) × Iclk (n = 0 to 3) when Icl
4:1. The relation of the timing of data output to the L bus and the rising edge of Bclk depe
the state of program execution. In the case shown in figure 8.1, where Bclk = Pclk = 1:1,
period required for access by the CPU is (3 + n) × Iclk + 1 × Bclk + 2 × Pclk.

Figure 8.2 shows an example of timing of write access to the peripheral bus when Iclk:E 4:4:1. From the L bus, to which the CPU is connected, data is output in synchronization When Iclk:Bclk = 1:1, a period of 3 Iclk + Bclk is required to transfer data from the L bu bus. In data transfer from the I bus to the peripheral bus, there are four BIclk cycles in a Pclk cycle when Bclk:Pclk = 4:1, and data can therefore be output onto the peripheral bu possible timings within one Pclk cycle. Accordingly, a maximum of four Bclk cycles of (four Bclk cycles in the example shown in the figure) is required before the rising edge which data is transferred from the I bus to the peripheral bus. Because of this, data is tra from the I bus to the peripheral bus in a period of (1 + m) × Bclk (m = 0 to 3) when Bclk 4:1. The relation of the timing of data output to the I bus and the rising edge of Pclk dep the state of program execution. In the case shown in figure 8.2, where Iclk = Bclk = 1:1, required for access by the CPU is 3 × Iclk + (1 + m) × Bclk + 2 × Pclk.

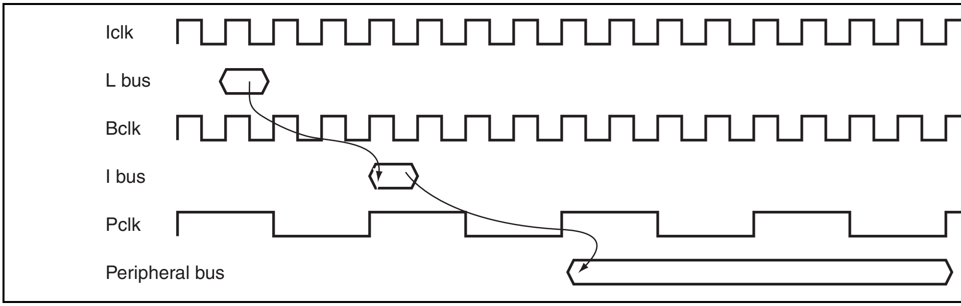


Figure 8.2 Timing of Write Access to the Peripheral Bus (Iclk:Bclk:Pclk = 4

Figure 8.3 shows an example of timing of read access to the peripheral bus when Iclk:Bc 4:2:1. Transfer from the L bus to the peripheral bus is performed in the same way as for access. In the case of reading, however, values output onto the peripheral bus must be tr to the CPU. Transfers from the external bus to the I bus and from the I bus to the L bus a performed in synchronization with rising edges of the respective bus clocks. 2 × Iclk cyc

Figure 8.3 Timing of Read Access to the Peripheral Bus (Iclk:Bclk:Pclk = 4:2

— Waveform output at compare match

— Input capture function

— Counter clear operation

— Multiple timer counters (TCNT) can be written to simultaneously

— Simultaneous clearing by compare match and input capture is possible

— Register simultaneous input/output is possible by synchronous counter operation

— A maximum 12-phase PWM output is possible in combination with synchronous

- Buffer operation settable for channels 0, 3, and 4
- Phase counting mode settable independently for each of channels 1 and 2
- Cascade connection operation
- Fast access via internal 16-bit bus
- 28 interrupt sources
- Automatic transfer of register data
- A/D converter start trigger can be generated
- Module standby mode can be settable
- A total of six-phase waveform output, which includes complementary PWM output, positive and negative phases of reset PWM output by interlocking operation of chan 4, is possible.
- AC synchronous motor (brushless DC motor) drive mode using complementary PW and reset PWM output is settable by interlocking operation of channels 0, 3, and 4, a selection of two types of waveform outputs (chopping and level) is possible.
- Dead time compensation counter available in channel 5
- In complementary PWM mode, interrupts at the crest and trough of the counter valu converter start triggers can be skipped.

TIMMTU1A_020020030800

		TGRB_0 TGRE_0	TGRB_1	TGRB_2	TGRB_3	TGRB_4	TG TG
General registers/ buffer registers		TGRC_0 TGRD_0 TGRF_0	—	—	TGRC_3 TGRD_3	TGRC_4 TGRD_4	—
I/O pins		TIOC0A TIOC0B TIOC0C TIOC0D	TIOC1A*1 TIOC1B*1	TIOC2A*1 TIOC2B*1	TIOC3A TIOC3B TIOC3C TIOC3D	TIOC4A TIOC4B TIOC4C TIOC4D	Inp TIC TIC TIC
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TG con ma inpu
Compare match output	0 output	√	√	√	√	√	—
	1 output	√	√	√	√	√	—
	Toggle output	√	√	√	√	√	—
Input capture function		√	√	√	√	√	√
Synchronous operation		√	√	√	√	√	—
PWM mode 1		√	√	√	√	√	—
PWM mode 2		√	√	√	—	—	—
Complementary PWM mode		—	—	—	√	√	—
Reset PWM mode		—	—	—	√	√	—
AC synchronous motor drive mode		√	—	—	√	√	—

TGRE_0 compare match	TCNT_4 underflow (trough) in complementary PWM mode

	capture 0B • Compare match or input capture 0C • Compare match or input capture 0D • Compare match 0E • Compare match 0F • Overflow	capture 1B*2 • Overflow • Underflow	capture 2B*2 • Overflow • Underflow	capture 3B • Compare match or input capture 3C • Compare match or input capture 3D • Overflow	capture 4B • Compare match or input capture 4C • Compare match or input capture 4D • Overflow or underflow	•

					• A/D converter start request at a match between TADCORB_4 and TCNT_4	
Interrupt skipping function	—	—	—	• Skips TGRA_3 compare match interrupts	• Skips TCIV_4 interrupts	—

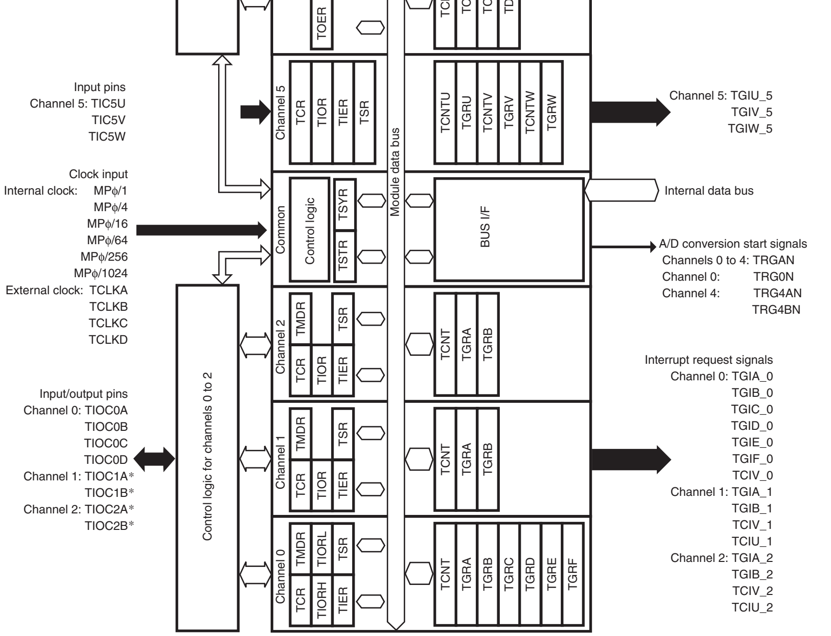
[Legend]

√: Possible

—: Not possible

Notes: 1. This pin is supported only by the SH7125.

2. Input capture is supported only by the SH7125.



[Legend]

TSTR: Timer start register
TSYR: Timer synchronous register
TCR: Timer control register
TMDR: Timer mode register
TIOR: Timer I/O control register
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIER: Timer interrupt enable register
TGCR: Timer gate control register
TOER: Timer output master enable register
TOCR: Timer output control register
TSR: Timer status register
TCNT: Timer counter
TCNTS: Timer subcounter

TCDR: Timer cycle data register
TCBR: Timer cycle buffer register
TDDR: Timer dead time data register
TGRA: Timer general register A
TGRB: Timer general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TGRU: Timer general register U
TGRV: Timer general register V
TGRW: Timer general register W

Note: * Supported only by the SH7125.

Figure 9.1 Block Diagram of MTU2

	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	TIOC0A	I/O	TGRA_0 input capture input/output compare output/PWM
	TIOC0B	I/O	TGRB_0 input capture input/output compare output/PWM
	TIOC0C	I/O	TGRC_0 input capture input/output compare output/PWM
	TIOC0D	I/O	TGRD_0 input capture input/output compare output/PWM
1	TIOC1A*	I/O	TGRA_1 input capture input/output compare output/PWM
	TIOC1B*	I/O	TGRB_1 input capture input/output compare output/PWM
2	TIOC2A*	I/O	TGRA_2 input capture input/output compare output/PWM
	TIOC2B*	I/O	TGRB_2 input capture input/output compare output/PWM
3	TIOC3A	I/O	TGRA_3 input capture input/output compare output/PWM
	TIOC3B	I/O	TGRB_3 input capture input/output compare output/PWM
	TIOC3C	I/O	TGRC_3 input capture input/output compare output/PWM
	TIOC3D	I/O	TGRD_3 input capture input/output compare output/PWM
4	TIOC4A	I/O	TGRA_4 input capture input/output compare output/PWM
	TIOC4B	I/O	TGRB_4 input capture input/output compare output/PWM
	TIOC4C	I/O	TGRC_4 input capture input/output compare output/PWM
	TIOC4D	I/O	TGRD_4 input capture input/output compare output/PWM
5	TIC5U	Input	TGRU_5 input capture input/external pulse input pin
	TIC5V	Input	TGRV_5 input capture input/external pulse input pin
	TIC5W	Input	TGRW_5 input capture input/external pulse input pin

Note: * Supported only by the SH7125.

Timer control register_3	TCR_3	R/W	H'00	H'FFFFC200	8, 1
Timer control register_4	TCR_4	R/W	H'00	H'FFFFC201	8
Timer mode register_3	TMDR_3	R/W	H'00	H'FFFFC202	8, 1
Timer mode register_4	TMDR_4	R/W	H'00	H'FFFFC203	8
Timer I/O control register H_3	TIORH_3	R/W	H'00	H'FFFFC204	8, 1
Timer I/O control register L_3	TIORL_3	R/W	H'00	H'FFFFC205	8
Timer I/O control register H_4	TIORH_4	R/W	H'00	H'FFFFC206	8, 1
Timer I/O control register L_4	TIORL_4	R/W	H'00	H'FFFFC207	8
Timer interrupt enable register_3	TIER_3	R/W	H'00	H'FFFFC208	8, 1
Timer interrupt enable register_4	TIER_4	R/W	H'00	H'FFFFC209	8
Timer output master enable register	TOER	R/W	H'C0	H'FFFFC20A	8
Timer gate control register	TGCR	R/W	H'80	H'FFFFC20D	8
Timer output control register 1	TOCR1	R/W	H'00	H'FFFFC20E	8, 1
Timer output control register 2	TOCR2	R/W	H'00	H'FFFFC20F	8
Timer counter_3	TCNT_3	R/W	H'0000	H'FFFFC210	16,
Timer counter_4	TCNT_4	R/W	H'0000	H'FFFFC212	16
Timer cycle data register	TCDR	R/W	H'FFFF	H'FFFFC214	16,
Timer dead time data register	TDDR	R/W	H'FFFF	H'FFFFC216	16
Timer general register A_3	TGRA_3	R/W	H'FFFF	H'FFFFC218	16,
Timer general register B_3	TGRB_3	R/W	H'FFFF	H'FFFFC21A	16
Timer general register A_4	TGRA_4	R/W	H'FFFF	H'FFFFC21C	16,
Timer general register B_4	TGRB_4	R/W	H'FFFF	H'FFFFC21E	16

Timer status register_1	TSR_1	R/W	H'C0	H'FFFFC22D	8
Timer interrupt skipping set register	TITCR	R/W	H'00	H'FFFFC230	8,
Timer interrupt skipping counter	TITCNT	R	H'00	H'FFFFC231	8
Timer buffer transfer set register	TBTER	R/W	H'00	H'FFFFC232	8
Timer dead time enable register	TDER	R/W	H'01	H'FFFFC234	8
Timer output level buffer register	TOLBR	R/W	H'00	H'FFFFC236	8
Timer buffer operation transfer mode register_3	TBTM_3	R/W	H'00	H'FFFFC238	8,
Timer buffer operation transfer mode register_4	TBTM_4	R/W	H'00	H'FFFFC239	8
Timer A/D converter start request control register	TADCR	R/W	H'0000	H'FFFFC240	16
Timer A/D converter start request cycle set register A_4	TADCORA_4	R/W	H'FFFF	H'FFFFC244	16
Timer A/D converter start request cycle set register B_4	TADCORB_4	R/W	H'FFFF	H'FFFFC246	16
Timer A/D converter start request cycle set buffer register A_4	TADCOBRA_4	R/W	H'FFFF	H'FFFFC248	16
Timer A/D converter start request cycle set buffer register B_4	TADCOBRB_4	R/W	H'FFFF	H'FFFFC24A	16

Timer I/O control register H_0	TIORH_0	R/W	H'00	H'FFFFC302	8, 1
Timer I/O control register L_0	TIORL_0	R/W	H'00	H'FFFFC303	8
Timer interrupt enable register_0	TIER_0	R/W	H'00	H'FFFFC304	8, 1
Timer status register_0	TSR_0	R/W	H'C0	H'FFFFC305	8
Timer counter_0	TCNT_0	R/W	H'0000	H'FFFFC306	16
Timer general register A_0	TGRA_0	R/W	H'FFFF	H'FFFFC308	16,
Timer general register B_0	TGRB_0	R/W	H'FFFF	H'FFFFC30A	16
Timer general register C_0	TGRC_0	R/W	H'FFFF	H'FFFFC30C	16,
Timer general register D_0	TGRD_0	R/W	H'FFFF	H'FFFFC30E	16
Timer general register E_0	TGRE_0	R/W	H'FFFF	H'FFFFC320	16,
Timer general register F_0	TGRF_0	R/W	H'FFFF	H'FFFFC322	16
Timer interrupt enable register 2_0	TIER2_0	R/W	H'00	H'FFFFC324	8, 1
Timer status register 2_0	TSR2_0	R/W	H'C0	H'FFFFC325	8
Timer buffer operation transfer mode register_0	TBTM_0	R/W	H'00	H'FFFFC326	8
Timer control register_1	TCR_1	R/W	H'00	H'FFFFC380	8, 1
Timer mode register_1	TMDR_1	R/W	H'00	H'FFFFC381	8
Timer I/O control register_1	TIOR_1	R/W	H'00	H'FFFFC382	8
Timer interrupt enable register_1	TIER_1	R/W	H'00	H'FFFFC384	8, 1
Timer status register_1	TSR_1	R/W	H'C0	H'FFFFC385	8

Timer interrupt enable register_2	TIER_2	R/W	H'00	H'FFFFC404	8,
Timer status register_2	TSR_2	R/W	H'C0	H'FFFFC405	8
Timer counter_2	TCNT_2	R/W	H'0000	H'FFFFC406	16
Timer general register A_2	TGRA_2	R/W	H'FFFF	H'FFFFC408	16
Timer general register B_2	TGRB_2	R/W	H'FFFF	H'FFFFC40A	16
Timer counter U_5	TCNTU_5	R/W	H'0000	H'FFFFC480	16
Timer general register U_5	TGRU_5	R/W	H'FFFF	H'FFFFC482	16
Timer control register U_5	TCRU_5	R/W	H'00	H'FFFFC484	8
Timer I/O control register U_5	TIORU_5	R/W	H'00	H'FFFFC486	8
Timer counter V_5	TCNTV_5	R/W	H'0000	H'FFFFC490	16
Timer general register V_5	TGRV_5	R/W	H'FFFF	H'FFFFC492	16
Timer control register V_5	TCRV_5	R/W	H'00	H'FFFFC494	8
Timer I/O control register V_5	TIORV_5	R/W	H'00	H'FFFFC496	8
Timer counter W_5	TCNTW_5	R/W	H'0000	H'FFFFC4A0	16
Timer general register W_5	TGRW_5	R/W	H'FFFF	H'FFFFC4A2	16
Timer control register W_5	TCRW_5	R/W	H'00	H'FFFFC4A4	8
Timer I/O control register W_5	TIORW_5	R/W	H'00	H'FFFFC4A6	8
Timer status register_5	TSR_5	R/W	H'00	H'FFFFC4B0	8
Timer interrupt enable register_5	TIER_5	R/W	H'00	H'FFFFC4B2	8
Timer start register_5	TSTR_5	R/W	H'00	H'FFFFC4B4	8
Timer compare match clear register	TCNTCMPCLR	R/W	H'00	H'FFFFC4B6	8

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	CCLR[2:0]	000	R/W	Counter Clear 0 to 2 These bits select the TCNT counter clearing sc See tables 9.4 and 9.5 for details.
4, 3	CKEG[1:0]	00	R/W	Clock Edge 0 and 1 These bits select the input clock edge. When th clock is counted using both edges, the input clo period is halved (e.g. MPφ/4 both edges = MPφ edge). If phase counting mode is used on chan and 2, this setting is ignored and the phase cou mode setting has priority. Internal clock edge s is valid when the input clock is MPφ/4 or slowe MPφ/1, or the overflow/underflow of another ch selected for the input clock, although values ca written, counter operation compiles with the ini 00: Count at rising edge 01: Count at falling edge 1x: Count at both edges
2 to 0	TPSC[2:0]	000	R/W	Time Prescaler 0 to 2 These bits select the TCNT counter clock. The source can be selected independently for each See tables 9.6 to 9.10 for details.

[Legend]

x: Don't care

				synchronous operation*
	1	0	0	TCNT clearing disabled
			1	TCNT cleared by TGRC compare mat capture*[2]
		1	0	TCNT cleared by TGRD compare mat capture*[2]
			1	TCNT cleared by counter clearing for a channel performing synchronous clear synchronous operation*[1]

Notes: 1. Synchronous operation is set by setting the SYNC bit in TSYR to 1.

2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared beca buffer register setting has priority, and compare match/input capture does not

Table 9.5 CCLR0 to CCLR2 (Channels 1 and 2)

Channel	Bit 7 Reserved*[2]	Bit 6 CCLR1	Bit 5 CCLR0	Description
1, 2	0	0	0	TCNT clearing disabled
			1	TCNT cleared by TGRA compare ma capture
		1	0	TCNT cleared by TGRB compare ma capture
			1	TCNT cleared by counter clearing for channel performing synchronous clea synchronous operation*[1]

Notes: 1. Synchronous operation is selected by setting the SYNC bit in TSYR to 1.

2. Bit 7 is reserved in channels 1 and 2. It is always read as 0 and cannot be mo

		1	0	External clock: counts on TCLKC pin in
			1	External clock: counts on TCLKD pin in

Table 9.7 TPSC0 to TPSC2 (Channel 1)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
1	0	0	0	Internal clock: counts on MPϕ/1
			1	Internal clock: counts on MPϕ/4
		1	0	Internal clock: counts on MPϕ/16
			1	Internal clock: counts on MPϕ/64
	1	0	0	External clock: counts on TCLKA pin in
			1	External clock: counts on TCLKB pin in
		1	0	Internal clock: counts on MPϕ/256
			1	Counts on TCNT_2 overflow/underflow

Note: This setting is ignored when channel 1 is in phase counting mode.

		1	0	External clock: counts on TCLKC pin i
			1	Internal clock: counts on MPφ/1024

Note: This setting is ignored when channel 2 is in phase counting mode.

Table 9.9 TPSC0 to TPSC2 (Channels 3 and 4)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
3, 4	0	0	0	Internal clock: counts on MPφ/1
			1	Internal clock: counts on MPφ/4
		1	0	Internal clock: counts on MPφ/16
			1	Internal clock: counts on MPφ/64
	1	0	0	Internal clock: counts on MPφ/256
			1	Internal clock: counts on MPφ/1024
		1	0	External clock: counts on TCLKA pin i
			1	External clock: counts on TCLKB pin i

9.3.2 Timer Mode Register (TMDR)

The TMDR registers are 8-bit readable/writable registers that are used to set the operating each channel. The MTU2 has five TMDR registers, one each for channels 0 to 4. TMDR settings should be changed only when TCNT operation is stopped.

Bit:	7	6	5	4	3	2	1	0
	-	BFE	BFB	BFA	MD[3:0]			
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0. The write value sh always be 0.
6	BFE	0	R/W	Buffer Operation E Specifies whether TGRE_0 and TGRF_0 are t in the normal way or to be used together for bu operation. When TGRF is used as a buffer register, TGRI compare match is generated. In channels 1 to 4, this bit is reserved. It is alwa as 0 and the write value should always be 0. 0: TGRE_0 and TGRF_0 operate normally 1: TGRE_0 and TGRF_0 used together for buf operation

				interrupt enable register 3/4 (TIER_3/4) shoul cleared to 0. In channels 1 and 2, which have no TGRD, bi reserved. It is always read as 0 and cannot be 0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer
4	BFA	0	R/W	Buffer Operation A Specifies whether TGRB is to operate in the r way, or TGRB and TGRD are to be used toge buffer operation. When TGRD is used as a bu register, TGRD input capture/output compare take place in modes other than complementa mode, but compare match with TGRD occurs complementary PWM mode. Since the TGFD be set if a compare match occurs during Tb ir complementary PWM mode, the TGIED bit in interrupt enable register 3/4 (TIER_3/4) shoul cleared to 0. In channels 1 and 2, which have no TGRC, bi reserved. It is always read as 0 and cannot be 0: TGRA and TGRC operate normally 1: TGRA and TGRC used together for buffer
3 to 0	MD[3:0]	0000	R/W	Modes 0 to 3 These bits are used to set the timer operating See table 9.11 for details.

		1	0	Phase counting mode 3*2
			1	Phase counting mode 4*2
1	0	0	0	Reset synchronous PWM mode*3
			1	Setting prohibited
		1	x	Setting prohibited
	1	0	0	Setting prohibited
			1	Complementary PWM mode 1 (transmit at crest)*3
		1	0	Complementary PWM mode 2 (transmit at trough)*3
			1	Complementary PWM mode 2 (transmit at crest and trough)*3

[Legend]

x: Don't care

Notes: 1. PWM mode 2 cannot be set for channels 3 and 4.

2. Phase counting mode cannot be set for channels 0, 3, and 4.

3. Reset synchronous PWM mode and complementary PWM mode can only be s channel 3. When channel 3 is set to reset synchronous PWM mode or comple PWM mode, the channel 4 settings become ineffective and automatically confo channel 3 settings. However, do not set channel 4 to reset synchronous PWM complementary PWM mode. Reset synchronous PWM mode and complement mode cannot be set for channels 0, 1, and 2.

When TGRC or TGRD is designated for buffer operation, this setting is invalid and the operates as a buffer register.

- TIORH_0, TIOR_1, TIOR_2, TIORH_3, TIORH_4

Bit:	7	6	5	4	3	2	1	0
	IOB[3:0]				IOA[3:0]			
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	IOB[3:0]	0000	R/W	I/O Control B0 to B3 Specify the function of TGRB. See the following tables. TIORH_0: Table 9.12 TIOR_1: Table 9.14 TIOR_2: Table 9.15 TIORH_3: Table 9.16 TIORH_4: Table 9.18
3 to 0	IOA[3:0]	0000	R/W	I/O Control A0 to A3 Specify the function of TGRA. See the following tables. TIORH_0: Table 9.20 TIOR_1: Table 9.22 TIOR_2: Table 9.23 TIORH_3: Table 9.24 TIORH_4: Table 9.26

				See the following tables. TIORL_0: Table 9.13 TIORL_3: Table 9.17 TIORL_4: Table 9.19
3 to 0	IOC[3:0]	0000	R/W	I/O Control C0 to C3 Specify the function of TGRC. See the following tables. TIORL_0: Table 9.21 TIORL_3: Table 9.25 TIORL_4: Table 9.27

- TIORU_5, TIORV_5, TIORW_5

Bit name:	7	6	5	4	3	2	1	0
	-	-	-	IOC[4:0]				
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
4 to 0	IOC[4:0]	00000	R/W	I/O Control C0 to C4 Specify the function of TGRU_5, TGRV_5, and TGRW_5. For details, see table 9.28.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/coun Input capture at TCNT_1 count-up/cour

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/count Input capture at TCNT_1 count-up/count

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFB bit in TMDR_0 is set to 1 and TGRD_0 is used as a buffer regis setting is invalid and input capture/output compare is not generated.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Input capture at generation of TGRC_0 match/input capture

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. The TIOC1B pin input/output function is supported only by the SH7125.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. The TIOC2B pin input/output function is supported only by the SH7125.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*[2]	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFB bit in TMDR_3 is set to 1 and TGRD_3 is used as a buffer regis setting is invalid and input capture/output compare is not generated.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*[2]	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFB bit in TMDR_4 is set to 1 and TGRD_4 is used as a buffer regis setting is invalid and input capture/output compare is not generated.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/coun Input capture at TCNT_1 count-up/cour

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/count Input capture at TCNT_1 count-up/count

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_0 is set to 1 and TGRC_0 is used as a buffer regis setting is invalid and input capture/output compare is not generated.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Input capture at generation of channel compare match/input capture

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. The TIOC1A pin input/output function is supported only by the SH7125.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. The TIOC2A pin input/output function is supported only by the SH7125.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_3 is set to 1 and TGRC_3 is used as a buffer regis setting is invalid and input capture/output compare is not generated.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_4 is set to 1 and TGRC_4 is used as a buffer regis setting is invalid and input capture/output compare is not generated.

	1	x	x	x		Setting prohibited
1	0	0	0	0	Input capture register	Setting prohibited
				1		Input capture at rising edge
			1	0		Input capture at falling edge
				1		Input capture at both edges
		1	x	x		Setting prohibited
	1	0	0	0		Setting prohibited
				1		Measurement of low pulse width of external Capture at trough in complementary PWM n
			1	0		Measurement of low pulse width of external Capture at crest in complementary PWM mo
				1		Measurement of low pulse width of external Capture at crest and trough in complementa mode
		1	0	0		Setting prohibited
				1		Measurement of high pulse width of externa signal Capture at trough in complementary PWM n
			1	0		Measurement of high pulse width of externa signal Capture at crest in complementary PWM mo
				1		Measurement of high pulse width of externa signal Capture at crest and trough in complementa mode

[Legend]

x: Don't care

Bit	Bit Name	Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
2	CMPCLR5U	0	R/W	TCNT Compare Clear 5U Enables or disables requests to clear TCNTU_ TGRU_5 compare match or input capture. 0: Disables TCNTU_5 to be cleared to H'0000 TCNTU_5 and TGRU_5 compare match or i capture 1: Enables TCNTU_5 to be cleared to H'0000 a TCNTU_5 and TGRU_5 compare match or i capture
1	CMPCLR5V	0	R/W	TCNT Compare Clear 5V Enables or disables requests to clear TCNTV_ TGRV_5 compare match or input capture. 0: Disables TCNTV_5 to be cleared to H'0000 TCNTV_5 and TGRV_5 compare match or i capture 1: Enables TCNTV_5 to be cleared to H'0000 a TCNTV_5 and TGRV_5 compare match or i capture

9.3.5 Timer Interrupt Enable Register (TIER)

The TIER registers are 8-bit readable/writable registers that control enabling or disablin interrupt requests for each channel. The MTU2 has seven TIER registers, two for chann one each for channels 1 to 5.

- TIER_0, TIER_1, TIER_2, TIER_3, TIER_4

Bit:	7	6	5	4	3	2	1	0
	TTGE	TTGE2	TCIEU	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TTGE	0	R/W	A/D Converter Start Request Enable Enables or disables generation of A/D conver requests by TGRA input capture/compare ma 0: A/D converter start request generation disa 1: A/D converter start request generation ena

				underflow (trough) enabled
5	TCIEU	0	R/W	Underflow Interrupt Enable Enables or disables interrupt requests (TCIU) b TCFU flag when the TCFU flag in TSR is set to channels 1 and 2. In channels 0, 3, and 4, bit 5 is reserved. It is a read as 0 and the write value should always be 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) b TCFV flag when the TCFV flag in TSR is set to 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
3	TGIED	0	R/W	TGR Interrupt Enable D Enables or disables interrupt requests (TGID) b TGFD bit when the TGFD bit in TSR is set to 1 channels 0, 3, and 4. In channels 1 and 2, bit 3 is reserved. It is alwa as 0 and the write value should always be 0. 0: Interrupt requests (TGID) by TGFD bit disab 1: Interrupt requests (TGID) by TGFD bit enabl

1	TGIEB	0	R/W	TGR Interrupt Enable B Enables or disables interrupt requests (TGIB) TGFB bit when the TGFB bit in TSR is set to 0: Interrupt requests (TGIB) by TGFB bit disa 1: Interrupt requests (TGIB) by TGFB bit enab
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) TGFA bit when the TGFA bit in TSR is set to 0: Interrupt requests (TGIA) by TGFA bit disa 1: Interrupt requests (TGIA) by TGFA bit enab

				TGRE_0. 0: A/D converter start request generation by co match between TCNT_0 and TGRE_0 disab 1: A/D converter start request generation by co match between TCNT_0 and TGRE_0 enab
6 to 2	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
1	TGIEF	0	R/W	TGR Interrupt Enable F Enables or disables interrupt requests by comp match between TCNT_0 and TGRF_0. 0: Interrupt requests (TGIF) by TGFE bit disab 1: Interrupt requests (TGIF) by TGFE bit enabl
0	TGIEE	0	R/W	TGR Interrupt Enable E Enables or disables interrupt requests by comp match between TCNT_0 and TGRE_0. 0: Interrupt requests (TGIE) by TGEE bit disab 1: Interrupt requests (TGIE) by TGEE bit enabl

2	TGIE5U	0	R/W	TGR Interrupt Enable 5U Enables or disables interrupt requests (TGIU_ when the CMFU5 bit in TSR_5 is set to 1. 0: Interrupt requests (TGIU_5) disabled 1: Interrupt requests (TGIU_5) enabled
1	TGIE5V	0	R/W	TGR Interrupt Enable 5V Enables or disables interrupt requests (TGIV_ when the CMFV5 bit in TSR_5 is set to 1. 0: Interrupt requests (TGIV_5) disabled 1: Interrupt requests (TGIV_5) enabled
0	TGIE5W	0	R/W	TGR Interrupt Enable 5W Enables or disables interrupt requests (TGIW when the CMFW5 bit in TSR_5 is set to 1. 0: Interrupt requests (TGIW_5) disabled 1: Interrupt requests (TGIW_5) enabled

Note: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial Value	R/W	Description
7	TCFD	1	R	Count Direction Flag Status flag that shows the direction in which TC counts in channels 1 to 4. In channel 0, bit 7 is reserved. It is always reac and the write value should always be 1. 0: TCNT counts down 1: TCNT counts up
6	—	1	R	Reserved This bit is always read as 1. The write value sh always be 1.
5	TCFU	0	R/(W)*[1]	Underflow Flag Status flag that indicates that TCNT underflow occurred when channels 1 and 2 are set to pha counting mode. Only 0 can be written, for flag c In channels 0, 3, and 4, bit 5 is reserved. It is a read as 0 and the write value should always be [Setting condition] • When the TCNT value underflows (change H'0000 to H'FFFF) [Clearing condition] • When 0 is written to TCFU after reading TC

				PWM mode, this flag is also set. [Clearing condition] • When 0 is written to TCFV after reading T 1*2
3	TGFD	0	R/(W)*1	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of T capture or compare match in channels 0, 3, a Only 0 can be written, for flag clearing. In cha and 2, bit 3 is reserved. It is always read as 0 write value should always be 0. [Setting conditions] • When TCNT = TGRD and TGRD is functi output compare register • When TCNT value is transferred to TGRD capture signal and TGRD is functioning a capture register [Clearing condition] • When 0 is written to TGFD after reading T 1*2

				• When TCNT value is transferred to TGRC capture signal and TGRC is functioning as capture register [Clearing condition] • When 0 is written to TGFC after reading TC 1*[2]
1	TGFB	0	R/(W)*[1]	Input Capture/Output Compare Flag B Status flag that indicates the occurrence of TG capture or compare match. Only 0 can be writ flag clearing. [Setting conditions] • When TCNT = TGRB and TGRB is functio output compare register • When TCNT value is transferred to TGRB capture signal and TGRB is functioning as capture register [Clearing condition] • When 0 is written to TGFB after reading TC 1*[2]

capture signal and TGRA is functioning a
capture register

[Clearing condition]

- When 0 is written to TGFA after reading T
  1*2

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed

2. If another flag setting condition occurs before writing 0 to the bit after reading flag will not be cleared by writing 0 to it once. In this case, read the bit as 1 ag write 0 to it.

				These bits are always read as 1. The write va should always be 1.
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
1	TGFF	0	R/(W)*[1]	Compare Match Flag F Status flag that indicates the occurrence of co match between TCNT_0 and TGRF_0. [Setting condition] • When TCNT_0 = TGRF_0 and TGRF_0 is functioning as compare register [Clearing condition] • When 0 is written to TGFF after reading T 1*[2]
0	TGFE	0	R/(W)*[1]	Compare Match Flag E Status flag that indicates the occurrence of co match between TCNT_0 and TGRE_0. [Setting condition] • When TCNT_0 = TGRE_0 and TGRE_0 is functioning as compare register [Clearing condition] • When 0 is written to TGFE after reading T 1*[2]

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed v

2. If another flag setting condition occurs before writing 0 to the bit after reading i flag will not be cleared by writing 0 to it once. In this case, read the bit as 1 aga write 0 to it.

				These bits are always read as 0. The write valu always be 0.
2	CMFU5	0	R/(W)*1	Compare Match/Input Capture Flag U5 Status flag that indicates the occurrence of TGI input capture or compare match. [Setting conditions] • When TCNTU_5 = TGRU_5 and TGRU_5 i functioning as output compare register • When TCNTU_5 value is transferred to TGI input capture signal and TGRU_5 is functio input capture register • When TCNTU_5 value is transferred to TGI TGRU_5 is functioning as a register for mea pulse width of the external input signal. The timing is specified by the IOC bits in timer I/ register U_5 (TIORU_5)*2 [Clearing condition] • When 0 is written to CMFU5 after reading C

input capture register

- When TCNTV_5 value is transferred to TGR TGRV_5 is functioning as a register for meas pulse width of the external input signal. The t timing is specified by the IOC bits in timer I/C register V_5 (TIORV_5)*2

[Clearing condition]

- When 0 is written to CMFV5 after reading CM input capture register

- When TCNTW_5 value is transferred to TG
TGRW_5 is functioning as a register for me
the pulse width of the external input signal.
transfer timing is specified by the IOC bits i
control register W_5 (TIORW_5)*[2]

[Clearing condition]

- When 0 is written to CMFW5 after reading
1

Notes: 1 Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed

2. The transfer timing is specified by the IOC bit in the timer I/O control register U_5/V_5/W_5 (TIORU_5, TIORV_5, TIORW_5).

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
2	TTSE	0	R/W	Timing Select E Specifies the timing for transferring data from T to TGRE_0 when they are used together for bu operation. In channels 3 and 4, bit 2 is reserved. It is alwa as 0 and the write value should always be 0. W using channel 0 in other than PWM mode, do n this bit to 1. 0: When compare match E occurs in channel 0 1: When TCNT_0 is cleared
1	TTSB	0	R/W	Timing Select B Specifies the timing for transferring data from T TGRB in each channel when they are used tog buffer operation. When using channel 0 in othe PWM mode, do not set this bit to 1. 0: When compare match B occurs in each cha 1: When TCNT is cleared in each channel

9.3.8 Timer Input Capture Control Register (TICCR)

TICCR is an 8-bit readable/writable register that specifies input capture conditions wher
and TCNT_2 are cascaded. The MTU2 has one TICCR in channel 1.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	I2BE	I2AE	I1BE	I1AE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
3	I2BE	0	R/W	Input Capture Enable Specifies whether to include the TIOC2B pin i TGRB_1 input capture conditions. 0: Does not include the TIOC2B pin in the TG input capture conditions 1: Includes the TIOC2B pin in the TGRB_1 in capture conditions

				Specifies whether to include the TIOC1B pin in TGRB_2 input capture conditions. 0: Does not include the TIOC1B pin in the TGR input capture conditions 1: Includes the TIOC1B pin in the TGRB_2 inp capture conditions
0	I1AE	0	R/W	Input Capture Enable Specifies whether to include the TIOC1A pin in TGRA_2 input capture conditions. 0: Does not include the TIOC1A pin in the TGF input capture conditions 1: Includes the TIOC1A pin in the TGRA_2 inp capture conditions

Note: This function is supported only by the SH7125. In the SH7124, write value should a H'00.

Bit	Bit Name	Initial Value	R/W	Description
15, 14	BF[1:0]	00	R/W	TADCOBRA_4/TADCOBRB_4 Transfer Timi Select the timing for transferring data from TADCOBRA_4 and TADCOBRB_4 to TADC and TADCORB_4. For details, see table 9.29.
13 to 8	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
7	UT4AE	0	R/W	Up-Count TRG4AN Enable Enables or disables A/D converter start reque (TRG4AN) during TCNT_4 up-count operatio 0: A/D converter start requests (TRG4AN) dis during TCNT_4 up-count operation 1: A/D converter start requests (TRG4AN) en during TCNT_4 up-count operation
6	DT4AE	0*	R/W	Down-Count TRG4AN Enable Enables or disables A/D converter start reque (TRG4AN) during TCNT_4 down-count opera 0: A/D converter start requests (TRG4AN) dis during TCNT_4 down-count operation 1: A/D converter start requests (TRG4AN) en during TCNT_4 down-count operation

				Enables or disables A/D converter start reque (TRG4BN) during TCNT_4 down-count operati 0: A/D converter start requests (TRG4BN) disa during TCNT_4 down-count operation 1: A/D converter start requests (TRG4BN) ena during TCNT_4 down-count operation
3	ITA3AE	0*	R/W	TGIA_3 Interrupt Skipping Link Enable Select whether to link A/D converter start requ (TRG4AN) with TGIA_3 interrupt skipping oper 0: Does not link with TGIA_3 interrupt skipping 1: Links with TGIA_3 interrupt skipping
2	ITA4VE	0*	R/W	TCIV_4 Interrupt Skipping Link Enable Select whether to link A/D converter start requ (TRG4AN) with TCIV_4 interrupt skipping oper 0: Does not link with TCIV_4 interrupt skipping 1: Links with TCIV_4 interrupt skipping
1	ITB3AE	0*	R/W	TGIA_3 Interrupt Skipping Link Enable Select whether to link A/D converter start requ (TRG4BN) with TGIA_3 interrupt skipping oper 0: Does not link with TGIA_3 interrupt skipping 1: Links with TGIA_3 interrupt skipping

interrupt skipping operation (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE timer A/D converter start request control register (TADCR) to 0).

3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/ converter start requests will not be issued.

* Do not set to 1 when complementary PWM mode is not selected.

Table 9.29 Setting of Transfer Timing by BF1 and BF0 Bits

Bit 7	Bit 6	
BF1	BF0	Description
0	0	Does not transfer data from the cycle set buffer register to t set register.
0	1	Transfers data from the cycle set buffer register to the cycle register at the crest of the TCNT_4 count.*[1]
1	0	Transfers data from the cycle set buffer register to the cycle register at the trough of the TCNT_4 count.*[2]
1	1	Transfers data from the cycle set buffer register to the cycle register at the crest and trough of the TCNT_4 count.*[2]

Notes: 1. Data is transferred from the cycle set buffer register to the cycle set register w crest of the TCNT_4 count is reached in complementary PWM mode, when c match occurs between TCNT_3 and TGRA_3 in reset-synchronized PWM mo when compare match occurs between TCNT_4 and TGRA_4 in PWM mode normal operation mode.

2. These settings are prohibited when complementary PWM mode is not selecte

Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: TADCORA_4 and TADCORB_4 must not be accessed in eight bits; they should always be accessed in 16 b

9.3.11 Timer A/D Converter Start Request Cycle Set Buffer Registers (TADCOB and TADCOBRB_4)

TADCOBRA_4 and TADCOBRB_4 are 16-bit readable/writable registers. When the cre trough of the TCNT_4 count is reached, these register values are transferred to TADCOR TADCORB_4, respectively.

TADCOBRA_4 and TADCOBRB_4 are initialized to H'FFFF.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: TADCOBRA_4 and TADCOBRB_4 must not be accessed in eight bits; they should always be accessed in 1

Note: The TCNT counters must not be accessed in eight bits; they should always be accessed in 16 bits.

9.3.13 Timer General Register (TGR)

The TGR registers are 16-bit readable/writable registers. The MTU2 has 21 TGR registe
channel 0, two each for channels 1 and 2, four each for channels 3 and 4, and three for c

TGRA, TGRB, TGRC, and TGRD function as either output compare or input capture re
TGRC and TGRD for channels 0, 3, and 4 can also be designated for operation as buffe
TGR buffer register combinations are TGRA and TGRC, and TGRB and TGRD.

TGRE_0 and TGRF_0 function as compare registers. When the TCNT_0 count matches
TGRE_0 value, an A/D converter start request can be issued. TGRF can also be designa
operation as a buffer register. TGR buffer register combination is TGRE and TGRF.

TGRU_5, TGRV_5, and TGRW_5 function as compare match, input capture, or externa
width measurement registers.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: The TGR registers must not be accessed in eight bits; they should always be accessed in 16 bits.
TGR registers are initialized to H'FFFF.

- TSTR

Bit:	7	6	5	4	3	2	1	0
	CST4	CST3	-	-	-	CST2	CST1	CST0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	CST4	0	R/W	Counter Start 4 and 3
6	CST3	0	R/W	These bits select operation or stoppage for TC If 0 is written to the CST bit during operation w TIOC pin designated for output, the counter sto the TIOC pin output compare output level is re TIOR is written to when the CST bit is cleared pin output level will be changed to the set initia value. 0: TCNT_4 and TCNT_3 count operation is sto 1: TCNT_4 and TCNT_3 performs count opera
5 to 3	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.

1: TCNT_2 to TCNT_0 performs count operat

- TSTR_5

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	CSTU5	CSTV5	CSTW5
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
2	CSTU5	0	R/W	Counter Start U5 Selects operation or stoppage for TCNTU_5. 0: TCNTU_5 count operation is stopped 1: TCNTU_5 performs count operation
1	CSTV5	0	R/W	Counter Start V5 Selects operation or stoppage for TCNTV_5. 0: TCNTV_5 count operation is stopped 1: TCNTV_5 performs count operation
0	CSTW5	0	R/W	Counter Start W5 Selects operation or stoppage for TCNTW_5. 0: TCNTW_5 count operation is stopped 1: TCNTW_5 performs count operation

Bit	Bit Name	Initial Value	R/W	Description
7	SYNC4	0	R/W	Timer Synchronous operation 4 and 3 These bits are used to select whether operatio independent of or synchronized with other cha When synchronous operation is selected, the T synchronous presetting of multiple channels, a synchronous clearing by counter clearing on ar channel, are possible. To set synchronous operation, the SYNC bits f least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC TCNT clearing source must also be set by mea bits CCLR0 to CCLR2 in TCR. 0: TCNT_4 and TCNT_3 operate independentl presetting/clearing is unrelated to other char 1: TCNT_4 and TCNT_3 performs synchronou operation TCNT synchronous presetting/synchronous is possible
6	SYNC3	0	R/W	
5 to 3	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.

synchronous clearing, in addition to the SYNC
TCNT clearing source must also be set by me
bits CCLR0 to CCLR2 in TCR.

0: TCNT_2 to TCNT_0 operates independent
presetting /clearing is unrelated to other ch

1: TCNT_2 to TCNT_0 performs synchronous
TCNT synchronous presetting/synchronous
is possible

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
0	RWE	1	R/W	Read/Write Enable Enables or disables access to the registers wh write-protection capability against accidental modification. 0: Disables read/write access to the registers 1: Enables read/write access to the registers [Clearing condition] • When 0 is written to the RWE bit after read RWE = 1

- Registers and counters having write-protection capability against accidental modificat
  22 registers: TCR_3, TCR_4, TMDR_3, TMDR_4, TIORH_3, TIORH_4, TIORL_3, TIORL_4, TIER_3, TIER_4, TGRA_3, TGRA_4, TGRB_3, TGRB_4, TOER, TOCR TOCR2, TGCR, TCDR, TDDR, TCNT_3, and TCNT_4.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	R	Reserved These bits are always read as 1. The write va always be 1.
5	OE4D	0	R/W	Master Enable TIOC4D This bit enables/disables the TIOC4D pin MT 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled
4	OE4C	0	R/W	Master Enable TIOC4C This bit enables/disables the TIOC4C pin MT 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled
3	OE3D	0	R/W	Master Enable TIOC3D This bit enables/disables the TIOC3D pin MT 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled
2	OE4B	0	R/W	Master Enable TIOC4B This bit enables/disables the TIOC4B pin MTU 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled
1	OE4A	0	R/W	Master Enable TIOC4A This bit enables/disables the TIOC4A pin MTU 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled

9.3.18 Timer Output Control Register 1 (TOCR1)

TOCR1 is an 8-bit readable/writable register that enables/disables PWM synchronized to output in complementary PWM mode/reset synchronized PWM mode, and controls outpu inversion of PWM output.

Bit:	7	6	5	4	3	2	1	0
	-	PSYE	-	-	TOCL	TOCS	OLSN	OLSP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R/(W)*	R/W	R/W	R/W

Note: * This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to th

Bit	Bit Name	Initial value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
6	PSYE	0	R/W	PWM Synchronous Output Enable This bit selects the enable/disable of toggle ou synchronized with the PWM period. 0: Toggle output is disabled 1: Toggle output is enabled
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.

				be used for the output level in complementary mode and reset-synchronized PWM mode. 0: TOCR1 setting is selected 1: TOCR2 setting is selected
1	OLSN	0	R/W	Output Level Select N*[3] This bit selects the reverse phase output leve synchronized PWM mode/complementary PW See table 9.30.
0	OLSP	0	R/W	Output Level Select P*[3] This bit selects the positive phase output leve synchronized PWM mode/complementary PW See table 9.31.

Notes: 1. This bit can be set to 1 only once after a power on reset. After 1 is written, 0 c written to the bit.

2. Setting the TOCL bit to 1 prevents accidental modification when the CPU goe control.

3. Clearing the TOCS bit to 0 makes this bit setting valid.

Table 9.30 Output Level Select Function

Bit 1	Function			
			Compare Match Output	
OLSN	Initial Output	Active Level	Up Count	Down Count
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The reverse phase waveform initial output value changes to active level after elap dead time after count start.

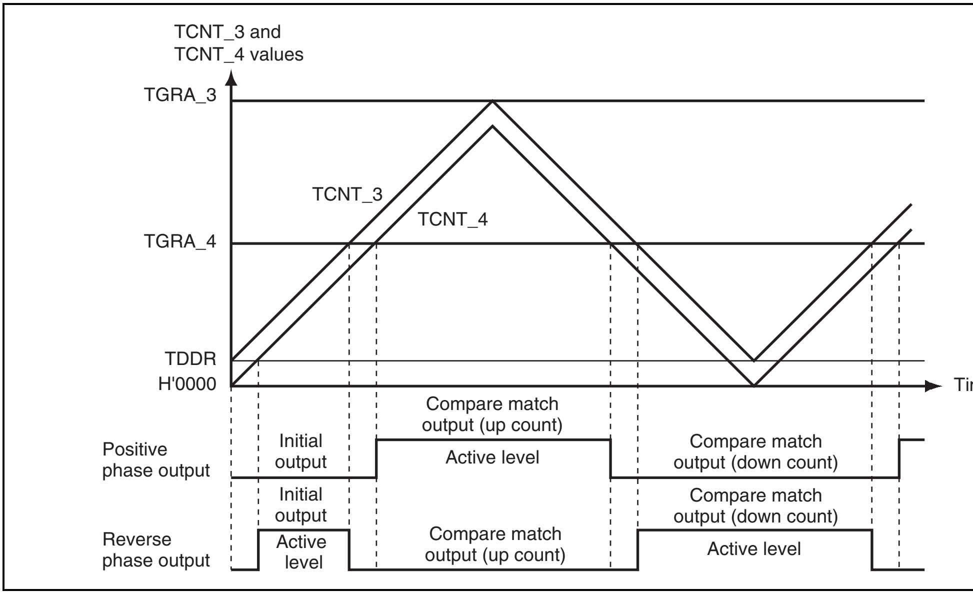


Figure 9.2 Complementary PWM Mode Output Level Example

Bit	Bit Name	value	R/W	Description
7, 6	BF[1:0]	00	R/W	TOLBR Buffer Transfer Timing Select These bits select the timing for transferring da TOLBR to TOCR2. For details, see table 9.32.
5	OLS3N	0	R/W	Output Level Select 3N* This bit selects the output level on TIOC4D in synchronized PWM mode/complementary PV See table 9.33.
4	OLS3P	0	R/W	Output Level Select 3P* This bit selects the output level on TIOC4B in synchronized PWM mode/complementary PV See table 9.34.
3	OLS2N	0	R/W	Output Level Select 2N* This bit selects the output level on TIOC4C in synchronized PWM mode/complementary PV See table 9.35.
2	OLS2P	0	R/W	Output Level Select 2P* This bit selects the output level on TIOC4A in synchronized PWM mode/complementary PV See table 9.36.
1	OLS1N	0	R/W	Output Level Select 1N* This bit selects the output level on TIOC3D in synchronized PWM mode/complementary PV See table 9.37.

BF1	BF0	Complementary PWM Mode	Reset-Synchronized PW
0	0	Does not transfer data from the buffer register (TOLBR) to TOCR2.	Does not transfer data fror buffer register (TOLBR) to
0	1	Transfers data from the buffer register (TOLBR) to TOCR2 at the crest of the TCNT_4 count.	Transfers data from the bu register (TOLBR) to TOCF TCNT_3/TCNT_4 is cleare
1	0	Transfers data from the buffer register (TOLBR) to TOCR2 at the trough of the TCNT_4 count.	Setting prohibited
1	1	Transfers data from the buffer register (TOLBR) to TOCR2 at the crest and trough of the TCNT_4 count.	Setting prohibited

Table 9.33 TIOC4D Output Level Select Function

Bit 5	Function			
			Compare Match Output	
OLS3N	Initial Output	Active Level	Up Count	Down Count
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The reverse phase waveform initial output value changes to the active level after e the dead time after count start.

Bit 3	Function			
			Compare Match Output	
OLS2N	Initial Output	Active Level	Up Count	Down Count
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The reverse phase waveform initial output value changes to the active level after the dead time after count start.

Table 9.36 TIOC4A Output Level Select Function

Bit 2	Function			
			Compare Match Output	
OLS2P	Initial Output	Active Level	Up Count	Down Count
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

Table 9.37 TIOC3D Output Level Select Function

Bit 1	Function			
			Compare Match Output	
OLS1N	Initial Output	Active Level	Up Count	Down Count
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The reverse phase waveform initial output value changes to the active level after the dead time after count start.

TOLBR is an 8-bit readable/writable register that functions as a buffer for TOCR2 and sp the PWM output level in complementary PWM mode and reset-synchronized PWM mod

Bit:	7	6	5	4	3	2	1	0
	-	-	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
5	OLS3N	0	R/W	Specifies the buffer value to be transferred to t OLS3N bit in TOCR2.
4	OLS3P	0	R/W	Specifies the buffer value to be transferred to t OLS3P bit in TOCR2.
3	OLS2N	0	R/W	Specifies the buffer value to be transferred to t OLS2N bit in TOCR2.
2	OLS2P	0	R/W	Specifies the buffer value to be transferred to t OLS2P bit in TOCR2.
1	OLS1N	0	R/W	Specifies the buffer value to be transferred to t OLS1N bit in TOCR2.
0	OLS1P	0	R/W	Specifies the buffer value to be transferred to t OLS1P bit in TOCR2.

Figure 9.3 PWM Output Level Setting Procedure in Buffer Operation

9.3.21 Timer Gate Control Register (TGCR)

TGCR is an 8-bit readable/writable register that controls the waveform output necessary brushless DC motor control in reset-synchronized PWM mode/complementary PWM m register settings are ineffective for anything other than complementary PWM mode/rese synchronized PWM mode.

Bit:	7	6	5	4	3	2	1	0
	-	BDC	N	P	FB	WF	VF	UF
Initial value:	1	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7	—	1	R	Reserved This bit is always read as 1. The write value s always be 1.
6	BDC	0	R/W	Brushless DC Motor This bit selects whether to make the functions register (TGCR) effective or ineffective. 0: Ordinary output 1: Functions of this register are made effectiv

				This bit selects whether the level output or the synchronized PWM/complementary PWM outp the positive pin (TIOC3B, TIOC4A, and TIOC4 output. 0: Level output 1: Reset synchronized PWM/complementary P output
3	FB	0	R/W	External Feedback Signal Enable This bit selects whether the switching of the ou the positive/reverse phase is carried out autom with the MTU2/channel 0 TGRA, TGRB, TGRC capture signals or by writing 0 or 1 to bits 2 to 0 TGCR. 0: Output switching is external input (Input sou channel 0 TGRA, TGRB, TGRC input captu 1: Output switching is carried out by software (UF, VF, WF settings).
2	WF	0	R/W	Output Phase Switch 2 to 0 These bits set the positive phase/negative pha phase on or off state. The setting of these bits only when the FB bit in this register is set to 1. case, the setting of bits 2 to 0 is a substitute fo input. See table 9.39.
1	VF	0	R/W	
0	UF	0	R/W	

	1	ON	OFF	OFF	OFF	ON
1	0	OFF	OFF	ON	ON	OFF
	1	OFF	OFF	OFF	OFF	OFF

9.3.22 Timer Subcounter (TCNTS)

TCNTS is a 16-bit read-only counter that is used only in complementary PWM mode.

The initial value of TCNTS is H'0000.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: Accessing the TCNTS in 8-bit units is prohibited. Always access in 16-bit units.

Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Accessing the TDDR in 8-bit units is prohibited. Always access in 16-bit units.

9.3.24 Timer Cycle Data Register (TCDR)

TCDR is a 16-bit register used only in complementary PWM mode. Set half the PWM ca value as the TCDR register value. This register is constantly compared with the TCNTS c complementary PWM mode, and when a match occurs, the TCNTS counter switches dire (decrement to increment).

The initial value of TCDR is H'FFFF.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Accessing the TCDR in 8-bit units is prohibited. Always access in 16-bit units.

R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W

Note: Accessing the TCBR in 8-bit units is prohibited. Always access in 16-bit units.

9.3.26 Timer Interrupt Skipping Set Register (TITCR)

TITCR is an 8-bit readable/writable register that enables or disables interrupt skipping a specifies the interrupt skipping count. The MTU2 has one TITCR.

Bit:	7	6	5	4	3	2	1	0
	T3AEN	3ACOR[2:0]			T4VEN	4VCOR[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7	T3AEN	0	R/W	T3AEN Enables or disables TGIA_3 interrupt skippin 0: TGIA_3 interrupt skipping disabled 1: TGIA_3 interrupt skipping enabled
6 to 4	3ACOR[2:0]	000	R/W	These bits specify the TGIA_3 interrupt skipp within the range from 0 to 7.* For details, see table 9.40.
3	T4VEN	0	R/W	T4VEN Enables or disables TCIV_4 interrupt skippin 0: TCIV_4 interrupt skipping disabled 1: TCIV_4 interrupt skipping enabled

Bit 6	Bit 5	Bit 4	
3ACOR2	**3ACOR1**	**3ACOR0**	**Description**
0	0	0	Does not skip TGIA_3 interrupts.
0	0	1	Sets the TGIA_3 interrupt skipping count to 1.
0	1	0	Sets the TGIA_3 interrupt skipping count to 2.
0	1	1	Sets the TGIA_3 interrupt skipping count to 3.
1	0	0	Sets the TGIA_3 interrupt skipping count to 4.
1	0	1	Sets the TGIA_3 interrupt skipping count to 5.
1	1	0	Sets the TGIA_3 interrupt skipping count to 6.
1	1	1	Sets the TGIA_3 interrupt skipping count to 7.

Table 9.41 Setting of Interrupt Skipping Count by Bits 4VCOR2 to 4VCOR0

Bit 2	Bit 1	Bit 0	
4VCOR2	**4VCOR1**	**4VCOR0**	**Description**
0	0	0	Does not skip TCIV_4 interrupts.
0	0	1	Sets the TCIV_4 interrupt skipping count to 1.
0	1	0	Sets the TCIV_4 interrupt skipping count to 2.
0	1	1	Sets the TCIV_4 interrupt skipping count to 3.
1	0	0	Sets the TCIV_4 interrupt skipping count to 4.
1	0	1	Sets the TCIV_4 interrupt skipping count to 5.
1	1	0	Sets the TCIV_4 interrupt skipping count to 6.
1	1	1	Sets the TCIV_4 interrupt skipping count to 7.

7	—	0	R	Reserved This bit is always read as 0.
6 to 4	3ACNT[2:0]	000	R	TGIA_3 Interrupt Counter While the T3AEN bit in TITCR is set to 1, the these bits is incremented every time a TGIA_ occurs. [Clearing conditions] • When the 3ACNT2 to 3ACNT0 value in TI matches the 3ACOR2 to 3ACOR0 value i • When the T3AEN bit in TITCR is cleared t • When the 3ACOR2 to 3ACOR0 bits in TIT cleared to 0
3	—	0	R	Reserved This bit is always read as 0.
2 to 0	4VCNT[2:0]	000	R	TCIV_4 Interrupt Counter While the T4VEN bit in TITCR is set to 1, the these bits is incremented every time a TCIV_ occurs. [Clearing conditions] • When the 4VCNT2 to 4VCNT0 value in TI matches the 4VCOR2 to 4VCOR2 value i • When the T4VEN bit in TITCR is cleared t • When the 4VCOR2 to 4VCOR2 bits in TIT cleared to 0

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
1, 0	BTE[1:0]	00	R/W	These bits enable or disable transfer from the registers* used in complementary PWM mode temporary registers and specify whether to link transfer with interrupt skipping operation. For details, see table 9.42.

Note: * Applicable buffer registers:
TGRC_3, TGRD_3, TGRC_4, TGRD_4, and TCBR

Notes: 1. Data is transferred according to the MD3 to MD0 bit setting in TMDR. For det
to section 9.4.8, Complementary PWM Mode.

2. When interrupt skipping is disabled (the T3AEN and T4VEN bits are cleared t
timer interrupt skipping set register (TITCR) or the skipping count set bits (3A
4VCOR) in TITCR are cleared to 0)), be sure to disable link of buffer transfer
interrupt skipping (clear the BTE1 bit in the timer buffer transfer set register (T
0). If link with interrupt skipping is enabled while interrupt skipping is disabled
transfer will not be performed.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
0	TDER	1	R/(W)	Dead Time Enable Specifies whether to generate dead time. 0: Does not generate dead time 1: Generates dead time* [Clearing condition] • When 0 is written to TDER after reading TD

Note: * TDDR must be set to 1 or a larger value.

Note: * Do not set to 1 when complementary PWM mode is not selected.

Bit	Bit Name	Initial Value	R/W	Description
7	CCE	0*	R/(W)	Compare Match Clear Enable Specifies whether to clear counters at TGRA_ compare match in complementary PWM mod 0: Does not clear counters at TGRA_3 compa 1: Clears counters at TGRA_3 compare matc [Setting condition] • When 1 is written to CCE after reading C(
6 to 1	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.

the trough immediately after TCNT_3 and TCN
operation.

For the Tb interval at the trough in complemen
PWM mode, see figure 9.40.

0: Outputs the initial value specified in TOCR

1: Retains the waveform output immediately be
synchronous clearing

[Setting condition]

- When 1 is written to WRE after reading WF

Note: * Do not set to 1 when complementary PWM mode is not selected.

9.3.31 Bus Master Interface

The timer counters (TCNT), general registers (TGR), timer subcounter (TCNTS), timer c
buffer register (TCBR), timer dead time data register (TDDR), timer cycle data register (T
timer A/D converter start request control register (TADCR), timer A/D converter start re
cycle set registers (TADCOR), and timer A/D converter start request cycle set buffer regi
(TADCOBR) are 16-bit registers. A 16-bit data bus to the bus master enables 16-bit read/
bit read/write is not possible. Always access in 16-bit units.

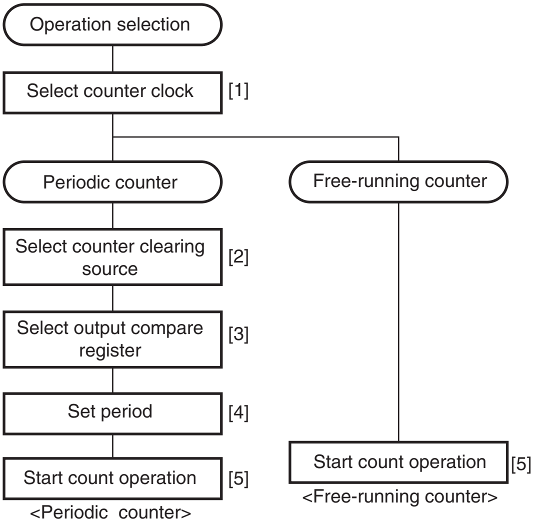
All registers other than the above registers are 8-bit registers. These are connected to the
16-bit data bus, so 16-bit read/writes and 8-bit read/writes are both possible.

Counter Operation:

When one of bits CST0 to CST4 in TSTR or bits CSTU5, CSTV5, and CSTW5 in TSTR to 1, the TCNT counter for the corresponding channel begins counting. TCNT can opera free-running counter, periodic counter, for example.

1. Example of Count Operation Setting Procedure

   Figure 9.4 shows an example of the count operation setting procedure.



[1] Select the counter clock with bits TPSC2 to TPSC0 in TCR. At the same time, select the input clock edge with bits CKEG1 and CKEG0 in TCR.

[2] For periodic counter operation, select the TGR to be used as the TCNT clearing source with bits CCLR2 to CCLR0 in TCR.

[3] Designate the TGR selected in [2] as an output compare register by means of TIOR.

[4] Set the periodic counter cycle in the TGR selected in [2].

[5] Set the CST bit in TSTR to 1 to start the counter operation.

Figure 9.4 Example of Counter Operation Setting Procedure

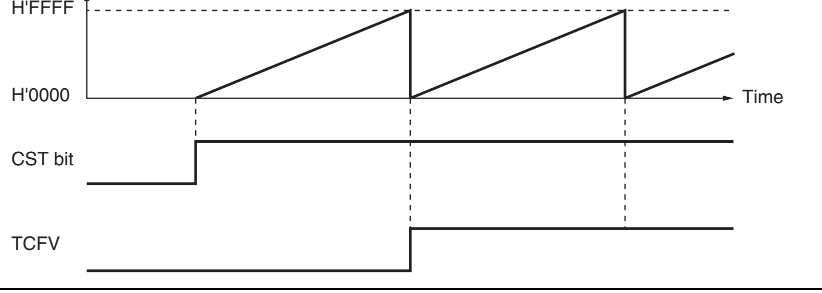


Figure 9.5 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for relevant channel performs periodic count operation. The TGR register for setting the designated as an output compare register, and counter clearing by compare match is s by means of bits CCLR0 to CCLR2 in TCR. After the settings have been made, TCN up-count operation as a periodic counter when the corresponding bit in TSTR is set to the count value matches the value in TGR, the TGF bit in TSR is set to 1 and TCNT i to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, the MTU2 reque interrupt. After a compare match, TCNT starts counting up again from H'0000.

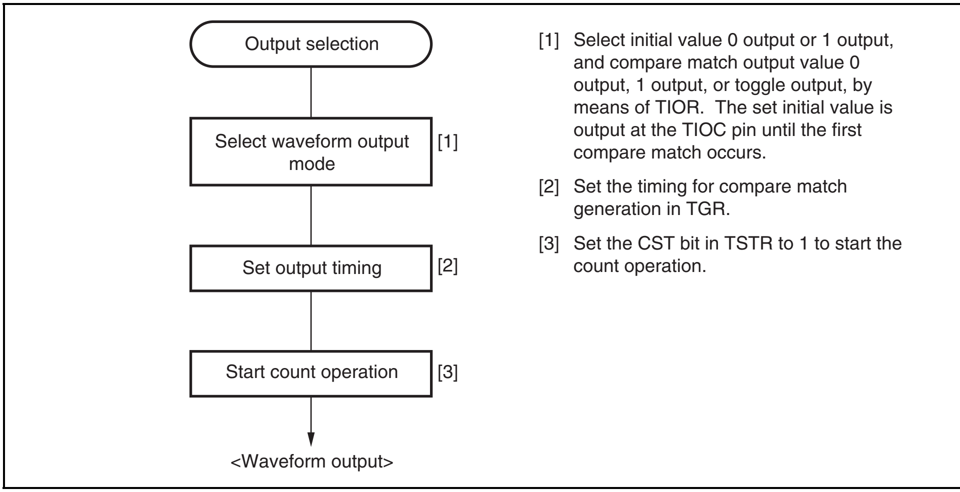
Figure 9.6 Periodic Counter Operation

Waveform Output by Compare Match:

The MTU2 can perform 0, 1, or toggle output from the corresponding output pin using c
match.

1. Example of Setting Procedure for Waveform Output by Compare Match

   Figure 9.7 shows an example of the setting procedure for waveform output by comp



[1] Select initial value 0 output or 1 output, and compare match output value 0 output, 1 output, or toggle output, by means of TIOR. The set initial value is output at the TIOC pin until the first compare match occurs.

[2] Set the timing for compare match generation in TGR.

[3] Set the CST bit in TSTR to 1 to start the count operation.

Figure 9.7 Example of Setting Procedure for Waveform Output by Compare

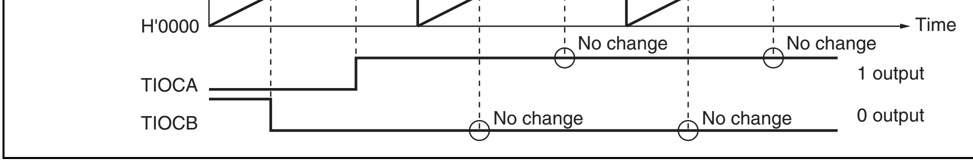


Figure 9.8 Example of 0 Output/1 Output Operation

Figure 9.9 shows an example of toggle output.

In this example, TCNT has been designated as a periodic counter (with counter clearin compare match B), and settings have been made such that the output is toggled by bot compare match A and compare match B.

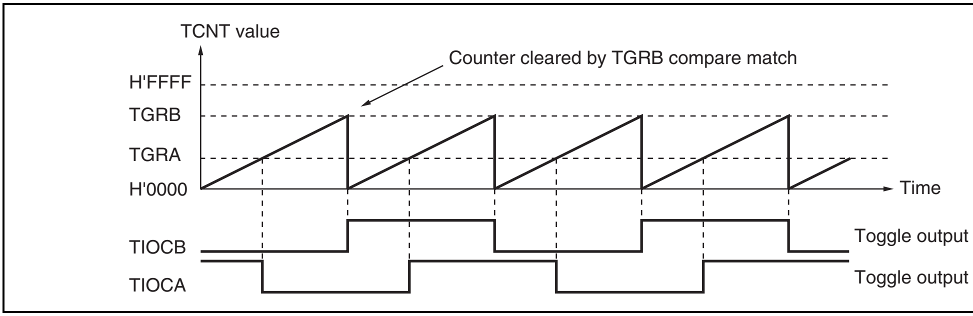
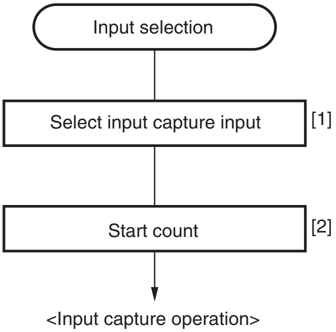


Figure 9.9 Example of Toggle Output Operation

1. Example of Input Capture Operation Setting Procedure

Figure 9.10 shows an example of the input capture operation setting procedure.



[1] Designate TGR as an input capture register by means of TIOR, and select rising edge, falling edge, or both edges as the input capture source and input signal edge.

[2] Set the CST bit in TSTR to 1 to start the count operation.

Figure 9.10 Example of Input Capture Operation Setting Procedure

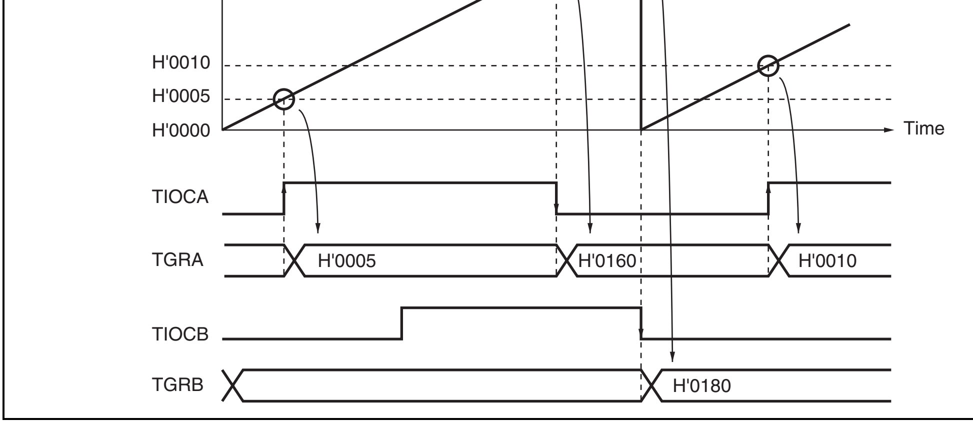
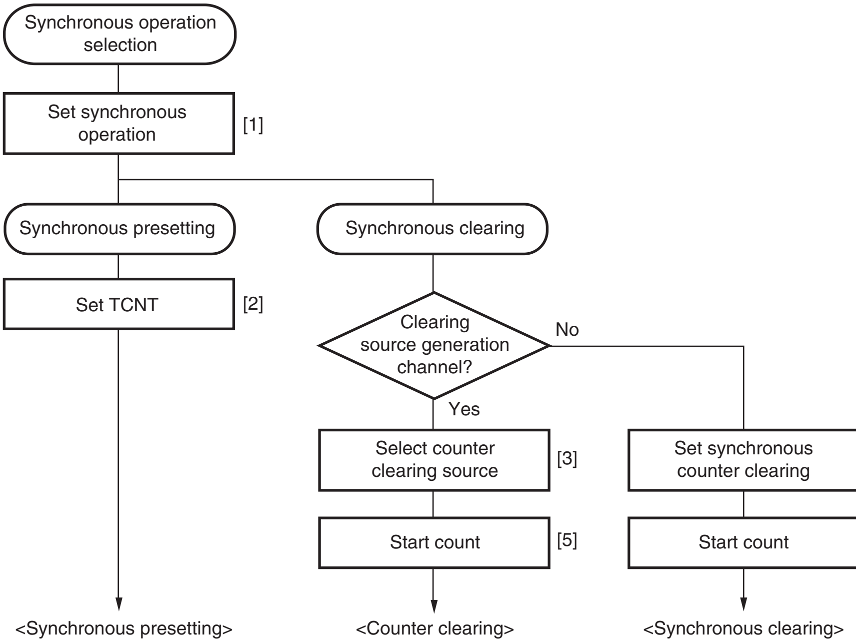


Figure 9.11 Example of Input Capture Operation

Example of Synchronous Operation Setting Procedure:

Figure 9.12 shows an example of the synchronous operation setting procedure.


Synchronous operation selection
Set synchronous operation
[1]
Synchronous presetting
Synchronous clearing
Set TCNT
[2]
Clearing source generation channel?
No
Yes
Select counter clearing source
[3]
Set synchronous counter clearing
Start count
[5]
Start count
<Synchronous presetting>
<Counter clearing>
<Synchronous clearing>

[1] Set to 1 the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation.

[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.

[3] Use bits CCLR2 to CCLR0 in TCR to specify TCNT clearing by input capture/output compare, etc.

[4] Use bits CCLR2 to CCLR0 in TCR to designate synchronous clearing for the counter clearing sourc

[5] Set to 1 the CST bits in TSTR for the relevant channels, to start the count operation.

Figure 9.12 Example of Synchronous Operation Setting Procedure

cycle.

For details of PWM modes, see section 9.4.5, PWM Modes.

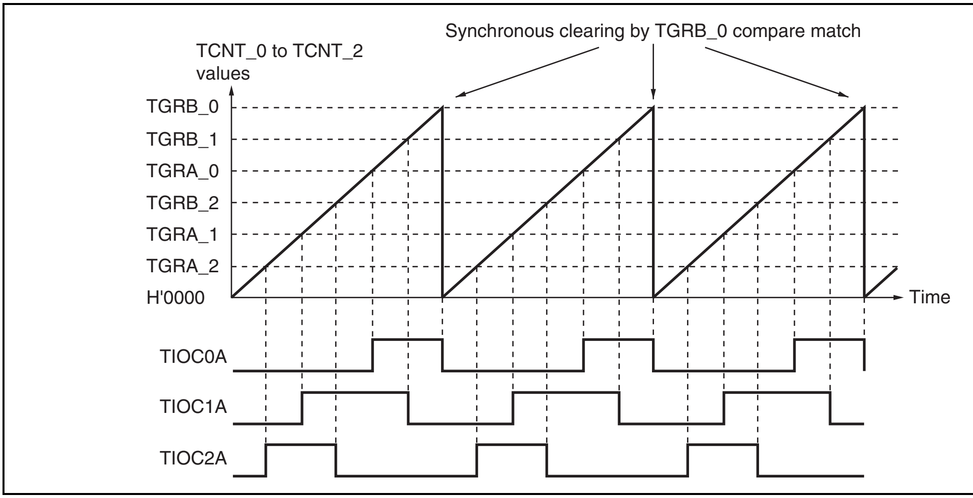


Figure 9.13 Example of Synchronous Operation

Table 9.43 shows the register combinations used in buffer operation.

Table 9.43 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
0	TGRA_0	TGRC_0
	TGRB_0	TGRD_0
	TGRE_0	TGRF_0
3	TGRA_3	TGRC_3
	TGRB_3	TGRD_3
4	TGRA_4	TGRC_4
	TGRB_4	TGRD_4

- When TGR is an output compare register

  When a compare match occurs, the value in the buffer register for the corresponding transferred to the timer general register.

  This operation is illustrated in figure 9.14.

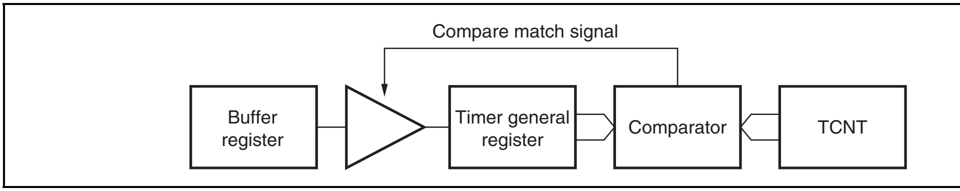
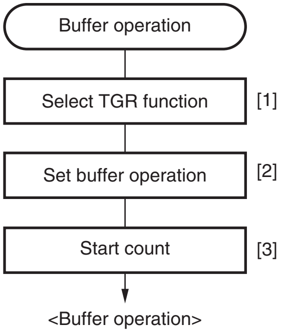


Figure 9.14 Compare Match Buffer Operation

Figure 9.15 Input Capture Buffer Operation

Example of Buffer Operation Setting Procedure: Figure 9.16 shows an example of the operation setting procedure.



[1] Designate TGR as an input capture register or output compare register by means of TIOR.

[2] Designate TGR for buffer operation with bits BFA and BFB in TMDR.

[3] Set the CST bit in TSTR to 1 start the count operation.

Figure 9.16 Example of Buffer Operation Setting Procedure

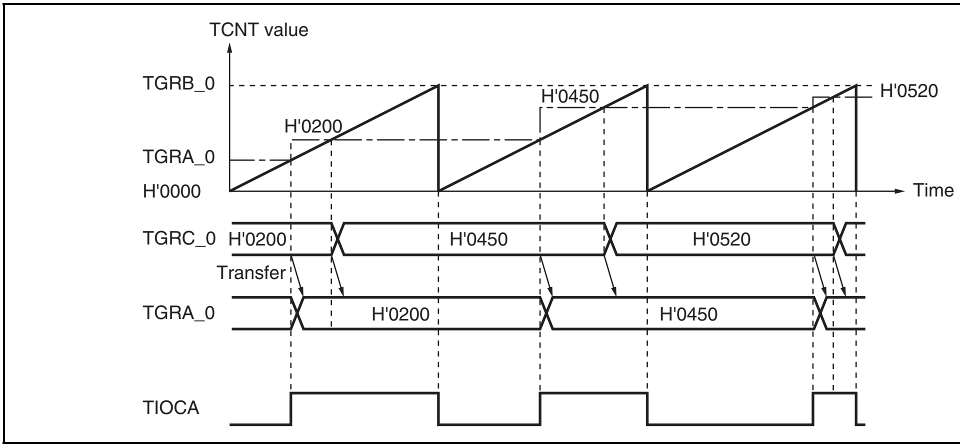


Figure 9.17 Example of Buffer Operation (1)

2. When TGR is an input capture register

   Figure 9.18 shows an operation example in which TGRA has been designated as an i
   capture register, and buffer operation has been designated for TGRA and TGRC.

   Counter clearing by TGRA input capture has been set for TCNT, and both rising and
   edges have been selected as the TIOCA pin input capture input edge.

   As buffer operation has been set, when the TCNT value is stored in TGRA upon the
   occurrence of input capture A, the value previously stored in TGRA is simultaneousl
   transferred to TGRC.

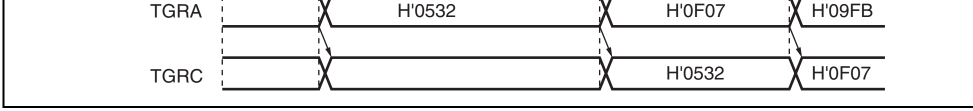


Figure 9.18 Example of Buffer Operation (2)

Selecting Timing for Transfer from Buffer Registers to Timer General Registers in B Operation: The timing for transfer from buffer registers to timer general registers can be in PWM mode 1 or 2 for channel 0 or in PWM mode 1 for channels 3 and 4 by setting the operation transfer mode registers (TBTM_0, TBTM_3, and TBTM_4). Either compare m (initial setting) or TCNT clearing can be selected for the transfer timing. TCNT clearing a transfer timing is one of the following cases.

- When TCNT overflows (H'FFFF to H'0000)
- When H'0000 is written to TCNT during counting
- When TCNT is cleared to H'0000 under the condition specified in the CCLR2 to CCL in TCR

Note: TBTM must be modified only while TCNT stops.

Figure 9.19 shows an operation example in which PWM mode 1 is designated for channe buffer operation is designated for TGRA_0 and TGRC_0. The settings used in this examp TCNT_0 clearing by compare match B, 1 output at compare match A, and 0 output at co match B. The TTSA bit in TBTM_0 is set to 1.

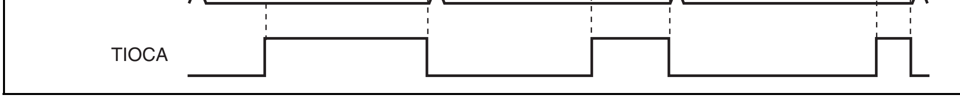


Figure 9.19 Example of Buffer Operation When TCNT_0 Clearing is Selected for to TGRA_0 Transfer Timing

9.4.4 Cascaded Operation

In cascaded operation, two 16-bit counters for different channels are used together as a 3 counter.

This function works by counting the channel 1 counter clock upon overflow/underflow TCNT_2 as set in bits TPSC0 to TPSC2 in TCR.

Underflow occurs only when the lower 16-bit TCNT is in phase-counting mode.

Table 9.44 shows the register combinations used in cascaded operation.

Note: When phase counting mode is set for channel 1, the counter clock setting is inva counters operates independently in phase counting mode.

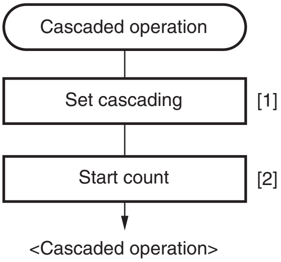
Table 9.44 Cascaded Combinations

Combination	Upper 16 Bits	Lower 16 Bits
Channels 1 and 2	TCNT_1	TCNT_2

For simultaneous input capture of TCNT_1 and TCNT_2 during cascaded operation, ad input capture input pins can be specified by the input capture control register (TICCR). capture in cascade connection, refer to section 9.7.22, Simultaneous Capture of TCNT_ TCNT_2 in Cascade Connection.

	I1AE bit = 1	TIOC2A, TIOC1A
Input capture from TCNT_2 to TGRB_2	I1BE bit = 0 (initial value)	TIOC2B
	I1BE bit = 1	TIOC2B, TIOC1B

Example of Cascaded Operation Setting Procedure: Figure 9.20 shows an example of setting procedure for cascaded operation.



[1] Set bits TPSC2 to TPSC0 in the channel 1 TCR to B'1111 to select TCNT_2 overflow/underflow counting.

[2] Set the CST bit in TSTR for the upper and lower channel to 1 to start the count operation.

Figure 9.20 Cascaded Operation Setting Procedure

Cascaded Operation Example (a): Figure 9.21 illustrates the operation when TCNT_2 overflow/underflow counting has been set for TCNT_1 and phase counting mode has bee designated for channel 2.

TCNT_1 is incremented by TCNT_2 overflow and decremented by TCNT_2 underflow.

TCNT_1 and TCNT_2 have been cascaded and the I2AE bit in TICCR has been set to 1
the TIOC2A pin in the TGRA_1 input capture conditions. In this example, the IOA0 to
in TIOR_1 have selected the TIOC1A rising edge for the input capture timing while the
IOA3 bits in TIOR_2 have selected the TIOC2A rising edge for the input capture timing

Under these conditions, the rising edge of both TIOC1A and TIOC2A is used for the TC
input capture condition. For the TGRA_2 input capture condition, the TIOC2A rising ed

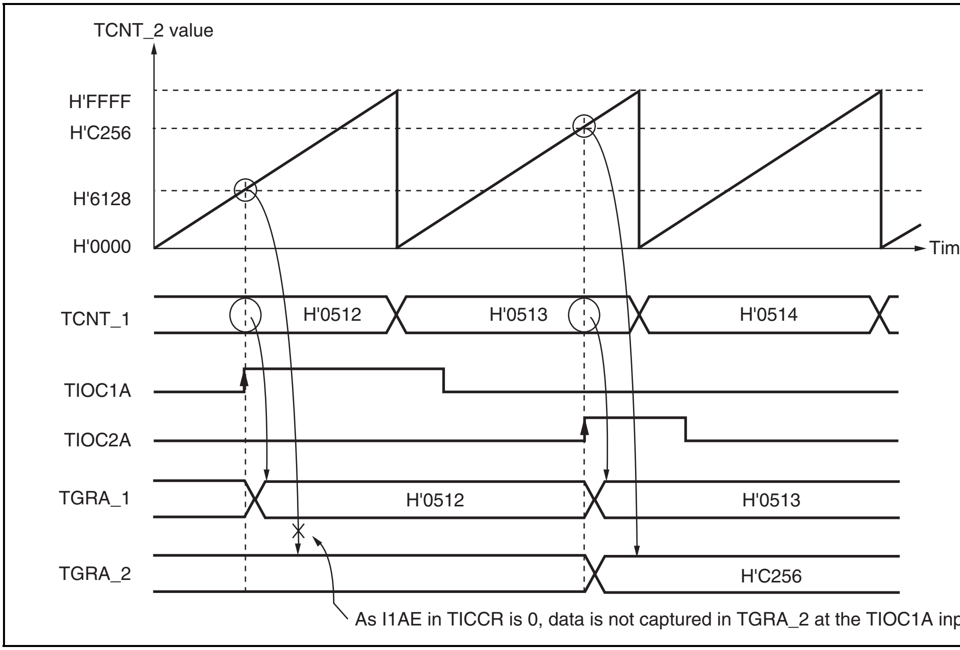


Figure 9.22 Cascaded Operation Example (b)

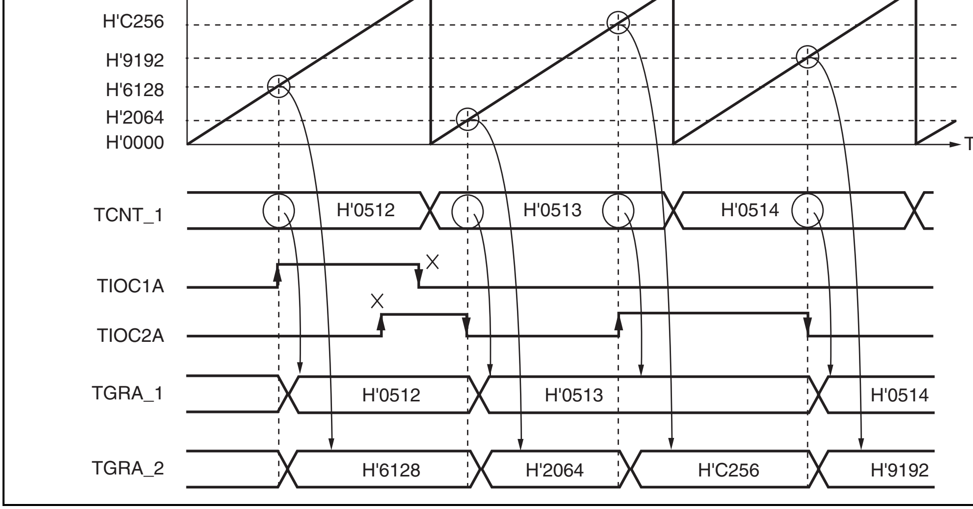


Figure 9.23 Cascaded Operation Example (c)

Cascaded Operation Example (d) in SH7125: Figure 9.24 illustrates the operation whe
TCNT_1 and TCNT_2 have been cascaded and the I2AE bit in TICCR has been set to 1 t
the TIOC2A pin in the TGRA_1 input capture conditions. In this example, the IOA0 to IO
in TIOR_1 have selected TGRA_0 compare match or input capture occurrence for the inp
capture timing while the IOA0 to IOA3 bits in TIOR_2 have selected the TIOC2A rising
the input capture timing.

Under these conditions, as TIOR_1 has selected TGRA_0 compare match or input captur
occurrence for the input capture timing, the TIOC2A edge is not used for TGRA_1 input
condition although the I2AE bit in TICCR has been set to 1.

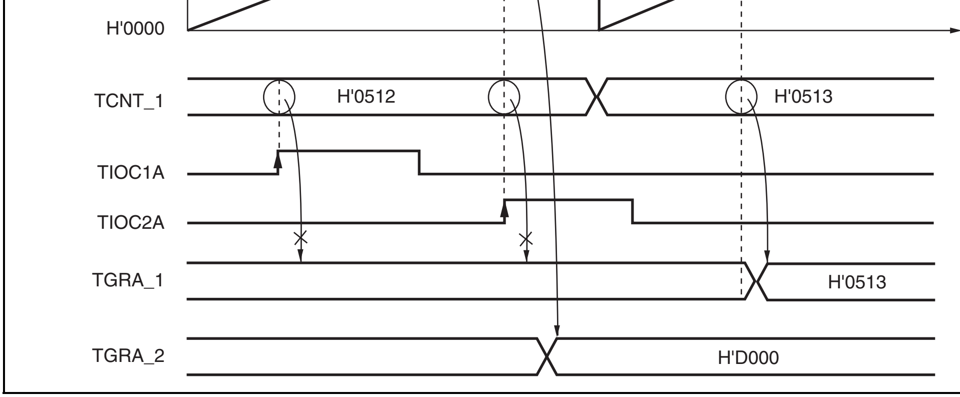


Figure 9.24 Cascaded Operation Example (d)

There are two PWM modes, as described below.

1. PWM mode 1

   PWM output is generated from the TIOCA and TIOCC pins by pairing TGRA with T TGRC with TGRD. The output specified by bits IOA0 to IOA3 and IOC0 to IOC3 in output from the TIOCA and TIOCC pins at compare matches A and C, and the output specified by bits IOB0 to IOB3 and IOD0 to IOD3 in TIOR is output at compare matc and D. The initial output value is the value set in TGRA or TGRC. If the set values of TGRs are identical, the output value does not change when a compare match occurs.

   In PWM mode 1, a maximum 8-phase PWM output is possible.

2. PWM mode 2

   PWM output is generated using one TGR as the cycle register and the others as duty r The output specified in TIOR is performed by means of compare matches. Upon cour clearing by a synchronization register compare match, the output value of each pin is value set in TIOR. If the set values of the cycle and duty registers are identical, the ou value does not change when a compare match occurs.

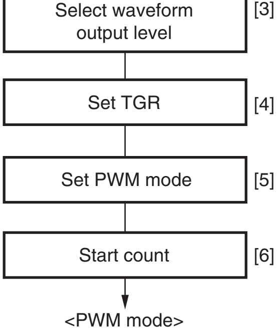
   In PWM mode 2, a maximum 8-phase PWM output is possible in combination use wi synchronous operation.

The correspondence between PWM output pins and registers is shown in table 9.46.

2	TGRA_2	TIOC2A*	TIOC2A*
	TGRB_2		TIOC2B*
3	TGRA_3	TIOC3A	Cannot be set
	TGRB_3		Cannot be set
	TGRC_3	TIOC3C	Cannot be set
	TGRD_3		Cannot be set
4	TGRA_4	TIOC4A	Cannot be set
	TGRB_4		Cannot be set
	TGRC_4	TIOC4C	Cannot be set
	TGRD_4		Cannot be set

Notes: In PWM mode 2, PWM output is not possible for the TGR register in which the pe

* Supported only by the SH7125.



[4] Set the cycle in the TGR selected in [2], and set the duty in the other TGR.

[5] Select the PWM mode with bits MD3 to MD0 in TMDR.

[6] Set the CST bit in TSTR to 1 to start the count operation.

Figure 9.25 Example of PWM Mode Setting Procedure

Examples of PWM Mode Operation: Figure 9.26 shows an example of PWM mode 1 o

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the initial output value and output value, and 1 is set as the TGRB output value.

In this case, the value set in TGRA is used as the period, and the values set in the TGRB r are used as the duty levels.

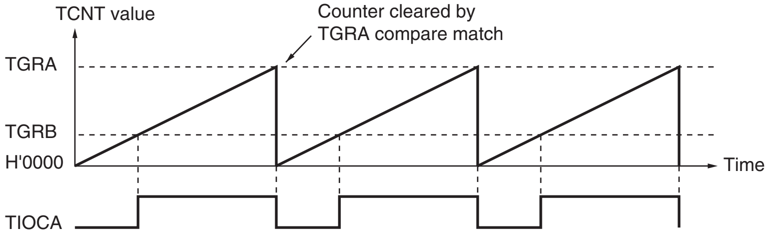


Figure 9.26 Example of PWM Mode Operation (1)

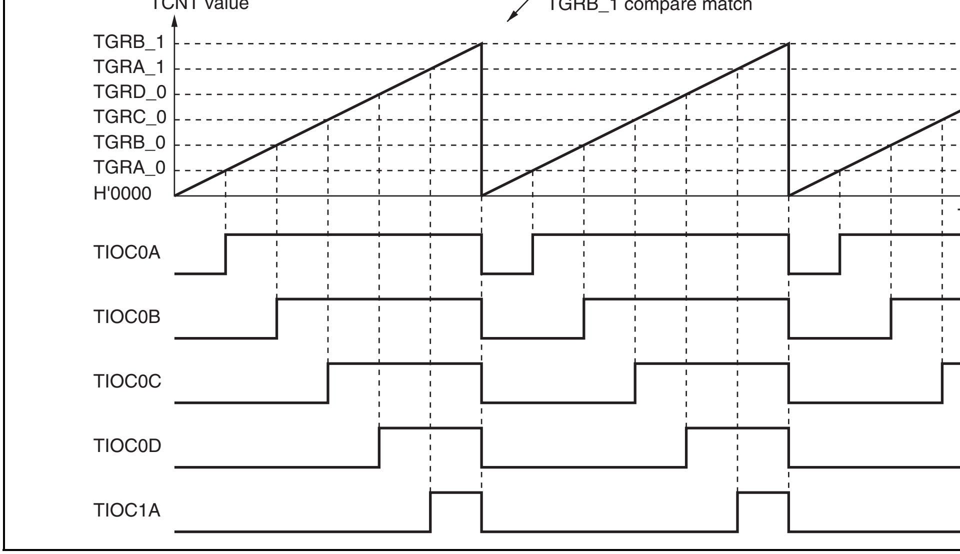


Figure 9.27 Example of PWM Mode Operation (2)

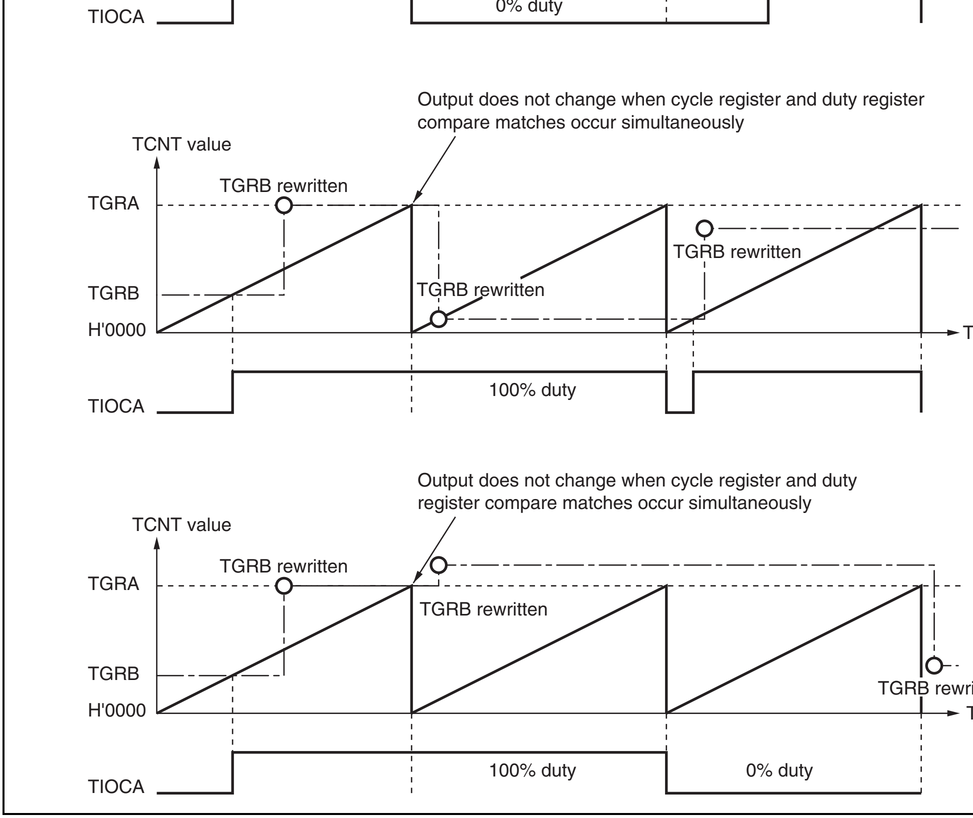

TIOCA
0% duty
Output does not change when cycle register and duty register compare matches occur simultaneously
TCNT value
TGRB rewritten
TGRA
TGRB rewritten
TGRB
TGRB rewritten
H'0000
100% duty
TIOCA
Output does not change when cycle register and duty register compare matches occur simultaneously
TCNT value
TGRB rewritten
TGRA
TGRB rewritten
TGRB
TGRB rewri
H'0000
100% duty
0% duty
TIOCA

Figure 9.28 Example of PWM Mode Operation (3)

This can be used for two-phase encoder pulse input.

If overflow occurs when TCNT is counting up, the TCFV flag in TSR is set; if underflo
when TCNT is counting down, the TCFU flag is set.

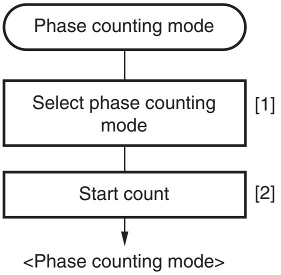
The TCFD bit in TSR is the count direction flag. Reading the TCFD flag reveals whethe
counting up or down.

Table 9.47 shows the correspondence between external clock pins and channels.

Table 9.47 Phase Counting Mode Clock Input Pins

	External Clock Pins	
Channels	**A-Phase**	**B-Phase**
When channel 1 is set to phase counting mode	TCLKA	TCLKB
When channel 2 is set to phase counting mode	TCLKC	TCLKD

Example of Phase Counting Mode Setting Procedure: Figure 9.29 shows an example
phase counting mode setting procedure.



[1] Select phase counting mode with bits MD3 to MD0 in TMDR.

[2] Set the CST bit in TSTR to 1 to start the count operation.

Figure 9.29 Example of Phase Counting Mode Setting Procedure

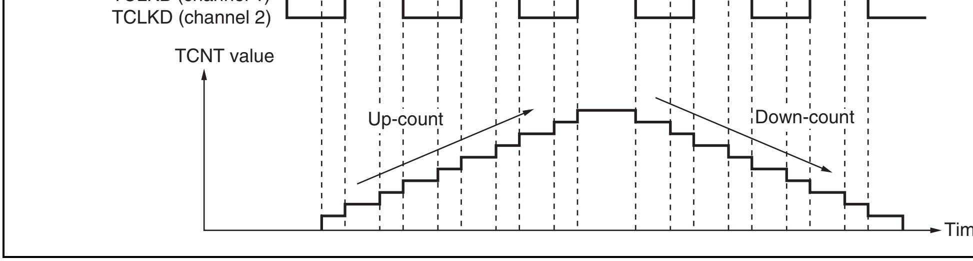


Figure 9.30 Example of Phase Counting Mode 1 Operation

Table 9.48 Up/Down-Count Conditions in Phase Counting Mode 1

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	
↓	Low level	

[Legend]

↑: Rising edge

↓: Falling edge

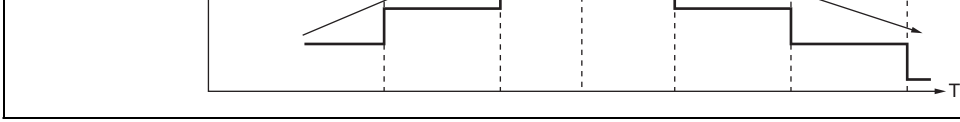


Figure 9.31 Example of Phase Counting Mode 2 Operation

Table 9.49 Up/Down-Count Conditions in Phase Counting Mode 2

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Don't care
Low level	↓	Don't care
↑	Low level	Don't care
↓	High level	Up-count
High level	↓	Don't care
Low level	↑	Don't care
↑	High level	Don't care
↓	Low level	Down-count

[Legend]

↑: Rising edge

↓: Falling edge

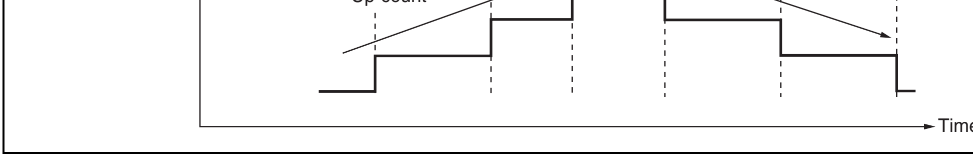


Figure 9.32 Example of Phase Counting Mode 3 Operation

Table 9.50 Up/Down-Count Conditions in Phase Counting Mode 3

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Don't care
Low level	↓	Don't care
↑	Low level	Don't care
↓	High level	Up-count
High level	↓	Down-count
Low level	↑	Don't care
↑	High level	Don't care
↓	Low level	Don't care

[Legend]

↑: Rising edge

↓: Falling edge

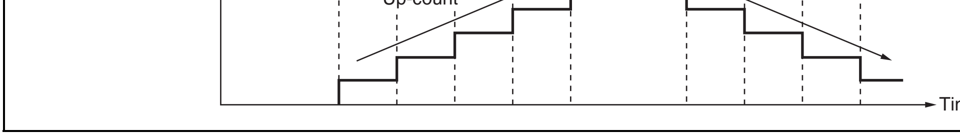


Figure 9.33 Example of Phase Counting Mode 4 Operation

Table 9.51 Up/Down-Count Conditions in Phase Counting Mode 4

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	Don't care
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	Don't care
↓	Low level	

[Legend]

↑: Rising edge

↓: Falling edge

source, and the pulse widths of 2-phase encoder 4-multiplication pulses are detected.

TGRA_1 and TGRB_1 for channel 1 are designated for input capture, and channel 0 TGR
TGRC_0 compare matches are selected as the input capture source and store the up/down
values for the control periods.

This procedure enables the accurate detection of position and speed.

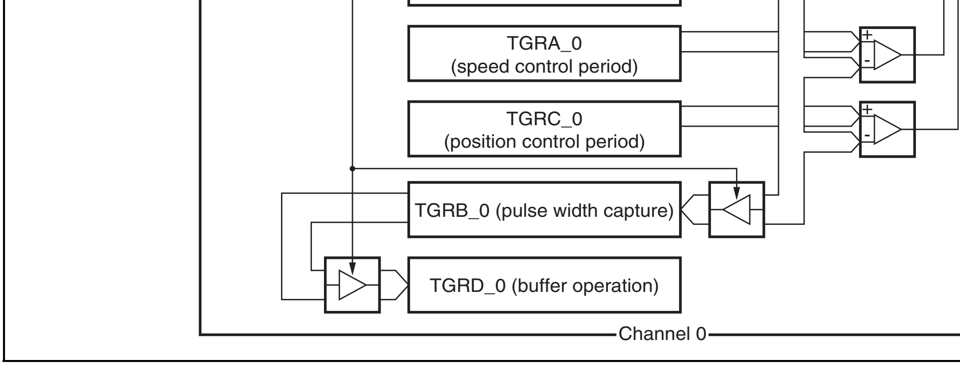

TGRA_0
(speed control period)
TGRC_0
(position control period)
TGRB_0 (pulse width capture)
TGRD_0 (buffer operation)
+
-
+
-
Channel 0

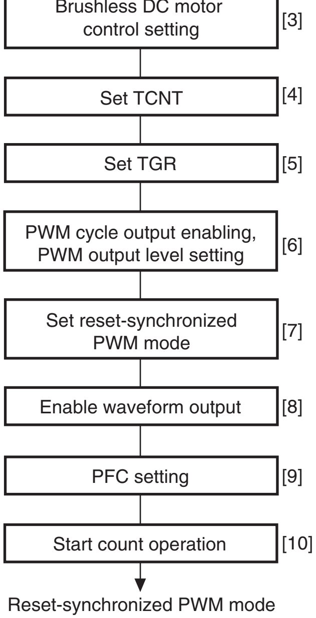
Figure 9.34   Phase Counting Mode Application Example

Table 9.52 Output Pins for Reset-Synchronized PWM Mode

Channel	Output Pin	Description
3	TIOC3B	PWM output pin 1
	TIOC3D	PWM output pin 1' (negative-phase waveform of PWM out
4	TIOC4A	PWM output pin 2
	TIOC4C	PWM output pin 2' (negative-phase waveform of PWM out
	TIOC4B	PWM output pin 3
	TIOC4D	PWM output pin 3' (negative-phase waveform of PWM out

Table 9.53 Register Settings for Reset-Synchronized PWM Mode

Register	Description of Setting
TCNT_3	Initial setting of H'0000
TCNT_4	Initial setting of H'0000
TGRA_3	Set count cycle for TCNT_3
TGRB_3	Sets the turning point for PWM waveform output by the TIOC3B and TIOC3I
TGRA_4	Sets the turning point for PWM waveform output by the TIOC4A and TIOC4(
TGRB_4	Sets the turning point for PWM waveform output by the TIOC4B and TIOC4I


Brushless DC motor control setting
[3]
Set TCNT
[4]
Set TGR
[5]
PWM cycle output enabling, PWM output level setting
[6]
Set reset-synchronized PWM mode
[7]
Enable waveform output
[8]
PFC setting
[9]
Start count operation
[10]
Reset-synchronized PWM mode

[3] When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCR) and set the feedback signal input source and output chopping or gate signal direct output.

[4] Reset TCNT_3 and TCNT_4 to H'0000.

[5] TGRA_3 is the period register. Set the waveform period value in TGRA_3. Set the transition timing of the PWM output waveforms in TGRB_3, TGRA_4, and TGRB_4. Set times within the compare-match range of TCNT_3.
$X \leq$ TGRA_3 (X: set value).

[6] Select enabling/disabling of toggle output synchronized with the PMW cycle using bit PSYE in the timer output control register (TOCR1), and set the PWM output level with bits OLSP and OLSN. When specifying the PWM output level by using TOLBR as a buffer for TOCR2, see figure 9.3.

[7] Set bits MD3 to MD0 in TMDR_3 to B'1000 to select the reset-synchronized PWM mode. Do not set to TMDR_

[8] Set the enabling/disabling of the PWM waveform output pin in TOER.

[9] Set the port control register and the port I/O register.

[10] Set the CST3 bit in the TSTR to 1 to start the count operation.

Note: The output waveform starts to toggle operation at the point of TCNT_3 = TGRA_3 = X by setting X = TGRA, i.e., cycle = duty.

Figure 9.35 Procedure for Selecting Reset-Synchronized PWM Mode

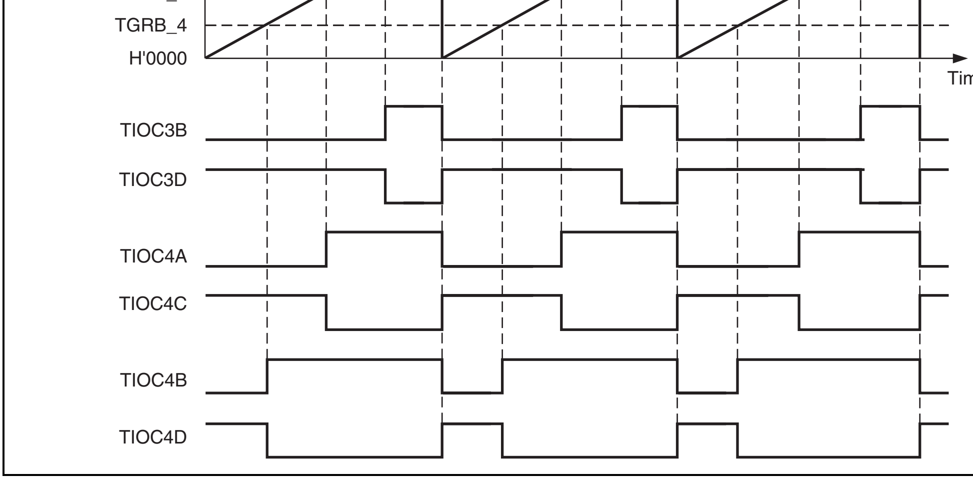


Figure 9.36 Reset-Synchronized PWM Mode Operation Example (When TOCR's OLSN = 1 and OLSP = 1)

A function to directly cut off the PWM output by using an external signal is supported a
function.

Table 9.54 Output Pins for Complementary PWM Mode

Channel	Output Pin	Description
3	TIOC3A	Toggle output synchronized with PWM period (or I/C
	TIOC3B	PWM output pin 1
	TIOC3C	I/O port*
	TIOC3D	PWM output pin 1' (non-overlapping negative-phase waveform of PWM PWM output without non-overlapping interval is also
4	TIOC4A	PWM output pin 2
	TIOC4B	PWM output pin 3
	TIOC4C	PWM output pin 2' (non-overlapping negative-phase waveform of PWM PWM output without non-overlapping interval is also
	TIOC4D	PWM output pin 3' (non-overlapping negative-phase waveform of PWM PWM output without non-overlapping interval is also

Note: * Avoid setting the TIOC3C pin as a timer I/O pin in the complementary PWM r

		register	
4	TCNT_4	Up-count start, initialized to H'0000	Maskable by TRW setting*
	TGRA_4	PWM output 2 compare register	Maskable by TRW setting*
	TGRB_4	PWM output 3 compare register	Maskable by TRW setting*
	TGRC_4	PWM output 2/TGRA_4 buffer register	Always readable/w
	TGRD_4	PWM output 3/TGRB_4 buffer register	Always readable/w
Timer dead time data register (TDDR)		Set TCNT_4 and TCNT_3 offset value (dead time value)	Maskable by TRW setting*
Timer cycle data register (TCDR)		Set TCNT_4 upper limit value (1/2 carrier cycle)	Maskable by TRW setting*
Timer cycle buffer register (TCBR)		TCDR buffer register	Always readable/w
Subcounter (TCNTS)		Subcounter for dead time generation	Read-only
Temporary register 1 (TEMP1)		PWM output 1/TGRB_3 temporary register	Not readable/writa
Temporary register 2 (TEMP2)		PWM output 2/TGRA_4 temporary register	Not readable/writa
Temporary register 3 (TEMP3)		PWM output 3/TGRB_4 temporary register	Not readable/writa

Note: * Access can be enabled or disabled according to the setting of bit 0 (RWE) in T (timer read/write enable register).

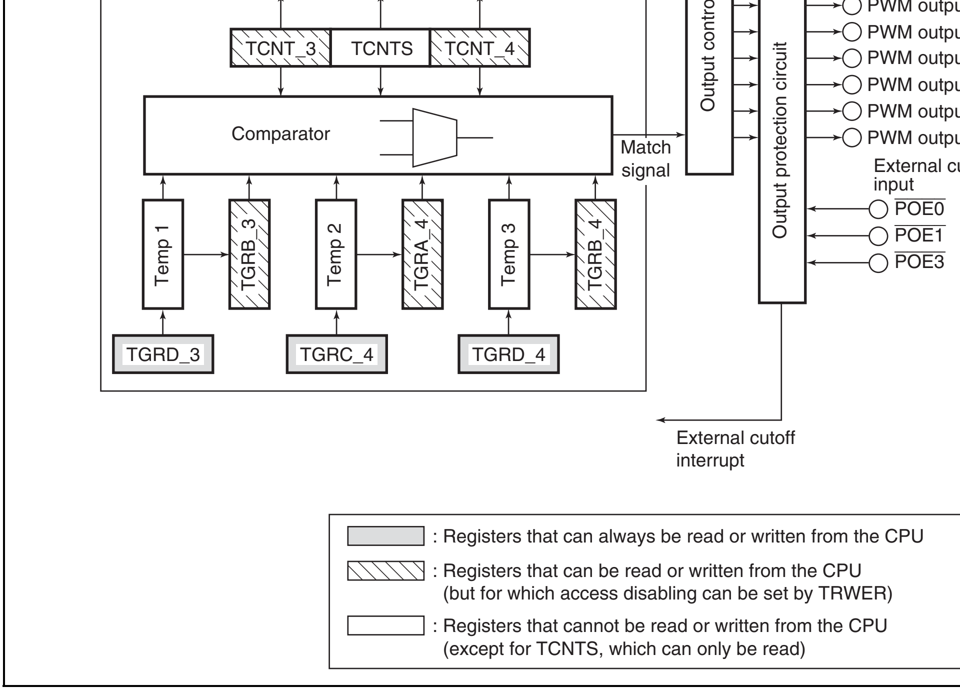
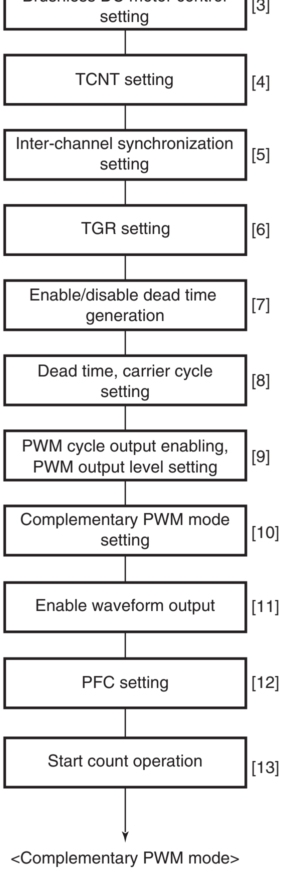

TCNT_3
TCNTS
TCNT_4
Comparator
Match signal
Temp 1
TGRB_3
Temp 2
TGRA_4
Temp 3
TGRB_4
TGRD_3
TGRC_4
TGRD_4
Output contro
Output protection circuit
PWM outpu
PWM outpu
PWM outpu
PWM outpu
PWM outpu
PWM outpu
External cu
input
$\overline{\text{POE0}}$
$\overline{\text{POE1}}$
$\overline{\text{POE3}}$
External cutoff interrupt
: Registers that can always be read or written from the CPU
: Registers that can be read or written from the CPU (but for which access disabling can be set by TRWER)
: Registers that cannot be read or written from the CPU (except for TCNTS, which can only be read)

Figure 9.37 Block Diagram of Channels 3 and 4 in Complementary PWM M


Brushless DC motor control setting
[3]
TCNT setting
[4]
Inter-channel synchronization setting
[5]
TGR setting
[6]
Enable/disable dead time generation
[7]
Dead time, carrier cycle setting
[8]
PWM cycle output enabling, PWM output level setting
[9]
Complementary PWM mode setting
[10]
Enable waveform output
[11]
PFC setting
[12]
Start count operation
[13]
<Complementary PWM mode>

[3] When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCR) and set the feedback signal input source and output chopping or gate signal direct output.

[4] Set the dead time in TCNT_3. Set TCNT_4 to H'0000.

[5] Set only when restarting by a synchronous clear from another channel during complementary PWM mode operation. In this case, synchronize the channel generating the synchronous clear with channels 3 and 4 using the timer synchro register (TSYR).

[6] Set the output PWM duty in the duty registers (TGRB_3, TGRA_4, TGRB_4) and buffer registers (TGRD_3, TGRC_4, TGRD_4). Set the same initial value in each corresponding TGR.

[7] This setting is necessary only when no dead time should be generated. Make appropriate settings in the timer dead time enable register (TDER) so that no dead time is generated.

[8] Set the dead time in the dead time register (TDDR), 1/2 the carrier cycle in the carrier cycle data register (TCDR) and carrier cycle buffer register (TCBR), and 1/2 the carrier cycle plus the dead time in TGRA_3 and TGRC_3. When no dead time generation is selected, set 1 in TDDR and 1/2 the carrier cycle + 1 in TGRA_3 and TGRC_3.

[9] Select enabling/disabling of toggle output synchronized with the PWM cycle using bit PSYE in the timer output control register 1 (TOCR1), and set the PWM output level with bits OLSP and OLSN. When specifying the PWM output level by using TOLBR as a buffer for TOCR_2, see figure 9.3.

[10] Select complementary PWM mode in timer mode register 3 (TMDR_3). Do not set in TMDR_4.

[11] Set enabling/disabling of PWM waveform output pin output in the timer output master enable register (TOER).

[12] Set the port control register and the port I/O register.

[13] Set bits CST3 and CST4 in TSTR to 1 simultaneously to start the count operation.

Figure 9.38 Example of Complementary PWM Mode Setting Procedure

When the CST bit is set to 1, TCNT_3 counts up to the value set in TGRA_3, then s down-counting when it matches TGRA_3. When the TCNT3 value matches TDDR, counter switches to up-counting, and the operation is repeated in this way.

TCNT_4 is initialized to H'0000.

When the CST bit is set to 1, TCNT_4 counts up in synchronization with TCNT_3, switches to down-counting when it matches TCDR. On reaching H'0000, TCNT4 sw up-counting, and the operation is repeated in this way.

TCNTS is a read-only counter. It need not be initialized.

When TCNT_3 matches TCDR during TCNT_3 and TCNT_4 up/down-counting, do counting is started, and when TCNTS matches TCDR, the operation switches to up- When TCNTS matches TGRA_3, it is cleared to H'0000.

When TCNT_4 matches TDDR during TCNT_3 and TCNT_4 down-counting, up-co started, and when TCNTS matches TDDR, the operation switches to down-counting TCNTS reaches H'0000, it is set with the value in TGRA_3.

TCNTS is compared with the compare register and temporary register in which the is set during the count operation only.

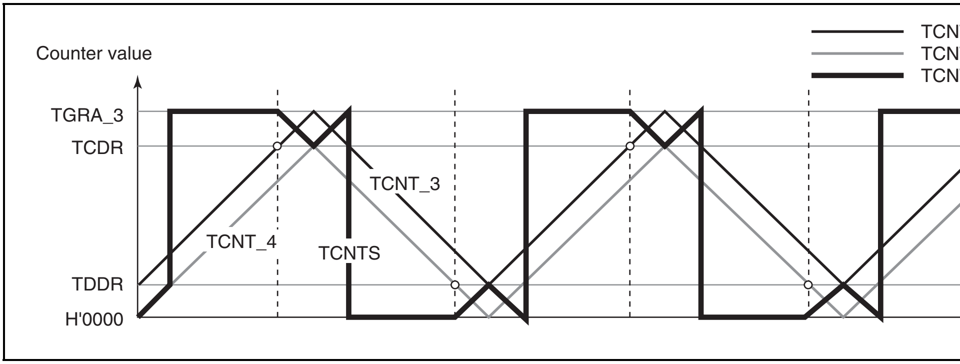


Figure 9.39 Complementary PWM Mode Counter Operation

Data in a compare register is changed by writing the new data to the corresponding bu register. The buffer registers can be read or written at any time.

The data written to a buffer register is constantly transferred to the temporary register interval. Data is not transferred to the temporary register in the Tb interval. Data writt buffer register in this interval is transferred to the temporary register at the end of the interval.

The value transferred to a temporary register is transferred to the compare register wh TCNTS for which the Tb interval ends matches TGRA_3 when counting up, or H'000 counting down. The timing for transfer from the temporary register to the compare reg be selected with bits MD3 to MD0 in the timer mode register (TMDR). Figure 9.40 sh example in which the mode is selected in which the change is made in the trough.

In the Tb interval (Tb1 in figure 9.40) in which data transfer to the temporary register performed, the temporary register has the same function as the compare register, and i compared with the counter. In this interval, therefore, there are two compare match re for one-phase output, with the compare register containing the pre-change data, and th temporary register containing the new data. In this interval, the three counters—TCNT TCNT_4, and TCNTS—and two registers—compare register and temporary register– compared, and PWM output controlled accordingly.

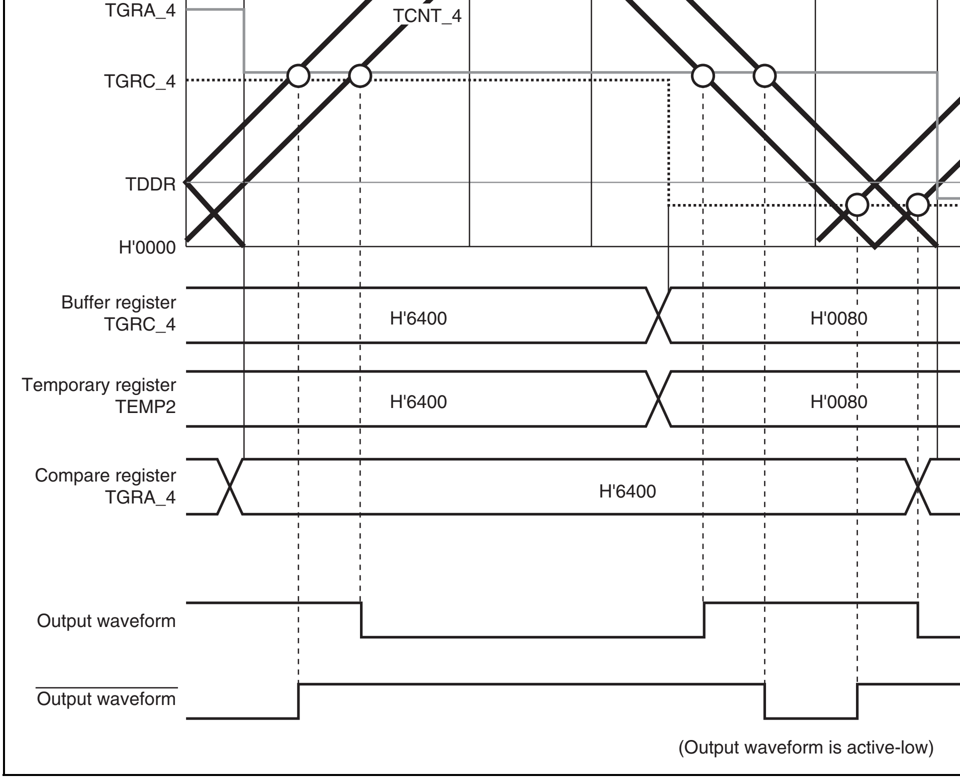


Figure 9.40 Example of Complementary PWM Mode Operation

When dead time is not needed, the TDER bit in the timer dead time enable register (T should be cleared to 0, TGRC_3 and TGRA_3 should be set to 1/2 the PWM carrier c and TDDR should be set to 1.

Set the respective initial PWM duty values in buffer registers TGRD_3, TGRC_4, and TGRD_4.

The values set in the five buffer registers excluding TDDR are transferred simultaneo the corresponding compare registers when complementary PWM mode is set.

Set TCNT_4 to H'0000 before setting complementary PWM mode.

Table 9.56 Registers and Counters Requiring Initialization

Register/Counter	Set Value
TGRC_3	1/2 PWM carrier cycle + dead time Td (1/2 PWM carrier cycle + 1 when dead time ge is disabled by TDER)
TDDR	Dead time Td (1 when dead time generation is disabled by TDER)
TCBR	1/2 PWM carrier cycle
TGRD_3, TGRC_4, TGRD_4	Initial PWM duty value for each phase
TCNT_4	H'0000

Note: The TGRC_3 set value must be the sum of 1/2 the PWM carrier cycle set in TCBR dead time Td set in TDDR. When dead time generation is disabled by TDER, TGR must be set to 1/2 the PWM carrier cycle + 1.

The non-overlap time is set in the timer dead time data register (TDDR). The value s TDDR is used as the TCNT_3 counter start value, and creates non-overlap between and TCNT_4. Complementary PWM mode should be cleared before changing the co TDDR.

6. Dead Time Suppressing

   Dead time generation is suppressed by clearing the TDER bit in the timer dead time register (TDER) to 0. TDER can be cleared to 0 only when 0 is written to it after rea TDER = 1.

   TGRA_3 and TGRC_3 should be set to 1/2 PWM carrier cycle + 1 and the timer dea data register (TDDR) should be set to 1.

   By the above settings, PWM waveforms without dead time can be obtained. Figure an example of operation without dead time.

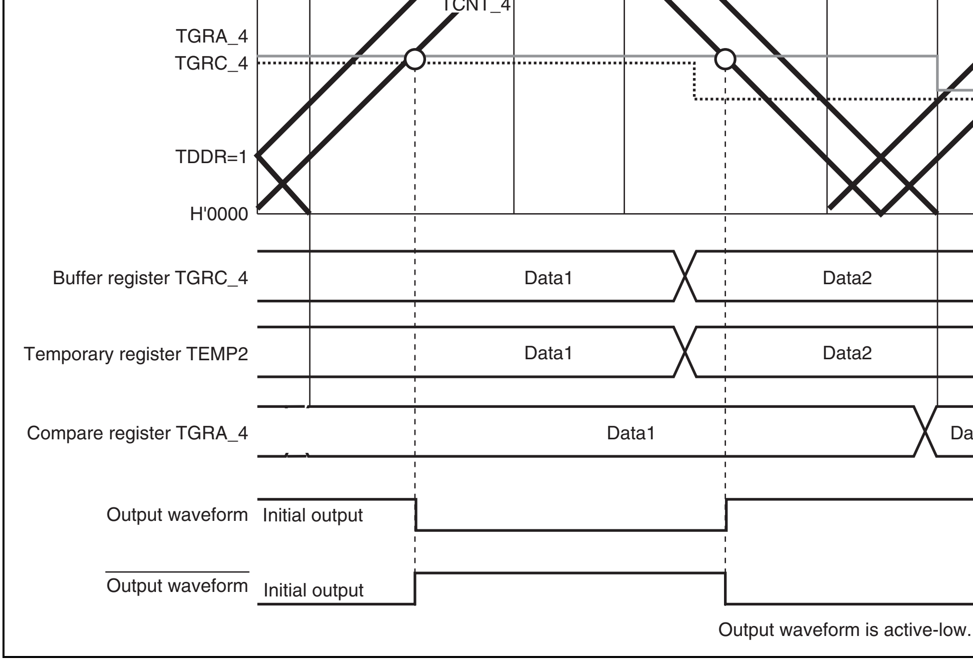


Figure 9.41 Example of Operation without Dead Time

and TCDR in accordance with the transfer timing selected with bits MD3 to MD0 in
mode register (TMDR).

The updated PWM cycle is reflected from the next cycle when the data update is per
the crest, and from the current cycle when performed in the trough. Figure 9.42 illus
operation when the PWM cycle is updated at the crest.

See the following section, Register Data Updating, for the method of updating the da
buffer register.

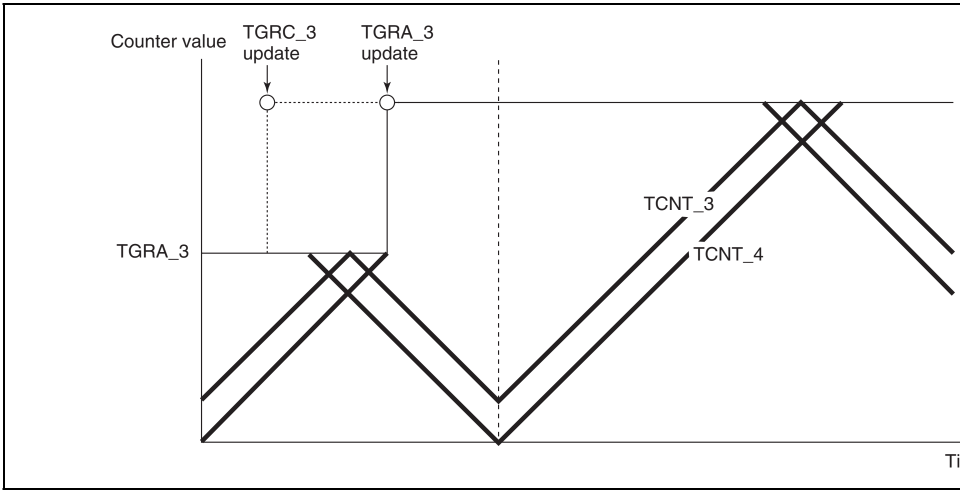


Figure 9.42 Example of PWM Cycle Updating

with bits MD3 to MD0 in the timer mode register (TMDR). Figure 9.43 shows an exa
data updating in complementary PWM mode. This example shows the mode in which
updating is performed at both the counter crest and trough.

When rewriting buffer register data, a write to TGRD_4 must be performed at the end
update. Data transfer from the buffer registers to the temporary registers is performed
simultaneously for all five registers after the write to TGRD_4.

A write to TGRD_4 must be performed after writing data to the registers to be update
when not updating all five registers, or when updating the TGRD_4 data. In this case,
written to TGRD_4 should be the same as the data prior to the write operation.

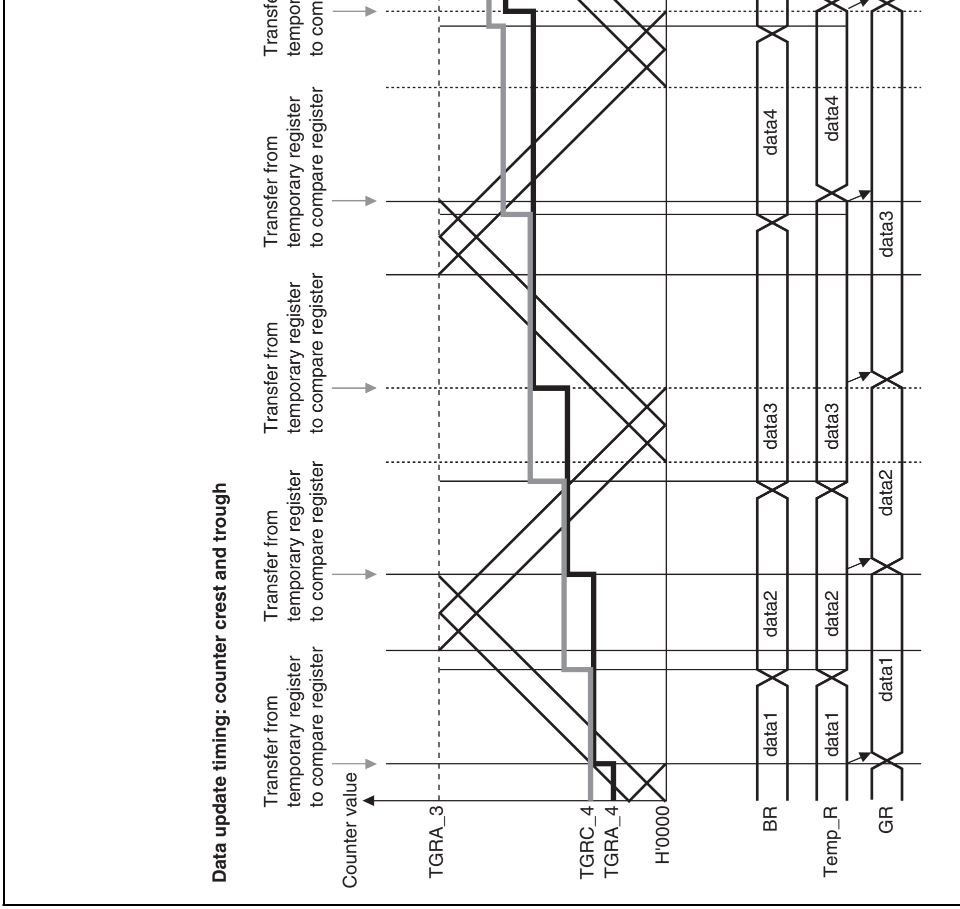

Data update timing: counter crest and trough
Transfer from temporary register to compare register
Transfer from temporary register to compare register
Transfer from temporary register to compare register
Transfer from temporary register to compare register
Transfer from temporary register to compare register
Transfer from temporary register to compare register
Counter value
TGRA_3
TGRC_4
TGRA_4
H'0000
BR
Temp_R
GR
data1
data2
data3
data4
data1
data2
data3
data4
data1
data2
data3

Figure 9.43   Example of Data Update in Complementary PWM Mode

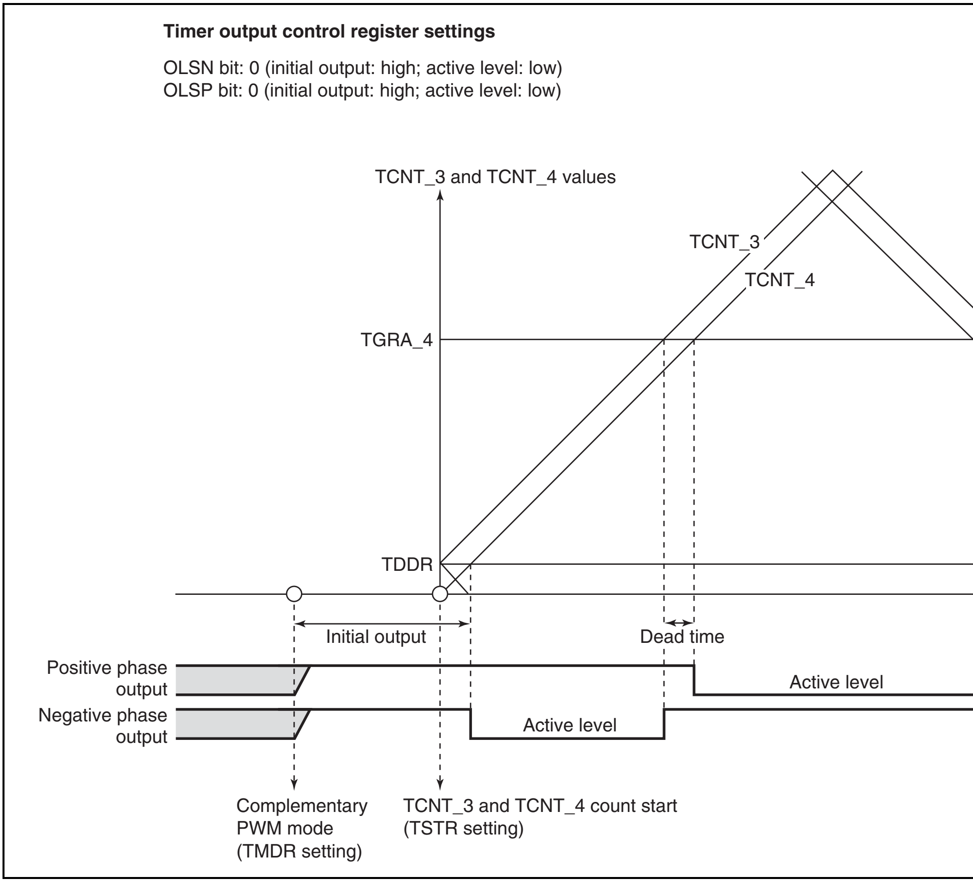

Timer output control register settings
OLSN bit: 0 (initial output: high; active level: low)
OLSP bit: 0 (initial output: high; active level: low)
TCNT_3 and TCNT_4 values
TCNT_3
TCNT_4
TGRA_4
TDDR
Initial output
Dead time
Positive phase output
Negative phase output
Active level
Active level
Complementary PWM mode (TMDR setting)
TCNT_3 and TCNT_4 count start (TSTR setting)

Figure 9.44 Example of Initial Output in Complementary PWM Mode (1)

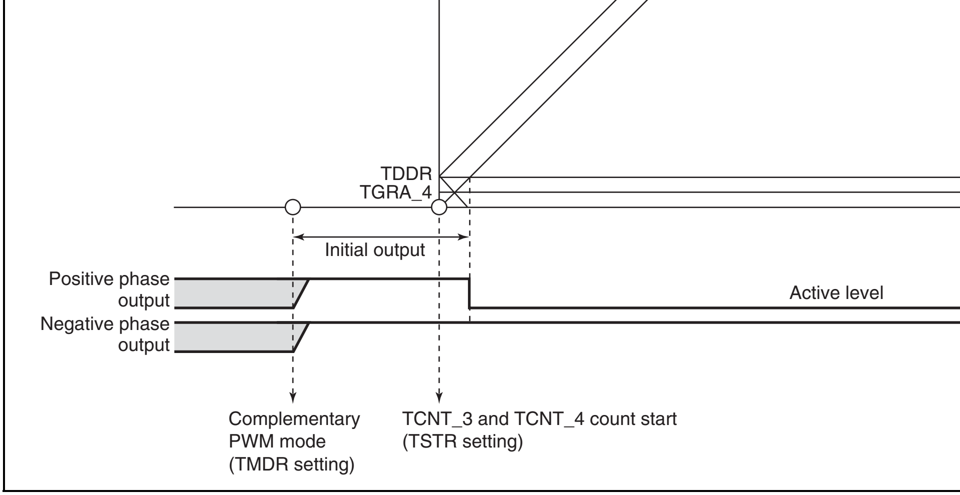

TDDR
TGRA_4
Initial output
Positive phase output
Negative phase output
Active level
Complementary PWM mode (TMDR setting)
TCNT_3 and TCNT_4 count start (TSTR setting)

Figure 9.45 Example of Initial Output in Complementary PWM Mode (2

overlap. Figures 9.46 to 9.48 show examples of waveform generation in complementa mode.

The positive phase/negative phase off timing is generated by a compare-match with th line counter, and the on timing by a compare-match with the dotted-line counter opera a delay of the dead time behind the solid-line counter. In the T1 period, compare-matc turns off the negative phase has the highest priority, and compare-matches occurring p are ignored. In the T2 period, compare-match **c** that turns off the positive phase has th priority, and compare-matches occurring prior to **c** are ignored.

In normal cases, compare-matches occur in the order **a** → **b** → **c** → **d** (or **c** → **d** → **a'** as shown in figure 9.46.

If compare-matches deviate from the **a** → **b** → **c** → **d** order, since the time for which negative phase is off is less than twice the dead time, the figure shows the positive ph being turned on. If compare-matches deviate from the **c** → **d** → **a'** → **b'** order, since t for which the positive phase is off is less than twice the dead time, the figure shows th negative phase is not being turned on.

If compare-match **c** occurs first following compare-match **a**, as shown in figure 9.47, match **b** is ignored, and the negative phase is turned off by compare-match **d**. This is turning off of the positive phase has priority due to the occurrence of compare-match (positive phase off timing) before compare-match **b** (positive phase on timing) (conse the waveform does not change since the positive phase goes from off to off).

Similarly, in the example in figure 9.48, compare-match **a'** with the new data in the te register occurs before compare-match **c**, but other compare-matches occurring up to **c** turns off the positive phase, are ignored. As a result, the negative phase is not turned c

Thus, in complementary PWM mode, compare-matches at turn-off timings take prece and turn-on timing compare-matches that occur before a turn-off timing compare-mat ignored.

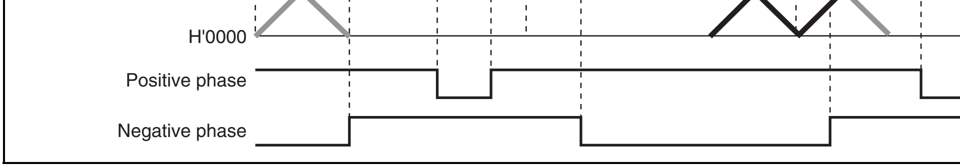


Figure 9.46 Example of Complementary PWM Mode Waveform Output (

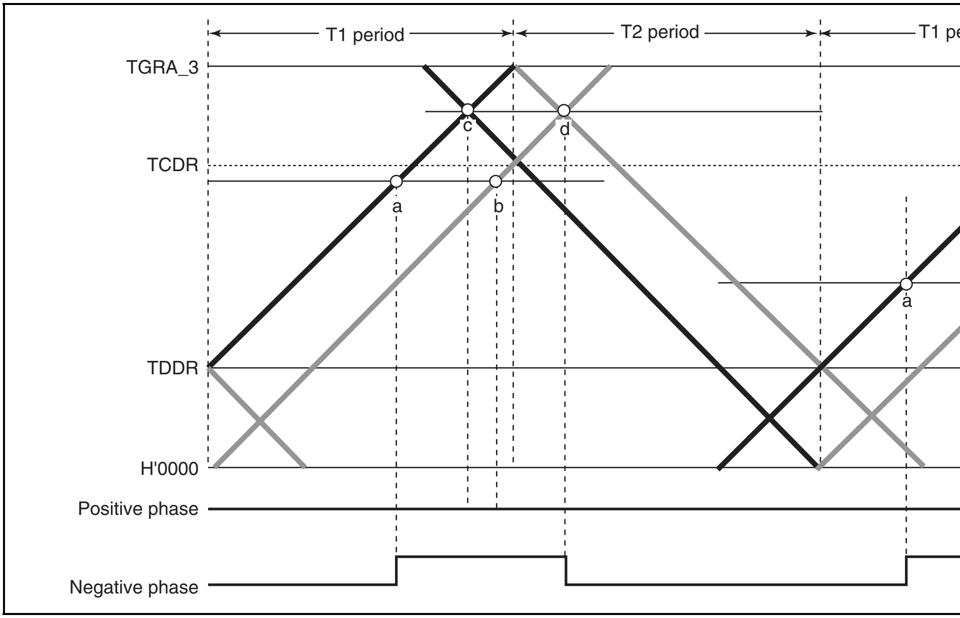


Figure 9.47 Example of Complementary PWM Mode Waveform Output (

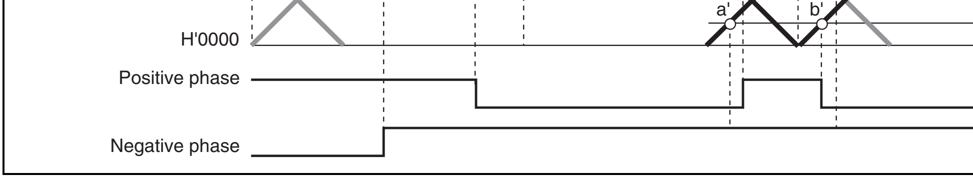


Figure 9.48 Example of Complementary PWM Mode Waveform Output (3

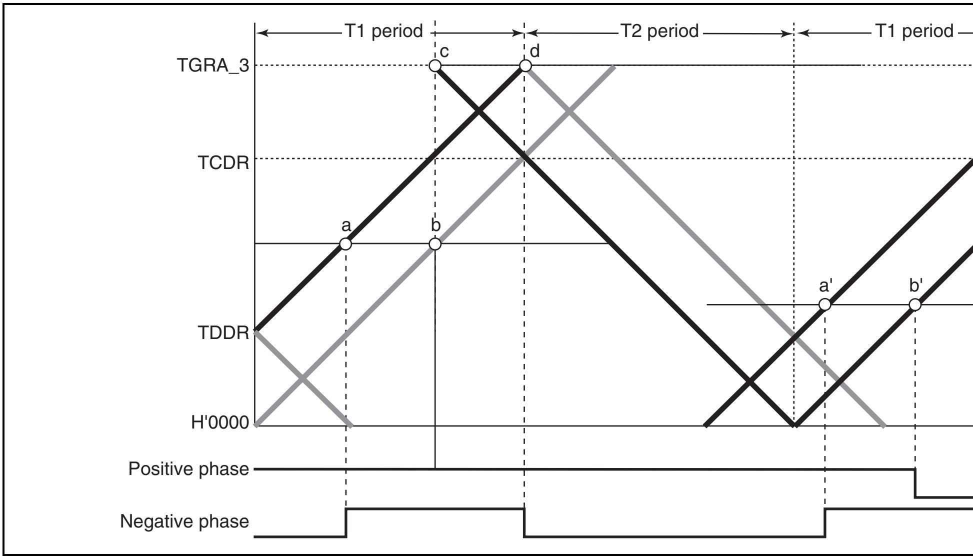


Figure 9.49 Example of Complementary PWM Mode 0% and 100% Waveform Ou

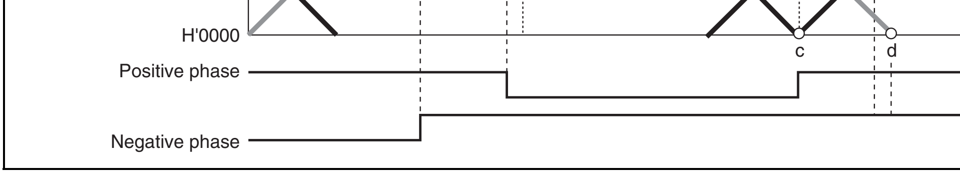


Figure 9.50 Example of Complementary PWM Mode 0% and 100% Waveform C

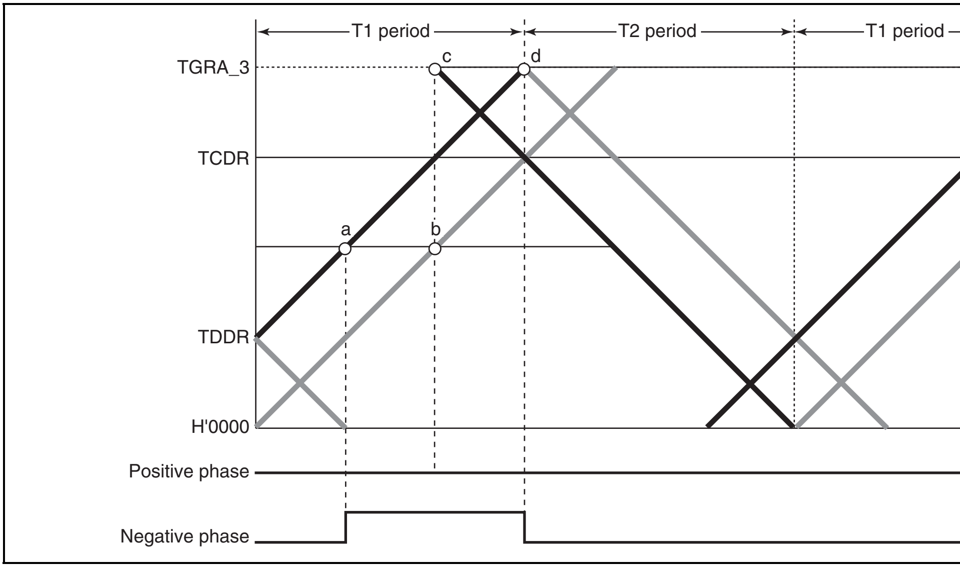


Figure 9.51 Example of Complementary PWM Mode 0% and 100% Waveform C

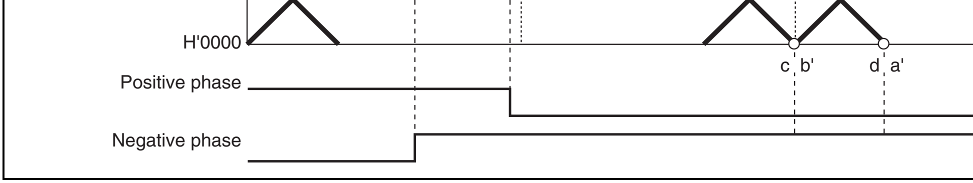


Figure 9.52 Example of Complementary PWM Mode 0% and 100% Waveform Ou

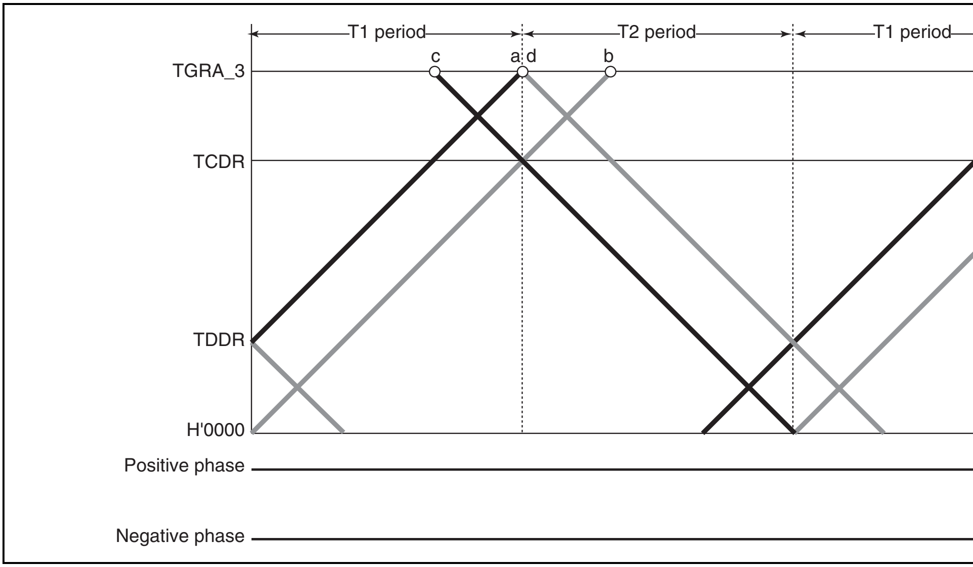


Figure 9.53 Example of Complementary PWM Mode 0% and 100% Waveform Ou

12. Toggle Output Synchronized with PWM Cycle

In complementary PWM mode, toggle output can be performed in synchronization w
PWM carrier cycle by setting the PSYE bit to 1 in the timer output control register (
An example of a toggle output waveform is shown in figure 9.54.

This output is toggled by a compare-match between TCNT_3 and TGRA_3 and a co
match between TCNT4 and H'0000.

The output pin for this toggle output is the TIOC3A pin. The initial output is 1.

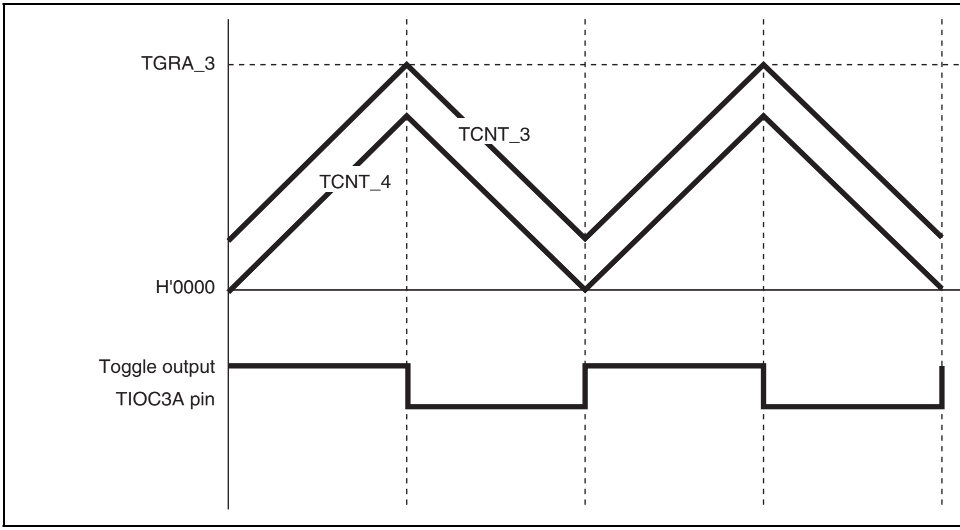


Figure 9.54 Example of Toggle Output Waveform Synchronized with PWM C

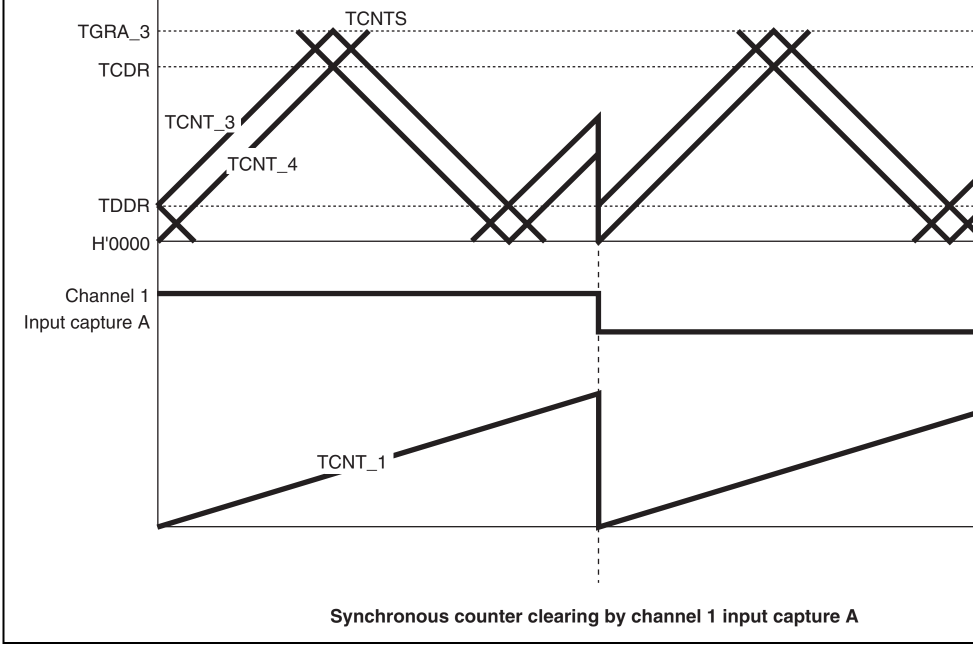


Figure 9.55 Counter Clearing Synchronized with Another Channel

In the MTU2, synchronous clearing generated in channels 0 to 2 in the MTU2 can ca
counter clearing.

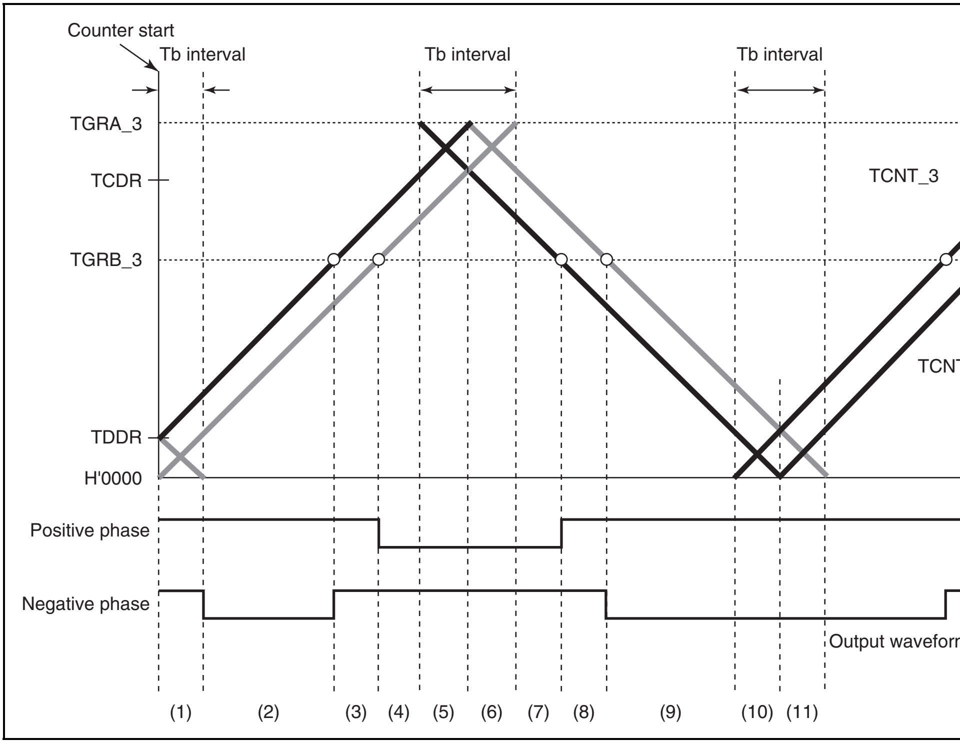
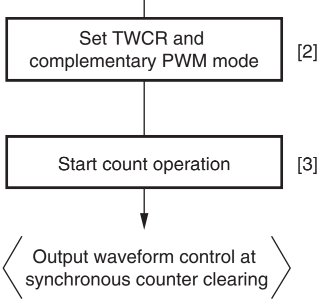


Figure 9.56 Timing for Synchronous Counter Clearing


Set TWCR and complementary PWM mode
[2]
Start count operation
[3]
Output waveform control at synchronous counter clearing

to it to suppress initial value output at counter clearing.

[3] Set bits CST3 and CST4 in TSTR to 1 to start count operation.

Figure 9.57 Example of Procedure for Setting Output Waveform Control at Synch Counter Clearing in Complementary PWM Mode

— Examples of Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Figures 9.58 to 9.61 show examples of output waveform control in which the MTU operates in complementary PWM mode and synchronous counter clearing is gener while the WRE bit in TWCR is set to 1. In the examples shown in figures 9.58 to 9 synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in figu respectively.

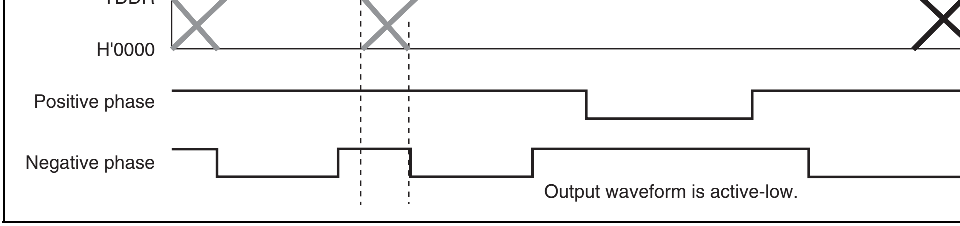


Figure 9.58 Example of Synchronous Clearing in Dead Time during Up-Cou
(Timing (3) in Figure 9.56; Bit WRE of TWCR in MTU2 is 1)

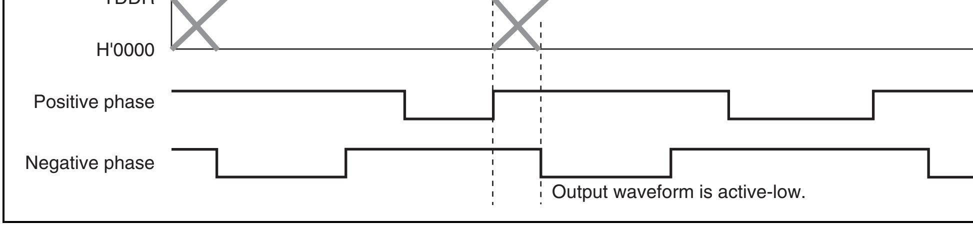


Figure 9.59 Example of Synchronous Clearing in Interval Tb at Crest (Timing (6) in Figure 9.56; Bit WRE of TWCR in MTU2 is 1)

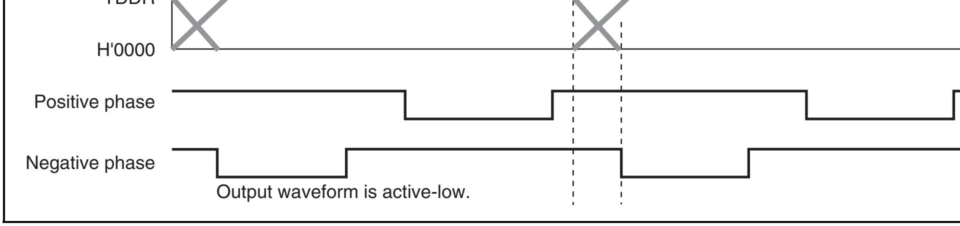


Figure 9.60 Example of Synchronous Clearing in Dead Time during Down-Co
(Timing (8) in Figure 9.56; Bit WRE of TWCR is 1)

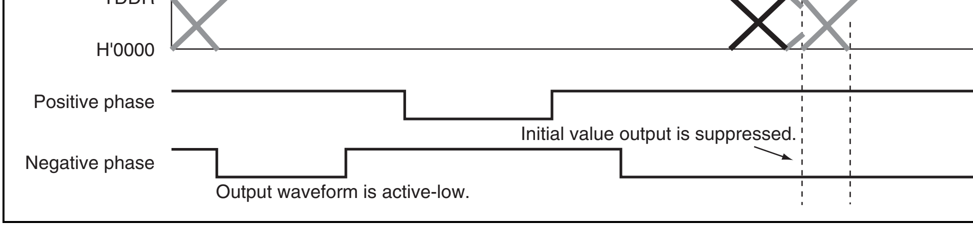

TDDR
H'0000
Positive phase
Negative phase
Initial value output is suppressed.
Output waveform is active-low.

Figure 9.61 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 9.56; Bit WRE of TWCR is 1)

3. Do not set the PWM duty value to H'0000.
4. Do not set the PSYE bit in timer output control register 1 (TOCR1) to 1.

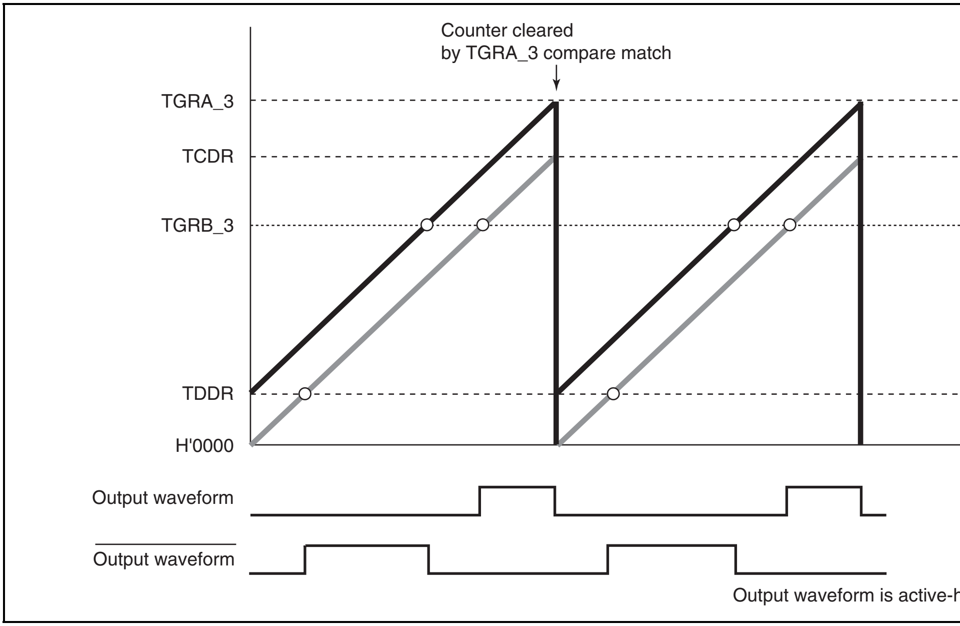
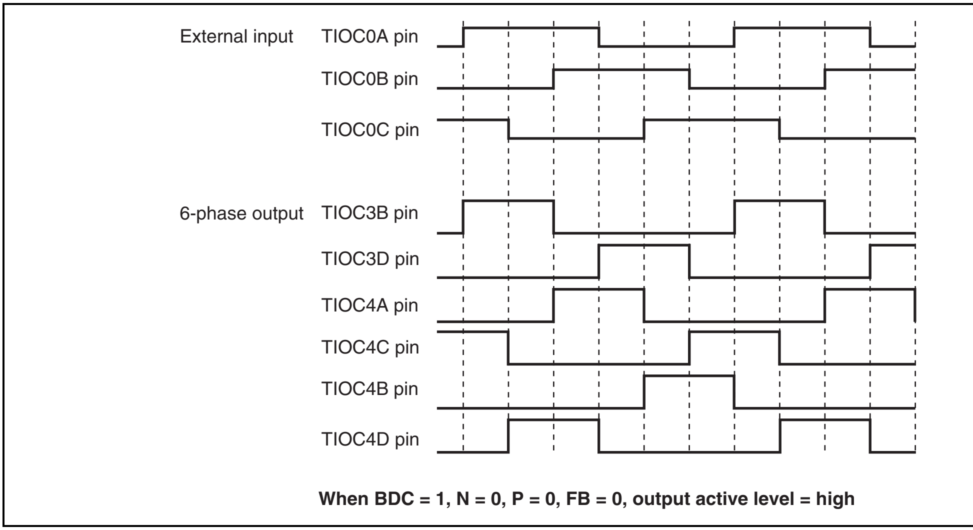


Figure 9.62 Example of Counter Clearing Operation by TGRA_3 Compare M

is cleared to 0 or set to 1.

The drive waveforms are output from the complementary PWM mode 6-phase output With this 6-phase output, in the case of on output, it is possible to use complementary mode output and perform chopping output by setting the N bit or P bit to 1. When the P bit is 0, level output is selected.

The 6-phase output active level (on output level) can be set with the OLSN and OLSP the timer output control register (TOCR) regardless of the setting of the N and P bits.



When BDC = 1, N = 0, P = 0, FB = 0, output active level = high

Figure 9.63 Example of Output Phase Switching by External Input (1)

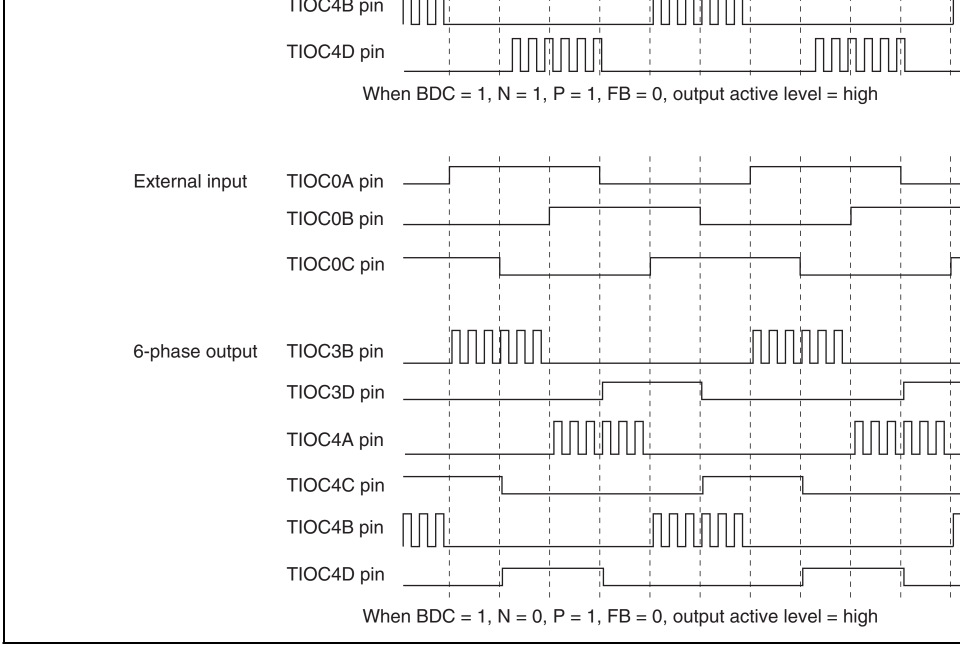
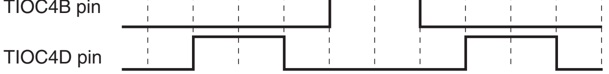
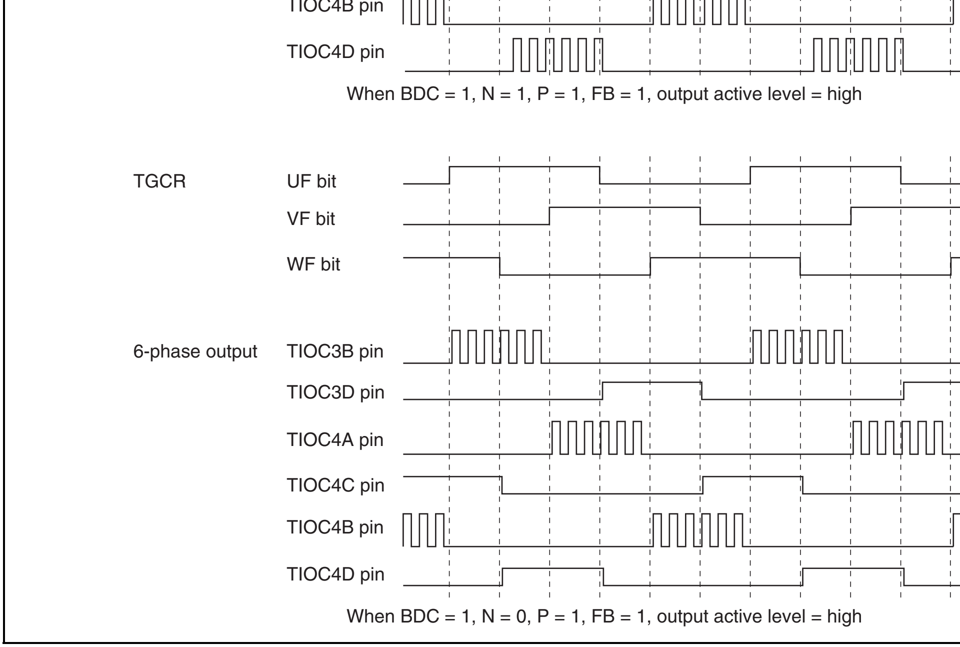


Figure 9.64 Example of Output Phase Switching by External Input (2)



When BDC = 1, N = 0, P = 0, FB = 1, output active level = high

Figure 9.65 Example of Output Phase Switching by Means of UF, VF, WF Bit Set



When BDC = 1, N = 1, P = 1, FB = 1, output active level = high

When BDC = 1, N = 0, P = 1, FB = 1, output active level = high

Figure 9.66 Example of Output Phase Switching by Means of UF, VF, WF Bit Se

Interrupts TGIA_3 (at the crest) and TCIV_4 (at the trough) in channels 3 and 4 can be sk to seven times by making settings in the timer interrupt skipping set register (TITCR).

Transfers from a buffer register to a temporary register or a compare register can be skipp coordination with interrupt skipping by making settings in the timer buffer transfer regist (TBTER). For the linkage with buffer registers, refer to description 3, Buffer Transfer Co Linked with Interrupt Skipping, below.

A/D converter start requests generated by the A/D converter start request delaying functi also be skipped in coordination with interrupt skipping by making settings in the timer A/ converter request control register (TADCR). For the linkage with the A/D converter start delaying function, refer to section 9.4.9, A/D Converter Start Request Delaying Function

The setting of the timer interrupt skipping setting register (TITCR) must be done while th TGIA_3 and TCIV_4 interrupt requests are disabled by the settings of registers TIER_3 TIER_4 along with under the conditions in which TGFA_3 and TCFV_4 flag settings by match never occur. Before changing the skipping count, be sure to clear the T3AEN and bits to 0 to clear the skipping counter.

1. Example of Interrupt Skipping Operation Setting Procedure

   Figure 9.67 shows an example of the interrupt skipping operation setting procedure. F 9.68 shows the periods during which interrupt skipping count can be changed.

compare match never occur.
Before changing the skipping count, be sure to clear the T3AEN and T4VEN bits to 0 to clear the skipping counter.

Figure 9.67 Example of Interrupt Skipping Operation Setting Procedur

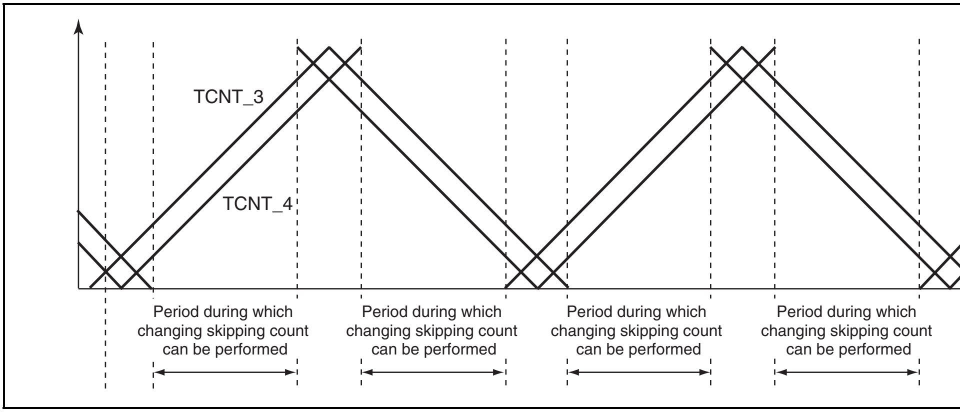

TCNT_3
TCNT_4
Period during which changing skipping count can be performed
Period during which changing skipping count can be performed
Period during which changing skipping count can be performed
Period during which changing skipping count can be performed

Figure 9.68 Periods during which Interrupt Skipping Count can be Chang

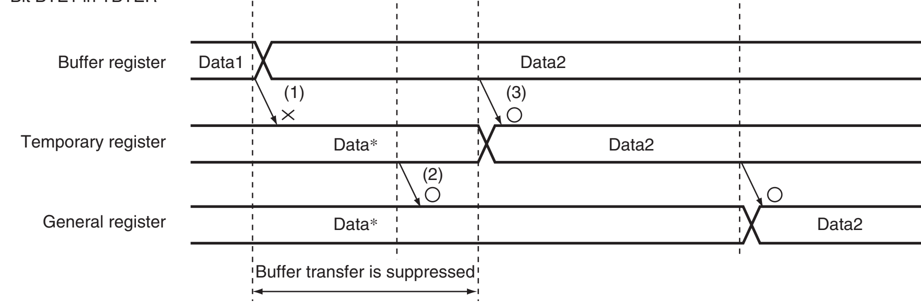
2. Example of Interrupt Skipping Operation

   Figure 9.69 shows an example of TGIA_3 interrupt skipping in which the interrupt s count is set to three by the 3ACOR bit and the T3AEN bit is set to 1 in the timer inte skipping set register (TITCR).

The data transfer timing is two types. That is, from the buffer register to the tempora and from the temporary register to the buffer register. These timings depend on a pro timing to the buffer register after an interrupt is generated.

Note that the buffer transfer-enabled period depends on the T3AEN and T4VEN bit the timer interrupt skipping set register (TITCR). Figure 9.72 shows the relationship the T3AEN and T4VEN bit settings in TITCR and buffer transfer-enabled period.

Note: This function must always be used in combination with interrupt skipping. When interrupt skipping is disabled (the T3AEN and T4VEN bits in the timer in skipping set register (TITCR) are cleared to 0 or the skipping count set bits (3AC 4VCOR) in TITCR are cleared to 0), make sure that buffer transfer is not linked interrupt skipping (clear the BTE1 bit in the timer buffer transfer set register (TI 0). If buffer transfer is linked with interrupt skipping while interrupt skipping is buffer transfer is never performed.

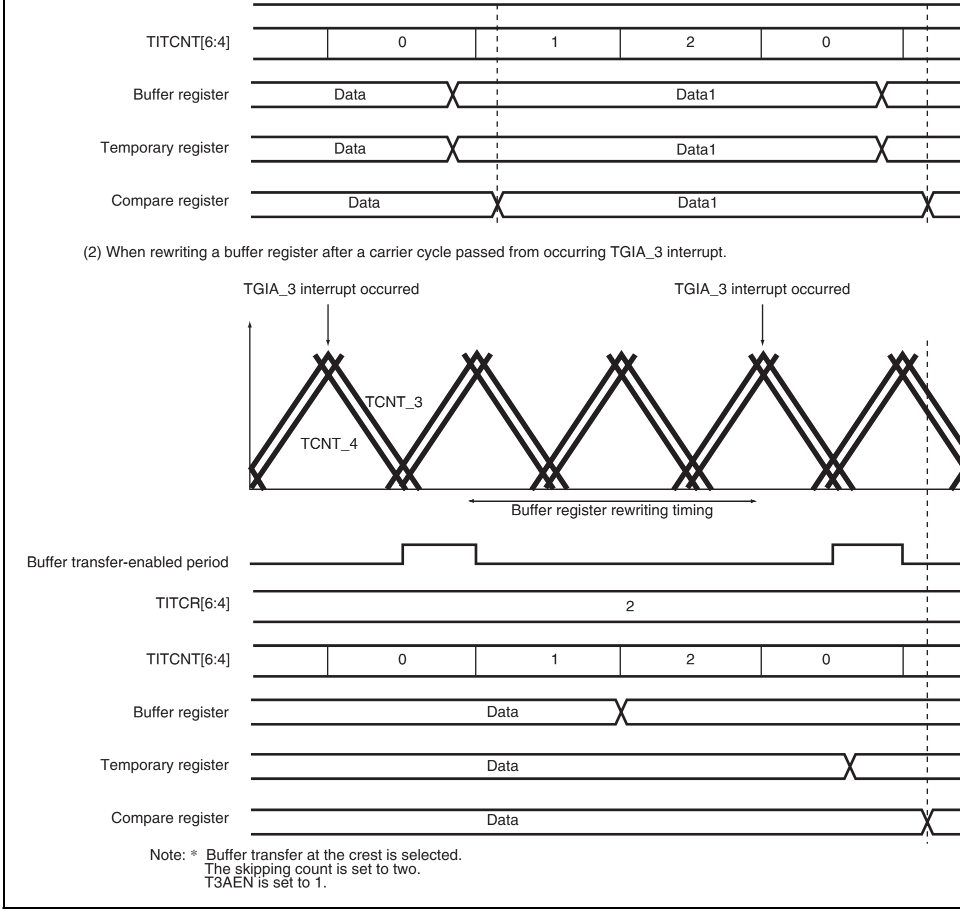


[Legend]

(1) No data is transferred from the buffer register to the temporary register in the buffer transfer-disabled period (bits BTE1 and BTE0 in TBTER are set to 0 and 1, respectively).
(2) Data is transferred from the temporary register to the general register even in the buffer transfer-disabled period.
(3) After buffer transfer is enabled, data is transferred from the buffer register to the temporary register.

Note: * When buffer transfer at the crest is selected.

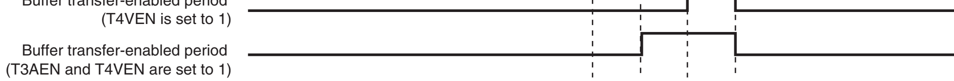
Figure 9.70 Example of Operation when Buffer Transfer is Suppressed (BTE1 = 0 and BTE0 = 1)



(2) When rewriting a buffer register after a carrier cycle passed from occurring TGIA_3 interrupt.

Note: * Buffer transfer at the crest is selected.
The skipping count is set to two.
T3AEN is set to 1.

Figure 9.71 Example of Operation when Buffer Transfer is Linked with Interrupt
(BTE1 = 1 and BTE0 = 0)


Buffer transfer-enabled period
(T4VEN is set to 1)
Buffer transfer-enabled period
(T3AEN and T4VEN are set to 1)

Note: * The skipping count is set to three.

Figure 9.72 Relationship between Bits T3AEN and T4VEN in TITCR and Buffer T
Enabled Period

TIORL_4, TIER_3 and TIER_4, TCNT_3 and TCNT_4, TGRA_3 and TGRA_4
and TGRB_4, TOER, TOCR, TGCR, TCDR, and TDDR.

This function enables miswriting due to CPU runaway to be prevented by disabling C
access to the mode registers, control registers, and counters. When the applicable reg
read in the access-disabled state, undefined values are returned. Writing to these regi
ignored.

2. Halting of PWM output by external signal

   The 6-phase PWM output pins can be set automatically to the high-impedance state b
   inputting specified external signals. There are four external signal input pins.

   See section 10, Port Output Enable (POE), for details.

3. Halting of PWM output when oscillator is stopped

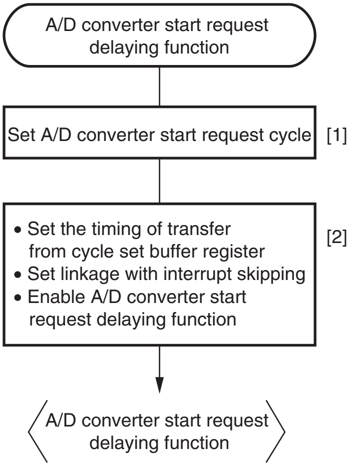
   If it is detected that the clock input to this LSI has stopped, the 6-phase PWM output
   automatically go to the high-impedance state. The pin states are not guaranteed when
   is restarted.

   See section 4.7, Function for Detecting Oscillator Stop.

A/D converter start requests (TRG4AN and TRG4BN) can be skipped in coordination wi interrupt skipping by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bi TADCR.

1. Example of Procedure for Specifying A/D Converter Start Request Delaying Functio

   Figure 9.73 shows an example of procedure for specifying the A/D converter start req delaying function.


A/D converter start request delaying function
Set A/D converter start request cycle
[1]
• Set the timing of transfer from cycle set buffer register
• Set linkage with interrupt skipping
• Enable A/D converter start request delaying function
[2]
A/D converter start request delaying function

[1] Set the cycle in the timer A/D converter start request cycl buffer register (TADCOBRA_4 or TADCOBRB_4) and tin A/D converter start request cycle register (TADCORA_4 o TADCORB_4). (The same initial value must be specified the cycle buffer register and cycle register.)

[2] Use bits BF1 and BF2 in the timer A/D converter start request control register (TADCR) to specify the timing of transfer from the timer A/D converter start request cycle buffer register to A/D converter start request cycle registe
- Specify whether to link with interrupt skipping through b ITA3AE, ITA4VE, ITB3AE, and ITB4VE.
- Use bits TU4AE, DT4AE, UT4BE, and DT4BE to enable A/D conversion start requests (TRG4AN or TRG4BN).

Notes: 1. Perform TADCR setting while TCNT_4 is stopped.
2. Do not set BF1 to 1 when complementary PWM mo is not selected.
3. Do not set ITA3AE, ITA4VE, ITB3AE, ITB4VE, DT4AE, or DT4BE to 1 when complementary PWM mode is not selected.

Figure 9.73 Example of Procedure for Specifying A/D Converter Start Request Delaying Function

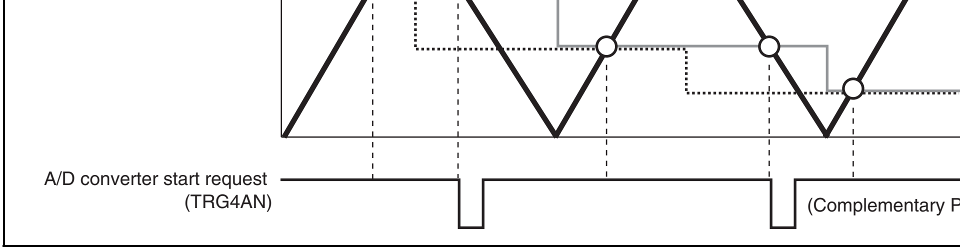


Figure 9.74 Basic Example of A/D Converter Start Request Signal (TRG4AN) O

3. Buffer Transfer

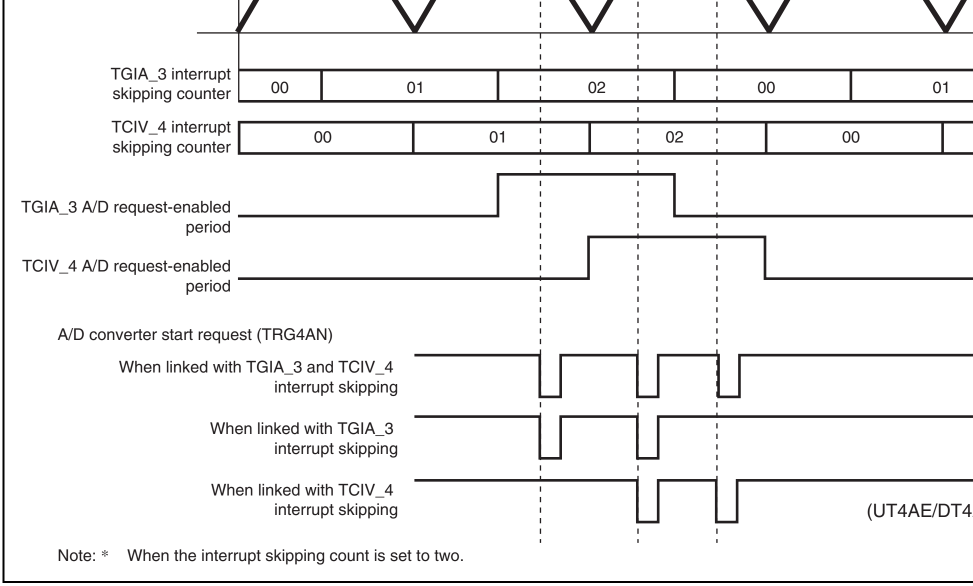
   The data in the timer A/D converter start request cycle set registers (TADCORA_4 a TADCORB_4) is updated by writing data to the timer A/D converter start request cy buffer registers (TADCOBRA_4 and TADCOBRB_4). Data is transferred from the registers to the respective cycle set registers at the timing selected with the BF1 and in the timer A/D converter start request control register (TADCR_4).

4. A/D Converter Start Request Delaying Function Linked with Interrupt Skipping

   A/D converter start requests (TRG4AN and TRG4BN) can be issued in coordination interrupt skipping by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4V the timer A/D converter start request control register (TADCR).

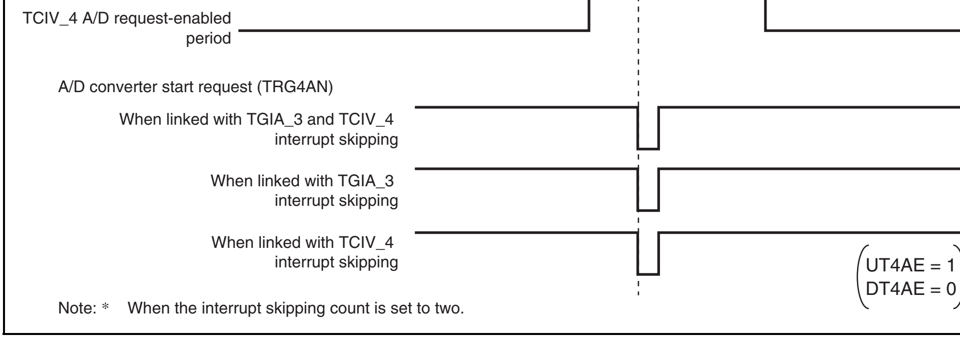
   Figure 9.75 shows an example of A/D converter start request signal (TRG4AN) oper when TRG4AN output is enabled during TCNT_4 up-counting and down-counting a converter start requests are linked with interrupt skipping.

   Figure 9.76 shows another example of A/D converter start request signal (TRG4AN) when TRG4AN output is enabled during TCNT_4 up-counting and A/D converter st requests are linked with interrupt skipping.


TGIA_3 interrupt skipping counter
00
01
02
00
01
TCIV_4 interrupt skipping counter
00
01
02
00
TGIA_3 A/D request-enabled period
TCIV_4 A/D request-enabled period
A/D converter start request (TRG4AN)
When linked with TGIA_3 and TCIV_4 interrupt skipping
When linked with TGIA_3 interrupt skipping
When linked with TCIV_4 interrupt skipping
(UT4AE/DT4

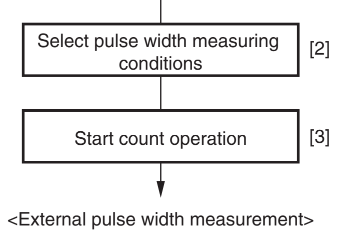
Note: * When the interrupt skipping count is set to two.

Figure 9.75 Example of A/D Converter Start Request Signal (TRG4AN) Operatio with Interrupt Skipping


TCIV_4 A/D request-enabled period
A/D converter start request (TRG4AN)
When linked with TGIA_3 and TCIV_4 interrupt skipping
When linked with TGIA_3 interrupt skipping
When linked with TCIV_4 interrupt skipping
UT4AE = 1
DT4AE = 0

Note: * When the interrupt skipping count is set to two.

Figure 9.76 Example of A/D Converter Start Request Signal (TRG4AN) Operatio with Interrupt Skipping


Select pulse width measuring conditions
[2]
Start count operation
[3]
<External pulse width measurement>

[3] Set bits CST in TSTR to 1 to start count operation.

Notes: 1. Do not set bits CMPCLR5U, CMPCLR5V, or CMPCLR5W in TCNTCMPCLR to 1.
2. Do not set bits TGIE5U, TGIE5V, or TGIE5W in TIER_5 to 1.
3. The value in TCNT is not captured in TGR.

Figure 9.77 Example of External Pulse Width Measurement Setting Procedu

Example of External Pulse Width Measurement:

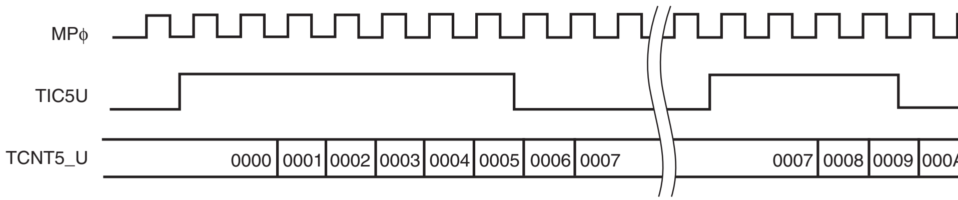


Figure 9.78 Example of External Pulse Width Measurement (Measuring High Pulse Width)

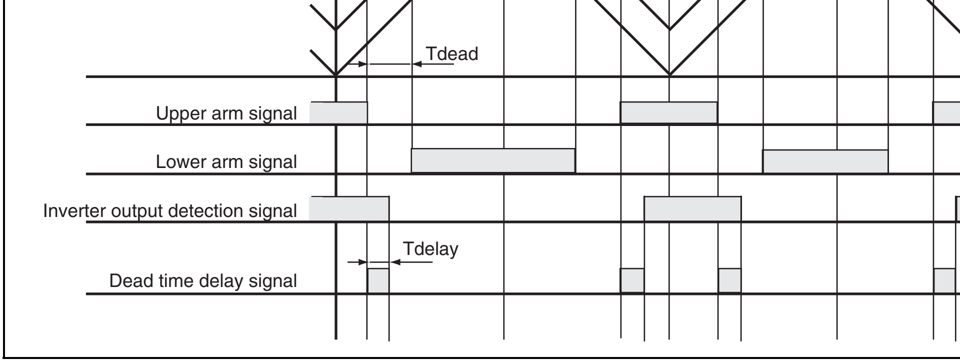
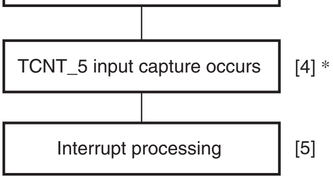


Figure 9.79 Delay in Dead Time in Complementary PWM Operation



the TCNT_5 value is captured in TGR_5.

[5] For U-phase dead time compensation, when an interrupt generated at the crest (TGIA_3) or trough (TCIV_4) in complementary PWM mode, read the TGRU_5 value, calculate the difference in time in TGRB_3, and write the corrected value to TGRD_3 in the interrupt processing. For the V phase and W phase, read the TGRV_5 and TGRW_5 values and write the corrected values to TGRC_ and TGRD_4, respectively, in the same way as for U-pha compensation.
The TCNT_5 value should be cleared through the TCNTCMPCLR setting or by software.

Notes: The PFC settings must be completed in advance.
* As an interrupt flag is set under the capture conditio specified in TIOR, do not enable interrupt requests i TIER_5.

Figure 9.80 Example of Dead Time Compensation Setting Procedure

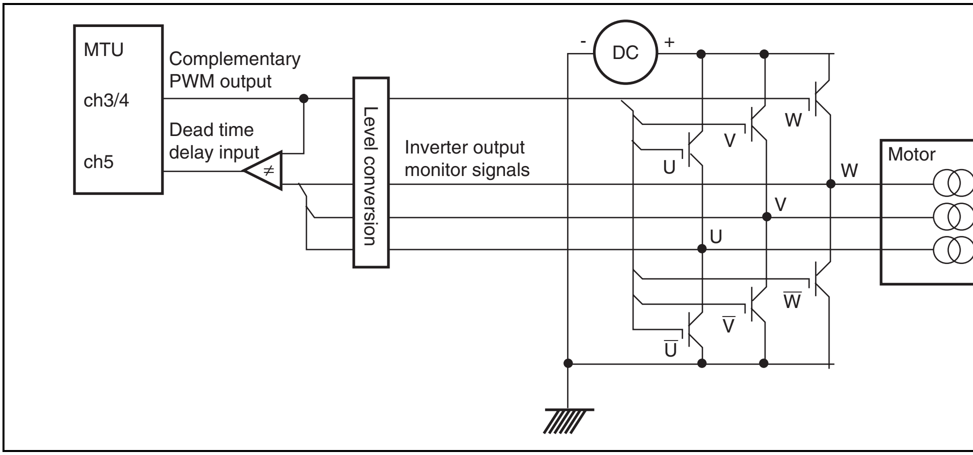


Figure 9.81 Example of Motor Control Circuit Configuration

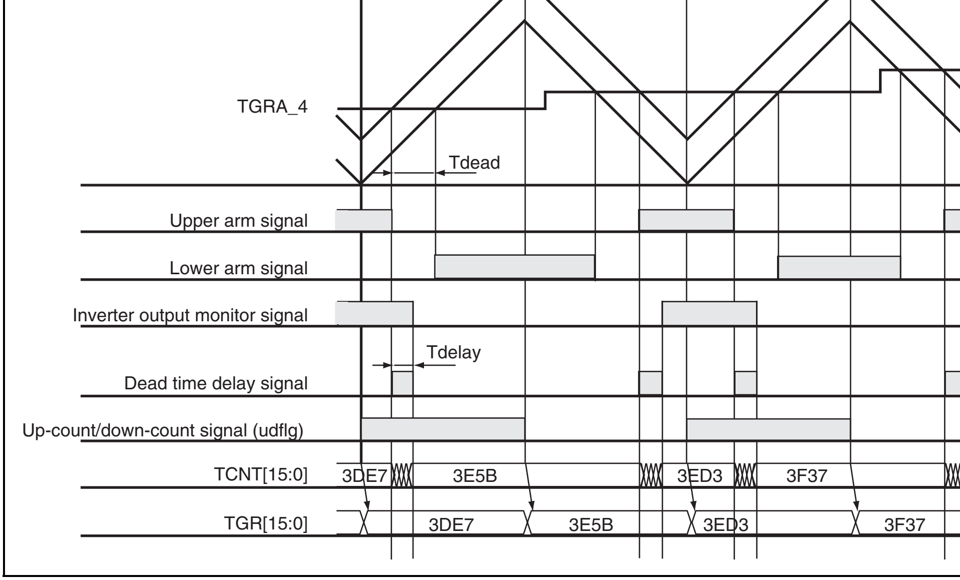


Figure 9.82 TCNT Capturing at Crest and/or Trough in Complementary PWM C

interrupt request is cleared by clearing the status flag to 0.

Relative channel priorities can be changed by the interrupt controller, however the priorit within a channel is fixed. For details, see section 6, Interrupt Controller (INTC).

Table 9.57 lists the MTU2 interrupt sources.

1	TGIA_1	TGRA_1 input capture/compare match	TGFA_1
	TGIB_1	TGRB_1 input capture/compare match	TGFB_1
	TCIV_1	TCNT_1 overflow	TCFV_1
	TCIU_1	TCNT_1 underflow	TCFU_1
2	TGIA_2	TGRA_2 input capture/compare match	TGFA_2
	TGIB_2	TGRB_2 input capture/compare match	TGFB_2
	TCIV_2	TCNT_2 overflow	TCFV_2
	TCIU_2	TCNT_2 underflow	TCFU_2
3	TGIA_3	TGRA_3 input capture/compare match	TGFA_3
	TGIB_3	TGRB_3 input capture/compare match	TGFB_3
	TGIC_3	TGRC_3 input capture/compare match	TGFC_3
	TGID_3	TGRD_3 input capture/compare match	TGFD_3
	TCIV_3	TCNT_3 overflow	TCFV_3
4	TGIA_4	TGRA_4 input capture/compare match	TGFA_4
	TGIB_4	TGRB_4 input capture/compare match	TGFB_4
	TGIC_4	TGRC_4 input capture/compare match	TGFC_4
	TGID_4	TGRD_4 input capture/compare match	TGFD_4
	TCIV_4	TCNT_4 overflow/underflow	TCFV_4
5	TGIU_5	TGRU_5 input capture/compare match	TGFU_5
	TGIV_5	TGRV_5 input capture/compare match	TGFV_5
	TGIW_5	TGRW_5 input capture/compare match	TGFW_5

Note: This table shows the initial state immediately after a reset. The relative channel p can be changed by the interrupt controller.

Underflow Interrupt: An interrupt is requested if the TCIEU bit in TIER is set to 1 whe TCFU flag in TSR is set to 1 by the occurrence of TCNT underflow on a channel. The int request is cleared by clearing the TCFU flag to 0. The MTU2 has two underflow interrup each for channels 1 and 2.

A/D converter start request signal TRGAN is issued to the A/D converter under either o
following conditions.

- When the TGFA flag in TSR is set to 1 by the occurrence of a TGRA input capture/c
  match on a particular channel while the TTGE bit in TIER is set to 1
- When the TCNT_4 count reaches the trough (TCNT_4 = H'0000) during complemen
  PWM operation while the TTGE2 bit in TIER_4 is set to 1

When either condition is satisfied, if A/D converter start signal TRGAN from the MTU2
selected as the trigger in the A/D converter, A/D conversion will start.

A/D Converter Activation by Compare Match between TCNT_0 and TGRE_0: Th
converter can be activated by generating A/D converter start request signal TRG0N whe
compare match occurs between TCNT_0 and TGRE_0 in channel 0.

When the TGFE flag in TSR2_0 is set to 1 by the occurrence of a compare match betwe
TCNT_0 and TGRE_0 in channel 0 while the TTGE2 bit in TIER2_0 is set to 1, A/D co
start request TGR0N is issued to the A/D converter. If A/D converter start signal TGR0
MTU2 is selected as the trigger in the A/D converter, A/D conversion will start.

A/D Converter Activation by A/D Converter Start Request Delaying Function: Th
converter can be activated by generating A/D converter start request signal TRG4AN or
when the TCNT_4 count matches the TADCORA or TADCORB value if the UT4AE, D
UT4BE, or DT4BE bit in the A/D converter start request control register (TADCR) is se
details, refer to section 9.4.9, A/D Converter Start Request Delaying Function.

A/D conversion will start if A/D converter start signal TRG4AN from the MTU2 is sele
trigger in the A/D converter when TRG4AN is generated or if TRG4BN from the MTU2
selected as the trigger in the A/D converter when TRG4BN is generated.

	complementary PWM mode	
TGRE_0 and TCNT_0	Compare match	TRG0N
TADCORA and TCNT_4		TRG4AN
TADCORB and TCNT_4		TRG4BN

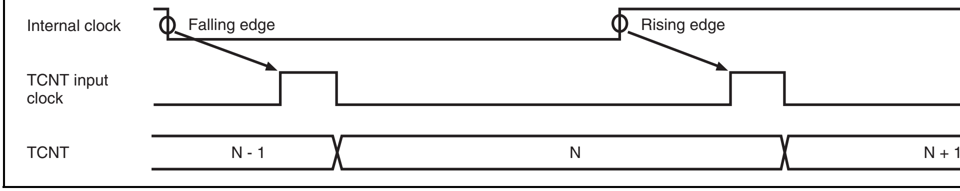


Figure 9.83 Count Timing in Internal Clock Operation (Channels 0 to 4

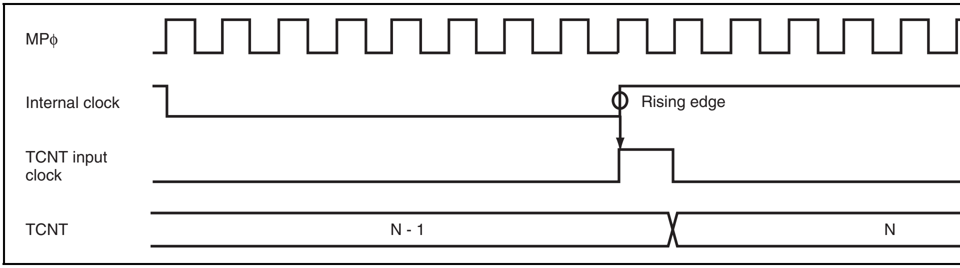


Figure 9.84 Count Timing in Internal Clock Operation (Channel 5)

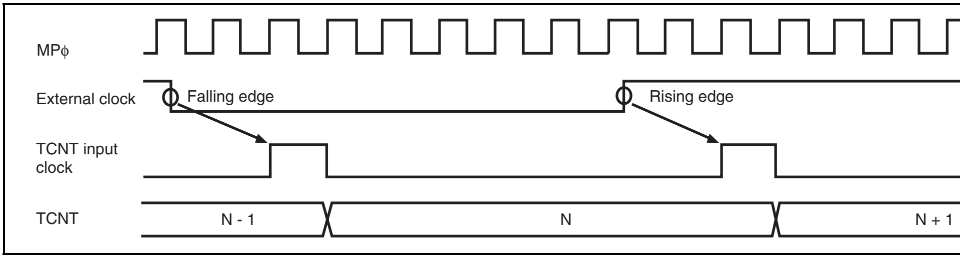


Figure 9.85 Count Timing in External Clock Operation (Channels 0 to 4

which TCNT and TGR match (the point at which the count value matched by TCNT is up When a compare match signal is generated, the output value set in TIOR is output at the c compare output pin (TIOC pin). After a match between TCNT and TGR, the compare ma signal is not generated until the TCNT input clock is generated.

Figure 9.87 shows output compare output timing (normal mode and PWM mode) and fig shows output compare output timing (complementary PWM mode and reset synchronous mode).

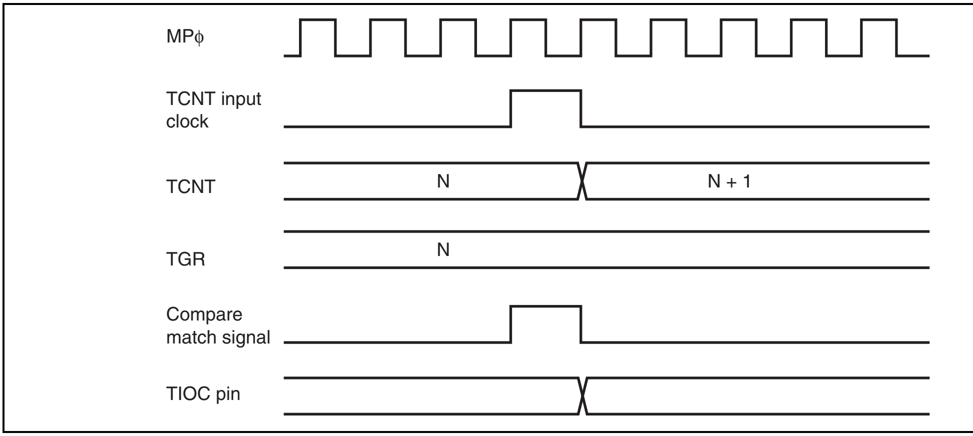


Figure 9.87 Output Compare Output Timing (Normal Mode/PWM Mode)

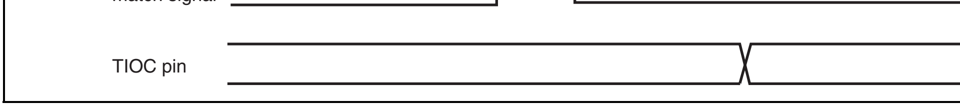


Figure 9.88 Output Compare Output Timing (Complementary PWM Mode/Reset Synchronous PWM Mode)

Input Capture Signal Timing: Figure 9.89 shows input capture signal timing.

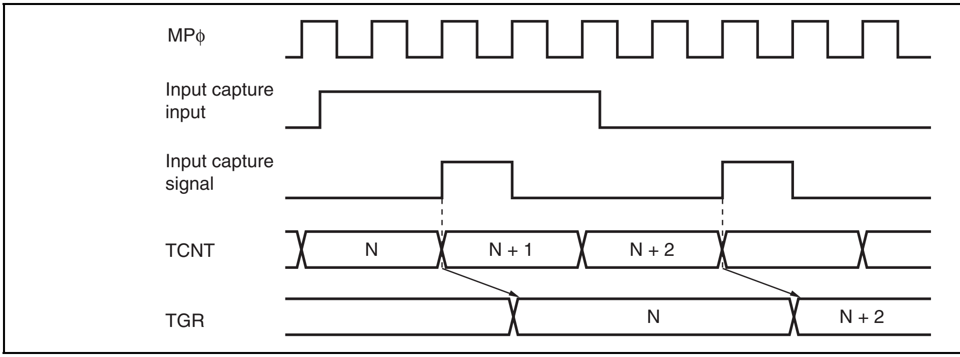


Figure 9.89 Input Capture Input Signal Timing

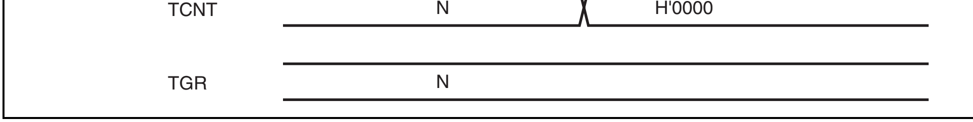


Figure 9.90 Counter Clear Timing (Compare Match)

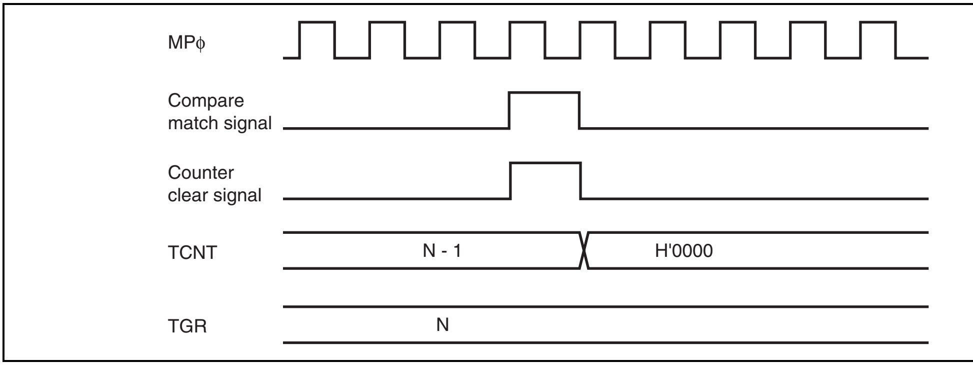


Figure 9.91 Counter Clear Timing (Compare Match) (Channel 5)

Figure 9.92 Counter Clear Timing (Input Capture)

Buffer Operation Timing: Figures 9.93 to 9.95 show the timing in buffer operation.

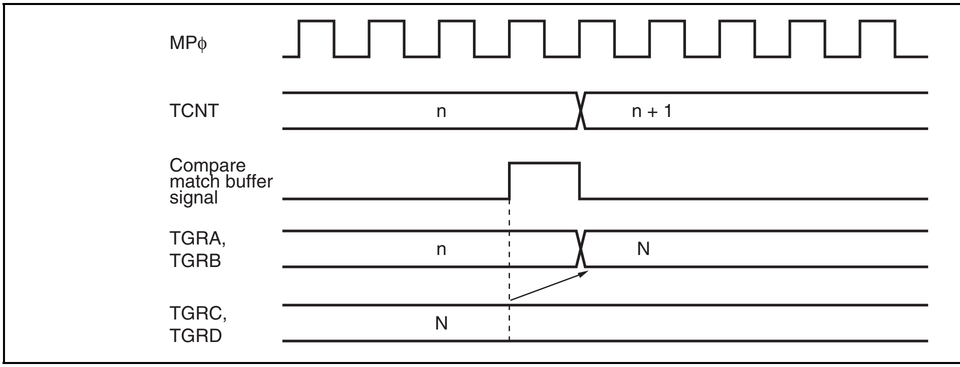


Figure 9.93 Buffer Operation Timing (Compare Match)

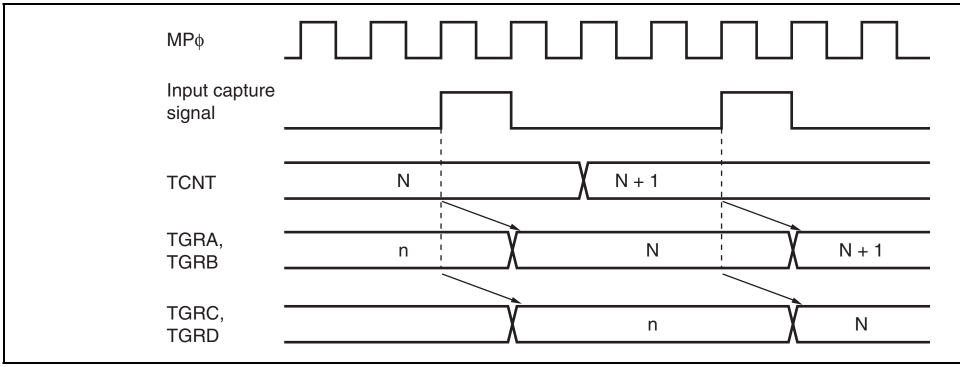


Figure 9.94 Buffer Operation Timing (Input Capture)

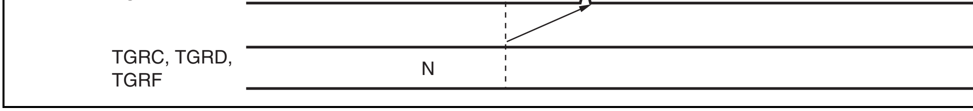


Figure 9.95 Buffer Transfer Timing (when TCNT Cleared)

Buffer Transfer Timing (Complementary PWM Mode): Figures 9.96 to 9.98 show the transfer timing in complementary PWM mode.

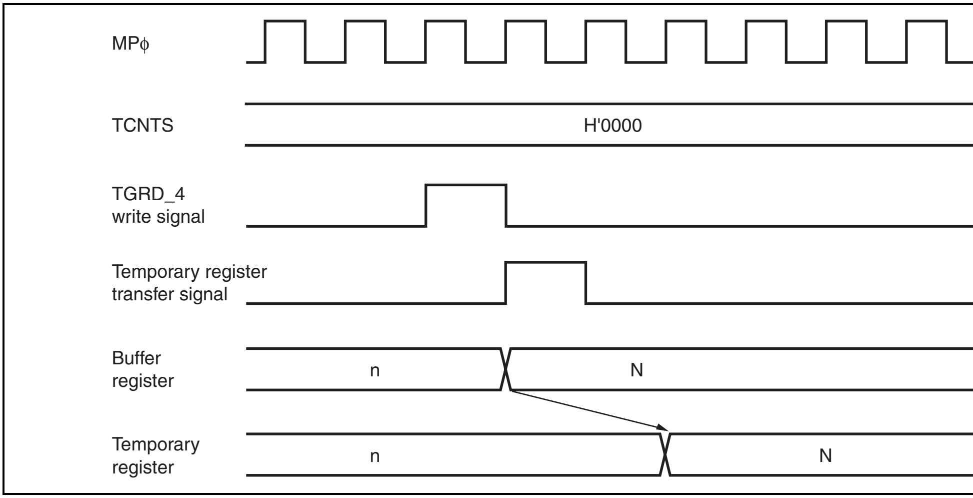


Figure 9.96 Transfer Timing from Buffer Register to Temporary Register (TCNT

Figure 9.97 Transfer Timing from Buffer Register to Temporary Registe
(TCNTS Operating)

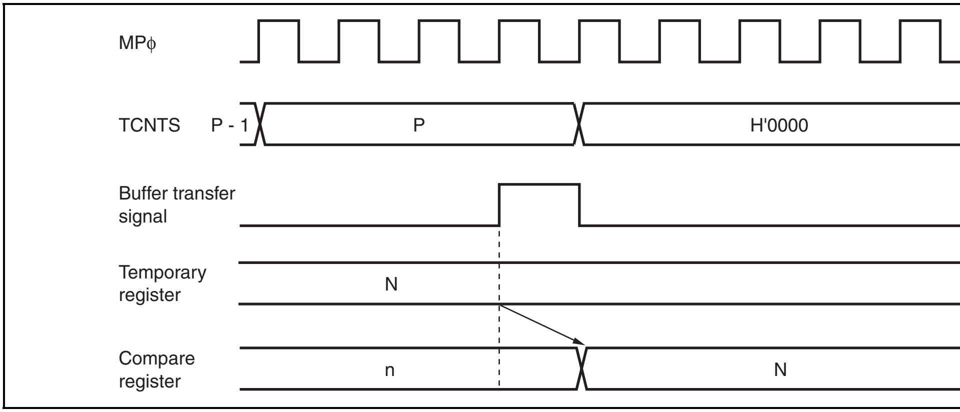


Figure 9.98 Transfer Timing from Temporary Register to Compare Regis

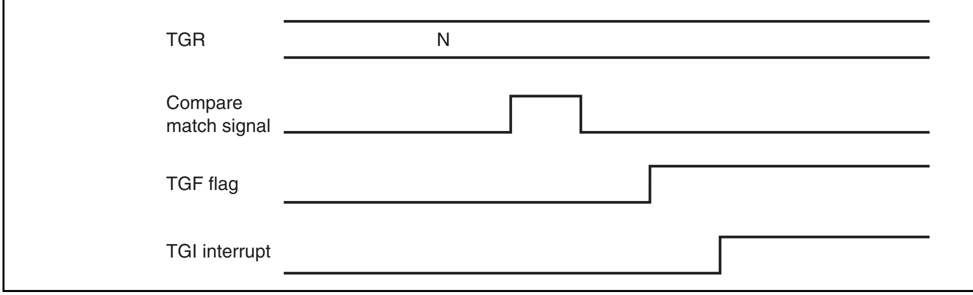


Figure 9.99 TGI Interrupt Timing (Compare Match) (Channels 0 to 4)

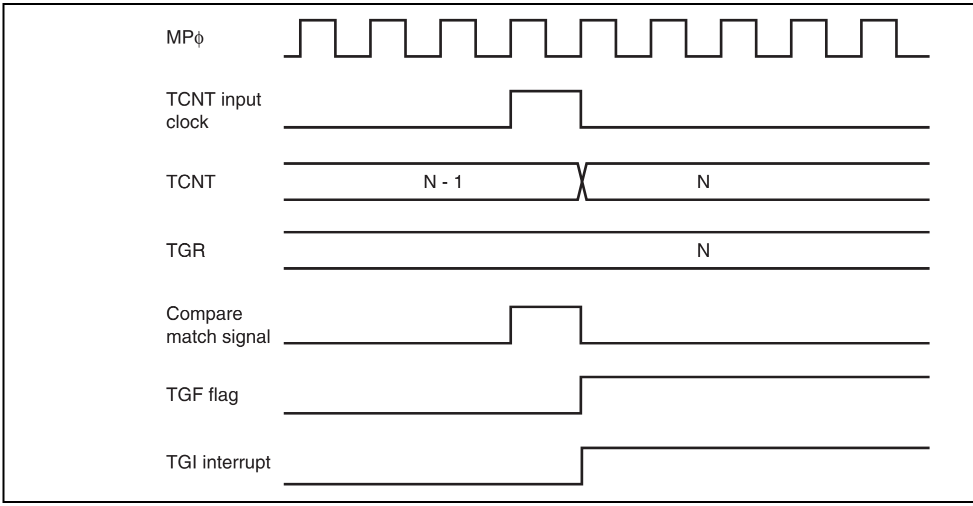


Figure 9.100 TGI Interrupt Timing (Compare Match) (Channel 5)

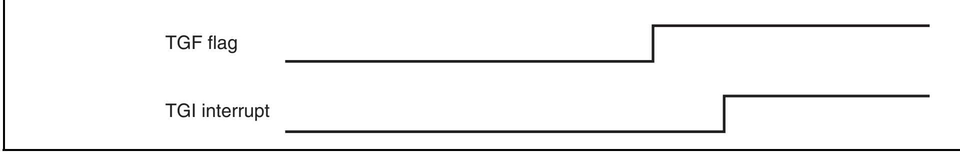


Figure 9.101 TGI Interrupt Timing (Input Capture) (Channels 0 to 4)

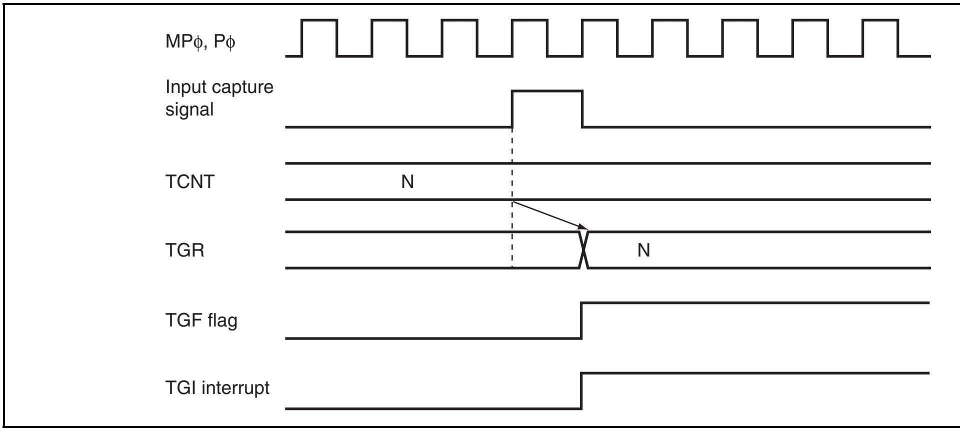


Figure 9.102 TGI Interrupt Timing (Input Capture) (Channel 5)

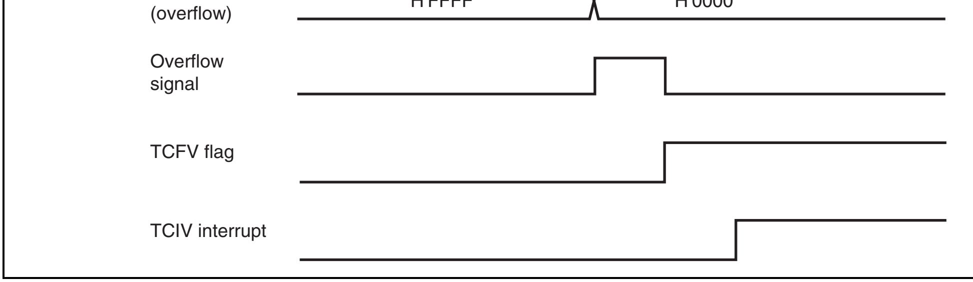


Figure 9.103 TCIV Interrupt Setting Timing

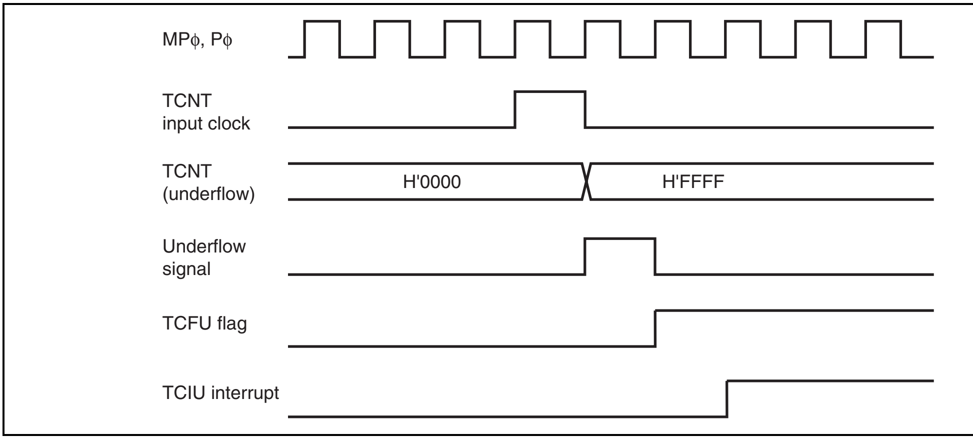


Figure 9.104 TCIU Interrupt Setting Timing

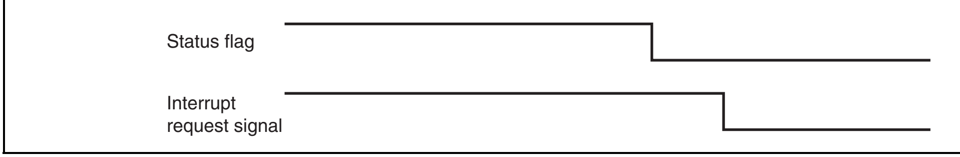


Figure 9.105 Timing for Status Flag Clearing by CPU (Channels 0 to 4)

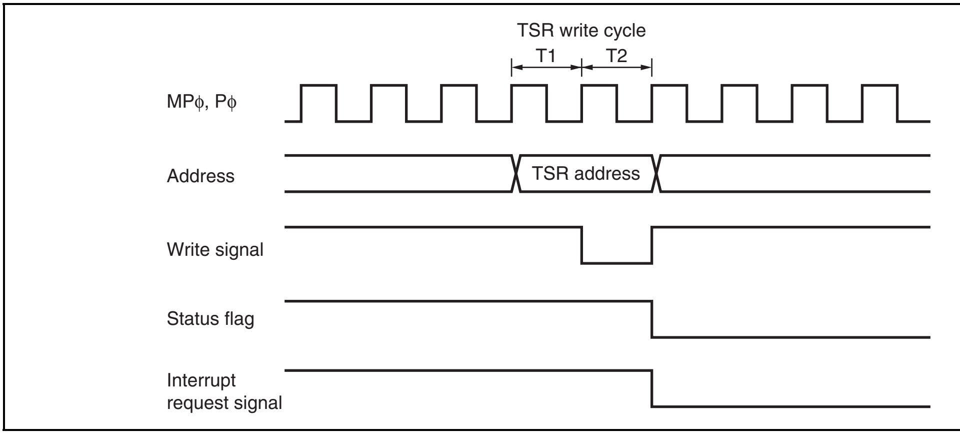
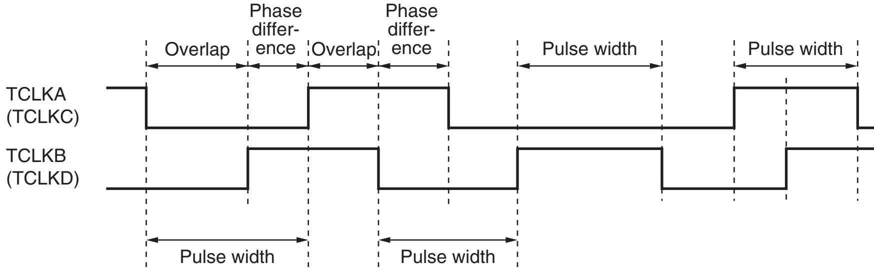


Figure 9.106 Timing for Status Flag Clearing by CPU (Channel 5)

The input clock pulse width must be at least 1.5 states in the case of single-edge detectio least 2.5 states in the case of both-edge detection. The MTU2 will not operate properly at pulse widths.

In phase counting mode, the phase difference and overlap between the two input clocks n least 1.5 states, and the pulse width must be at least 2.5 states. Figure 9.107 shows the inp conditions in phase counting mode.



Notes: Phase difference and overlap : 1.5 states or more
Pulse width : 2.5 states or more

Figure 9.107 Phase Difference, Overlap, and Pulse Width in Phase Counting M

- Channel 5

$$f = \frac{MP\phi}{N}$$

Where f: Counter frequency
MPϕ: MTU2 peripheral clock operating frequency
N: TGR set value

9.7.4 Contention between TCNT Write and Clear Operations

If the counter clear signal is generated in the T2 state of a TCNT write cycle, TCNT clea
precedence and the TCNT write is not performed.

Figure 9.108 shows the timing in this case.

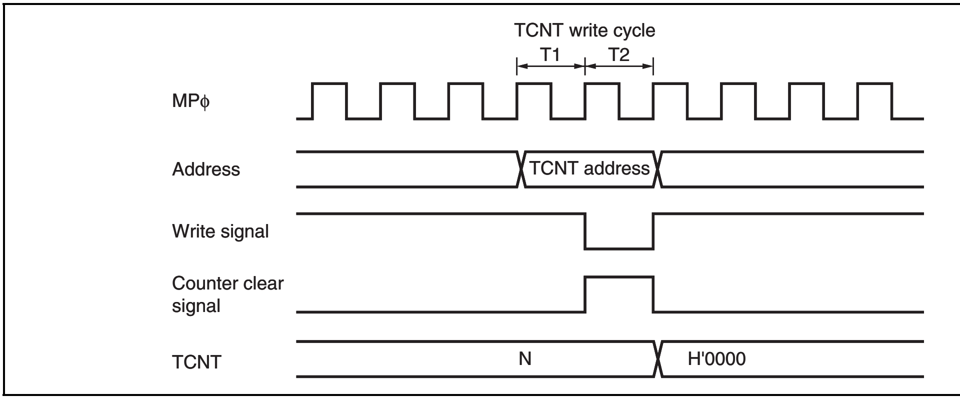


Figure 9.108 Contention between TCNT Write and Clear Operations

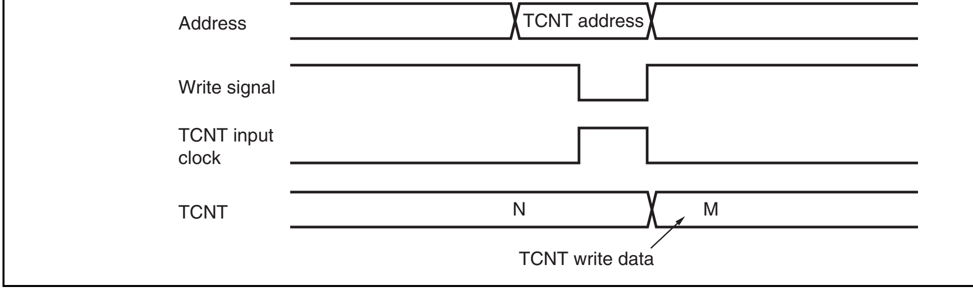


Figure 9.109   Contention between TCNT Write and Increment Operations

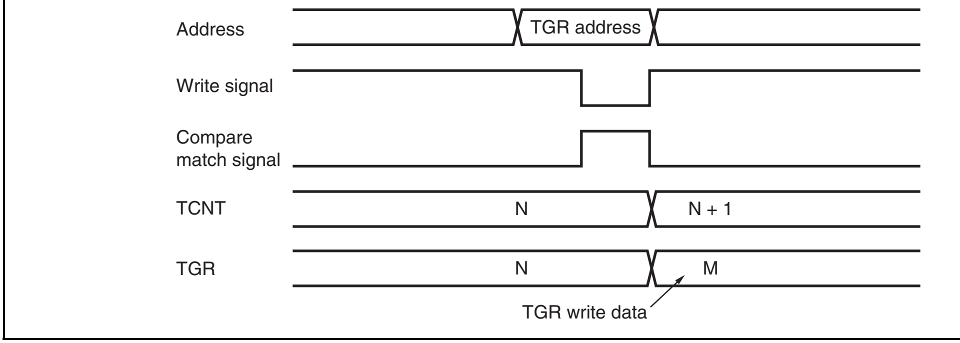


Figure 9.110 Contention between TGR Write and Compare Match

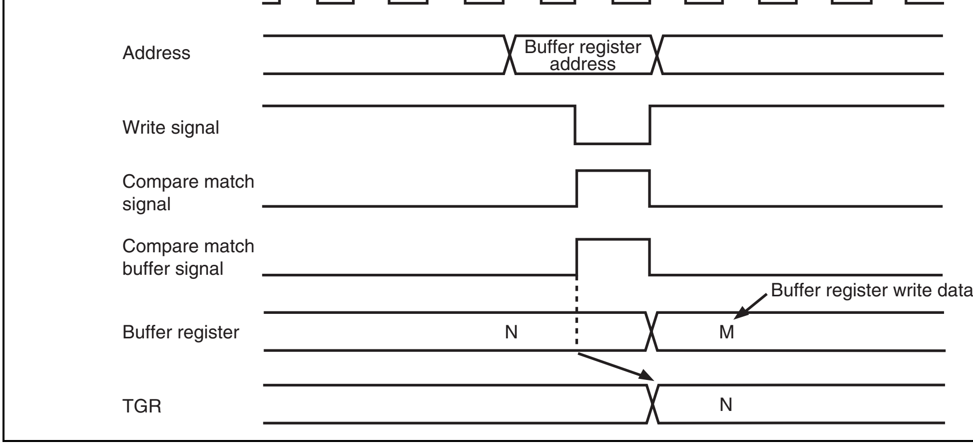


Figure 9.111 Contention between Buffer Register Write and Compare Matc

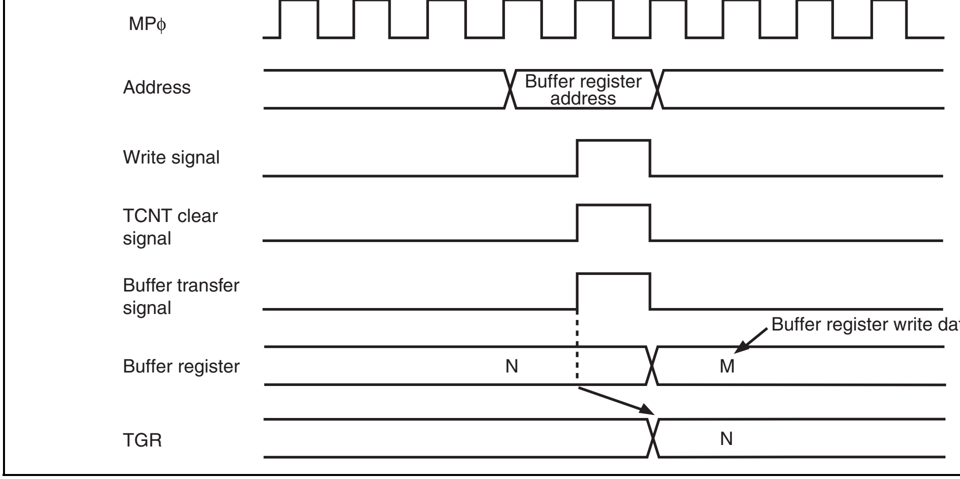


Figure 9.112 Contention between Buffer Register Write and TCNT Clea

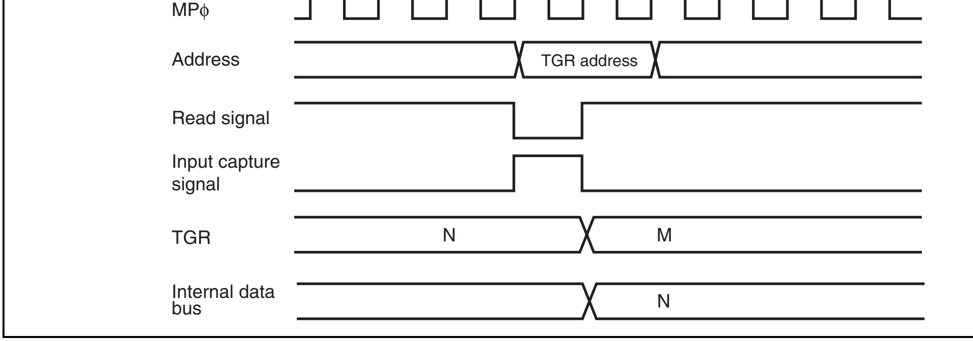


Figure 9.113 Contention between TGR Read and Input Capture (Channels 0 t

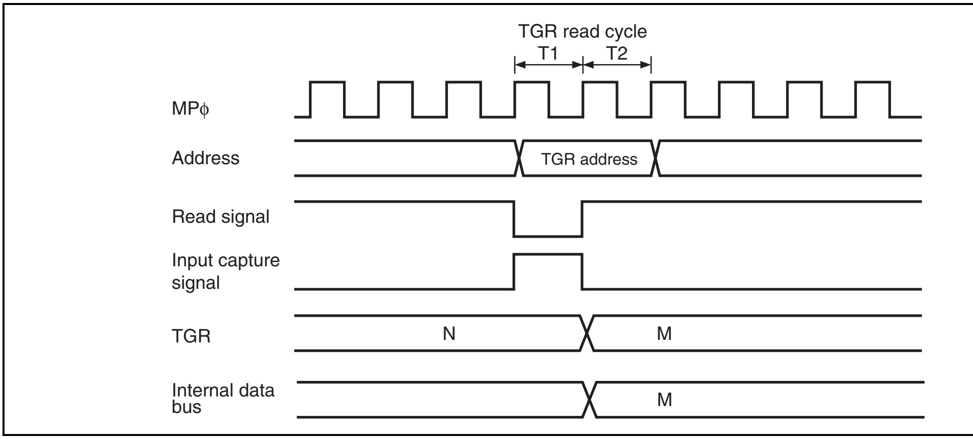


Figure 9.114 Contention between TGR Read and Input Capture (Channel

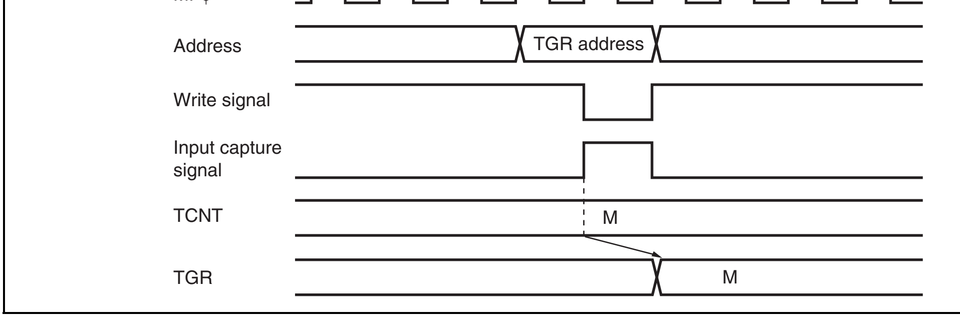


Figure 9.115 Contention between TGR Write and Input Capture (Channels

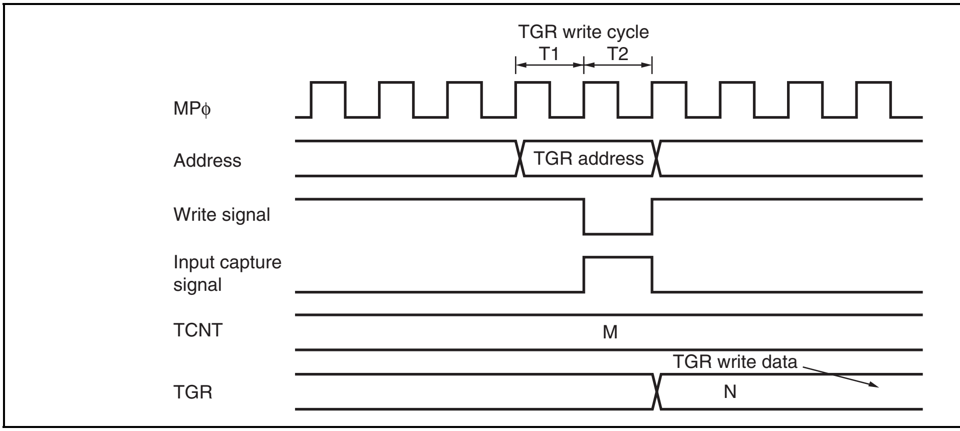


Figure 9.116 Contention between TGR Write and Input Capture (Channel

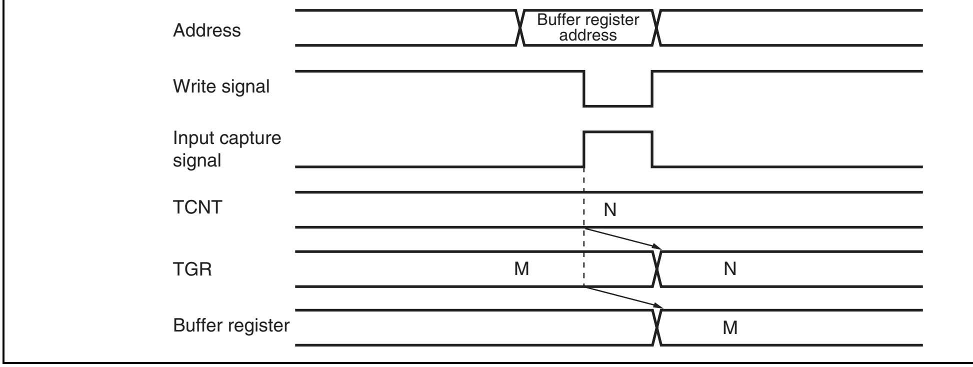


Figure 9.117 Contention between Buffer Register Write and Input Captur

9.7.12 TCNT_2 Write and Overflow/Underflow Contention in Cascade Connecti

With timer counters TCNT_1 and TCNT_2 in a cascade connection, when a contention o during TCNT_1 count (during a TCNT_2 overflow/underflow) in the T2 state of the TCN write cycle, the write to TCNT_2 is conducted, and the TCNT_1 count signal is disabled. point, if there is match with TGRA_1 and the TCNT_1 value, a compare signal is issued. Furthermore, when the TCNT_1 count clock is selected as the input capture source of cha TGRA_0 to TGRD_0 carry out the input capture operation. In addition, when the compar match/input capture is selected as the input capture source of TGRB_1, TGRB_1 carries capture operation. The timing is shown in figure 9.118.

For cascade connections, be sure to synchronize settings for channels 1 and 2 when settin clearing.

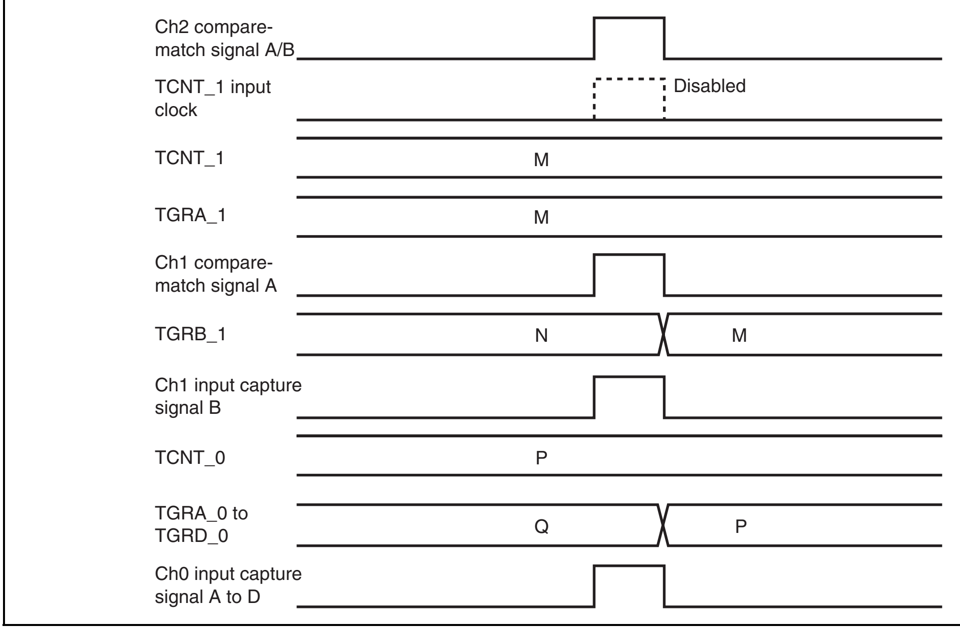

Ch2 compare-match signal A/B
TCNT_1 input clock
Disabled
TCNT_1
M
TGRA_1
M
Ch1 compare-match signal A
TGRB_1
N
M
Ch1 input capture signal B
TCNT_0
P
TGRA_0 to TGRD_0
Q
P
Ch0 input capture signal A to D

Figure 9.118 TCNT_2 Write and Overflow/Underflow Contention with Cas Connection

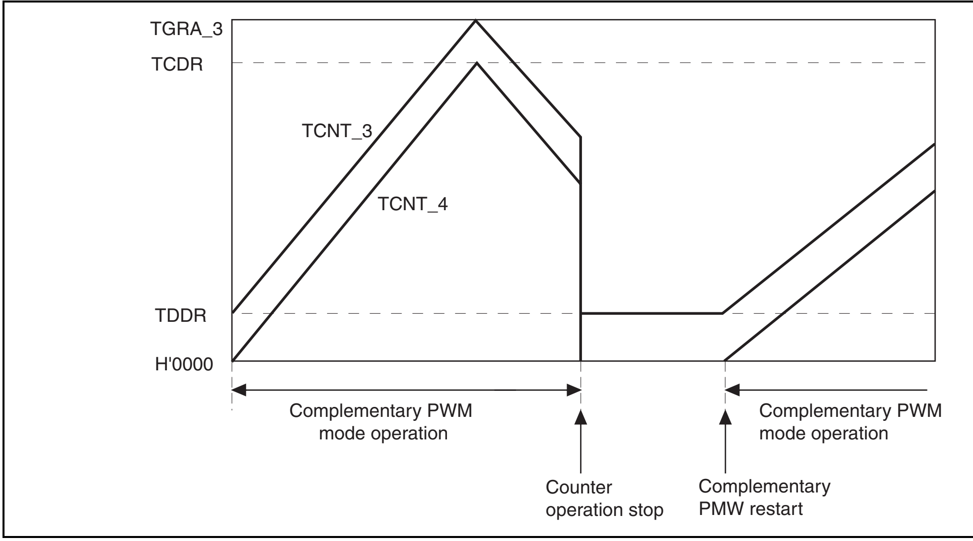


Figure 9.119 Counter Value during Complementary PWM Mode Stop

9.7.14 Buffer Operation Setting in Complementary PWM Mode

In complementary PWM mode, conduct rewrites by buffer operation for the PWM cycle register (TGRA_3), timer cycle data register (TCDR), and duty setting registers (TGRB_ TGRA_4, and TGRB_4).

In complementary PWM mode, channel 3 and channel 4 buffers operate in accordance w settings BFA and BFB of TMDR_3. When the BFA bit in TMDR_3 is set to 1, TGRC_3 as a buffer register for TGRA_3. At the same time, TGRC_4 functions as the buffer regis TGRA_4, and TCBR functions as the TCDR's buffer register.

The TGFC bit and TGFD bit in TSR_3 and TSR_4 are not set when TGRC_3 and TGRI operating as buffer registers.

Figure 9.120 shows an example of operations for TGR_3, TGR_4, TIOC3, and TIOC4, TMDR_3's BFA and BFB bits set to 1, and TMDR_4's BFA and BFB bits set to 0.

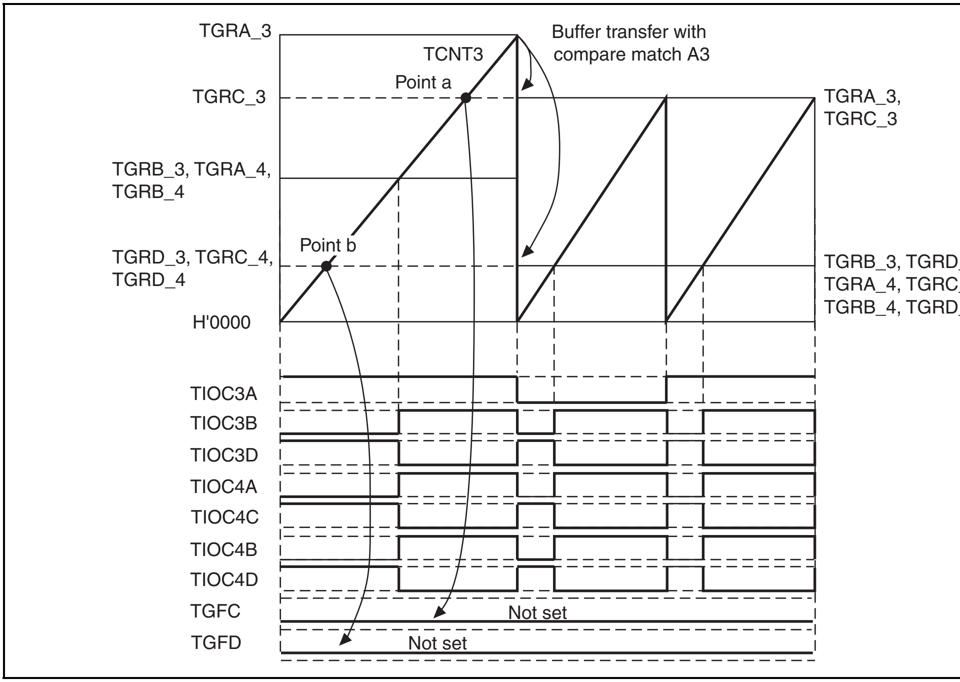


Figure 9.120 Buffer Operation and Compare-Match Flags in Reset Synchronous PWM Mode

Figure 9.121 shows a TCFV bit operation example in reset synchronous PWM mode wit
value for cycle register TGRA_3 of H'FFFF, when a TGRA_3 compare-match has been s
without synchronous setting for the counter clear source.

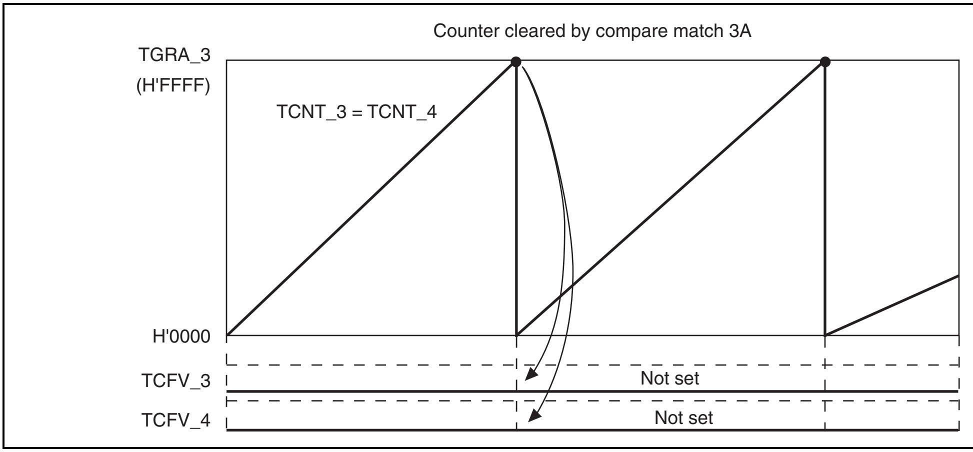


Figure 9.121 Reset Synchronous PWM Mode Overflow Flag

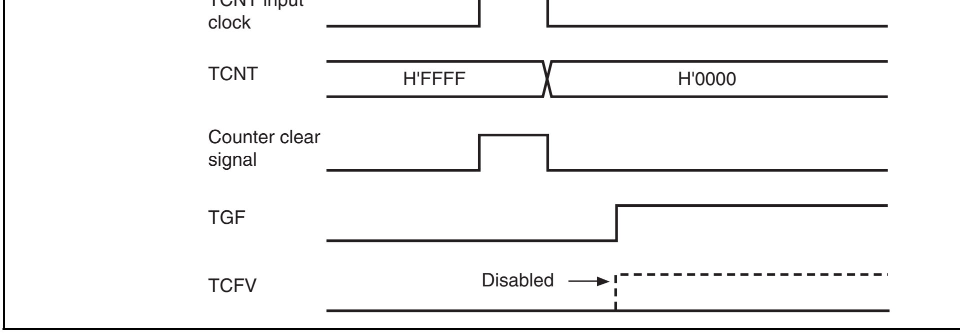


Figure 9.122 Contention between Overflow and Counter Clearing

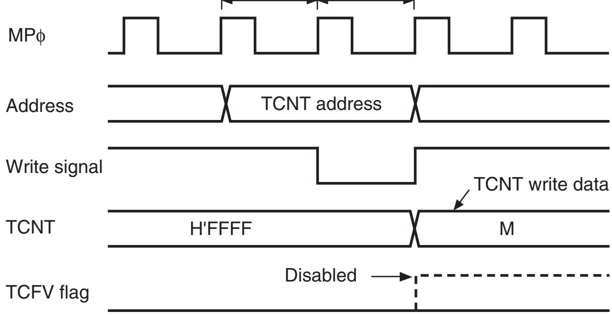


Figure 9.123 Contention between TCNT Write and Overflow

9.7.19 Cautions on Transition from Normal Operation or PWM Mode 1 to Reset-Synchronized PWM Mode

When making a transition from channel 3 or 4 normal operation or PWM mode 1 to reset synchronized PWM mode, if the counter is halted with the output pins (TIOC3B, TIOC3 TIOC4A, TIOC4C, TIOC4B, TIOC4D) in the high-level state, followed by the transition synchronized PWM mode and operation in that mode, the initial pin output will not be co

When making a transition from normal operation to reset-synchronized PWM mode, writ registers TIORH_3, TIORL_3, TIORH_4, and TIORL_4 to initialize the output pins to lo output, then set an initial register value of H'00 before making the mode transition.

When making a transition from PWM mode 1 to reset-synchronized PWM mode, first sw normal operation, then initialize the output pins to low level output and set an initial regis of H'00 before making the transition to reset-synchronized PWM mode.

clear the CPU interrupt source. Interrupts should therefore be disabled before entering n standby mode.

9.7.22 Simultaneous Capture of TCNT_1 and TCNT_2 in Cascade Connection

When timer counters 1 and 2 (TCNT_1 and TCNT_2) are operated as a 32-bit counter in connection, the cascade counter value cannot be captured successfully even if input-cap is simultaneously done to TIOC1A and TIOC2A or to TIOC1B and TIOC2B. This is be input timing of TIOC1A and TIOC2A or of TIOC1B and TIOC2B may not be the same external input-capture signals to be input into TCNT_1 and TCNT_2 are taken in synch with the internal clock. For example, TCNT_1 (the counter for upper 16 bits) does not c count-up value by overflow from TCNT_2 (the counter for lower 16 bits) but captures th value before the count-up. In this case, the values of TCNT_1 = H'FFF1 and TCNT_2 = should be transferred to TGRA_1 and TGRA_2 or to TGRB_1 and TGRB_2, but the va TCNT_1 = H'FFF0 and TCNT_2 = H'0000 are erroneously transferred.

The MTU2 has a new function that allows simultaneous capture of TCNT_1 and TCNT single input-capture input as the trigger. This function allows reading of the 32-bit coun that TCNT_1 and TCNT_2 are captured at the same time.

See section 9.3.8, Timer Input Capture Control Register (TICCR), for details.

- Phase counting modes 1 to 4 (channels 1 and 2)
- Complementary PWM mode (channels 3 and 4)
- Reset-synchronized PWM mode (channels 3 and 4)

The MTU2 output pin initialization method for each of these modes is described in this se

9.8.2 Reset Start Operation

The MTU2 output pins (TIOC*) are initialized low by a reset and in standby mode. Since pin function selection is performed by the pin function controller (PFC), when the PFC is MTU2 pin states at that point are output to the ports. When MTU2 output is selected by th immediately after a reset, the MTU2 output initial level, low, is output directly at the port the active level is low, the system will operate at this point, and therefore the PFC setting be made after initialization of the MTU2 output pins is completed.

Note: Channel number and port notation are substituted for *.

Table 9.59 Mode Transition Combinations

	After					
Before	**Normal**	**PWM1**	**PWM2**	**PCM**	**CPWM**	**RP**
Normal	(1)	(2)	(3)	(4)	(5)	(6)
PWM1	(7)	(8)	(9)	(10)	(11)	(12
PWM2	(13)	(14)	(15)	(16)	None	No
PCM	(17)	(18)	(19)	(20)	None	No
CPWM	(21)	(22)	None	None	(23) (24)	(25
RPWM	(26)	(27)	None	None	(28)	(29

[Legend]

Normal: Normal mode

PWM1: PWM mode 1

PWM2: PWM mode 2

PCM: Phase counting modes 1 to 4

CPWM: Complementary PWM mode

RPWM: Reset-synchronized PWM mode

not initialize the pins. If initialization is required, carry it out in normal mode, then sw PWM mode 2.

- In normal mode or PWM mode 2, if TGRC and TGRD operate as buffer registers, set TIOR will not initialize the buffer register pins. If initialization is required, clear buff carry out initialization, then set buffer mode again.
- In PWM mode 1, if either TGRC or TGRD operates as a buffer register, setting TIOR initialize the TGRC pin. To initialize the TGRC pin, clear buffer mode, carry out initi then set buffer mode again.
- When making a transition to a mode (CPWM, RPWM) in which the pin output level i selected by the timer output control register (TOCR) setting, switch to normal mode a perform initialization with TIOR, then restore TIOR to its initial value, and temporari channel 3 and 4 output with the timer output master enable register (TOER). Then op unit in accordance with the mode setting procedure (TOCR setting, TMDR setting, T setting).

Note: Channel number is substituted for * indicated in this article.

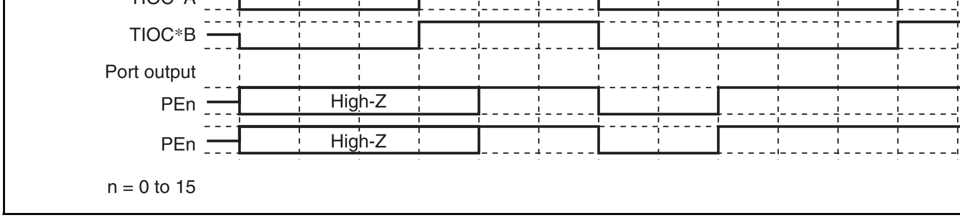


Figure 9.124 Error Occurrence in Normal Mode, Recovery in Normal Mo

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. After a reset, the TMDR setting is for normal mode.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TI
4. Initialize the pins with TIOR. (The example shows initial high output, with low out compare-match occurrence.)
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Not necessary when restarting in normal mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

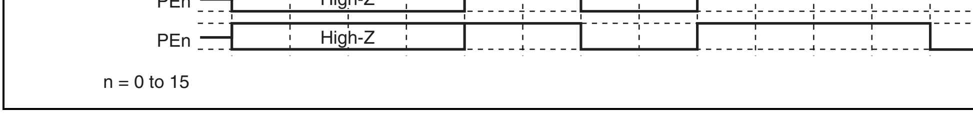


Figure 9.125 Error Occurrence in Normal Mode, Recovery in PWM Mode

1 to 10 are the same as in figure 9.124.

11. Set PWM mode 1.
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized. I initialization is required, initialize in normal mode, then switch to PWM mode 1.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

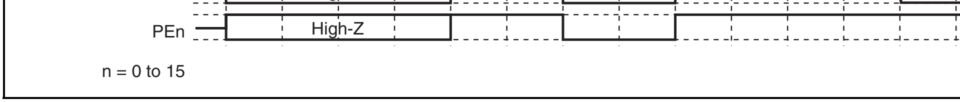


Figure 9.126   Error Occurrence in Normal Mode, Recovery in PWM Mod

1 to 10 are the same as in figure 9.124.

11. Set PWM mode 2.
12. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initia initialization is required, initialize in normal mode, then switch to PWM mode 2.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Note: PWM mode 2 can only be set for channels 0 to 2, and therefore TOER setting is necessary.

Figure 9.127 Error Occurrence in Normal Mode, Recovery in Phase Counting

1 to 10 are the same as in figure 9.124.

11. Set phase counting mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Note: Phase counting mode can only be set for channels 1 and 2, and therefore TOER s not necessary.

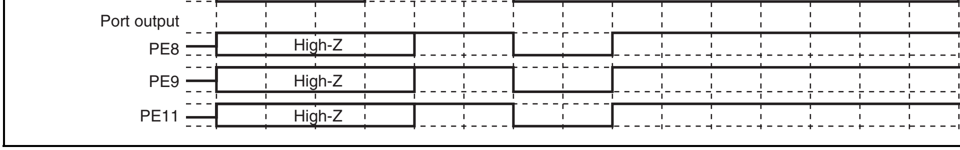


Figure 9.128 Error Occurrence in Normal Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 9.124.

11. Initialize the normal mode waveform generation section with TIOR.
12. Disable operation of the normal mode waveform generation section with TIOR.
13. Disable channel 3 and 4 output with TOER.
14. Select the complementary PWM output level and cyclic output enabling/disabling v TOCR.
15. Set complementary PWM.
16. Enable channel 3 and 4 output with TOER.
17. Set MTU2 output with the PFC.
18. Operation is restarted by TSTR.

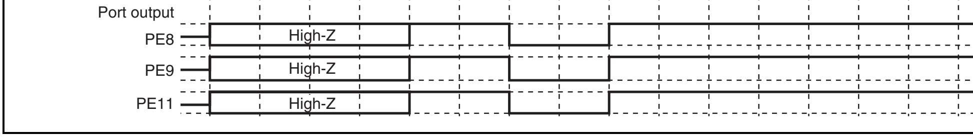


Figure 9.129 Error Occurrence in Normal Mode, Recovery in Reset-Synchronized PWM Mode

1 to 13 are the same as in figure 9.124.

14. Select the reset-synchronized PWM output level and cyclic output enabling/disabling TOCR.
15. Set reset-synchronized PWM.
16. Enable channel 3 and 4 output with TOER.
17. Set MTU2 output with the PFC.
18. Operation is restarted by TSTR.

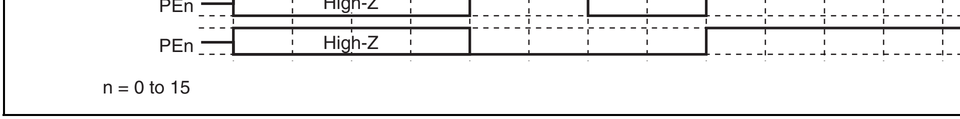


Figure 9.130 Error Occurrence in PWM Mode 1, Recovery in Normal Mo

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. Set PWM mode 1.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TI
4. Initialize the pins with TIOR. (The example shows initial high output, with low ou compare-match occurrence. In PWM mode 1, the TIOC*B side is not initialized.)
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Set normal mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

PEn
High-Z
PEn
High-Z
n = 0 to 15

Figure 9.131 Error Occurrence in PWM Mode 1, Recovery in PWM Mode

1 to 10 are the same as in figure 9.130.

11. Not necessary when restarting in PWM mode 1.
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Figure 9.132 Error Occurrence in PWM Mode 1, Recovery in PWM Mod

1 to 10 are the same as in figure 9.130.

11. Set PWM mode 2.
12. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initi
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Note: PWM mode 2 can only be set for channels 0 to 2, and therefore TOER setting is necessary.

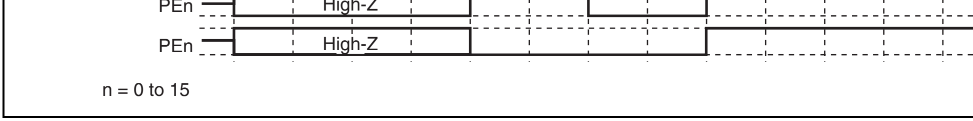


Figure 9.133 Error Occurrence in PWM Mode 1, Recovery in Phase Counting

1 to 10 are the same as in figure 9.130.

11. Set phase counting mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Note: Phase counting mode can only be set for channels 1 and 2, and therefore TOER s not necessary.

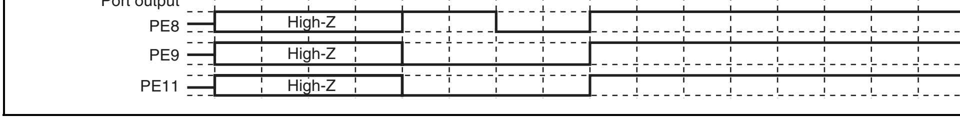


Figure 9.134 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 9.130.

11. Set normal mode for initialization of the normal mode waveform generation sectior
12. Initialize the PWM mode 1 waveform generation section with TIOR.
13. Disable operation of the PWM mode 1 waveform generation section with TIOR.
14. Disable channel 3 and 4 output with TOER.
15. Select the complementary PWM output level and cyclic output enabling/disabling v TOCR.
16. Set complementary PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU2 output with the PFC.
19. Operation is restarted by TSTR.

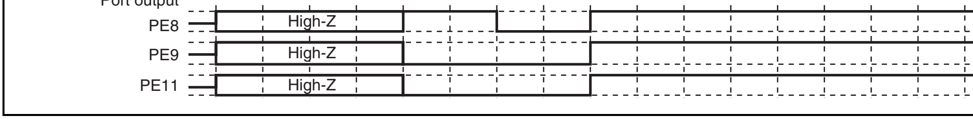


Figure 9.135 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronized PWM Mode

1 to 14 are the same as in figure 9.134.

15. Select the reset-synchronized PWM output level and cyclic output enabling/disabling TOCR.
16. Set reset-synchronized PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU2 output with the PFC.
19. Operation is restarted by TSTR.

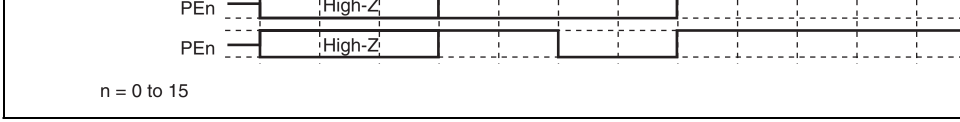


Figure 9.136 Error Occurrence in PWM Mode 2, Recovery in Normal Mo

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. Set PWM mode 2.
3. Initialize the pins with TIOR. (The example shows initial high output, with low out compare-match occurrence. In PWM mode 2, the cycle register pins are not initializ example, TIOC *A is the cycle register.)
4. Set MTU2 output with the PFC.
5. The count operation is started by TSTR.
6. Output goes low on compare-match occurrence.
7. An error occurs.
8. Set port output with the PFC and output the inverse of the active level.
9. The count operation is stopped by TSTR.
10. Set normal mode.
11. Initialize the pins with TIOR.
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

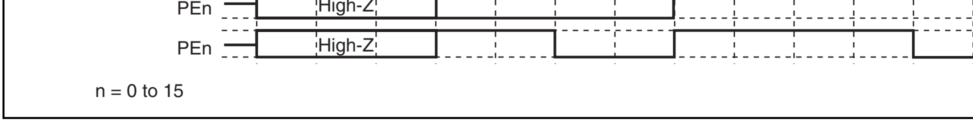


Figure 9.137 Error Occurrence in PWM Mode 2, Recovery in PWM Mode

1 to 9 are the same as in figure 9.136.

10. Set PWM mode 1.
11. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized.)
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

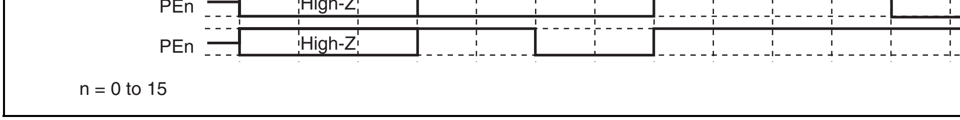


Figure 9.138 Error Occurrence in PWM Mode 2, Recovery in PWM Mod

1 to 9 are the same as in figure 9.136.

10. Not necessary when restarting in PWM mode 2.
11. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initia
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

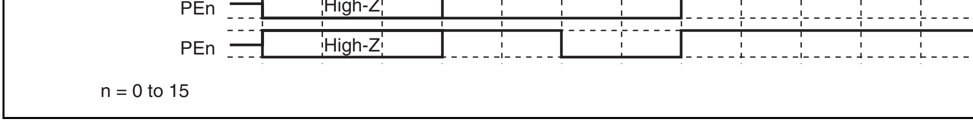


Figure 9.139 Error Occurrence in PWM Mode 2, Recovery in Phase Counting

1 to 9 are the same as in figure 9.136.

10. Set phase counting mode.
11. Initialize the pins with TIOR.
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

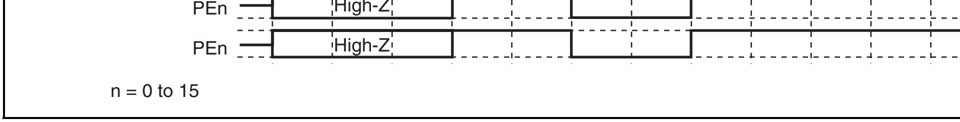


Figure 9.140 Error Occurrence in Phase Counting Mode, Recovery in Normal

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. Set phase counting mode.
3. Initialize the pins with TIOR. (The example shows initial high output, with low out compare-match occurrence.)
4. Set MTU2 output with the PFC.
5. The count operation is started by TSTR.
6. Output goes low on compare-match occurrence.
7. An error occurs.
8. Set port output with the PFC and output the inverse of the active level.
9. The count operation is stopped by TSTR.
10. Set in normal mode.
11. Initialize the pins with TIOR.
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

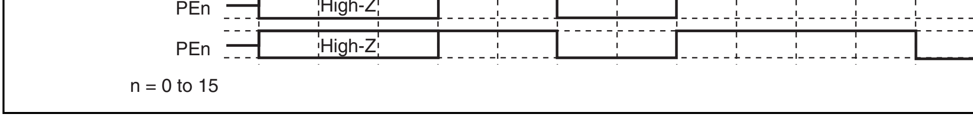


Figure 9.141 Error Occurrence in Phase Counting Mode, Recovery in PWM M

1 to 9 are the same as in figure 9.140.

10. Set PWM mode 1.
11. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

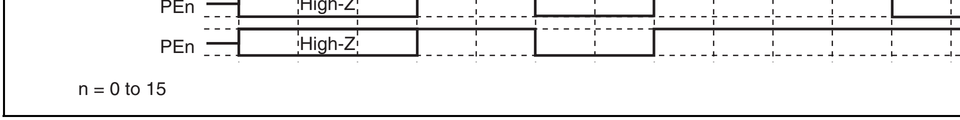


Figure 9.142   Error Occurrence in Phase Counting Mode, Recovery in PWM M

1 to 9 are the same as in figure 9.140.

10. Set PWM mode 2.
11. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initia
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

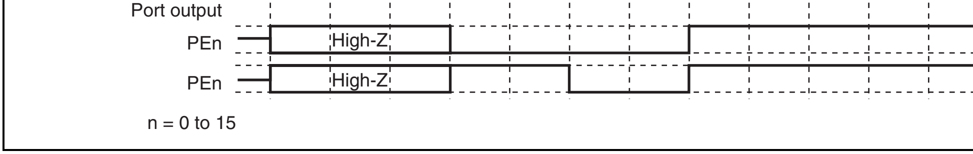


Figure 9.143 Error Occurrence in Phase Counting Mode, Recovery in Phase Counting Mode

1 to 9 are the same as in figure 9.140.

10. Not necessary when restarting in phase counting mode.
11. Initialize the pins with TIOR.
12. Set MTU2 output with the PFC.
13. Operation is restarted by TSTR.

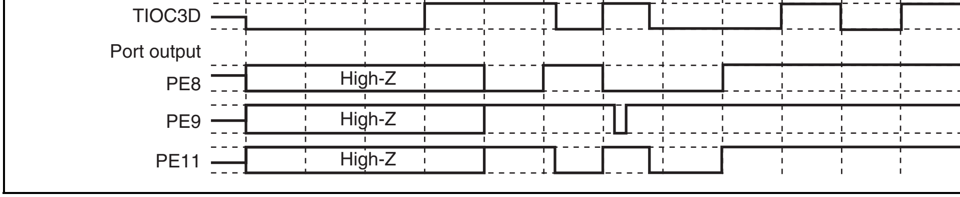


Figure 9.144 Error Occurrence in Complementary PWM Mode, Recovery in Normal Mode

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. Select the complementary PWM output level and cyclic output enabling/disabling v TOCR.
3. Set complementary PWM.
4. Enable channel 3 and 4 output with TOER.
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. The complementary PWM waveform is output on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR. (MTU2 output becomes the complementa output initial value.)
11. Set normal mode. (MTU2 output goes low.)
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

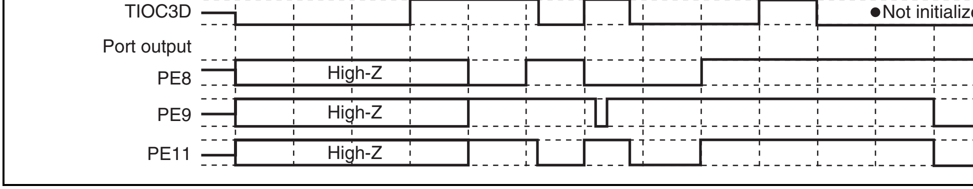


Figure 9.145 Error Occurrence in Complementary PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 9.144.

11. Set PWM mode 1. (MTU2 output goes low.)
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

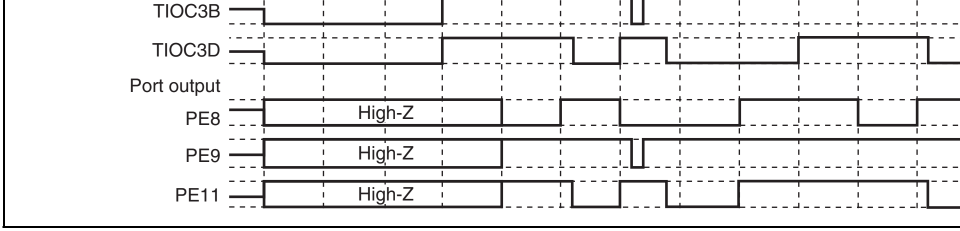


Figure 9.146 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 9.144.

11. Set MTU2 output with the PFC.
12. Operation is restarted by TSTR.
13. The complementary PWM waveform is output on compare-match occurrence.

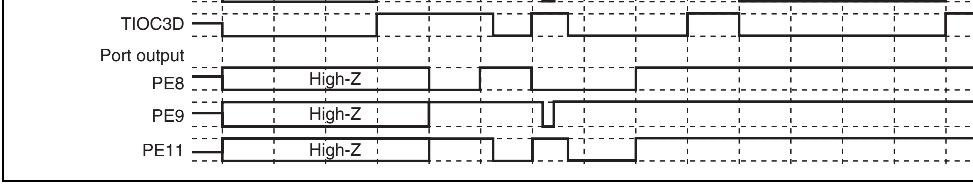


Figure 9.147 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 9.144.

11. Set normal mode and make new settings. (MTU2 output goes low.)
12. Disable channel 3 and 4 output with TOER.
13. Select the complementary PWM mode output level and cyclic output enabling/disabl TOCR.
14. Set complementary PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set MTU2 output with the PFC.
17. Operation is restarted by TSTR.

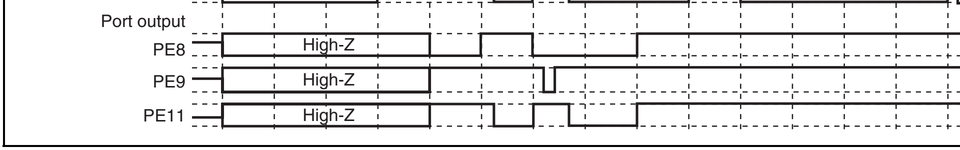


Figure 9.148 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronized PWM Mode

1 to 10 are the same as in figure 9.144.

11. Set normal mode. (MTU2 output goes low.)
12. Disable channel 3 and 4 output with TOER.
13. Select the reset-synchronized PWM mode output level and cyclic output enabling/d with TOCR.
14. Set reset-synchronized PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set MTU2 output with the PFC.
17. Operation is restarted by TSTR.

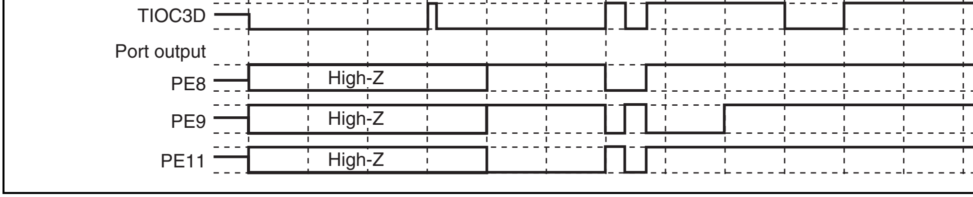


Figure 9.149 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Normal Mode

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. Select the reset-synchronized PWM output level and cyclic output enabling/disabling TOCR.
3. Set reset-synchronized PWM.
4. Enable channel 3 and 4 output with TOER.
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. The reset-synchronized PWM waveform is output on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR. (MTU2 output becomes the reset-synchron PWM output initial value.)
11. Set normal mode. (MTU2 positive phase output is low, and negative phase output is
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

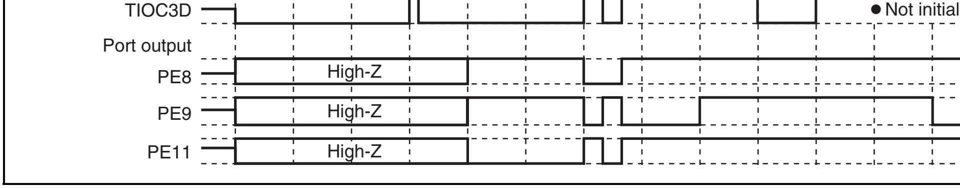


Figure 9.150 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 9.149.

11. Set PWM mode 1. (MTU2 positive phase output is low, and negative phase output
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

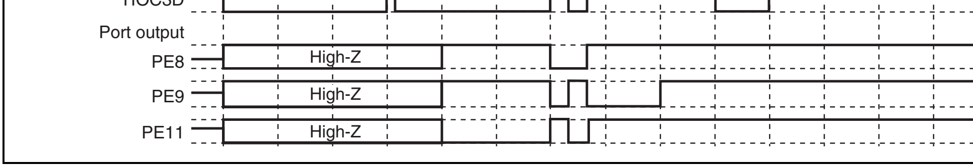


Figure 9.151 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 9.149.

11. Disable channel 3 and 4 output with TOER.
12. Select the complementary PWM output level and cyclic output enabling/disabling wi TOCR.
13. Set complementary PWM. (The MTU2 cyclic output pin goes low.)
14. Enable channel 3 and 4 output with TOER.
15. Set MTU2 output with the PFC.
16. Operation is restarted by TSTR.

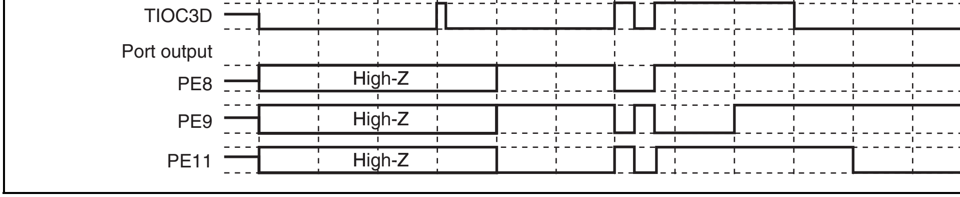


Figure 9.152 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Reset-Synchronized PWM Mode

1 to 10 are the same as in figure 9.149.

11. Set MTU2 output with the PFC.
12. Operation is restarted by TSTR.
13. The reset-synchronized PWM waveform is output on compare-match occurrence.

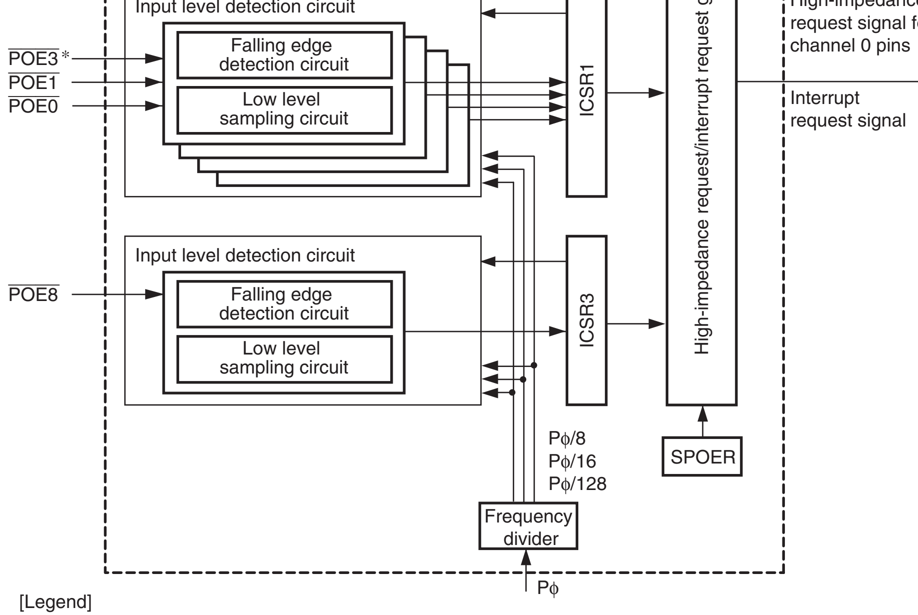
- Each of the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, and $\overline{\text{POE8}}$ input pins can be set for falling edge, P Pϕ/16 × 16, or Pϕ/128 × 16 low-level sampling.
- High-current pins and the pins for channel 0 of the MTU2 can be placed in high-imp state by $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, and $\overline{\text{POE8}}$ pin falling-edge or low-level sampling.
- High-current pins can be placed in high-impedance state when the high-current pin o levels are compared and simultaneous active-level output continues for one cycle or
- High-current pins and the pins for channel 0 of the MTU2 can be placed in high-imp state by modifying the POE register settings.
- Interrupts can be generated by input-level sampling or output-level comparison resul

The POE has input level detection circuits, output level comparison circuits, and a high- request/interrupt request generating circuit as shown in figure 10.1, Block Diagram of P

In addition to control by the POE, high-current pins can be placed in high-impedance sta the oscillator stops or in software standby state. For details, refer to appendix A, Pin Sta

Note: * The $\overline{\text{POE3}}$ pin is supported only by the SH7125.

TIMMTU1A_020020030800


Input level detection circuit
Falling edge detection circuit
Low level sampling circuit
POE3*
POE1
POE0
ICSR1
High-impedance request/interrupt request g
High-impedanc
request signal f
channel 0 pins
Interrupt
request signal
Input level detection circuit
POE8
Falling edge detection circuit
Low level sampling circuit
ICSR3
Pφ/8
Pφ/16
Pφ/128
SPOER
Frequency divider
Pφ

[Legend]

ICSR1: Input level control/status register 1
ICSR3: Input level control/status register 3
OCSR1: Output level control/status register 1
POECR1: Port output enable control register 1
POECR2: Port output enable control register 2
SPOER: Software port output enable register

Note: * This pin is supported only by the SH7125.

Figure 10.1 Block Diagram of POE

Note: * When the $\overline{\text{POE3}}$ function is selected in the PFC, the pin is pulled up inside th nothing is input to it. The $\overline{\text{POE3}}$ pin is supported only by the SH7125.

Table 10.2 shows output-level comparisons with pin combinations.

Table 10.2 Pin Combinations

Pin Combination	I/O	Description
PE9/TIOC3B and PE11/TIOC3D	Output	The high-current pins for the MTU2 are p high-impedance state when the pins simultaneously output an active level (lov when the output level select P (OLSP) bi timer output control register (TOCR) in th 0 or high level when the bit is 1) for one c cycles of the peripheral clock (Pϕ). This active level comparison is done whe MTU2 output function or general output f selected in the pin function controller. If a function is selected, the output level is no checked. Pin combinations for output comparison a impedance control can be selected by P(registers.
PE12/TIOC4A and PE14/TIOC4C		
PE13/TIOC4B and PE15/TIOC4D		

Output level control/status register 1	OCSR1	R/W	H'0000	H'FFFFD002	8, 1
Input level control/status register 3	ICSR3	R/W	H'0000	H'FFFFD008	8, 1
Software port output enable register	SPOER	R/W	H'00	H'FFFFD00A	8
Port output enable control register 1	POECR1	R/W	H'00	H'FFFFD00B	8
Port output enable control register 2	POECR2	R/W	H'7700	H'FFFFD00C	8, 1

Bit	Bit Name	Initial value	R/W	Description
15	POE3F	0	R/(W)*[1]	POE3 Flag (Supported only by the SH7125.) This flag indicates that a high impedance reque been input to the POE3 pin. [Clearing conditions] • By writing 0 to POE3F after reading POE3F (when the falling edge is selected by bits 7 ICSR1) • By writing 0 to POE3F after reading POE3F a high level input to POE3 is sampled at Pϕ or Pϕ/128 clock (when low-level sampling is by bits 7 and 6 in ICSR1) [Setting condition] • When the input set by ICSR1 bits 7 and 6 o the POE3 pin
14	—	0	R/(W)*[1]	Reserved This bit is always read as 0. The write value sh always be 0.

				• a high level input to POE1 is sampled at Pϕ/8 or Pϕ/128 clock (when low-level sampling is s by bits 3 and 2 in ICSR1) [Setting condition] • When the input set by ICSR1 bits 3 and 2 oc the $\overline{\text{POE1}}$ pin
12	POE0F	0	R/(W)*[1]	POE0 Flag This flag indicates that a high impedance reques been input to the $\overline{\text{POE0}}$ pin. [Clearing conditions] • By writing 0 to POE0F after reading POE0F = (when the falling edge is selected by bits 1 ar ICSR1) • By writing 0 to POE0F after reading POE0F = a high level input to POE0 is sampled at Pϕ/8 or Pϕ/128 clock (when low-level sampling is s by bits 1 and 0 in ICSR1) [Setting condition] • When the input set by ICSR1 bits 1 and 0 oc the $\overline{\text{POE0}}$ pin
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value always be 0.

				These bits select the input mode of the POE3 p 00: Accept request on falling edge of POE3 inp 01: Accept request when POE3 input has been for 16 Pϕ/8 clock pulses and all are low leve 10: Accept request when POE3 input has been for 16 Pϕ/16 clock pulses and all are low lev 11: Accept request when POE3 input has been for 16 Pϕ/128 clock pulses and all are low le
5, 4	—	All 0	R/W*[2]	Reserved These bits are always read as 0. The write valu always be 0.
3, 2	POE1M[1:0]	00	R/W*[2]	POE1 mode 1, 0 These bits select the input mode of the $\overline{\text{POE1}}$ p 00: Accept request on falling edge of POE1 inp 01: Accept request when POE1 input has been for 16 Pϕ/8 clock pulses and all are low leve 10: Accept request when POE1 input has been for 16 Pϕ/16 clock pulses and all are low lev 11: Accept request when POE1 input has been for 16 Pϕ/128 clock pulses and all are low le

for 16 × φ/128 clock pulses and all are low le

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed w

2. Can be modified only once after a power-on reset.

10.3.2 Output Level Control/Status Register 1 (OCSR1)

OCSR1 is a 16-bit readable/writable register that controls the enable/disable of both outp comparison and interrupts, and indicates status.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	OSF1	-	-	-	-	-	OCE1	OIE1	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*1	R	R	R	R	R	R/W*2	R/W	R	R	R	R	R	R

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

2. Can be modified only once after a power-on reset.

Bit	Bit Name	Initial value	R/W	Description
15	OSF1	0	R/(W)*1	Output Short Flag 1 This flag indicates that any one of the three pairs MTU2 2-phase outputs to be compared has simultaneously become an active level. [Clearing condition] • By writing 0 to OSF1 after reading OSF1 = 1 [Setting condition] • When any one of the three pairs of 2-phase o has simultaneously become an active level

8	OIE1	0	R/W	Output Short Interrupt Enable 1 This bit enables or disables interrupt requests w OSF1 bit in OCSR is set to 1. 0: Interrupt requests disabled 1: Interrupt requests enabled
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed

2. Can be modified only once after a power-on reset.

10.3.3 Input Level Control/Status Register 3 (ICSR3)

ICSR3 is a 16-bit readable/writable register that selects the $\overline{\text{POE8}}$ pin input mode, contro enable/disable of interrupts, and indicates status.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	POE8F	-	-	POE8E	PIE3	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/(W)*1	R	R	R/W*2	R/W	R	R	R	R	R	R

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

2. Can be modified only once after a power-on reset.

				(when the falling edge is selected by bits 1 a ICSR3)· • By writing 0 to POE8F after reading POE8F a high level input to POE8 is sampled at Pf/ or Pf/128 clock (when low-level sampling is by bits 1 and 0 in ICSR3) [Setting condition] • When the input condition set by bits 1 and 0 ICSR3 occurs at the $\overline{\text{POE8}}$ pin
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
9	POE8E	0	R/W*[2]	POE8 High-Impedance Enable This bit specifies whether to place the pins in hi impedance state when the POE8F bit in ICSR3 to 1. 0: Does not place the pins in high-impedance st 1: Places the pins in high-impedance state
8	PIE3	0	R/W	Port Interrupt Enable 3 (Supported only by the SH7125. Write 0 to this SH7124.) This bit enables or disables interrupt requests w POE8 bit in ICSR3 is set to 1. 0: Interrupt requests disabled 1: Interrupt requests enabled

10: Accept request when POE8 input has bee
for 16 Pϕ/16 clock pulses and all are low le

11: Accept request when POE8 input has bee
for 16 Pϕ/128 clock pulses and all are low

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed
2. Can be modified only once after a power-on reset.

10.3.4 Software Port Output Enable Register (SPOER)

SPOER is an 8-bit readable/writable register that controls high-impedance state of the p

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	MTU2 CH0HIZ	MTU2 CH34HIZ
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.
2	—	0	R/W	Reserved This bit is always read as 0. The write value always be 0.

				1: Places the pins in high-impedance state [Setting condition] • By writing 1 to MTU2CH0HIZ
0	MTU2CH34HIZ	0	R/W	MTU2 Channel 3 and 4 Output High-Impedar This bit specifies whether to place the high-c pins for the MTU2 in high-impedance state. 0: Does not place the pins in high-impedance [Clearing conditions] • Power-on reset • By writing 0 to MTU2CH34HIZ after readi MTU2CH34HIZ = 1 1: Places the pins in high-impedance state [Setting condition] • By writing 1 to MTU2CH34HIZ

Bit	Bit Name	Initial value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.
3	MTU2PE3ZE	0	R/W*	MTU2 PE3 High-Impedance Enable This bit specifies whether to place the PE3/ pin for channel 0 in the MTU2 in high-impec state when either POE8F or MTU2CH0HIZ to 1. 0: Does not place the pin in high-impedance 1: Places the pin in high-impedance state
2	MTU2PE2ZE	0	R/W*	MTU2 PE2 High-Impedance Enable This bit specifies whether to place the PE2/ pin for channel 0 in the MTU2 in high-impec state when either POE8F or MTU2CH0HIZ to 1. 0: Does not place the pin in high-impedance 1: Places the pin in high-impedance state
1	MTU2PE1ZE	0	R/W*	MTU2 PE1 High-Impedance Enable This bit specifies whether to place the PE1/ pin for channel 0 in the MTU2 in high-impec state when either POE8F or MTU2CH0HIZ to 1. 0: Does not place the pin in high-impedance 1: Places the pin in high-impedance state

10.3.6 Port Output Enable Control Register 2 (POECR2)

POECR2 is a 16-bit readable/writable register that controls high-impedance state of the p

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	MTU2 P1CZE	MTU2 P2CZE	MTU2 P3CZE	-	-	-	-	-	-	-	-	-	-
Initial value:	0	1	1	1	0	1	1	1	0	0	0	0	0	0
R/W:	R	R/W*	R/W*	R/W*	R	R/W*	R/W*	R/W*	R	R	R	R	R	R

Note: * Can be modified only once after a power-on reset.

Bit	Bit Name	Initial value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
14	MTU2P1CZE	1	R/W*	MTU2 Port 1 Output Comparison/High-Impec Enable This bit specifies whether to compare output the MTU2 high-current PE9/TIOC3B and PE11/TIOC3D pins and to place them in high impedance state when the OSF1 bit is set to the OEC1 bit is 1 or when any one of the PO POE1F, POE3F, and MTU2CH34HIZ bits is s 0: Does not compare output levels or place th high-impedance state 1: Compares output levels and places the pir high-impedance state

				high-impedance state 1: Compares output levels and places the p high-impedance state
12	MTU2P3CZE	1	R/W*	MTU2 Port 3 Output Comparison/High-Impe Enable This bit specifies whether to compare outpu the MTU2 high-current PE13/TIOC4B and PE15/TIOC4D pins and to place them in hig impedance state when the OSF1 bit is set t the OEC1 bit is 1 or when any one of the PO POE1F, POE3F, and MTU2CH34HIZ bits is 0: Does not compare output levels or place high-impedance state 1: Compares output levels and places the p high-impedance state
11	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
10 to 8	—	All 1	R/W*	Reserved These bits are always read as 1. The write v should always be 1.
7 to 0	—	0	R	Reserved These bits are always read as 0. The write v should always be 0.

Note: * Can be modified only once after a power-on reset.

MTU2 high-current pins (PE12/TIOC4A and PE14/TIOC4C)	Input level detection, output level comparison, or SPOER setting	MTU2P2CZE • ((POE3F + POE1F + POE0F) + (OSF1 • OCE1) + (MTU2CH34H
MTU2 high-current pins (PE13/TIOC4B and PE15/TIOC4D)	Input level detection, output level comparison, or SPOER setting	MTU2P3CZE • ((POE3F + POE1F + POE0F) + OCE1) + (MTU2CH34HIZ))
MTU2 channel 0 pin (PE0/TIOC0A)	Input level detection or SPOER setting	MTU2PE0ZE ((POE8F • POE8E) + (MTU2CH
MTU2 channel 0 pin (PE1/TIOC0B)	Input level detection or SPOER setting	MTU2PE1ZE ((POE8F • POE8E) + (MTU2CH
MTU2 channel 0 pin (PE2/TIOC0C)	Input level detection or SPOER setting	MTU2PE2ZE ((POE8F • POE8E) + (MTU2CH
MTU2 channel 0 pin (PE3/TIOC0D)	Input level detection or SPOER setting	MTU2PE3ZE ((POE8F • POE8E) + (MTU2CH

10.4.1 Input Level Detection Operation

If the input conditions set by ICSR1 occur on the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, and $\overline{\text{POE8}}$ pins, t current pins and the pins for channel 0 of the MTU2 are placed in high-impedance state. l however, that these high-current and MTU2 pins enter high-impedance state only when g input/output function or MTU2 function is selected for these pins.

(1) Falling Edge Detection

When a change from a high to low level is input to the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, and $\overline{\text{POE8}}$ p high-current pins and the pins for channel 0 of the MTU2 are placed in high-impedance s Figure 10.2 shows a sample timing after the level changes in input to the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, P and $\overline{\text{POE8}}$ pins until the respective pins enter high-impedance state.

Note: * This pin is supported only by the SH7125.

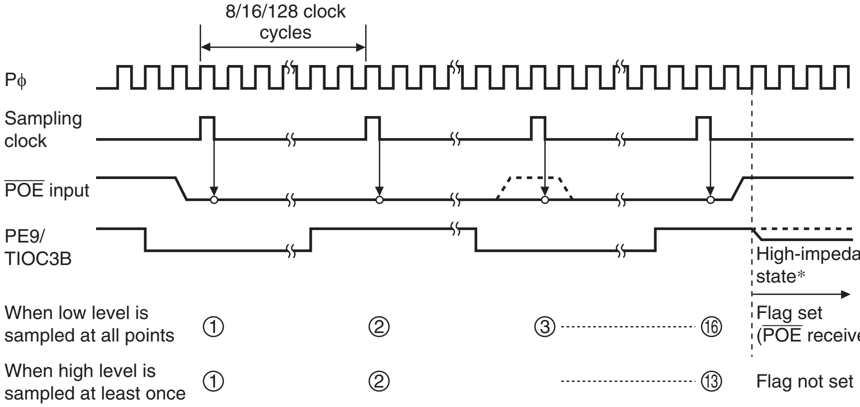
Note: * The other high-current pins also enter the high-impedance state in the similar timing.

Figure 10.2 Falling Edge Detection

(2) Low-Level Detection

Figure 10.3 shows the low-level detection operation. Sixteen continuous low levels are s
with the sampling clock selected by ICSR1. If even one high level is detected during thi
the low level is not accepted.

The timing when the high-current pins enter the high-impedance state after the sampling
input is the same in both falling-edge detection and in low-level detection.



Note: * Other high-current pins also go to the high-impedance state at the same timing.

Figure 10.3 Low-Level Detection Operation

Figure 10.4 Output-Level Compare Operation

10.4.3 Release from High-Impedance State

High-current pins that have entered high-impedance state due to input-level detection can released either by returning them to their initial state with a power-on reset, or by clearing the flags in bits 12 to 15 (POE0F to POE3F and POE8F) in ICSR1. However, note that w level sampling is selected by bits 0 to 7 in ICSR1, just writing 0 to a flag is ignored (the f cleared); flags can be cleared by writing 0 to it only after a high level is input to the POE is sampled.

High-current pins that have entered high-impedance state due to output-level detection ca released either by returning them to their initial state with a power-on reset, or by clearing in bit 15 (OCF1) in OCSR1. However, note that just writing 0 to a flag is ignored (the fla cleared); flags can be cleared only after an inactive level is output from the high-current p Inactive-level outputs can be achieved by setting the MTU2 internal registers.

OEI3	Output enable interrupt 3	POE8F	PIE3 • POE8F

This also occurs when a power-on reset is issued from the WDT for pins that are being ha
high impedance due to short-circuit detection by the MTU2.

Figure 10.5 shows the state of a pin for which the POE input has selected high impedance
handling with the timer output selected when a power-on reset is issued from the WDT.

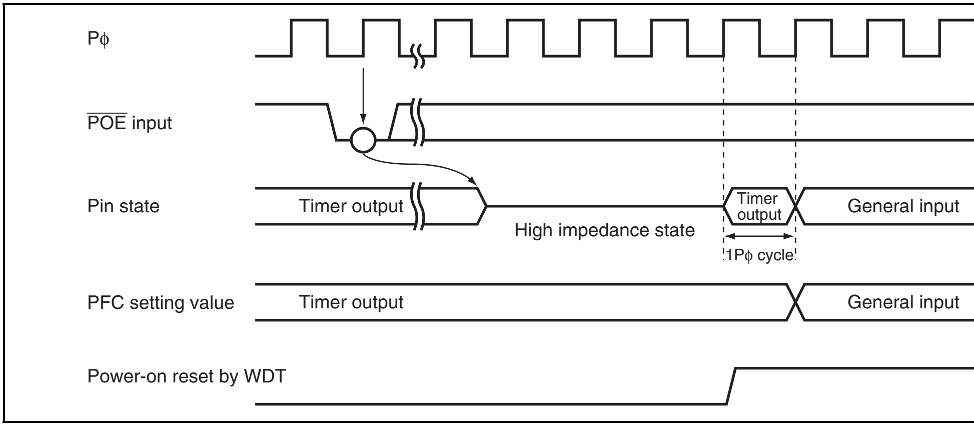


Figure 10.5 Pin State when a Power-On Reset is Issued from the Watchdog Ti

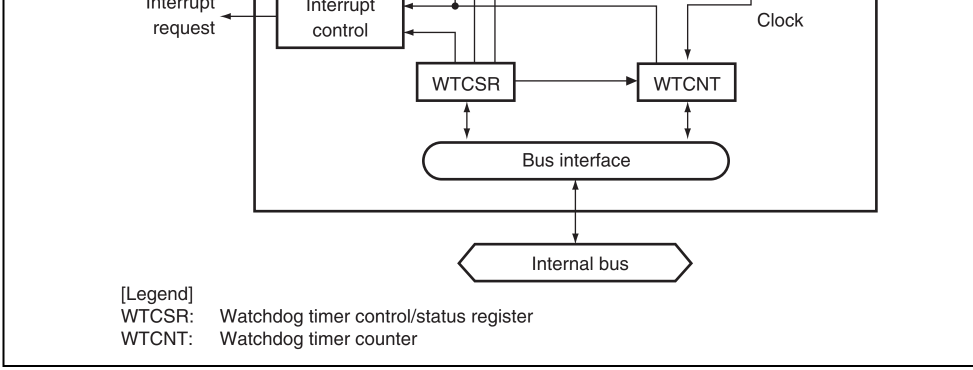
11.1 Features

- Can be used to ensure the clock settling time: Use the WDT to revoke software stanc
- Can switch between watchdog timer mode and interval timer mode.
- Generates internal resets in watchdog timer mode: Internal resets occur after counter
- An interrupt is generated in interval timer mode

  An interval timer interrupt is generated when the counter overflows.
- Choice of eight counter input clocks

  Eight clocks (×1 to ×1/4096) that are obtained by dividing the peripheral clock can b
- Choice of two resets

  Power-on reset and manual reset are available.



[Legend]
WTCSR: Watchdog timer control/status register
WTCNT: Watchdog timer counter

Figure 11.1 Block Diagram of WDT

11.3.1 Watchdog Timer Counter (WTCNT)

WTCNT is an 8-bit readable/writable register that increments on the selected clock. Whe overflow occurs, it generates a reset in watchdog timer mode and an interrupt in interval t mode. The WTCNT counter is not initialized by an internal reset due to the WDT overflo WTCNT counter is initialized to H'00 only by a power-on reset using the $\overline{\text{RES}}$ pin. Use a access to write to the WTCNT counter, with H'5A in the upper byte. Use a byte access to WTCNT.

Note: WTCNT differs from other registers in that it is more difficult to write to. See sec 11.3.3, Notes on Register Access, for details.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: WTCSR differs from other registers in that it is more difficult to write to. See se
11.3.3, Notes on Register Access, for details.

Bit:	7	6	5	4	3	2	1	0
	TME	WT/IT	RSTS	WOVF	IOVF	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TME	0	R/W	Timer Enable Starts and stops timer operation. Clear this bit t using the WDT to revoke software standby moc 0: Timer disabled: Count-up stops and WTCNT retained 1: Timer enabled
6	WT/IT	0	R/W	Timer Mode Select Selects whether to use the WDT as a watchdog an interval timer. 0: Interval timer mode 1: Watchdog timer mode Note: If WT/IT is modified when the WDT is op the up-count may not be performed cor

				timer mode. This bit is not set in interval timer mo 0: No overflow 1: WTCNT has overflowed in watchdog timer mo
3	IOVF	0	R/W	Interval Timer Overflow Indicates that the WTCNT has overflowed in inte mode. This bit is not set in watchdog timer mode 0: No overflow 1: WTCNT has overflowed in interval timer mode
2 to 0	CKS[2:0]	000	R/W	Clock Select 2 to 0 These bits select the clock to be used for the WT count from the eight types obtainable by dividing peripheral clock (Pϕ). The overflow period that is inside the parenthesis in the table is the value wh peripheral clock (Pϕ) is 40 MHz. 000: Pϕ (6.4 μs) 001: Pϕ /4 (25.6 μs) 010: Pϕ /16 (102.4 μs) 011: Pϕ /32 (204.8 μs) 100: Pϕ /64 (409.6 μs) 101: Pϕ /256 (1.64 ms) 110: Pϕ /1024 (6.55 ms) 111: Pϕ /4096 (26.21 ms) Note: If bits CKS2 to CKS0 are modified when is operating, the up-count may not be pe correctly. Ensure that these bits are mod when the WDT is not operating.

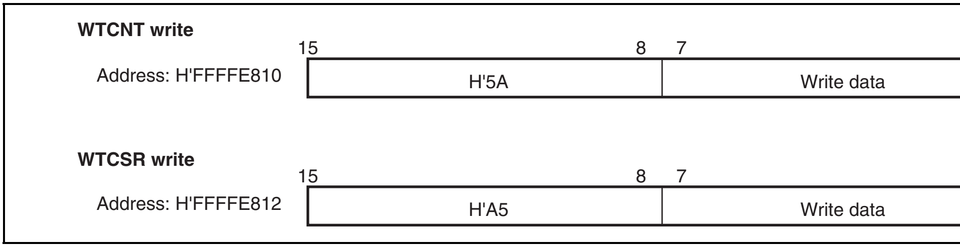


Figure 11.2 Writing to WTCNT and WTCSR

count overflows.

2. Set the type of count clock used in the CKS2 to CKS0 bits in WTCSR and the initial v the counter in the WTCNT counter. These values should ensure that the time till coun overflow is longer than the clock oscillation settling time.
3. Transition to software standby mode by executing a SLEEP instruction to stop the clo
4. The WDT starts counting by detecting a change in the level input to the NMI or IRQ p
5. When the WDT count overflows, the CPG starts supplying the clock and the LSI resu operation. The WOVF flag in WTCSR is not set when this happens.

11.4.2 Using Watchdog Timer Mode

While operating in watchdog timer mode, the WDT generates an internal reset of the type specified by the RSTS bit in WTCSR and asserts a signal through the $\overline{\text{WDTOVF}}$ pin ever the counter overflows.

1. Set the WT/IT bit in WTCSR to 1, set the reset type in the RSTS bit, set the type of co clock in the CKS2 to CKS0 bits, and set the initial value of the counter in the WTCN counter.
2. Set the TME bit in WTCSR to 1 to start the count in watchdog timer mode.
3. While operating in watchdog timer mode, rewrite the counter periodically to prevent t counter from overflowing.
4. When the counter overflows, the WDT sets the WOVF flag in WTCSR to 1, asserts a through the $\overline{\text{WDTOVF}}$ pin for one cycle of the count clock specified by the CKS2 to C bits, and generates a reset of the type specified by the RSTS bit. The counter then resu counting.

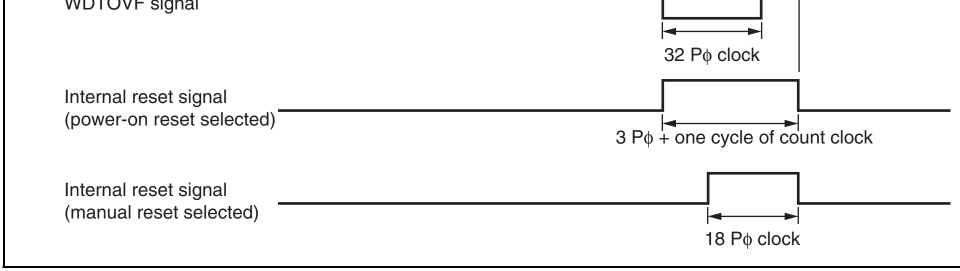


Figure 11.3 Operation in Watchdog Timer Mode
(When WTCNT Count Clock is Specified to Pϕ/32 by CKS2 to CKS0)

11.4.3 Using Interval Timer Mode

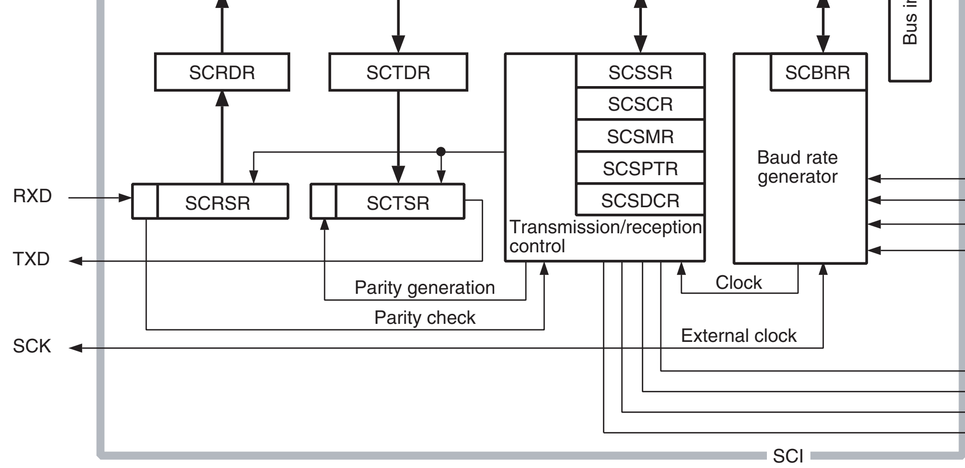
When operating in interval timer mode, interval timer interrupts are generated at every o
the counter. This enables interrupts to be generated at set periods.

1. Clear the WT/IT bit in WTCSR to 0, set the type of count clock in the CKS2 to CKS
   set the initial value of the counter in the WTCNT counter.
2. Set the TME bit in WTCSR to 1 to start the count in interval timer mode.
3. When the counter overflows, the WDT sets the IOVF flag in WTCSR to 1 and an int
   timer interrupt request is sent to the INTC. The counter then resumes counting.

11.5.2 $\overline{\text{WDTOVF}}$ Signal Connection

If $\overline{\text{WDTOVF}}$ is not used, leave the pin open. Do not pull down the $\overline{\text{WDTOVF}}$ pin. When absolutely necessary, pull it down through a resistor of 1 MΩ or larger.

- Choice of asynchronous or clock synchronous serial communication mode
- Asynchronous mode (channels 0 to 2 in the SH7125, channels 0 to 2 in the SH7124)
  - Serial data communication is performed by start-stop in character units. The SCI
    communicate with a universal asynchronous receiver/transmitter (UART), an asy
    communication interface adapter (ACIA), or any other communications chip that
    a standard asynchronous serial system. There are twelve selectable serial data communication formats.
  - Data length: 7 or 8 bits
  - Stop bit length: 1 or 2 bits
  - Parity: Even, odd, or none
  - Multiprocessor communications
  - Receive error detection: Parity, overrun, and framing errors
  - Break detection: Break is detected by reading the RXD pin level directly when a
    error occurs.
- Clock synchronous mode (channels 0 to 2 in the SH7125, channels 0 and 2 in the SH
  - Serial data communication is synchronized with a clock signal. The SCIF can co
    with other chips having a clock synchronous communication function.
  - Data length: 8 bits
  - Receive error detection: Overrun errors
- Full duplex communication: The transmitting and receiving sections are independent
  SCI can transmit and receive simultaneously. Both sections use double buffering, so
  speed continuous data transfer is possible in both transmit and receive directions.
- On-chip baud rate generator with selectable bit rates
- Internal or external transmit/receive clock source: From either baud rate generator (i
  clock) or SCK pin (external clock)
- Choice of LSB-first or MSB-first data transfer (except for 7-bit data in asynchronous



[Legend]
SCRSR: Receive shift register
SCRDR: Receive data register
SCTSR: Transmit shift register
SCTDR: Transmit data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCSSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register

Figure 12.1 Block Diagram of SCI

1	SCK1*	I/O	SCI1 clock input/output
	RXD1	Input	SCI1 receive data input
	TXD1	Output	SCI1 transmit data output
2	SCK2	I/O	SCI2 clock input/output
	RXD2	Input	SCI2 receive data input
	TXD2	Output	SCI2 transmit data output

Notes: 1. Pin names SCK, RXD, and TXD are used in the description for all channels, o the channel designation.

2. This pin is supported only by the SH7125. Channel 1 in the SH7124 is only fo asynchronous mode.

	Serial control register_0	SCSCR_0	R/W	H'00	H'FFFFC004	8
	Transmit data register_0	SCTDR_0	—	—	H'FFFFC006	8
	Serial status register_0	SCSSR_0	R/W	H'84	H'FFFFC008	8
	Receive data register_0	SCRDR_0	—	—	H'FFFFC00A	8
	Serial direction control register_0	SCSDCR_0	R/W	H'F2	H'FFFFC00C	8
	Serial port register_0	SCSPTR_0	R/W	H'0x	H'FFFFC00E	8
1	Serial mode register_1	SCSMR_1	R/W	H'00	H'FFFFC080	8
	Bit rate register_1	SCBRR_1	R/W	H'FF	H'FFFFC082	8
	Serial control register_1	SCSCR_1	R/W	H'00	H'FFFFC084	8
	Transmit data register_1	SCTDR_1	—	—	H'FFFFC086	8
	Serial status register_1	SCSSR_1	R/W	H'84	H'FFFFC088	8
	Receive data register_1	SCRDR_1	—	—	H'FFFFC08A	8
	Serial direction control register_1	SCSDCR_1	R/W	H'F2	H'FFFFC08C	8
	Serial port register_1	SCSPTR_1	R/W	H'0x	H'FFFFC08E	8
2	Serial mode register_2	SCSMR_2	R/W	H'00	H'FFFFC100	8
	Bit rate register_2	SCBRR_2	R/W	H'FF	H'FFFFC102	8
	Serial control register_2	SCSCR_2	R/W	H'00	H'FFFFC104	8
	Transmit data register_2	SCTDR_2	—	—	H'FFFFC106	8
	Serial status register_2	SCSSR_2	R/W	H'84	H'FFFFC108	8
	Receive data register_2	SCRDR_2	—	—	H'FFFFC10A	8
	Serial direction control register_2	SCSDCR_2	R/W	H'F2	H'FFFFC10C	8
	Serial port register_2	SCSPTR_2	R/W	H'0x	H'FFFFC10E	8

12.3.2 Receive Data Register (SCRDR)

SCRDR is a register that stores serial receive data. After receiving one byte of serial dat transfers the received data from the receive shift register (SCRSR) into SCRDR for stora completes operation. After that, SCRSR is ready to receive data.

Since SCRSR and SCRDR work as a double buffer in this way, data can be received co

SCRDR is a read-only register and cannot be written to by the CPU.

Bit:	7	6	5	4	3	2	1	0
Initial value:	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R

12.3.3 Transmit Shift Register (SCTSR)

SCTSR transmits serial data. The SCI loads transmit data from the transmit data registe into SCTSR, and then transmits the data serially from the TXD pin, LSB (bit 0) first. Af transmitting one data byte, the SCI automatically loads the next transmit data from SCT SCTSR and starts transmitting again. If the TDRE flag in the serial status register (SCS to 1, the SCI does not transfer data from SCTDR to SCTSR. The CPU cannot read or w SCTSR directly.

Bit:	7	6	5	4	3	2	1	0
Initial value:	-	-	-	-	-	-	-	-
R/W:	-	-	-	-	-	-	-	-

R/W: R/W R/W R/W R/W R/W R/W R/W R/W

12.3.5 Serial Mode Register (SCSMR)

SCSMR is an 8-bit register that specifies the SCI serial communication format and select clock source for the baud rate generator.

The CPU can always read and write to SCSMR.

Bit:	7	6	5	4	3	2	1	0
	$C/\overline{A}$	CHR	PE	$O/\overline{E}$	STOP	MP	CKS[1:0]	
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7	$C/\overline{A}$	0	R/W	Communication Mode Selects whether the SCI operates in asynchror clock synchronous mode. 0: Asynchronous mode 1: Clock synchronous mode (Channel 1 in the is not available.)

				Selects whether to add a parity bit to transmit to check the parity of receive data, in asynchr mode. In clock synchronous mode, a parity bi added nor checked, regardless of the PE sett 0: Parity bit not added or checked 1: Parity bit added and checked* Note: * When PE is set to 1, an even or odd is added to transmit data, depending parity mode (O/$\overline{E}$) setting. Receive da is checked according to the even/odc mode setting.
4	O/$\overline{E}$	0	R/W	Parity mode Selects even or odd parity when parity bits ar and checked. The O/$\overline{E}$ setting is used only in asynchronous mode and only when the parity (PE) is set to 1 to enable parity addition and c The O/$\overline{E}$ setting is ignored in clock synchrono or in asynchronous mode when parity additior checking is disabled. 0: Even parity 1: Odd parity If even parity is selected, the parity bit is adde transmit data to make an even number of 1s i transmitted character and parity bit combined data is checked to see if it has an even numb the received character and parity bit combinec If odd parity is selected, the parity bit is addec transmit data to make an odd number of 1s in transmitted character and parity bit combined data is checked to see if it has an odd numbe the received character and parity bit combinec

				bit is 1, it is treated as a stop bit, but if the seco bit is 0, it is treated as the start bit of the next i character. Notes: 1. When transmitting, a single 1-bit is a the end of each transmitted characte 2. When transmitting, two 1 bits are ad end of each transmitted character.
2	MP	0	R/W	Multiprocessor Mode (only in asynchronous m Enables or disables multiprocessor mode. The O/$\overline{\text{E}}$ bit settings are ignored in multiprocessor 0: Multiprocessor mode disabled 1: Multiprocessor mode enabled
1, 0	CKS[1:0]	00	R/W	Clock Select 1 and 0 Select the internal clock source of the on-chip generator. Four clock sources are available. P Pϕ/16 and Pϕ/64. For further information on th source, bit rate register settings, and baud rat section 12.3.10, Bit Rate Register (SCBRR). 00: Pϕ 01: Pϕ/4 10: Pϕ/16 11: Pϕ/64 Note: Pϕ: Peripheral clock

Bit	Bit Name	Initial value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable Enables or disables a transmit-data-empty int (TXI) to be issued when the TDRE flag in the status register (SCSSR) is set to 1 after seria data is sent from the transmit data register (S the transmit shift register (SCTSR). TXI can be canceled by clearing the TDRE fla after reading TDRE = 1 or by clearing the TIE 0: Transmit-data-empty interrupt request (TXI disabled 1: Transmit-data-empty interrupt request (TXI enabled
6	RIE	0	R/W	Receive Interrupt Enable Enables or disables a receive-data-full interru and a receive error interrupt (ERI) to be issue the RDRF flag in SCSSR is set to 1 after the s received is transferred from the receive shift r (SCRSR) to the receive data register (SCRDF RXI can be canceled by clearing the RDRF fla reading RDRF =1. ERI can be canceled by cle FER, PER, or ORER flag to 0 after reading 1 flag. Both RXI and ERI can also be canceled clearing the RIE bit to 0. 0: Receive-data-full interrupt (RXI) and receiv interrupt (ERI) requests are disabled 1: Receive-data-full interrupt (RXI) and receiv interrupt (ERI) requests are enabled

				transmitter is enabled. Select the tr format in the serial mode register (S before setting TE to 1.
4	RE	0	R/W	Receive Enable Enables or disables the SCI serial receiver. 0: Receiver disabled*[1] 1: Receiver enabled*[2] Notes: 1. Clearing RE to 0 does not affect the flags (RDRF, FER, PER, and ORER flags retain their previous values. 2. Serial reception starts when a start detected in asynchronous mode, or synchronous clock input is detected synchronous mode. Select the rece format in SCSMR before setting RE
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (only when MF SCSMR in asynchronous mode) When this bit is set to 1, receive data in which multiprocessor bit is 0 is skipped and setting of RDRF, FER, and ORER status flags in SCSSR prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically to 0 and normal receiving operation is resumed details, see section 12.4.4, Multiprocessor Communication Function.

1, 0	CKE[1:0]	00	R/W	Clock Enable 1 and 0 Select the SCI clock source and enable or dis output from the SCK pin. Depending on the combination of CKE1 and CKE0, the SCK pin used for serial clock output or serial clock inpu When selecting the clock output in clock sync mode, set the C/$\overline{\text{A}}$ bit in SCSMR to 1 and ther CKE1 and CKE0. For details on clock source see table 12.14 in section 12.4, Operation. • Asynchronous mode 00: Internal clock, SCK pin used for input pin signal is ignored.) 01: Internal clock, SCK pin used for clock outp 10: External clock, SCK pin used for clock inp 11: External clock, SCK pin used for clock inp Clock synchronous mode 00: Internal clock, SCK pin used for synchron output 01: Internal clock, SCK pin used for synchron output 10: External clock, SCK pin used for synchror input 11: External clock, SCK pin used for synchror input Notes: 1. The output clock frequency is 16 ti bit rate. 2. The input clock frequency is 16 tim rate.

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial value	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Register Empty Indicates whether data has been transferred transmit data register (SCTDR) to the transm register (SCTSR) and SCTDR has become r be written with next serial transmit data. 0: Indicates that SCTDR holds valid transmit [Clearing condition] • When 0 is written to TDRE after reading T 1: Indicates that SCTDR does not hold valid data [Setting conditions] • By a power-on reset or in standby mode • When the TE bit in SCSCR is 0 • When data is transferred from SCTDR to and data can be written to SCTDR

1: Indicates that valid received data is store
SCRDR

[Setting condition]

- When serial reception ends normally an data is transferred from SCRSR to SCR

Note: SCRDR and the RDRF flag are not af retain their previous states even if an detected during data reception or if th the serial control register (SCSCR) is 0. If reception of the next data is comp while the RDRF flag is still set to 1, ar error will occur and the received data lost.

1: Indicates that an overrun error occurred du
reception*2

[Setting condition]

- When the next serial reception is complet
RDRF = 1

Notes: 1. The ORER flag is not affected an
its previous value when the RE bi
SCSCR is cleared to 0.

2. The receive data prior to the over
is retained in SCRDR, and the da
received subsequently is lost. Sub
serial reception cannot be continu
the ORER flag is set to 1.

- When 0 is written to FER after reading F

1: Indicates that a framing error occurred du reception

[Setting condition]

- When the SCI founds that the stop bit at of the received data is 0 after completing reception*2

Notes: 1. The FER flag is not affected and its previous value when the RE SCSCR is cleared to 0.

2. In 2-stop-bit mode, only the first checked for a value to 1; the sec bit is not checked. If a framing e occurs, the receive data is trans SCRDR but the RDRF flag is no Subsequent serial reception can continued while the FER flag is s

- When 0 is written to PER after reading P

1: Indicates that a parity error occurred durin
reception*[2]

[Setting condition]

- When the number of 1s in the received d
parity does not match the even or odd pa
specified by the $O/\overline{E}$ bit in the serial mod
(SCSMR).

Notes: 1. The PER flag is not affected and
its previous value when the RE bi
SCSCR is cleared to 0.

2. If a parity error occurs, the receiv
transferred to SCRDR but the RD
is not set. Subsequent serial rece
cannot be continued while the PE
set to 1.

				1: Indicates that transmission has ended [Setting conditions] • By a power-on reset or in standby mode • When the TE bit in SCSCR is 0 • When TDRE = 1 during transmission of of a 1-byte serial transmit character
1	MPB	0	R	Multiprocessor Bit Stores the multiprocessor bit found in the re data. When the RE bit in SCSCR is cleared previous state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer Specifies the multiprocessor bit value to be the transmit frame.

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed v

Initial value:	0	0	0	0	0	Undefined	0	1
R/W:	R/W	-	-	-	R/W	W	-	W

Bit	Bit Name	Initial value	R/W	Description
7	EIO	0	R/W	Error Interrupt Only Enables or disables RXI interrupts. While the E set to 1, the SCI does not request an RXI inter the CPU even if the RIE bit is set to 1. 0: The RIE bit enables or disables RXI and ER interrupts. While the RIE bit is 1, RXI and EF interrupts are sent to the INTC. 1: While the RIE bit is 1, only the ERI interrupt the INTC.
6 to 4	—	All 0	—	Reserved These bits are always read as 0. The write valu always be 0.
3	SPB1IO	0	R/W	Clock Port Input/Output in Serial Port Specifies the input/output direction of the SCK serial port. To output the data specified in the S bit through the SCK pin as a port output pin, se bit in SCSMR and the CKE1 and CKE0 bits in to 0. 0: Does not output the SPB1DT bit value throu SCK pin. 1: Outputs the SPB1DT bit value through the S

				This bit is always read as 0. The write value s always be 0.
0	SPB0DT	1	W	Serial Port Break Data Controls the TXD pins together with the TE bi SCSCR. However, the TXD pin function should be sele the Pin Function Controller (PFC). This bit is write-only bit. Undefined value is re

Setting value of TE bit in SCSCR	Setting value of SPB0DT bit	TXD pin state
0	0	Low output
0	1	High output (initial state)
1	*	Transmit data output in a with serial core logic.

Note: * Don't care

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	R	Reserved These bits are always read as 1. The write valu always be 1.
3	DIR	0	R/W	Data Transfer Direction Selects the serial/parallel conversion format. V an 8-bit transmit/receive format. 0: SCTDR contents are transmitted in LSB-firs Receive data is stored in SCRDR in LSB-firs 1: SCTDR contents are transmitted in MSB-firs Receive data is stored in SCRDR in MSB-fir
2	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
1	—	1	R	Reserved This bit is always read as 1. The write value sh always be 1.
0	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.

Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Asynchronous mode:

$$N = \frac{P\phi}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

- Clock synchronous mode:

$$N = \frac{P\phi}{8 \times 2^{2n-1} \times B} \times 10^6 - 1$$

B: Bit rate (bits/s)
N: SCBRR setting for baud rate generator ($0 \leq N \leq 255$)
(The setting value should satisfy the electrical characteristics.)
Pϕ: Operating frequency for peripheral modules (MHz)
n: Baud rate generator clock source ($n = 0, 1, 2, 3$) (for the clock sources and n, see table 12.3.)

$$\text{Error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

300	2	64	0.16	2	77	0.16	2	90	0.16	2	103	0.16	2	116	0.16	2	1
600	1	129	0.16	1	155	0.16	1	181	0.16	1	207	0.16	1	233	0.16	2	6
1200	1	64	0.16	1	77	0.16	1	90	0.16	1	103	0.16	1	116	0.16	1	1
2400	0	129	0.16	0	155	0.16	0	181	0.16	0	207	0.16	0	233	0.16	1	6
4800	0	64	0.16	0	77	0.16	0	90	0.16	0	103	0.16	0	116	0.16	0	1
9600	0	32	-1.36	0	38	0.16	0	45	-0.93	0	51	0.16	0	58	-0.69	0	6
14400	0	21	-1.36	0	25	0.16	0	29	1.27	0	34	-0.79	0	38	0.16	0	4
19200	0	15	1.73	0	19	-2.34	0	22	-0.93	0	25	0.16	0	28	1.02	0	3
28800	0	10	-1.36	0	12	0.16	0	14	1.27	0	16	2.12	0	19	-2.34	0	2
31250	0	9	0.00	0	11	0.00	0	13	0.00	0	15	0.00	0	17	0.00	0	1
38400	0	7	1.73	0	9	-2.34	0	10	3.57	0	12	0.16	0	14	-2.34	0	1

1200	1	142	0.16	1	155	0.16	1	168	0.16	1	181	0.16	1	194	0.16	1	20
2400	1	71	-0.54	1	77	0.16	1	84	-0.43	1	90	0.16	1	97	-0.35	1	10
4800	0	142	0.16	0	155	0.16	0	168	0.16	0	181	0.16	0	194	0.16	0	20
9600	0	71	-0.54	0	77	0.16	0	84	-0.43	0	90	0.16	0	97	-0.35	0	10
14400	0	47	-0.54	0	51	0.16	0	55	0.76	0	60	-0.39	0	64	0.16	0	68
19200	0	35	-0.54	0	38	0.16	0	41	0.76	0	45	-0.93	0	48	-0.35	0	51
28800	0	23	-0.54	0	25	0.16	0	27	0.76	0	29	1.27	0	32	-1.36	0	34
31250	0	21	0.00	0	23	0.00	0	25	0.00	0	27	0.00	0	29	0.00	0	31
38400	0	17	-0.54	0	19	-2.34	0	20	0.76	0	22	-0.93	0	23	1.73	0	25

1200	1	220	0.16	1	233	0.16	1	246	0.16	2	64
2400	1	110	-0.29	1	116	0.16	1	123	-0.24	1	129
4800	0	220	0.16	0	233	0.16	0	246	0.16	1	64
9600	0	110	-0.29	0	116	0.16	0	123	-0.24	0	129
14400	0	73	-0.29	0	77	0.16	0	81	0.57	0	86
19200	0	54	0.62	0	58	-0.69	0	61	-0.24	0	64
28800	0	36	-0.29	0	38	0.16	0	40	0.57	0	42
31250	0	33	0.00	0	35	0.00	0	37	0.00	0	39
38400	0	27	-1.18	0	28	1.02	0	30	-0.24	0	32

10000	0	249	1	74	1	87	1	99	1	112	1
25000	0	99	0	119	0	139	0	159	0	179	0
50000	0	49	0	59	0	69	0	79	0	89	0
100000	0	24	0	29	0	34	0	39	0	44	0
250000	0	9	0	11	0	13	0	15	0	17	0
500000	0	4	0	5	0	6	0	7	0	8	0
1000000	—	—	0	2	—	—	0	3	—	—	0
2500000	0	0*	—	—	—	—	—	—	—	—	0
5000000			—	—	—	—	—	—	—	—	0

10000	1	137	1	149	1	162	1	174	1	187	1
25000	0	219	0	239	1	64	1	69	1	74	1
50000	0	109	0	119	0	129	0	139	0	149	0
100000	0	54	0	59	0	64	0	69	0	74	0
250000	0	21	0	23	0	25	0	27	0	29	0
500000	0	10	0	11	0	12	0	13	0	14	0
1000000	—	—	0	5	—	—	0	6	—	—	0
2500000	—	—	—	—	—	—	—	—	0	2	—
5000000	—	—	—	—	—	—	—	—	—	—	—

10000	1	212	1	224	1	237	1
25000	1	84	1	89	1	94	1
50000	0	169	0	179	0	189	0
100000	0	84	0	89	0	94	0
250000	0	33	0	35	0	37	0
500000	0	16	0	17	0	18	0
1000000	—	—	0	8	—	—	0
2500000	—	—	—	—	—	—	0
5000000	—	—	—	—	—	—	0

[Legend]

Blank:	No setting possible
—:	Setting possible, but error occurs
*:	Continuous transmission/reception is disabled.
Note:	Settings with an error of 1% or less are recommended.

16	500000	0	0
18	562500	0	0
20	625000	0	0
22	687500	0	0
24	750000	0	0
26	812500	0	0
28	875000	0	0
30	937500	0	0
32	1000000	0	0
34	1062500	0	0
36	1125000	0	0
38	1187500	0	0
40	1250000	0	0

24	6.0000	375000
26	6.5000	406250
28	7.0000	437500
30	7.5000	468750
32	8.0000	500000
34	8.5000	531250
36	9.0000	562500
38	9.5000	593750
40	10.0000	625000

24	4.0000	4000000.0
26	4.3333	4333333.3
28	4.6667	4666666.7
30	5.0000	5000000.0
32	5.3333	5333333.3
34	5.6667	5666666.7
36	6.0000	6000000.0
38	6.3333	6333333.3
40	6.6667	6666666.7

combination of the C/A bit in SCSMR and the CKE1 and CKE0 bits in the serial control (SCSCR) as shown in table 12.14.

(1) Asynchronous Mode (Channels 0 to 2 in the SH7125, Channels 0 to 2 in the SH

- Data length is selectable: 7 or 8 bits.
- Parity bit is selectable. So is the stop bit length (1 or 2 bits). The combination of the p selections constitutes the communication format and character length.
- In receiving, it is possible to detect framing errors, parity errors, overrun errors, and b
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the clock supplied by th chip baud rate generator and can output a clock with a frequency 16 times the bit r
  - When an external clock is selected, the external clock input must have a frequency the bit rate. (The on-chip baud rate generator is not used.)

(2) Clock Synchronous Mode (Channels 0 to 2 in the SH7125, Channels 0 and 2 in SH7124)

- The transmission/reception format has a fixed 8-bit data length.
- In receiving, it is possible to detect overrun errors.
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the on-chip baud rate ge and outputs a serial clock signal to external devices.
  - When an external clock is selected, the SCI operates on the input serial clock. The baud rate generator is not used.

			1				2 bits
		1	0			Set	1 bit
			1				2 bits
1	x	x	x	Clock synchronous	8-bit	Not set	None

[Legend]

x: Don't care

Table 12.14 SCSMR and SCSCR Settings and SCI Clock Source Selection

SCSMR	SCSCR Settings				
Bit 7 C/$\overline{A}$	Bit 1 CKE1	Bit 0 CKE0	Mode	Clock Source	SCK Pin Function
0	0	0	Asynchronous	Internal	SCI does not use the SCK pin.
		1			Clock with a frequency 16 times is output.
	1	0		External	Input a clock with frequency 16 ti bit rate.
		1			
1	0	0	Clock synchronous	Internal	Serial clock is output.
		1			
	1	0		External	Input the serial clock.
		1			

monitors the line and starts serial communication when the line goes to the space (low) st indicating a start bit. One serial character consists of a start bit (low), data (LSB first), pa (high or low), and stop bit (high), in that order.

When receiving in asynchronous mode, the SCI synchronizes at the falling edge of the sta The SCI samples each data bit on the eighth pulse of a clock with a frequency 16 times th Receive data is latched at the center of each bit.

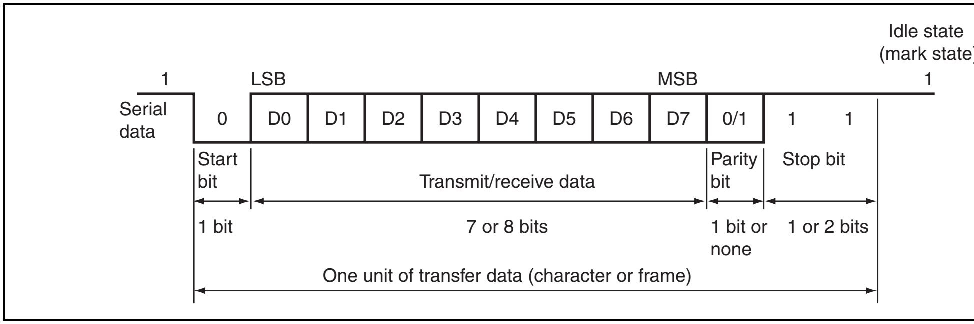


Figure 12.2 Example of Data Format in Asynchronous Communication (8-Bit Data with Parity and Two Stop Bits)

0	0	0	1	S	8-bit data	STOP	STOP	
0	1	0	0	S	8-bit data	P	STOP	
0	1	0	1	S	8-bit data	P	STOP	
1	0	0	0	S	7-bit data	STOP		
1	0	0	1	S	7-bit data	STOP	STOP	
1	1	0	0	S	7-bit data	P	STOP	
1	1	0	1	S	7-bit data	P	STOP	STOP
0	x	1	0	S	8-bit data	MPB	STOP	
0	x	1	1	S	8-bit data	MPB	STOP	
1	x	1	0	S	7-bit data	MPB	STOP	
1	x	1	1	S	7-bit data	MPB	STOP	STOP

[Legend]
S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit
x: Don't care

frequency of this output clock is equal to 16 times the desired bit rate.

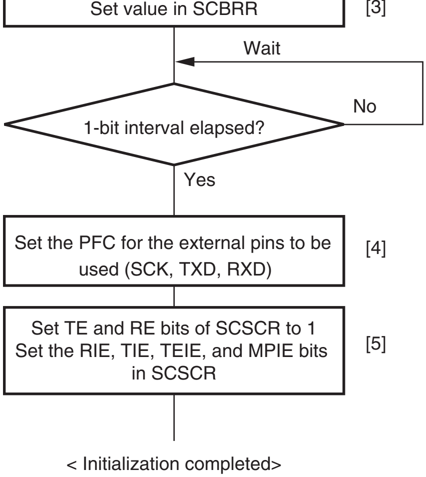
(3) Transmitting and Receiving Data

SCI Initialization (Asynchronous Mode):

Before transmitting or receiving, clear the TE and RE bits to 0 in the serial control registe (SCSCR), then initialize the SCI as follows.

When changing the operation mode or the communication format, always clear the TE an to 0 before following the procedure given below. Clearing the TE bit to 0 sets the TDRE and initializes the transmit shift register (SCTSR). Clearing the RE bit to 0, however, doe initialize the RDRF, PER, FER, and ORER flags or receives data register (SCRDR), whic their previous contents.

When an external clock is used, the clock should not be stopped during initialization or su operation. SCI operation becomes unreliable if the clock is stopped.

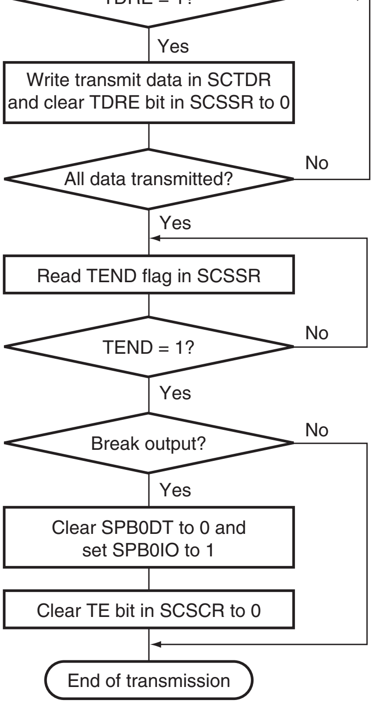

Set value in SCBRR
[3]
Wait
1-bit interval elapsed?
No
Yes
Set the PFC for the external pins to be used (SCK, TXD, RXD)
[4]
Set TE and RE bits of SCSCR to 1
Set the RIE, TIE, TEIE, and MPIE bits in SCSCR
[5]
< Initialization completed>

setting.

[5] Set the TE bit or RE bit in SCSCR to 1. Also make settings of the RIE, TIE, TEIE, and MPIE bits. At this time, the TXD, RXD, and SCK pins are ready to be used. The TXD pin is in a mark stat during transmitting, and RXD pin is in idle state for waiting the start bit during receiving.

Note : * In simultaneous transmit/receive operation, the TE and RE bits must be cleared to 0 or set to 1 simultaneously.

Figure 12.3 Sample Flowchart for SCI Initialization


TDRE = 1?
Yes
Write transmit data in SCTDR and clear TDRE bit in SCSSR to 0
All data transmitted?
No
Yes
Read TEND flag in SCSSR
TEND = 1?
No
Yes
Break output?
No
Yes
Clear SPB0DT to 0 and set SPB0IO to 1
Clear TE bit in SCSCR to 0
End of transmission

the TDRE flag to 0.

[2] Serial transmission continuation procedure:

To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to SCTDR, and then clear the TDRE flag to 0.

[3] Break output at the end of serial transmission:

To output a break in serial transmission, clear the SPB0DT bit to 0 and set the SPB0IO bit to 1 in SCSPTR, then clear the TE bit in SCSCR to 0.

Figure 12.4 Sample Flowchart for Transmitting Serial Data

B. Transmit data: 8-bit or 7-bit data is output in LSB-first order.

C. Parity bit or multiprocessor bit: One parity bit (even or odd parity) or one multipr bit is output. (A format in which neither parity nor multiprocessor bit is output ca selected.)

D. Stop bit(s): One or two 1 bits (stop bits) are output.

E. Mark state: 1 is output continuously until the start bit that starts the next transmis sent.

3. The SCI checks the TDRE flag at the timing for sending the stop bit.
If the TDRE flag is 0, the data is transferred from SCTDR to SCTSR, the stop bit is then serial transmission of the next frame is started.
If the TDRE flag is 1, the TEND flag in SCSSR is set to 1, the stop bit is sent, and th "mark state" is entered in which 1 is output. If the TEIE bit in SCSCR is set to 1 at th TEI interrupt request is generated.

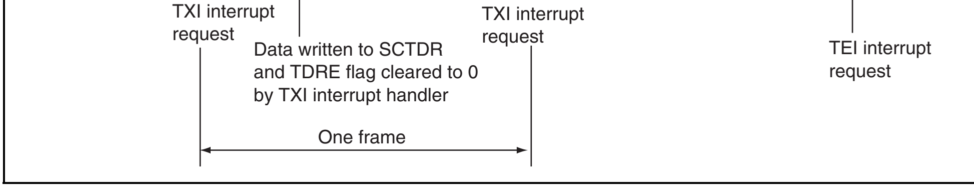
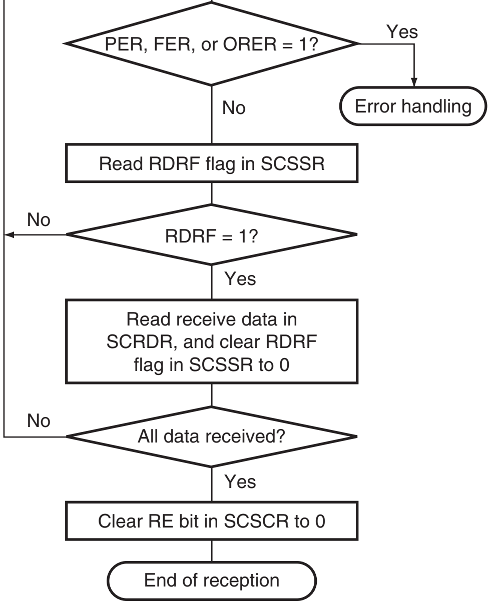

TXI interrupt request
Data written to SCTDR and TDRE flag cleared to 0 by TXI interrupt handler
TXI interrupt request
TEI interrupt request
One frame

Figure 12.5 Example of Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)



cleared to 0. Reception cannot be resumed if any of these flags are set to In the case of a framing error, a break can also be detected by reading the value of the RXD pin.

[2] SCI status check and receive data read

Read SCSSR and check that RDRF = then read the receive data in SCRDR clear the RDRF flag to 0.

[3] Serial reception continuation procedure

To continue serial reception, clear the RDRF flag to 0 before the stop bit for th current frame is received.

Figure 12.6 Sample Flowchart for Receiving Serial Data

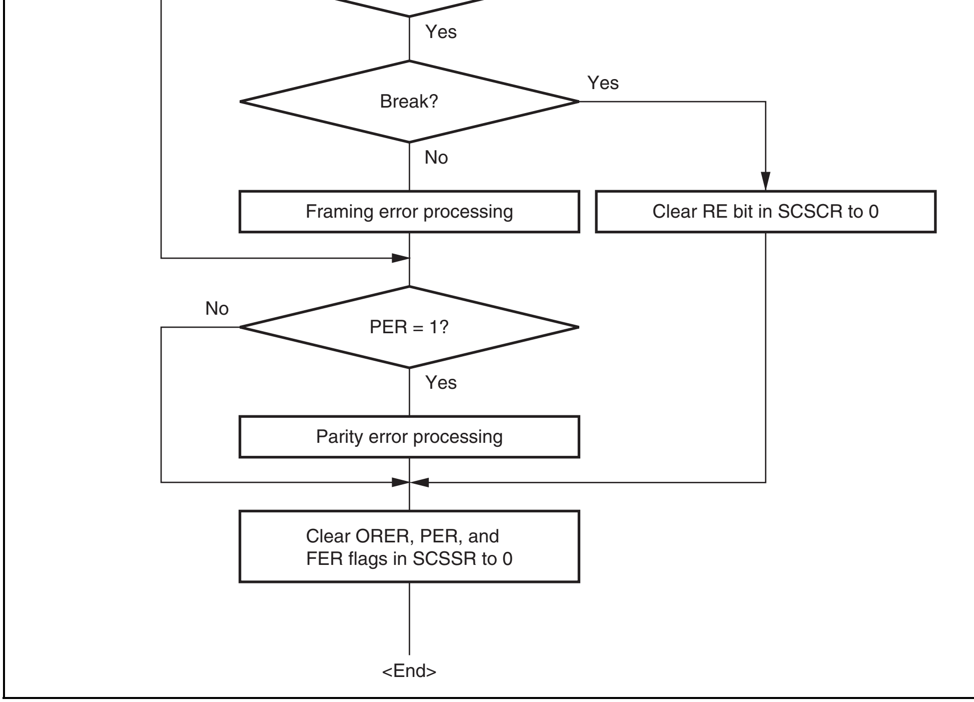


Figure 12.6 Sample Flowchart for Receiving Serial Data (cont)

B. Stop bit check: The SCI checks whether the stop bit is 1. If there are two stop bit
first is checked.

C. Status check: The SCI checks whether the RDRF flag is 0 and the received data c
transferred from the receive shift register (SCRSR) to SCRDR.

If all the above checks are passed, the RDRF flag is set to 1 and the received data is
SCRDR. If a receive error is detected, the SCI operates as shown in table 12.16.

Note: When a receive error occurs, subsequent reception cannot be continued. In a
the RDRF flag will not be set to 1 after reception; be sure to clear the error f

4. If the EIO bit in SCSPTR is cleared to 0 and the RIE bit in SCSCR is set to 1 when t
flag changes to 1, a receive-data-full interrupt (RXI) request is generated. If the RIE
SCSCR is set to 1 when the ORER, PER, or FER flag changes to 1, a receive error i
(ERI) request is generated.

Table 12.16 Receive Errors and Error Conditions

Receive Error	Abbreviation	Error Condition	Data Transfer
Overrun error	ORER	When the next data reception is completed while the RDRF flag in SCSSR is set to 1	The received data is transferred from SC SCRDR.
Framing error	FER	When the stop bit is 0	The received data is transferred from SC SCRDR.
Parity error	PER	When the received data does not match the even or odd parity specified in SCSMR	The received data is transferred from SC SCRDR.

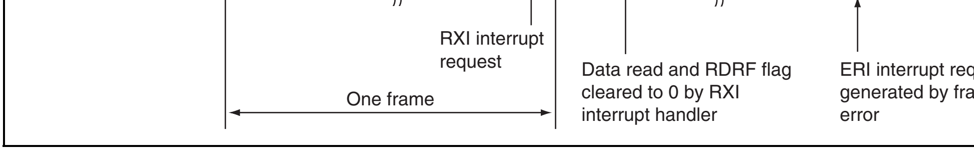


Figure 12.7 Example of SCI Receive Operation (8-Bit Data, Parity, One Stop Bit)

12.4.3 Clock Synchronous Mode (Channel 1 in the SH7124 is not Available)

In clock synchronous mode, the SCIF transmits and receives data in synchronization with pulses. This mode is suitable for high-speed serial communication.

The SCI transmitter and receiver are independent, so full-duplex communication is possib sharing the same clock. Both the transmitter and receiver have a double-buffered structur data can be read or written during transmission or reception, enabling continuous data tra

Figure 12.8 shows the general format in clock synchronous serial communication.

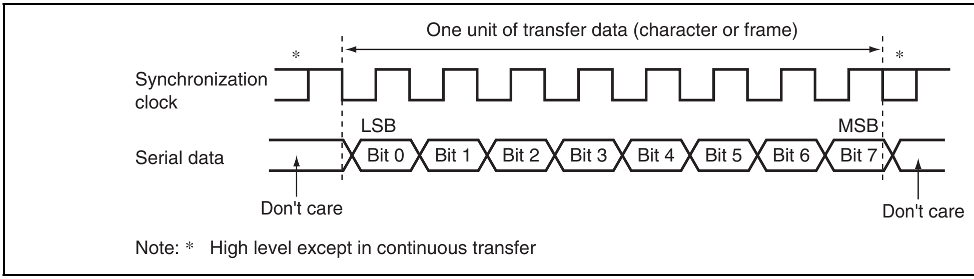


Figure 12.8 Data Format in Clock Synchronous Communication

(2) Clock

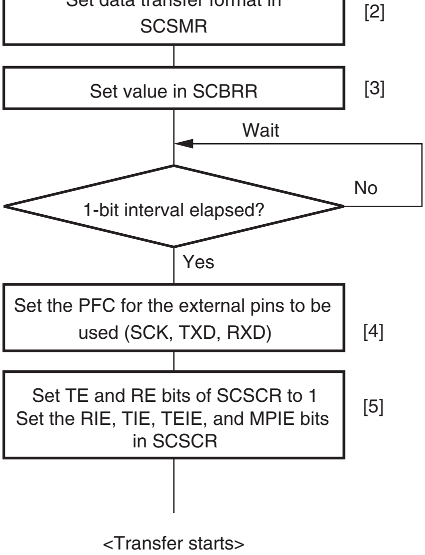
An internal clock generated by the on-chip baud rate generator or an external clock inpu SCK pin can be selected as the SCI transmit/receive clock. For selection of the SCI cloc see table 12.14.

When the SCI operates on an internal clock, it outputs the clock signal at the SCK pin. E pulses are output per transmitted or received character. When the SCI is not transmitting receiving, the clock signal remains in the high state. When only reception is performed, synchronous clock continues to be output until an overrun error occurs or the RE bit is c 0. For the reception of n characters, select the external clock as the clock source. If the i clock has to be used, set RE and TE to 1, then transmit n characters of dummy data at th time as receiving the n characters of data.

(3) Transmitting and Receiving Data

SCI Initialization (Clock Synchronous Mode):

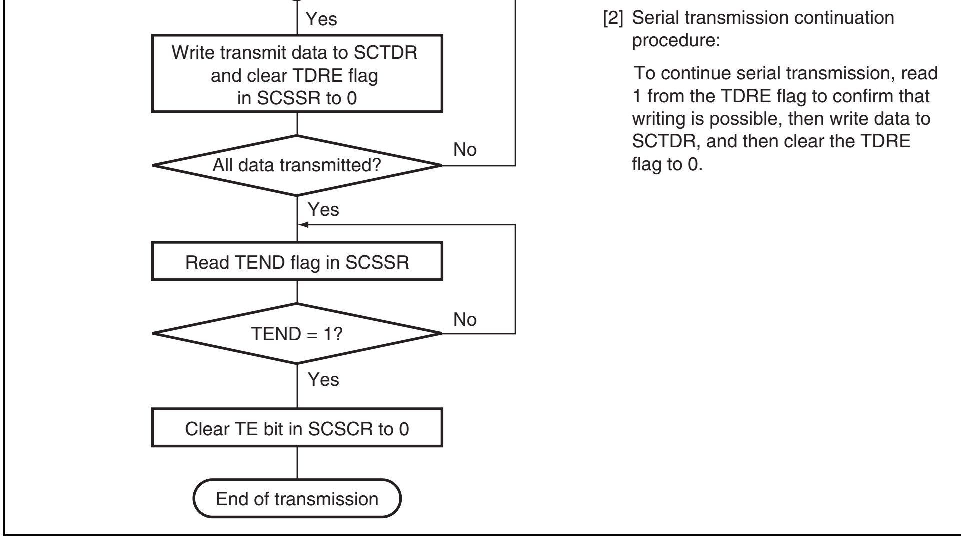
Before transmitting, receiving, or changing the mode or communication format, the soft clear the TE and RE bits to 0 in the serial control register (SCSCR), then initialize the S Clearing TE to 0 sets the TDRE flag to 1 and initializes the transmit shift register (SCTS Clearing RE to 0, however, does not initialize the RDRF, PER, FER, and ORER flags a data register (SCRDR), which retain their previous contents.


Set data transfer format in
SCSMR
[2]
Set value in SCBRR
[3]
Wait
1-bit interval elapsed?
No
Yes
Set the PFC for the external pins to be used (SCK, TXD, RXD)
[4]
Set TE and RE bits of SCSCR to 1
Set the RIE, TIE, TEIE, and MPIE bits in SCSCR
[5]
<Transfer starts>

[5] Set the TE bit or RE bit in SCR to 1.* Also make settings of the RIE, TIE, TEIE, and MPIE bits. At this time, the TXD, RXD, and SCK pins are ready to be used. The TXD pin is in a mark state during transmitting. When synchronous clock output (clock master) is set during receiving in clock synchronous mode, outputting clocks from the SCK pin starts.

Note: * In simultaneous transmit and receive operations, the TE and RE bits should both be cleared to 0 or set to 1 simultaneously.

Figure 12.9 Sample Flowchart for SCI Initialization


Yes
Write transmit data to SCTDR and clear TDRE flag in SCSSR to 0
All data transmitted?
No
Yes
Read TEND flag in SCSSR
TEND = 1?
No
Yes
Clear TE bit in SCSCR to 0
End of transmission

[2] Serial transmission continuation procedure:

To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to SCTDR, and then clear the TDRE flag to 0.

Figure 12.10 Sample Flowchart for Transmitting Serial Data

3. The SCI checks the TDRE flag at the timing for sending the MSB (bit 7). If the TDR
   0, the data is transferred from SCTDR to SCTSR and serial transmission of the next f
   started, If the TDRE flag is 1, the TEND flag in SCSSR is set to 1, the MSB (bit 7) is
   then the TXD pin holds the states.

   If the TEIE bit in SCSCR is set to 1 at this time, a TEI interrupt request is generated.
4. After the end of serial transmission, the SCK pin is held in the high state.

Figure 12.11 shows an example of SCI transmit operation.

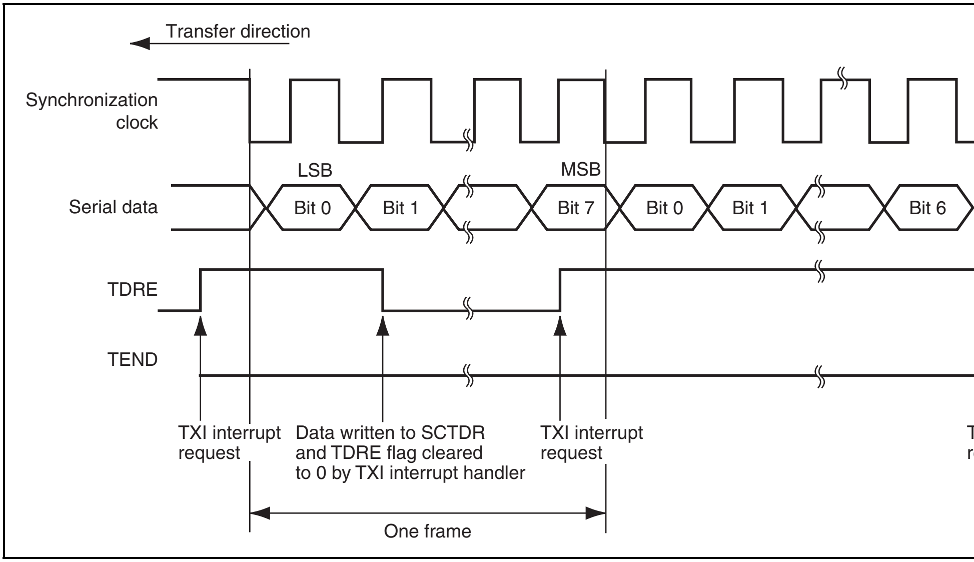
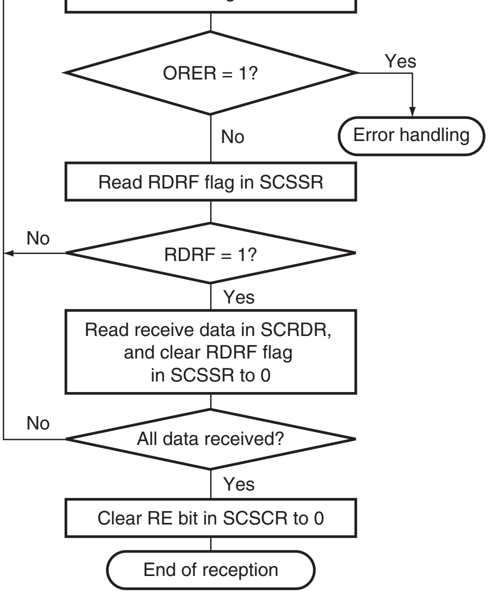


Figure 12.11 Example of SCI Transmit Operation



error handling, then clear the ORER fla to 0. Reception cannot be resumed wh the ORER flag is set to 1.

[2] SCI status check and receive data rea

Read SCSSR and check that RDRF = then read the receive data in SCRDR, and clear the RDRF flag to 0. The transition of the RDRF flag from 0 to 1 can also be identified by an RXI interru

[3] Serial reception continuation procedur

To continue serial reception, read the receive data register (SCRDR) and cle the RDRF flag to 0 before the MSB (bi of the current frame is received.

Figure 12.12 Sample Flowchart for Receiving Serial Data (1)

Figure 12.12 Sample Flowchart for Receiving Serial Data (2)

In receiving, the SCI operates as follows:

1. The SCI synchronizes with serial clock input or output and initializes internally.
2. Receive data is shifted into SCRSR in order from the LSB to the MSB. After receivin data, the SCI checks whether the RDRF flag is 0 and the receive data can be transferr SCRSR to SCRDR. If this check is passed, the SCI sets the RDRF flag to 1 and stores received data in SCRDR. If a receive error is detected, the SCI operates as shown in t 12.16. In this state, subsequent reception cannot be continued. In addition, the RDRF not be set to 1 after reception; be sure to clear the RDRF flag to 0.
3. After setting RDRF to 1, if the receive-data-full interrupt enable bit (RIE) is set to 1 i SCSCR, the SCI requests a receive-data-full interrupt (RXI). If the ORER bit is set to RIE bit in SCSCR is also set to 1, the SCI requests a receive error interrupt (ERI).

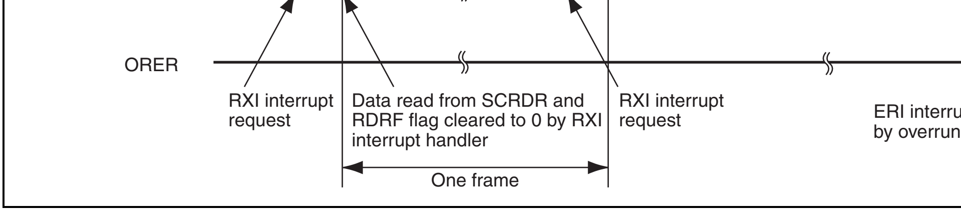
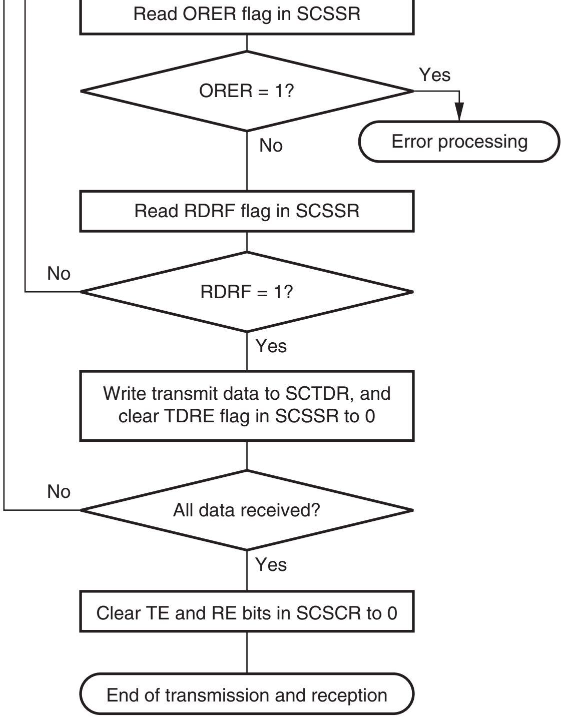


Figure 12.13 Example of SCI Receive Operation

Transmitting and Receiving Serial Data Simultaneously (Clock Synchronous Mode 12.14 shows a sample flowchart for transmitting and receiving serial data simultaneousl

Use the following procedure for serial data transmission and reception after enabling th transmission and reception.


Read ORER flag in SCSSR
ORER = 1?
Yes
Error processing
No
Read RDRF flag in SCSSR
No
RDRF = 1?
Yes
Write transmit data to SCTDR, and clear TDRE flag in SCSSR to 0
No
All data received?
Yes
Clear TE and RE bits in SCSCR to 0
End of transmission and reception

[3] SCI status check and receive data rea
Read SCSSR and check that the RDF
set to 1, then read the receive data in
and clear the RDRF flag to 0. Transiti
RDRF flag from 0 to 1 can also be ide
an RXI interrupt.

[4] Serial transmission/reception continua
procedure:
To continue serial transmission/recept
before the MSB (bit 7) of the current fr
received, finish reading the RDRF flag
SCRDR, and clearing the RDRF flag t
before the MSB (bit 7) of the current fr
transmitted, read 1 from the TDRE flag
confirm that writing is possible. Then
to SCTDR and clear the TDRE flag to

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first c
TE bit and RE bit to 0, then set both these bits to 1 simultaneously.

Figure 12.14 Sample Flowchart for Transmitting/Receiving Serial Data

multiprocessor bit is 0, the cycle is a data transmission cycle. Figure 12.15 shows an exa inter-processor communication using the multiprocessor format. The transmitting statio sends the ID code of the receiving station with which it wants to perform serial commun data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multi bit added. The receiving station skips data until data with a 1 multiprocessor bit is sent. with a 1 multiprocessor bit is received, the receiving station compares that data with its The station whose ID matches then receives the data sent next. Stations whose ID does continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI uses the MPIE bit in SCSCR to implement this function. When the MPIE bit is transfer of receive data from SCRSR to SCRDR, error flag detection, and setting the SC flags, RDRF, FER, and OER to 1 are inhibited until data with a 1 multiprocessor bit is r On reception of receive character with a 1 multiprocessor bit, the MPB bit in SCSSR is and the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE SCSCR is set to 1 at this time, an RXI interrupt is generated.

When the multiprocessor format is selected, the parity bit setting is invalid. All other bit are the same as those in normal asynchronous mode. The clock used for multiprocessor communication is the same as that in normal asynchronous mode.

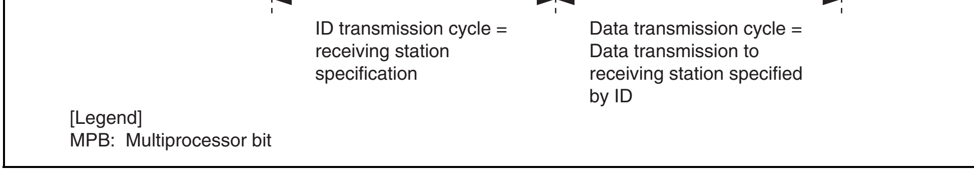
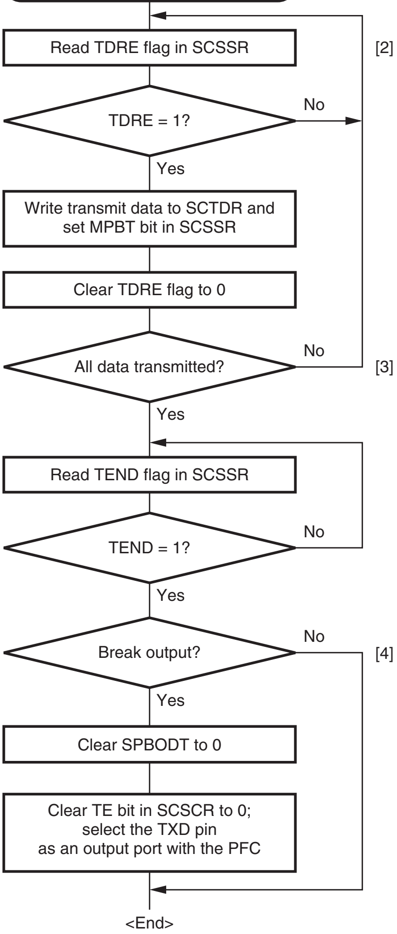


Figure 12.15   Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

for one frame, and transmission is enabled. However, data is not transmitted.



[2] SCI status check and transmit data write:
Read SCSSR and check that the TDRE flag is set to 1, then write transmit data to SCTDR. Set the MPBT bit in SCSSR to 0 or 1. Finally, clear the TDRE flag to 0.

After initializing the SCI, when an ID is written to SCTDR register so as to transmit the ID, data is immediately transferred, and then the TDER flag is set to 1. The MPBT bit must be held 1 because the ID is not transmitted from the TXD pin at this time. When the TDRE flag is set to 1 after data following the ID is written to SCTDR, clear the MPBT bit to 0.

[3] Serial transmission continuation procedure:

To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to SCTDR, and then clear the TDRE flag to 0.

[4] Break output at the end of serial transmission:
To output a break during serial transmission, first clear the SPBODT bit in the serial port register (SCSPTR) to 0, then clear the TE bit in SCSCR to 0 and use the PFC to select the TXD pin as an output port.

Figure 12.16 Sample Multiprocessor Serial Transmission Flowchart

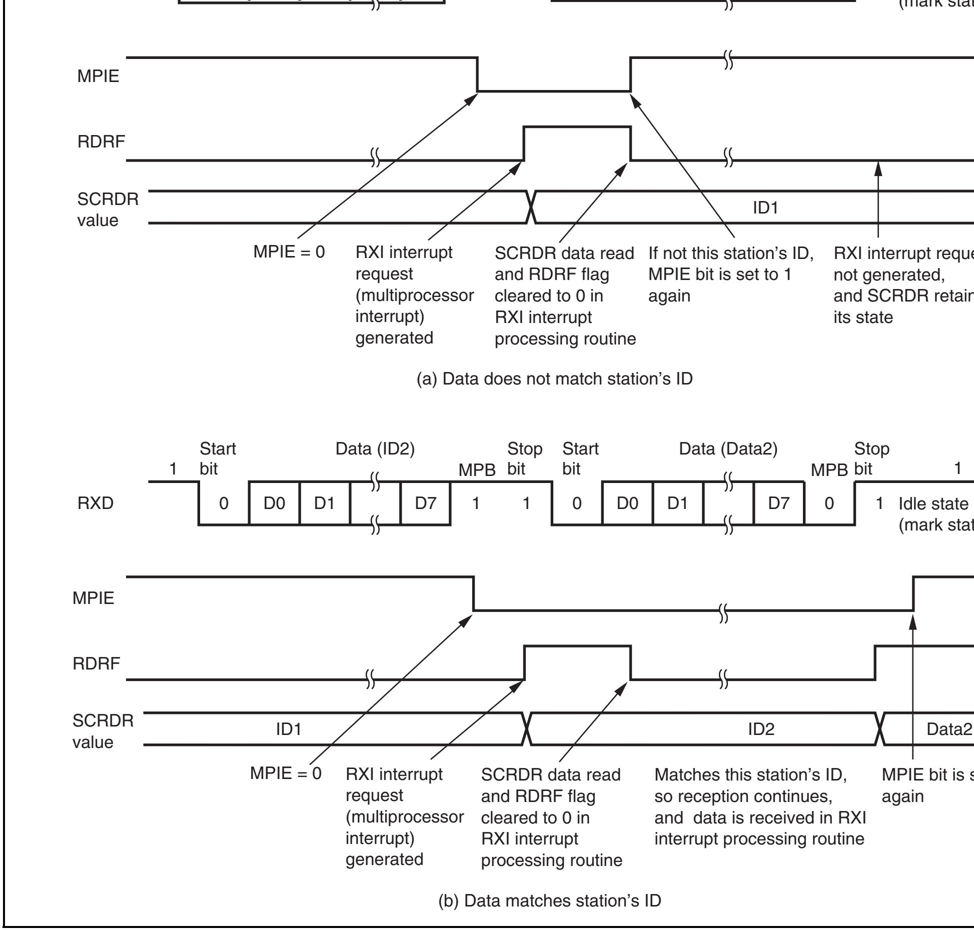
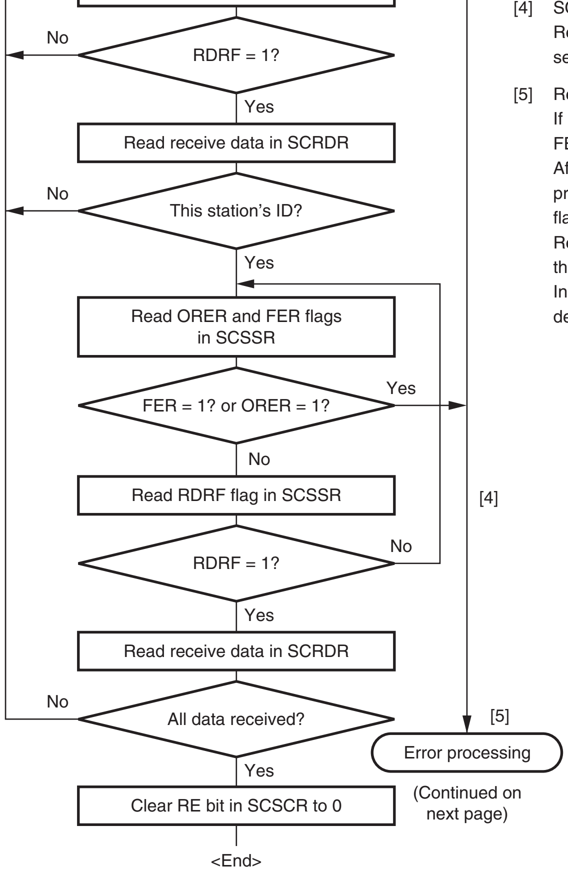

(mark sta
MPIE
RDRF
SCRDR
value
ID1
MPIE = 0
RXI interrupt request (multiprocessor interrupt) generated
SCRDR data read and RDRF flag cleared to 0 in RXI interrupt processing routine
If not this station's ID, MPIE bit is set to 1 again
RXI interrupt reque not generated, and SCRDR retair its state
(a) Data does not match station's ID
Start bit
Data (ID2)
MPB
Stop bit
Start bit
Data (Data2)
MPB
Stop bit
1
RXD
0
D0
D1
D7
1
1
0
D0
D1
D7
0
1
Idle state (mark stat
MPIE
RDRF
SCRDR
value
ID1
ID2
Data2
MPIE = 0
RXI interrupt request (multiprocessor interrupt) generated
SCRDR data read and RDRF flag cleared to 0 in RXI interrupt processing routine
Matches this station's ID, so reception continues, and data is received in RXI interrupt processing routine
MPIE bit is s again
(b) Data matches station's ID

Figure 12.17 Example of SCI Operation in Reception (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)



[4] SCI status check and data reception:
Read SCSSR and check that the RDRF fl
set to 1, then read the data in SCRDR.

[5] Receive error processing and break detec
If a receive error occurs, read the ORER a
FER flags in SCSSR to identify the error.
After performing the appropriate error
processing, ensure that the ORER and FE
flags are all cleared to 0.
Reception cannot be resumed if either of
these flags is set to 1.
In the case of a framing error, a break car
detected by reading the RXD pin value.

Figure 12.18 Sample Multiprocessor Serial Reception Flowchart (1)

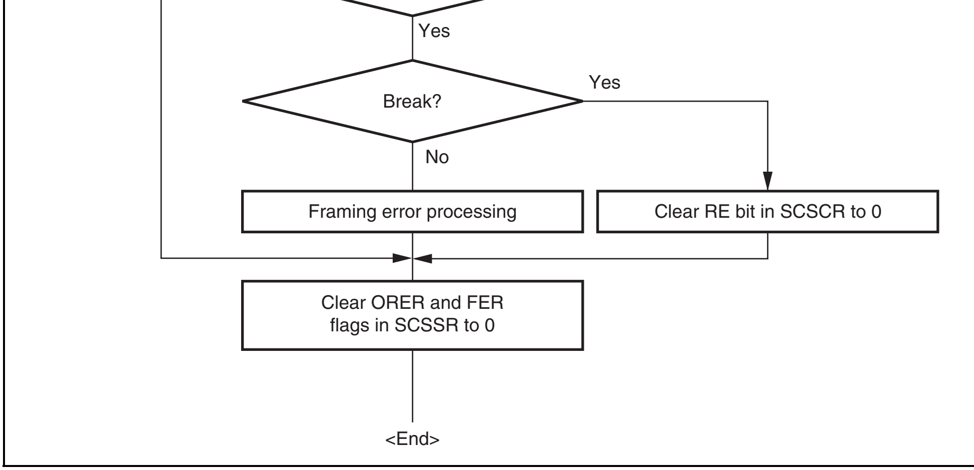

Yes
Break?
Yes
No
Framing error processing
Clear RE bit in SCSCR to 0
Clear ORER and FER flags in SCSSR to 0
<End>

Figure 12.18 Sample Multiprocessor Serial Reception Flowchart (2)

generated. When the ORER, FER, or PER flag in SCSSR is set to 1, an ERI interrupt re generated. When the TEND flag in SCSSR is set to 1, a TEI interrupt request is generate

The TXI interrupt indicates that transmit data can be written, and the TEI interrupt indic transmission has been completed.

Table 12.17 SCI Interrupt Sources

Interrupt Source	Description
ERI	Interrupt caused by receive error (ORER, FER, or PER)
RXI	Interrupt caused by receive data full (RDRF)
TXI	Interrupt caused by transmit data empty (TDRE)
TEI	Interrupt caused by transmit end (TENT)

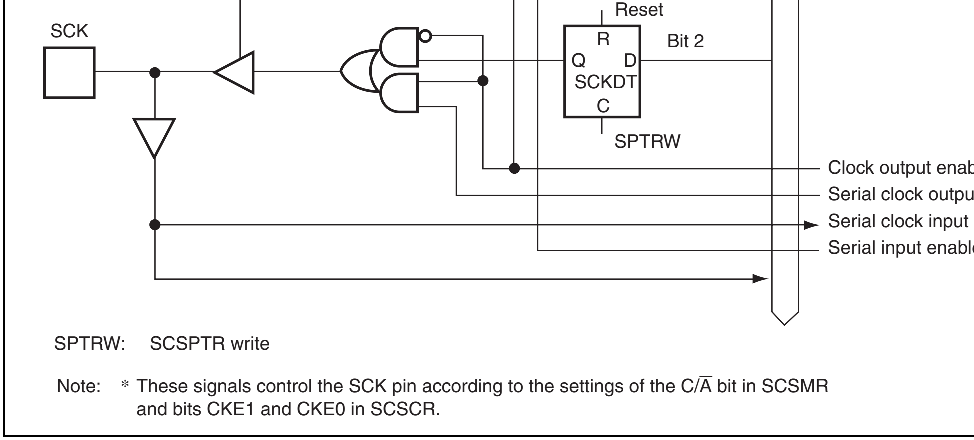

SCK
Reset
R
Q
D
SCKDT
C
Bit 2
SPTRW
Clock output enab
Serial clock outpu
Serial clock input
Serial input enabl
SPTRW: SCSPTR write
Note: * These signals control the SCK pin according to the settings of the C/A bit in SCSMR and bits CKE1 and CKE0 in SCSCR.

Figure 12.19 SPB1IO bit, SPB1DT bit, and SCK Pin

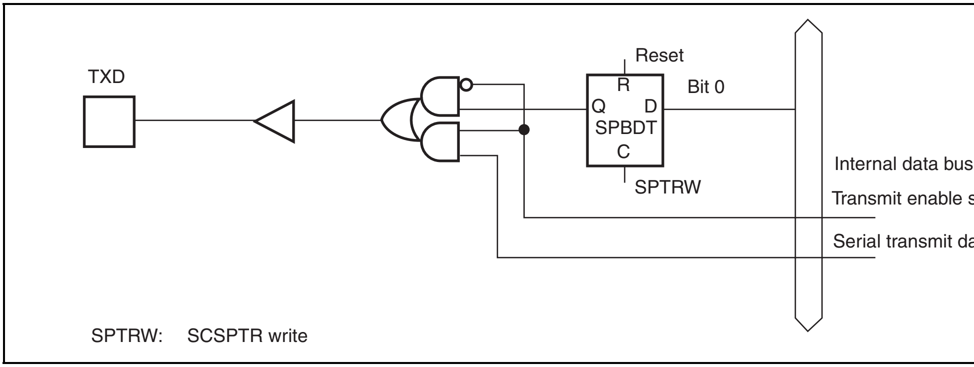


Figure 12.20 SPB0DT bit and TXD Pin

If new data is written in SCTDR when TDRE is 0, however, the old data stored in SCT lost because the data has not yet been transferred to SCTSR. Before writing transmit dat SCTDR, be sure to check that the TDRE flag is set to 1.

12.7.2 Multiple Receive Error Occurrence

If multiple receive errors occur at the same time, the status flags in SCSSR are set as sho table 12.18. When an overrun error occurs, data is not transferred from the receive shift (SCRSR) to the receive data register (SCRDR) and the received data will be lost.

Table 12.18 SCSSR Status Flag Values and Transfer of Received Data

	SCSSR Status Flags				Recei Trans SCRS
Receive Errors Generated	**RDRF**	**ORER**	**FER**	**PER**	**SCRD**
Overrun error	1	1	0	0	Not tra
Framing error	0	0	1	0	Transf
Parity error	0	0	0	1	Transf
Overrun error + framing error	1	1	1	0	Not tra
Overrun error + parity error	1	1	0	1	Not tra
Framing error + parity error	0	0	1	1	Transf
Overrun error + framing error + parity error	1	1	1	1	Not tra

register (SCSPTR). This feature can be used to send a break signal.

Until TE bit is set to 1 (enabling transmission) after initializing, TXD pin does not work. the period, mark status is performed by SPB0DT bit. Therefore, the SPB0DT bit should b at first (high level output).

To send a break signal during serial transmission, clear the SPB0DT bit to 0 (low level), t the TE bit to 0 (halting transmission). When the TE bit is cleared to 0, the transmitter is in regardless of the current transmission state, and 0 is output from the TXD pin.

12.7.5 Receive Data Sampling Timing and Receive Margin (Asynchronous Mode)

The SCI operates on a base clock with a frequency of 16 times the transfer rate in asynch mode. In reception, the SCI synchronizes internally with the fall of the start bit, which it s on the base clock. Receive data is latched at the rising edge of the eighth base clock pulse timing is shown in figure 12.21.

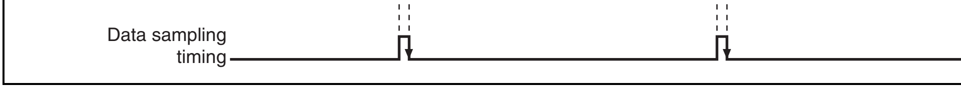


Figure 12.21 Receive Data Sampling Timing in Asynchronous Mode

The receive margin in asynchronous mode can therefore be expressed as shown in ec

Equation 1:

$$M = \left| \left(0.5 - \frac{1}{2N}\right) - (L - 0.5)\,F - \frac{|D - 0.5|}{N}(1+F) \right| \times 100\ \%$$

Where: M: Receive margin (%)
N: Ratio of bit rate to clock (N = 16)
D: Clock duty (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute deviation of clock frequency

From equation 1, if F = 0 and D = 0.5, the receive margin is 46.875%, as given by ec

Equation 2:

When D = 0.5 and F = 0:

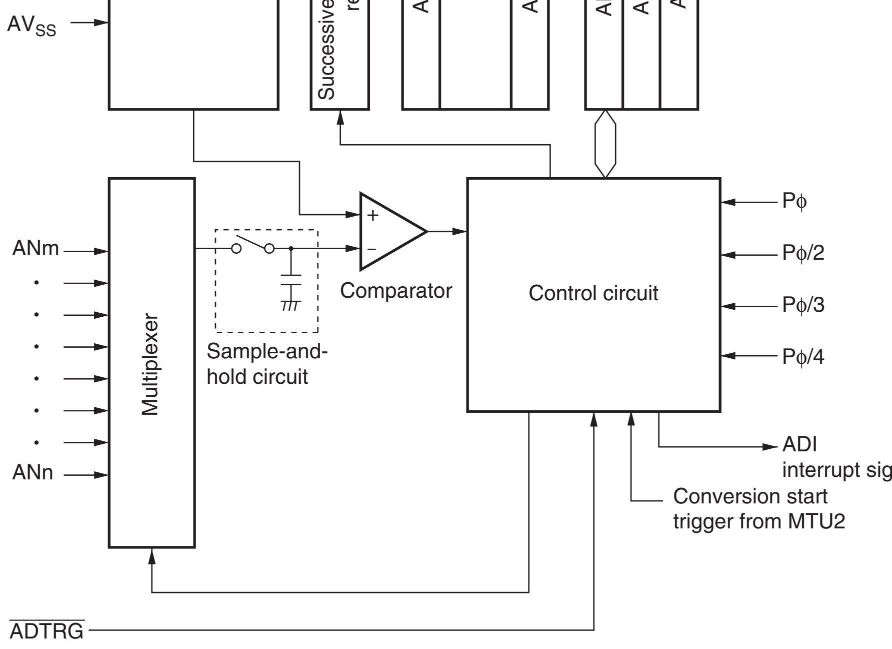
$$M = (0.5 - 1/(2 \times 16)) \times 100\%$$
$$= 46.875\%$$

This is a theoretical value. A reasonable margin to allow in system designs is 20% to

for SCI operation to be halted. Register access is enabled by clearing module standby mo
details, see section 19, Power-Down Modes.

- Three operating modes
  - Single mode: Single-channel A/D conversion
  - Continuous scan mode: Repetitive A/D conversion on up to four channels
  - Single-cycle scan mode: Continuous A/D conversion on up to four channels
- Data registers
  - Conversion results are held in a 16-bit data register for each channel
- Sample-and-hold function
- Three methods for conversion start
  - Software
  - Conversion start trigger from multifunction timer pulse unit 2 (MTU2)
  - External trigger signal
- Interrupt request
  - An A/D conversion end interrupt request (ADI) can be generated
- Module standby mode can be set

ADCMS20C_000020020700



[Legend]

ADCR:	A/D control register
ADCSR:	A/D control/status register
ADTSR:	A/D trigger select register
ADDRm to ADDRn:	A/D data registers m to n

Note: The register number corresponds to the channel number of the module. (m to n = 0 to 7)

Figure 13.1 Block Diagram of A/D Converter (for One Module)

	$\overline{\text{ADTRG}}$	Input	A/D external trigger input pin*
A/D module 0 (A/D_0)	AN0	Input	Analog input pin 0
	AN1	Input	Analog input pin 1
	AN2	Input	Analog input pin 2
	AN3	Input	Analog input pin 3
A/D module 1 (A/D_1)	AN4	Input	Analog input pin 4
	AN5	Input	Analog input pin 5
	AN6	Input	Analog input pin 6
	AN7	Input	Analog input pin 7

Notes: The connected A/D module differs for each pin. The control registers of each moc be set.

* This pin is supported only by the SH7125.

A/D data register 2	ADDR2	R	H'0000	H'FFFFC904	16
A/D data register 3	ADDR3	R	H'0000	H'FFFFC906	16
A/D control/status register_0	ADCSR_0	R/W	H'0000	H'FFFFC910	16
A/D control register_0	ADCR_0	R/W	H'0000	H'FFFFC912	16
A/D data register 4	ADDR4	R	H'0000	H'FFFFC980	16
A/D data register 5	ADDR5	R	H'0000	H'FFFFC982	16
A/D data register 6	ADDR6	R	H'0000	H'FFFFC984	16
A/D data register 7	ADDR7	R	H'0000	H'FFFFC986	16
A/D control/status register_1	ADCSR_1	R/W	H'0000	H'FFFFC990	16
A/D control register_1	ADCR_1	R/W	H'0000	H'FFFFC992	16
A/D trigger select register_0	ADTSR_0	R/W	H'0000	H'FFFFE890	8, 1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
											-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

13.3.2 A/D Control/Status Registers_0 and _1 (ADCSR_0 and ADCSR_1)

ADCSR for each module controls A/D conversion operations.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	ADF	ADIE	-	-	TRGE	-	CONADF	STC	CKSL[1:0]		ADM[1:0]		ADCS	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial Value	R/W	Description
15	ADF	0	R/(W)*	A/D End Flag A status flag that indicates the end of A/D co [Setting conditions] • When A/D conversion ends in single mo • When A/D conversion ends on all specifi channels in scan mode [Clearing condition] • When 0 is written after reading ADF = 1

11	TRGE	0	R/W	Trigger Enable Enables or disables triggering of A/D convers ADTRG and an MTU2 trigger. 0: A/D conversion triggering is disabled 1: A/D conversion triggering is enabled When changing the operating mode, first clea ADST bit to 0.
10	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
9	CONADF	0	R/W	ADF Control Controls setting of the ADF bit in 2-channel sc mode. The setting of this bit is valid only whe triggering of A/D conversion is enabled (TRG 2-channel scan mode. The setting of this bit i in single mode or 4-channel scan mode. 0: The ADF bit is set when A/D conversion st the group 0 trigger or group 1 trigger has fi 1: The ADF bit is set when A/D conversion st the group 0 trigger and A/D conversion sta the group 1 trigger have both finished. Not triggering order has no affect. When changing the operating mode, first clea ADST bit to 0.

				Select the A/D conversion time. 00: Pϕ/4 01: Pϕ/3 10: Pϕ/2 11: Pϕ When changing the A/D conversion time, firs ADST bit to 0. CKSL[1:0] = B'11 can be set while Pϕ ≤ 25 M
5, 4	ADM[1:0]	00	R/W	A/D Mode 1 and 0 Select the A/D conversion mode. 00: Single mode 01: 4-channel scan mode 10: Setting prohibited 11: 2-channel scan mode When changing the operating mode, first cle ADST bit to 0.
3	ADCS	0	R/W	A/D Continuous Scan Selects either single-cycle scan or continuou scan mode. This bit is valid only when scan selected. 0: Single-cycle scan 1: Continuous scan When changing the operating mode, first cle ADST bit to 0.

ADCR for each module controls A/D conversion.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	ADST	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
13	ADST	0	R/W	A/D Start Starts or stops A/D conversion. When this bit 1, A/D conversion is started. When this bit is to 0, A/D conversion is stopped and the A/D enters the idle state. In single or single-cycle mode, this bit is automatically cleared to 0 wh conversion ends on the selected single chann continuous scan mode, A/D conversion is cor performed for the selected channels in seque this bit is cleared by a software, reset, or in s standby mode or module standby mode.
12 to 0	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.

		1
	1	0
		1

			Analog Input Channels	
Bit 2	Bit 1	Bit 0	2-Channel Scan Mode* (Activated by software)	
CH2	CH1	CH0	A/D_0	A/D_1
0	0	0	AN0	AN4
		1	AN0, AN1	AN4, AN5
	1	0	AN2	AN6
		1	AN2, AN3	AN6, AN7
1	0	0	Setting prohibited	Setting prohibited
		1		
	1	0		
		1		

	1
1	0
	1

Note: * Continuous scan mode or single-scan mode can be selected with the ADCS bi

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	TRG11S[3:0]	0000	R/W	A/D Trigger 1 Group 1 Select 3 to 0 Select an external trigger or MTU2 trigger to s conversion for group 1 when A/D module 1 is channel scan mode. 0000: External trigger pin ($\overline{\text{ADTRG}}$) input 0001: TRGA input capture/compare match fo MTU2 channel or TCNT_4 underflow (t complementary PWM mode (TRGAN) 0010: MTU2 channel 0 compare match (TRG 0011: MTU2 A/D conversion start request del (TRG4AN) 0100: MTU2 A/D conversion start request del (TRG4BN) 0101: Setting prohibited 0110: Setting prohibited 0111: Setting prohibited 1xxx: Setting prohibited When switching the selector, first clear the AD the A/D control register (ADCR) to 0. Specify different trigger sources for the group group 1 conversion requests so that a group (conversion request is not generated simultane with a group 1 conversion request in 2-chann mode.

0011: MTU2 A/D conversion start request dela
(TRG4AN)

0100: MTU2 A/D conversion start request dela
(TRG4BN)

0101: Setting prohibited

0110: Setting prohibited

0111: Setting prohibited

1xxx: Setting prohibited

When switching the selector, first clear the ADS
the A/D control register (ADCR) to 0.

Specify different trigger sources for the group 0
group 1 conversion requests so that a group 0
conversion request is not generated simultaneo
with a group 1 conversion request in 2-channe
mode.

0011: MTU2 A/D conversion start request del
(TRG4AN)

0100: MTU2 A/D conversion start request del
(TRG4BN)

0101: Setting prohibited

0110: Setting prohibited

0111: Setting prohibited

1xxx: Setting prohibited

When switching the selector, first clear the AD
the A/D control register (ADCR) to 0.

Specify different trigger sources for the group
group 1 conversion requests so that a group 0
conversion request is not generated simultane
with a group 1 conversion request in 2-chann
mode.

0011: MTU2 A/D conversion start request dela
(TRG4AN)

0100: MTU2 A/D conversion start request dela
(TRG4BN)

0101: Setting prohibited

0110: Setting prohibited

0111: Setting prohibited

1xxx: Setting prohibited

When switching the selector, first clear the ADS
the A/D control register (ADCR) to 0.

Specify different trigger sources for the group 0
group 1 conversion requests so that a group 0
conversion request is not generated simultaneo
with a group 1 conversion request in 2-channe
mode.

[Legend]

x: Don't care

operations are as follows:

1. A/D conversion is started when the ADST bit in ADCR is set to 1, according to soft MTU2, or external trigger input.
2. When A/D conversion is completed, the result is transferred to the A/D data register corresponding to the channel.
3. On completion of conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is s this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D converion ends, t bit is automatically cleared to 0 and the A/D converter enters the idle state.
   When the ADST bit is cleared to 0 during A/D conversion, A/D conversion stops an converter enters the idle state.

13.4.2 Continuous Scan Mode

In continuous scan mode, A/D conversion is to be performed sequentially on the specifi channels.

1. When the ADST bit in ADCR is set to 1 by software, MTU2, or external trigger inpu conversion starts on the channel with the lowest number in the group (AN0, AN1, ...
2. When A/D conversion for each channel is completed, the result is sequentially trans the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF bit in ADCSR i If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conve Conversion of the first channel in the group starts again.
4. Steps 2 to 3 are repeated as long as the ADST bit remains set to 1. When the ADST cleared to 0, A/D conversion stops and the A/D converter enters the idle state.

4. After A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D co enters the idle state. When the ADST bit is cleared to 0 during A/D conversion, A/D conversion stops and the A/D converter enters the idle state.

13.4.4 Input Sampling and A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit for each module. The A/D conv samples the analog input when the A/D conversion start delay time (t_D) has passed after th bit in ADCR is set to 1, then starts conversion. Figure 13.2 shows the A/D conversion tim Table 13.4 shows the A/D conversion time.

As indicated in figure 13.2, the A/D conversion time (t_{CONV}) includes t_D and the input samp (t_{SPL}). The length of t_D varies depending on the timing of the write access to ADCR. The to conversion time therefore varies within the ranges indicated in table 13.4.

In scan mode, the values given in table 13.4 apply to the first conversion time. The values table 13.5 apply to the second and subsequent conversions.

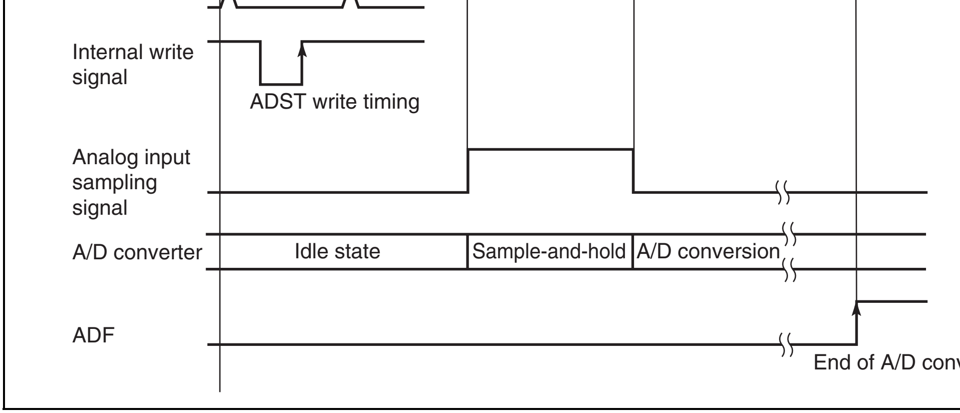


Figure 13.2 A/D Conversion Timing

time

		STC = 1										
		CKSL1 = 0						CKSL1 = 1				
		CKSL0 = 0			CKSL0 = 1			CKSL0 = 0			CKS	
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**T**
A/D conversion start delay time	t_D	2	—	6	2	—	5	2	—	4	2	—
Input sampling time	t_{SPL}	—	36	—	—	27	—	—	18	—	—	9
A/D conversion time	t_{CONV}	258	—	262	194	—	197	130	—	132	66	—

Note: All values represent the number of states for Pϕ.

Table 13.5 A/D Conversion Time (Scan Mode)

				Conversion Time Calculation Ex	
STC	**CKSL1**	**CKSL0**	**Conversion Time (State)**	**Pϕ = 25 MHz**	**Pϕ = 40 MHz**
0	0	0	200 (Fixed)	8 µs	5 µs
		1	150 (Fixed)	6 µs	3.8 µs
	1	0	100 (Fixed)	4 µs	2.5 µs
		1	50 (Fixed)	2 µs	Setting prohi
1	0	0	256 (Fixed)	10.2 µs	6.4 µs
		1	192 (Fixed)	7.7 µs	4.8 µs
	1	0	128 (Fixed)	5.1 µs	3.2 µs
		1	64 (Fixed)	2.6 µs	Setting prohi

13.4.6 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGE bit in the A/D control/statu (ADCSR) is set to 1 while the TRGS3 to TRGS0 bits in the A/D trigger select register_0 (ADTSR_0) is set to external trigger input, external trigger input is enabled at the $\overline{\text{ADTR}}$ falling edge of the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCR, starting A/D conversio operations, in both single and scan modes, are the same as when the ADST bit has been software. Figure 13.3 shows the timing.

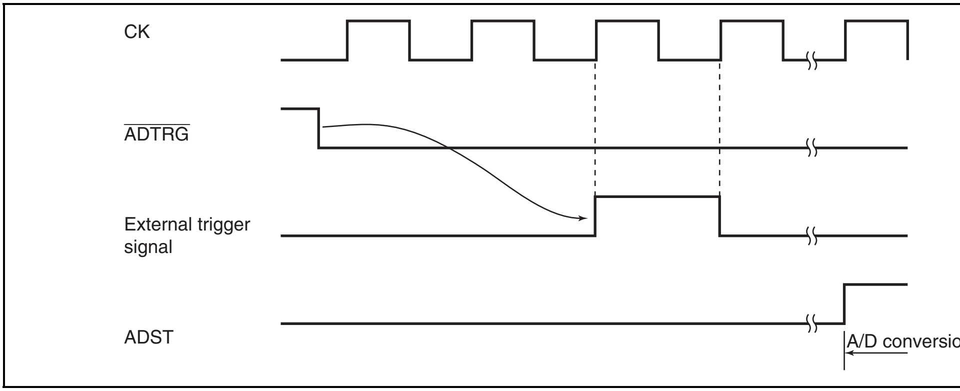


Figure 13.3 External Trigger Input Timing

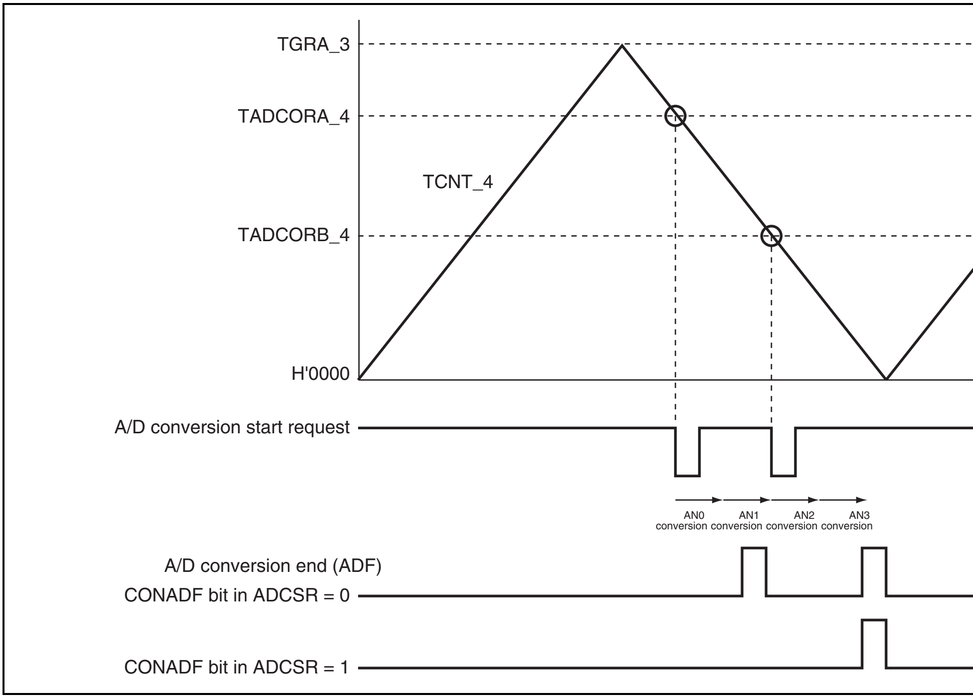


Figure 13.4 Example of 2-Channel Scanning

when the digital output changes from the minimum voltage value B'0000000000 (H'0
B'0000000001 (H'001) (see figure 13.6).

- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion charac when the digital output changes from B'1111111110 (H'3FE) to B'1111111111 (H'3F figure 13.6).

- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristic between zero voltage full-scale voltage. Does not include offset error, full-scale error, or quantization error figure 13.6).

- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset err scale error, quantization error, and nonlinearity error.

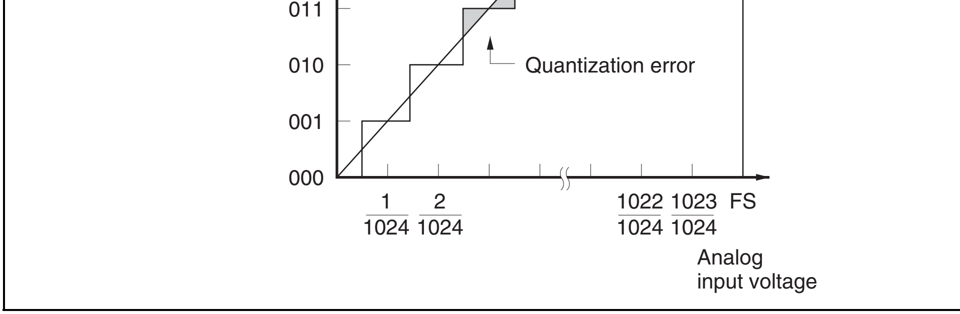


Figure 13.5 Definitions of A/D Conversion Accuracy

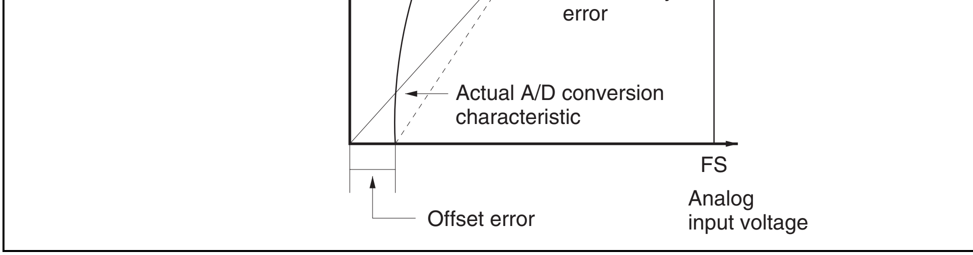


Figure 13.6 Definitions of A/D Conversion Accuracy

This LSI's analog input is designed such that conversion accuracy is guaranteed for an i
for which the signal source impedance is 1 kΩ or less. This specification is provided to
A/D converter's sample-and-hold circuit input capacitance to be charged within the sam
if the sensor output impedance exceeds 1 kΩ, charging may be insufficient and it may n
possible to guarantee A/D conversion accuracy. However, for A/D conversion in single
a large capacitance provided externally, the input load will essentially comprise only th
input resistance of 10 kΩ, and the signal source impedance is ignored. However, as a lo
filter effect is obtained in this case, it may not be possible to follow an analog signal wi
differential coefficient (e.g., 5 mV/μs or greater) (see figure 13.7). When converting a h
analog signal or converting in scan mode, a low-impedance buffer should be inserted.

13.7.3 Influences on Absolute Accuracy

Adding capacitance results in coupling with GND, and therefore noise in GND may adv
affect absolute precision. Be sure to make the connection to an electrically stable GND
AVss.

Care is also required to insure that filter circuits do not interfere in the accuracy by the p
circuit digital signals on the mounting board (i.e, acting as antennas).

13.7.4 Range of Analog Power Supply and Other Pin Settings

If the conditions below are not met, the reliability of the device may be adversely affecte

- Analog input voltage range

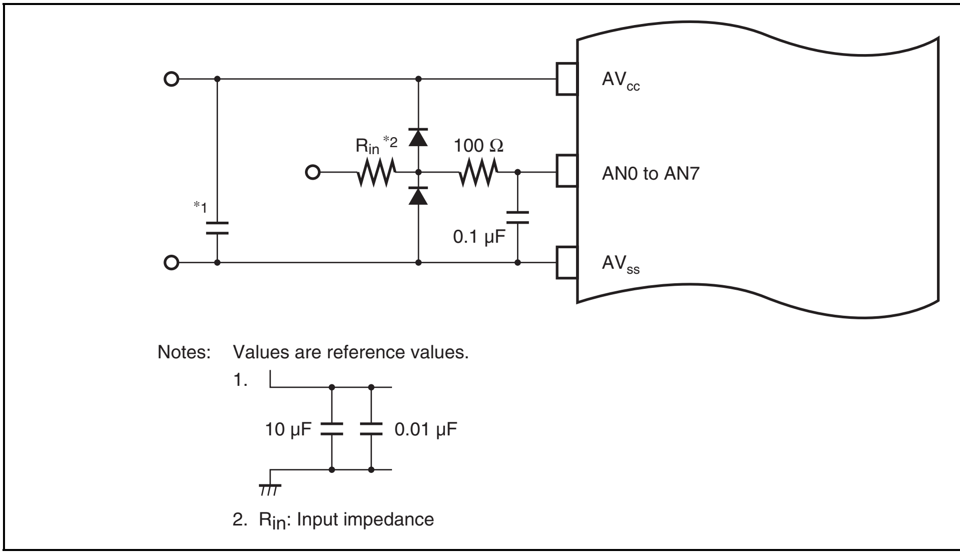
  The voltage applied to analog input pin ANn during A/D conversion should be in the AVss ≤ VAN ≤ AVref.
- Relationship between AVcc, AVss and Vcc, Vss

  Set Vcc ≤ AVcc ≤ 5.5V, AVss = Vss for the relationship between AVcc, AVss and V If the A/D converter is not used, the AVcc and AVss pins must not be left open.

13.7.5 Notes on Board Design

In board design, digital circuitry and analog circuitry should be as mutually isolated as po and layout in which digital circuit signal lines and analog circuit signal lines cross or are proximity should be avoided as far as possible. Failure to do so may result in incorrect op of the analog circuitry due to inductance, adversely affecting A/D conversion values. Als circuitry must be isolated from the analog input signals (AN0 to AN7), and analog power (AVcc) by the analog ground (AVss). Also, the analog ground (AVss) should be connect point to a stable ground (Vss) on the board.

the analog input pin voltage. Careful consideration is therefore required when deciding c
constants.



Notes: Values are reference values.

1\.

2. R_{in}: Input impedance

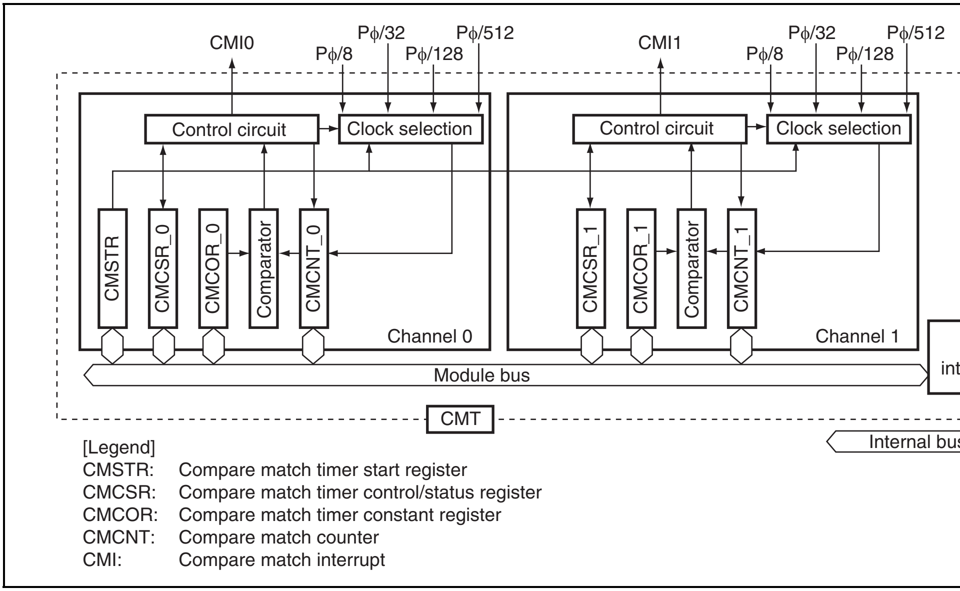
Figure 13.8 Example of Analog Input Protection Circuit

Table 13.7 Analog Pin Specifications

Item	Min.	Max.	Unit	Condition
Analog input capacitance	—	20	pF	—
Permissible signal source impedance	—	3	kΩ	Conversion tim
	—	1	kΩ	Conversion tim

- Interrupt request on compare match
- Module standby mode can be set.

Figure 14.1 shows a block diagram of CMT.



[Legend]
CMSTR: Compare match timer start register
CMCSR: Compare match timer control/status register
CMCOR: Compare match timer constant register
CMCNT: Compare match counter
CMI: Compare match interrupt

Figure 14.1 Block Diagram of CMT

register					
Compare match timer control/status register_0	CMCSR_0	R/W	H'0000	H'FFFFCE02	8, 1
Compare match counter_0	CMCNT_0	R/W	H'0000	H'FFFFCE04	8, 1
Compare match constant register_0	CMCOR_0	R/W	H'FFFF	H'FFFFCE06	8, 1
Compare match timer control/status register_1	CMCSR_1	R/W	H'0000	H'FFFFCE08	8, 1
Compare match counter_1	CMCNT_1	R/W	H'0000	H'FFFFCE0A	8, 1
Compare match constant register_1	CMCOR_1	R/W	H'FFFF	H'FFFFCE0C	8, 1

Bit	Bit Name	value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
1	STR1	0	R/W	Count Start 1 Specifies whether compare match counter 1 c or is stopped. 0: CMCNT_1 count is stopped 1: CMCNT_1 count is started
0	STR0	0	R/W	Count Start 0 Specifies whether compare match counter 0 c or is stopped. 0: CMCNT_0 count is stopped 1: CMCNT_0 count is started

14.2.2 Compare Match Timer Control/Status Register (CMCSR)

CMCSR is a 16-bit register that indicates compare match generation, enables interrupts
the counter input clock.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	CMF	CMIE	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	(R/W)*1	R/W	R	R	R	R

Note: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

				• When 0 is written to this bit after reading C [Setting condition] 1: CMCNT and CMCOR values match
6	CMIE	0	R/W	Compare Match Interrupt Enable Enables or disables compare match interrupt (C generation when CMCNT and CMCOR values (CMF=1). 0: Compare match interrupt (CMI) disabled 1: Compare match interrupt (CMI) enabled
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
1, 0	CKS[1:0]	00	R/W	Clock Select 1 and 0 Select the clock to be input to CMCNT from fou clocks obtained by dividing the peripheral oper clock (Pϕ). When the STR bit in CMSTR is set CMCNT starts counting on the clock selected w CKS1 and CKS0. 00: Pϕ/8 01: Pϕ/32 10: Pϕ/128 11: Pϕ/512

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed w

2. If another flag setting condition occurs before writing 0 to the bit after reading i flag will not be cleared by simply writing 0 to it. In this case, read the bit as 1 o and write 0 to it.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.2.4 Compare Match Constant Register (CMCOR)

CMCOR is a 16-bit register that sets the interval up to a compare match with CMCNT.

The initial value of CMCOR is H'FFFF.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 14.2 shows the operation of the compare match counter.

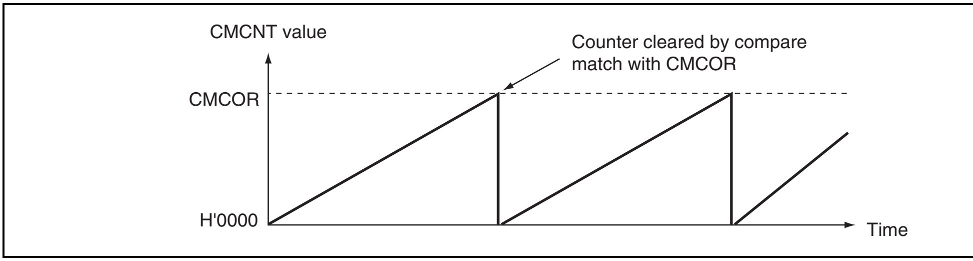


Figure 14.2 Counter Operation

14.3.2 CMCNT Count Timing

One of four internal clocks (Pϕ/8, Pϕ/32, Pϕ/128, and Pϕ/512) obtained by dividing the Pϕ can be selected with bits CKS1 and CKS0 in CMCSR. Figure 14.3 shows the timing.

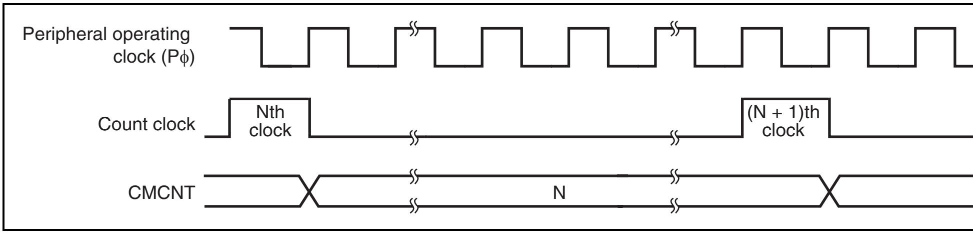


Figure 14.3 Count Timing

14.4.2 Timing of Setting Compare Match Flag

When CMCOR and CMCNT match, a compare match signal is generated and the CMF
CMCSR is set to 1. The compare match signal is generated in the last cycle in which the
match (when the CMCNT value is updated to H'0000). That is, after a match between C
and CMCNT, the compare match signal is not generated until the next CMCNT counter
input. Figure 14.4 shows the timing of CMF bit setting.

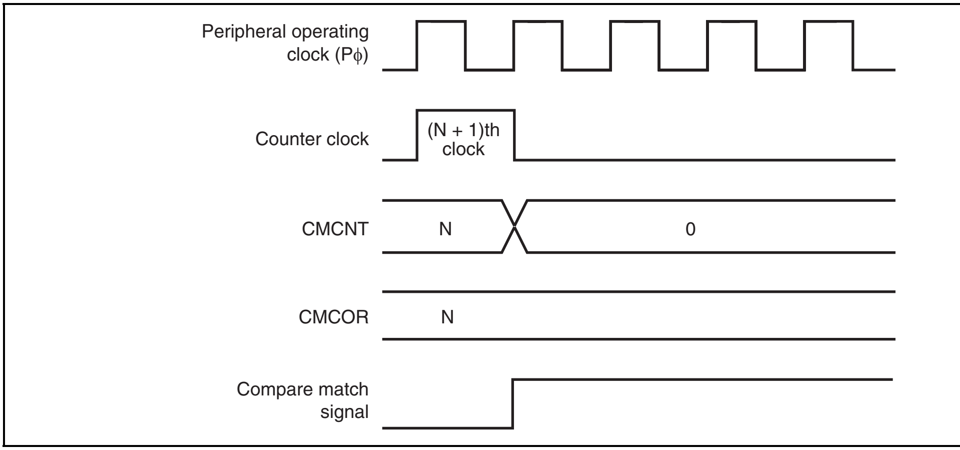


Figure 14.4 Timing of CMF Setting

14.4.3 Timing of Clearing Compare Match Flag

The CMF bit in CMCSR is cleared by reading 1 from this bit, then writing 0.

When the compare match signal is generated in the T2 cycle while writing to CMCNT, cl
CMCNT has priority over writing to it. In this case, CMCNT is not written to. Figure 14.
the timing to clear the CMCNT counter.

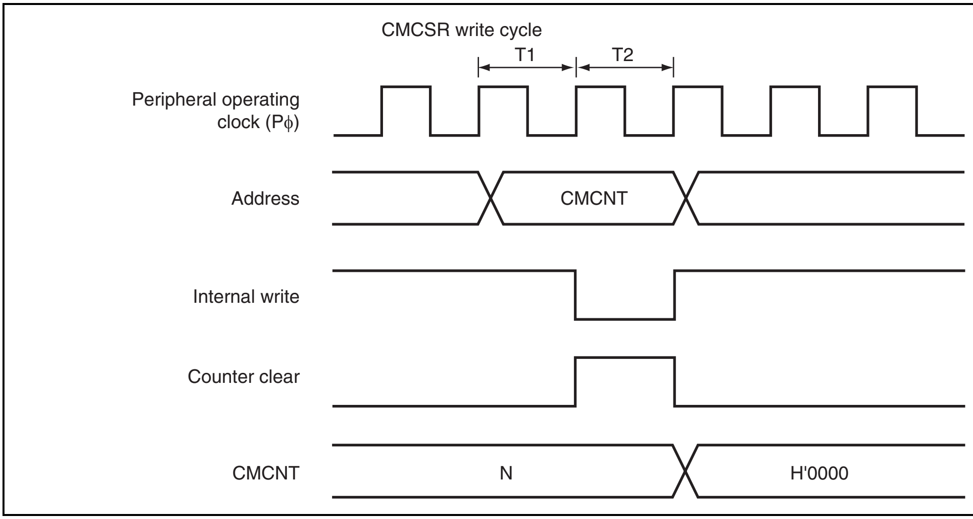


Figure 14.5 Conflict between Write and Compare-Match Processes of CMCN

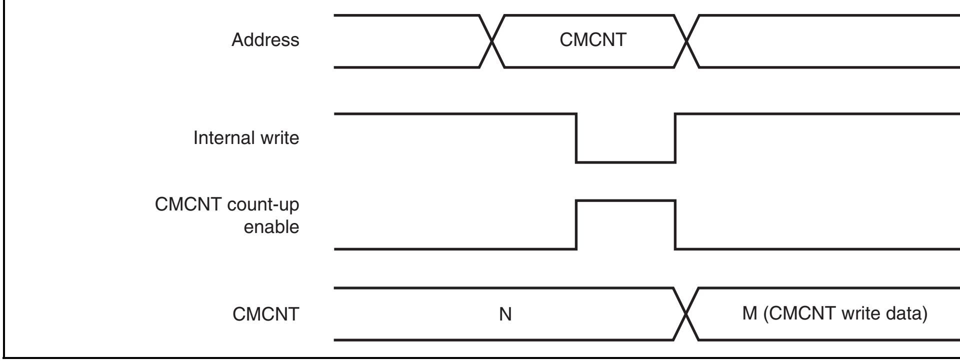


Figure 14.6 Conflict between Word-Write and Count-Up Processes of CMC

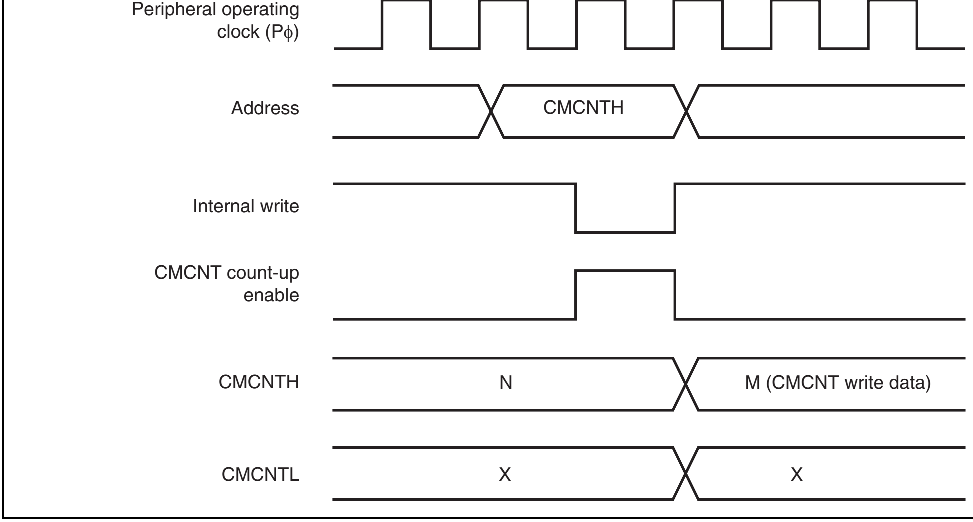


Figure 14.7 Conflict between Byte-Write and Count-Up Processes of CMCN

14.5.5 Compare Match between CMCNT and CMCOR

Do not set the same value in CMCNT and CMCOR while CMCNT is not counting. If set
CMF bit in CMCSR is set to 1 and CMCNT is cleared to H'0000.

Port	(Related Module)	(Related Module)	(Related Module)	(Related Module)	(Relate
A	PA0 I/O (port)	$\overline{\text{POE0}}$ input (POE)	RXD0 input (SCI)	—	—
	PA1 I/O (port)	$\overline{\text{POE1}}$ input (POE)	TXD0 output (SCI)	—	—
	PA2 I/O (port)	IRQ0 input (INTC)	SCK0 I/O (SCI)	—	—
	PA3 I/O (port)	IRQ1 input (INTC)	RXD1 input (SCI)	$\overline{\text{TRST}}$ input (H-UDI)*2	—
	PA4 I/O (port)	IRQ2 input (INTC)	TXD1 output (SCI)	TMS input (H-UDI)*2	—
	PA5 I/O (port)	IRQ3 input (INTC)	SCK1 I/O (SCI)	—	—
	PA6 I/O (port)	TCLKA input (MTU2)	—	—	—
	PA7 I/O (port)	TCLKB input (MTU2)	SCK2 I/O (SCI)	TCK input (H-UDI)*2	—
	PA8 I/O (port)	TCLKC input (MTU2)	RXD2 input (SCI)	TDI input (H-UDI)*2	—
	PA9 I/O (port)	TCLKD input (MTU2)	TXD2 output (SCI)	$\overline{\text{POE8}}$ input (POE)	TDO ou
	PA10 I/O (port)	RXD0 input (SCI)	—	—	—
	PA11 I/O (port)	TXD0 output (SCI)	$\overline{\text{ADTRG}}$ input (A/D)	—	—
	PA12 I/O (port)	SCK0 I/O (SCI)	—	—	—
	PA13 I/O (port)	SCK1 I/O (SCI)	—	—	—
	PA14 I/O (port)	RXD1 input (SCI)	—	—	—
	PA15 I/O (port)	TXD1 output (SCI)	—	—	—
B	PB1 I/O (port)	TIC5W input (MTU2)	—	—	—
	PB2 I/O (port)	IRQ0 input (INTC)	$\overline{\text{POE0}}$ input (POE)	—	—
	PB3 I/O (port)	IRQ1 input (INTC)	$\overline{\text{POE1}}$ input (POE)	TIC5V input (MTU2)	—
	PB5 I/O (port)	IRQ3 input (INTC)	TIC5U input (MTU2)	—	—
	PB16 I/O (port)	$\overline{\text{POE3}}$ input (POE)	—	—	—

	PE7 I/O (port)	TIOC2B I/O (MTU2)	—	—	—
	PE8 I/O (port)	TIOC3A I/O (MTU2)	—	—	—
	PE9 I/O (port)	TIOC3B I/O (MTU2)	—	—	—
	PE10 I/O (port)	TIOC3C I/O (MTU2)	—	—	—
	PE11 I/O (port)	TIOC3D I/O (MTU2)	—	—	—
	PE12 I/O (port)	TIOC4A I/O (MTU2)	—	—	—
	PE13 I/O (port)	TIOC4B I/O (MTU2)	$\overline{\text{MRES}}$ input (INTC)	—	—
	PE14 I/O (port)	TIOC4C I/O (MTU2)	—	—	—
	PE15 I/O (port)	TIOC4D I/O (MTU2)	$\overline{\text{IRQOUT}}$ output (INTC)	—	—
F	PF0 input (port)	AN0 input (A/D)	—	—	—
	PF1 input (port)	AN1 input (A/D)	—	—	—
	PF2 input (port)	AN2 input (A/D)	—	—	—
	PF3 input (port)	AN3 input (A/D)	—	—	—
	PF4 input (port)	AN4 input (A/D)	—	—	—
	PF5 input (port)	AN5 input (A/D)	—	—	—
	PF6 input (port)	AN6 input (A/D)	—	—	—
	PF7 input (port)	AN7 input (A/D)	—	—	—

Notes: 1. During A/D conversion, the AN input function is enabled.

2. These functions ($\overline{\text{TRST}}$, TMS, TCK, TDI, and TDO) are not supported on the 3 versions (SH71251A and SH71241A) and 16 Kbyte versions (SH71250A and SH71240A).

	PA8 I/O (port)	TCLKC input (MTU2)	RXD2 input (SCI)	TDI input (H-UDI)*[2]	—
	PA9 I/O (port)	TCLKD input (MTU2)	TXD2 output (SCI)	$\overline{\text{POE8}}$ input (POE)	TDO ou
B	PB1 I/O (port)	TIC5W input (MTU2)	—	—	—
	PB3 I/O (port)	IRQ1 input (INTC)	$\overline{\text{POE1}}$ input (POE)	TIC5V input (MTU2)	—
	PB5 I/O (port)	IRQ3 input (INTC)	TIC5U input (MTU2)	—	—
E	PE0 I/O (port)	TIOC0A I/O (MTU2)	—	—	—
	PE1 I/O (port)	TIOC0B I/O (MTU2)	RXD0 input (SCI)	—	—
	PE2 I/O (port)	TIOC0C I/O (MTU2)	TXD0 output (SCI)	—	—
	PE3 I/O (port)	TIOC0D I/O (MTU2)	SCK0 I/O (SCI)	—	—
	PE8 I/O (port)	TIOC3A I/O (MTU2)	—	—	—
	PE9 I/O (port)	TIOC3B I/O (MTU2)	—	—	—
	PE10 I/O (port)	TIOC3C I/O (MTU2)	—	—	—
	PE11 I/O (port)	TIOC3D I/O (MTU2)	—	—	—
	PE12 I/O (port)	TIOC4A I/O (MTU2)	—	—	—
	PE13 I/O (port)	TIOC4B I/O (MTU2)	$\overline{\text{MRES}}$ input (INTC)	—	—
	PE14 I/O (port)	TIOC4C I/O (MTU2)	—	—	—
	PE15 I/O (port)	TIOC4D I/O (MTU2)	$\overline{\text{IRQOUT}}$ output (INTC)	—	—

PF7 input (port)	AN7 input (A/D)	—	—	—

Notes: 1. During A/D conversion, the AN input function is enabled.

2. These functions ($\overline{\text{TRST}}$, TMS, TCK, TDI, and TDO) are not supported on the 3 versions (SH71251A and SH71241A) and 16 Kbyte versions (SH71250A and SH71240A).

47	PLLVss	PLLVss
42	EXTAL	EXTAL
41	XTAL	XTAL
46	MD1	MD1
45	FWE/(ASEBRKAK/ ASEBRK*1)	FWE
39	RES	RES
40	WDTOVF	WDTOVF
44	NMI	NMI
43	ASEMD0	ASEMD0
38	PA0	PA0/POE0/RXD0
36	PA1	PA1/POE1/TXD0
34	PA2	PA2/IRQ0/SCK0
32	PA3/(TRST*1)	PA3/IRQ1/RXD1
31	PA4/(TMS*1)	PA4/IRQ2/TXD1
30	PA5	PA5/IRQ3/SCK1
29	PA6	PA6/TCLKA
28	PA7/(TCK*1)	PA7/TCLKB/SCK2
27	PA8/(TDI*1)	PA8/TCLKC/RXD2
26	PA9/(TDO*1)	PA9/TCLKD/TXD2/POE8
25	PA10	PA10/RXD0
23	PA11	PA11/TXD0/ADTRG
21	PA12	PA12/SCK0
20	PA13	PA13/SCK1

62	POE3	PB16/POE3
17	PE0	PE0/TIOC0A
16	PE1	PE1/TIOC0B/RXD0
15	PE2	PE2/TIOC0C/TXD0
14	PE3	PE3/TIOC0D/SCK0
13	PE4	PE4/TIOC1A/RXD1
12	PE5	PE5/TIOC1B/TXD1
11	PE6	PE6/TIOC2A/SCK1
10	PE7	PE7/TIOC2B
9	PE8	PE8/TIOC3A
5	PE9	PE9/TIOC3B
7	PE10	PE10/TIOC3C
3	PE11	PE11/TIOC3D
2	PE12	PE12/TIOC4A
1	PE13	PE13/TIOC4B/$\overline{\text{MRES}}$
64	PE14	PE14/TIOC4C
63	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$
60	PF0/AN0	PF0/AN0
59	PF1/AN1	PF1/AN1
58	PF2/AN2	PF2/AN2
57	PF3/AN3	PF3/AN3
56	PF4/AN4	PF4/AN4
55	PF5/AN5	PF5/AN5

Table 15.4 SH7124 Pin Functions in Each Operating Mode

	Pin Name	
	Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities
4, 17	Vcc	Vcc
6, 19	Vss	Vss
8, 25	VCL	VCL
48	AVcc	AVcc
39	AVss	AVss
35	PLLVss	PLLVss
30	EXTAL	EXTAL
29	XTAL	XTAL
34	MD1	MD1
33	FWE/($\overline{\text{ASEBRKAK}}$/ $\overline{\text{ASEBRK}}$*1)	FWE
27	$\overline{\text{RES}}$	$\overline{\text{RES}}$
28	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
32	NMI	NMI
31	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$
26	PA0	PA0/$\overline{\text{POE0}}$/RXD0
24	PA1	PA1/$\overline{\text{POE1}}$/TXD0
23	PA3/($\overline{\text{TRST}}$*1)	PA3/IRQ1/RXD1

37	PB3	PB3/IRQ1/POE1/TIC5V
36	PB5	PB5/IRQ3/TIC5U
15	PE0	PE0/TIOC0A
14	PE1	PE1/TIOC0B/RXD0
13	PE2	PE2/TIOC0C/TXD0
12	PE3	PE3/TIOC0D/SCK0
11	PE8	PE8/TIOC3A
9	PE9	PE9/TIOC3B
10	PE10	PE10/TIOC3C
7	PE11	PE11/TIOC3D
5	PE12	PE12/TIOC4A
3	PE13	PE13/TIOC4B/$\overline{\text{MRES}}$
2	PE14	PE14/TIOC4C
1	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$
47	PF0/AN0	PF0/AN0
46	PF1/AN1	PF1/AN1
45	PF2/AN2	PF2/AN2
44	PF3/AN3	PF3/AN3
43	PF4/AN4	PF4/AN4
42	PF5/AN5	PF5/AN5
41	PF6/AN6	PF6/AN6
40	PF7/AN7	PF7/AN7

Notes: 1. Fixed to TMS, $\overline{\text{TRST}}$, TDI, TDO, TCK, and $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ when using t
(in $\overline{\text{ASEMD0}}$ = low).

2. E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kb
(SH71250A and SH71240A) versions.

Port A control register L4	PACRL4	R/W	H'0000	H’FFFFD110	8,
Port A control register L3	PACRL3	R/W	H'0000	H’FFFFD112	8,
Port A control register L2	PACRL2	R/W	H'0000	H’FFFFD114	8,
Port A control register L1	PACRL1	R/W	H'0000	H’FFFFD116	8,
Port B I/O register H	PBIORH	R/W	H'0000	H'FFFFD184	8,
Port B I/O register L	PBIORL	R/W	H'0000	H'FFFFD186	8,
Port B control register H1	PBCRH1	R/W	H'0000	H'FFFFD18E	8,
Port B control register L2	PBCRL2	R/W	H'0000	H'FFFFD194	8,
Port B control register L1	PBCRL1	R/W	H'0000	H'FFFFD196	8,
Port E I/O register L	PEIORL	R/W	H'0000	H'FFFFD306	8,
Port E control register L4	PECRL4	R/W	H'0000	H'FFFFD310	8,
Port E control register L3	PECRL3	R/W	H'0000	H'FFFFD312	8,
Port E control register L2	PECRL2	R/W	H'0000	H'FFFFD314	8,
Port E control register L1	PECRL1	R/W	H'0000	H'FFFFD316	8,
IRQOUT function control register	IFCR	R/W	H'0000	H'FFFFD322	8,

The initial value of PAIORL is H'0000.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	PA15 IOR	PA14 IOR	PA13 IOR	PA12 IOR	PA11 IOR	PA10 IOR	PA9 IOR	PA8 IOR	PA7 IOR	PA6 IOR	PA5 IOR	PA4 IOR	PA3 IOR	PA2 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.1.2 Port A Control Registers L1 to L4 (PACRL1 to PACRL4)

PACRL1 to PACRL4 are 16-bit readable/writable registers that are used to select the fun
the multiplexed pins on port A.

SH7125:

- Port A Control Register L4 (PACRL4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PA15 MD2	PA15 MD1	PA15 MD0	-	PA14 MD2	PA14 MD1	PA14 MD0	-	PA13 MD2	PA13 MD1	PA13 MD0	-	PA12 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.

10	PA14MD2	0	R/W	PA14 Mode
9	PA14MD1	0	R/W	Select the function of the PA14/RXD1 pin.
8	PA14MD0	0	R/W	000: PA14 I/O (port) 110: RXD1 input (SCI) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
6	PA13MD2	0	R/W	PA13 Mode
5	PA13MD1	0	R/W	Select the function of the PA13/SCK1 pin.
4	PA13MD0	0	R/W	000: PA13 I/O (port) 110: SCK1 I/O (SCI) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
2	PA12MD2	0	R/W	PA12 Mode
1	PA12MD1	0	R/W	Select the function of the PA12/SCK0 pin.
0	PA12MD0	0	R/W	000: PA12 I/O (port) 110: SCK0 I/O (SCI) Other than above: Setting prohibited

14	PA11MD2	0	R/W	PA11 Mode
13	PA11MD1	0	R/W	Select the function of the PA11/TXD0/$\overline{\text{ADTR}}$
12	PA11MD0	0	R/W	000: PA11 I/O (port)
				010: $\overline{\text{ADTRG}}$ input (A/D)
				110: TXD0 output (SCI)
				Other than above: Setting prohibited
11	—	0	R	Reserved
				This bit is always read as 0. The write value s always be 0.
10	PA10MD2	0	R/W	PA10 Mode
9	PA10MD1	0	R/W	Select the function of the PA10/RXD0 pin.
8	PA10MD0	0	R/W	000: PA10 I/O (port)
				110: RXD0 input (SCI)
				Other than above: Setting prohibited
7	—	0	R	Reserved
				This bit is always read as 0. The write value s always be 0.

				111: POE8 input (POE) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
2	PA8MD2	0	R/W	PA8 Mode
1	PA8MD1	0	R/W	Select the function of the PA8/TCLKC/RXD
0	PA8MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low) is fixed to TDI input. 000: PA8 I/O (port) 001: TCLKC input (MTU2) 110: RXD2 input (SCI) Other than above: Setting prohibited

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 K (SH71250A and SH71240A) versions.

14	PA7MD2	0	R/W	PA7 Mode
13	PA7MD1	0	R/W	Select the function of the PA7/TCLKB/SCK2/
12	PA7MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), is fixed to TCK input. 000: PA7 I/O (port) 001: TCLKB input (MTU2) 110: SCK2 I/O (SCI) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
10	PA6MD2	0	R/W	PA6 Mode
9	PA6MD1	0	R/W	Select the function of the PA6/TCLKA pin.
8	PA6MD0	0	R/W	000: PA6 I/O (port) 001: TCLKA input (MTU2) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
6	PA5MD2	0	R/W	PA5 Mode
5	PA5MD1	0	R/W	Select the function of the PA5/IRQ3/SCK1 pi
4	PA5MD0	0	R/W	000: PA5 I/O (port) 001: SCK1 I/O (SCI) 111: IRQ3 input (INTC) Other than above: Setting prohibited

001: TXD1 output (SCI)

111: IRQ2 input (INTC)

Other than above: Setting prohibited

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 K
(SH71250A and SH71240A) versions.

- Port A Control Register L1 (PACRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PA3 MD2	PA3 MD1	PA3 MD0	-	PA2 MD2	PA2 MD1	PA2 MD0	-	PA1 MD2	PA1 MD1	PA1 MD0	-	PA0 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
14 13 12	PA3MD2 PA3MD1 PA3MD0	0 0 0	R/W R/W R/W	PA3 Mode Select the function of the PA3/IRQ1/RXD1/$\overline{\text{T}}$ When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low) is fixed to $\overline{\text{TRST}}$ input. 000: PA3 I/O (port) 001: RXD1 input (SCI) 111: IRQ1 input (INTC) Other than above: Setting prohibited

				Other than above: Setting prohibited
7	—	0	R	Reserved
				This bit is always read as 0. The write value s always be 0.
6	PA1MD2	0	R/W	PA1 Mode
5	PA1MD1	0	R/W	Select the function of the PA1/$\overline{\text{POE1}}$/TXD0 p
4	PA1MD0	0	R/W	000: PA1 I/O (port)
				001: TXD0 output (SCI)
				111: $\overline{\text{POE1}}$ input (POE)
				Other than above: Setting prohibited
3	—	0	R	Reserved
				This bit is always read as 0. The write value s always be 0.
2	PA0MD2	0	R/W	PA0 Mode
1	PA0MD1	0	R/W	Select the function of the PA0/$\overline{\text{POE0}}$/RXD0 p
0	PA0MD0	0	R/W	000: PA0 I/O (port)
				001: RXD0 input (SCI)
				111: $\overline{\text{POE0}}$ input (POE)
				Other than above: Setting prohibited

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kb (SH71250A and SH71240A) versions.

should always be 0.

- Port A Control Register L3 (PACRL3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	PA9 MD2	PA9 MD1	PA9 MD0	-	PA8 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.
6	PA9MD2	0	R/W	PA9 Mode
5	PA9MD1	0	R/W	Select the function of the PA9/TCLKD/TXD2/TDO/$\overline{POE8}$ pin. When th is in use ($\overline{ASEMD0}$ = low), function is fixed t output.
4	PA9MD0	0	R/W	000: PA9 I/O (port) 001: TCLKD input (MTU2) 110: TXD2 output (SCI) 111: $\overline{POE8}$ input (POE) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value always be 0.

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kb (SH71250A and SH71240A) versions.

- Port A Control Register L2 (PACRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PA7 MD2	PA7 MD1	PA7 MD0	-	PA6 MD2	PA6 MD1	PA6 MD0	-	-	-	-	-	PA4 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
14	PA7MD2	0	R/W	PA7 Mode
13	PA7MD1	0	R/W	Select the function of the PA7/TCLKB/SCK2/ When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), t is fixed to TCK input.
12	PA7MD0	0	R/W	000: PA7 I/O (port) 001: TCLKB input (MTU2) 110: SCK2 I/O (SCI) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.

2	PA4MD2	0	R/W	PA4 Mode
1	PA4MD1	0	R/W	Select the function of the PA4/IRQ2/TXD1/T When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low) is fixed to TMS input.
0	PA4MD0	0	R/W	000: PA4 I/O (port) 001: TXD1 output (SCI) 111: IRQ2 input (INTC) Other than above: Setting prohibited

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 K (SH71250A and SH71240A) versions.

- Port A Control Register L1 (PACRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PA3 MD2	PA3 MD1	PA3 MD0	-	-	-	-	-	PA1 MD2	PA1 MD1	PA1 MD0	-	PA0 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value always be 0.

11 to 7	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
6 5 4	PA1MD2 PA1MD1 PA1MD0	0 0 0	R/W R/W R/W	PA1 Mode Select the function of the PA1/$\overline{\text{POE1}}$/TXD0 p 000: PA1 I/O (port) 001: TXD0 output (SCI) 111: $\overline{\text{POE1}}$ input (POE) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
2 1 0	PA0MD2 PA0MD1 PA0MD0	0 0 0	R/W R/W R/W	PA0 Mode Select the function of the PA0/$\overline{\text{POE0}}$/RXD0 p 000: PA0 I/O (port) 001: RXD0 input (SCI) 100: $\overline{\text{POE0}}$ output (POE) Other than above: Setting prohibited

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kb (SH71250A and SH71240A) versions.

to 1, and an input pin if the bit is cleared to 0.

However, bit 2 of PBIORL and bit 0 of PBIORH are disabled in SH7124.

Bits 15 to 6, 4, and 0 of PBIORL and bits 15 to 1 of PBIORH are reserved. These bits ar read as 0. The write value should always be 0.

The initial value of PBIORL and PBIORH are H'0000, respectively.

- Port B I/O Register H (PBIORH)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Port B I/O Register L (PBIORL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	PB5 IOR	-	PB3 IOR	PB2 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W

R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * After a power-on reset, write can be performed only once.

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
0	PB16MD	1	R/W*	PB16 Mode Select the function of the PB16/$\overline{\text{POE3}}$ pin. 0: PB16 I/O (port) 1: $\overline{\text{POE3}}$ input (POE)

- Port B Control Register L2 (PBCRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	PB5 MD2	PB5 MD1	PB5 MD0	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.

should always be 0.

- Port B Control Register L1 (PBCRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PB3 MD2	PB3 MD1	PB3 MD0	-	PB2 MD2	PB2 MD1	PB2 MD0	-	PB1 MD2	PB1 MD1	PB1 MD0	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
14	PB3MD2	0	R/W	PB3 Mode
13	PB3MD1	0	R/W	Select the function of the PB3/IRQ1/$\overline{\text{POE1}}$/T
12	PB3MD0	0	R/W	000: PB3 I/O (port) 001: IRQ1 input (INTC) 010: $\overline{\text{POE1}}$ input (POE) 011: TIC5V input (MTU2) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value always be 0.

				always be 0.
6	PB1MD2	0	R/W	PB1 Mode
5	PB1MD1	0	R/W	Select the function of the PB1/TIC5W pin.
4	PB1MD0	0	R/W	000: PB1 I/O (port) 011: TIC5W input (MTU2) Other than above: Setting prohibited
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.

SH7124:

- Port B Control Register H1 (PBCRH1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.

6	PB5MD2	0	R/W	PB5 Mode
5	PB5MD1	0	R/W	Select the function of the PB5/IRQ3/TIC5U
4	PB5MD0	0	R/W	000: PB5 I/O (port) 001: IRQ3 input (INTC) 011: TIC5U input (MTU2) Other than above: Setting prohibited
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.

- Port B Control Register L1 (PBCRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PB3 MD2	PB3 MD1	PB3 MD0	-	-	-	-	-	PB1 MD2	PB1 MD1	PB1 MD0	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value always be 0.

				These bits are always read as 0. The write va should always be 0.
6	PB1MD2	0	R/W	PB1 Mode
5	PB1MD1	0	R/W	Select the function of the PB1/TIC5W pin.
4	PB1MD0	0	R/W	000: PB1 I/O (port)
				011: TIC5W input (MTU2)
				Other than above: Setting prohibited
3 to 0	—	All 0	R	Reserved
				These bits are always read as 0. The write va should always be 0.

However, bits 7 to 4 of PEIORL are disabled in SH7124.

The initial value of PEIORL is H'0000.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	PE15 IOR	PE14 IOR	PE13 IOR	PE12 IOR	PE11 IOR	PE10 IOR	PE9 IOR	PE8 IOR	PE7 IOR	PE6 IOR	PE5 IOR	PE4 IOR	PE3 IOR	PE2 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.1.6 Port E Control Registers L1 to L4 (PECRL1 to PECRL4)

PECRL1 to PECRL4, are 16-bit readable/writable registers that are used to select the fu
the multiplexed pins on port E.

SH7125:

- Port E Control Register L4 (PECRL4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PE15 MD2	PE15 MD1	PE15 MD0	-	PE14 MD2	PE14 MD1	PE14 MD0	-	-	PE13 MD1	PE13 MD0	-	PE12 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value always be 0.

				always be 0.
10 9 8	PE14MD2 PE14MD1 PE14MD0	0 0 0	R/W R/W R/W	PE14 Mode Select the function of the PE14/TIOC4C pin. 000: PE14 I/O (port) 001: TIOC4C I/O (MTU2) Other than above: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write va should always be 0.
5 4	PE13MD1 PE13MD0	0 0	R/W R/W	PE13 Mode Select the function of the PE13/TIOC4B/$\overline{\text{MRE}}$ 00: PE13 I/O (port) 01: TIOC4B I/O (MTU2) 10: $\overline{\text{MRES}}$ input (INTC) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
2 1 0	PE12MD2 PE12MD1 PE12MD0	0 0 0	R/W R/W R/W	PE12 Mode Select the function of the PE12/TIOC4A pin. 000: PE12 I/O (port) 001: TIOC4A I/O (MTU2) Other than above: Setting prohibited

14	PE11MD2	0	R/W	PE11 Mode
13	PE11MD1	0	R/W	Select the function of the PE11/TIOC3D pin
12	PE11MD0	0	R/W	000: PE11 I/O (port)
				001: TIOC3D I/O (MTU2)
				Other than above: Setting prohibited
11	—	0	R	Reserved
				This bit is always read as 0. The write value always be 0.
10	PE10MD2	0	R/W	PE10 Mode
9	PE10MD1	0	R/W	Select the function of the PE10/TIOC3C pin
8	PE10MD0	0	R/W	000: PE10 I/O (port)
				001: TIOC3C I/O (MTU2)
				Other than above: Setting prohibited
7	—	0	R	Reserved
				This bit is always read as 0. The write value always be 0.
6	PE9MD2	0	R/W	PE9 Mode
5	PE9MD1	0	R/W	Select the function of the PE9/TIOC3B pin.
4	PE9MD0	0	R/W	000: PE9 I/O (port)
				001: TIOC3B I/O (MTU2)
				Other than above: Setting prohibited
3	—	0	R	Reserved
				This bit is always read as 0. The write value always be 0.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PE7 MD2	PE7 MD1	PE7 MD0	-	PE6 MD2	PE6 MD1	PE6 MD0	-	PE5 MD2	PE5 MD1	PE5 MD0	-	PE4 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
14	PE7MD2	0	R/W	PE7 Mode
13	PE7MD1	0	R/W	Select the function of the PE7/TIOC2B pin.
12	PE7MD0	0	R/W	000: PE7 I/O (port) 001: TIOC2B I/O (MTU2) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
10	PE6MD2	0	R/W	PE6 Mode
9	PE6MD1	0	R/W	Select the function of the PE6/TIOC2A/SCK1
8	PE6MD0	0	R/W	000: PE6 I/O (port) 001: TIOC2A I/O (MTU2) 110: SCK1 I/O (SCI) Other than above: Setting prohibited

				Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
2	PE4MD2	0	R/W	PE4 Mode
1	PE4MD1	0	R/W	Select the function of the PE4/TIOC1A/RXD
0	PE4MD0	0	R/W	000: PE4 I/O (port) 001: TIOC1A I/O (MTU2) 110: RXD1 input (SCI) Other than above: Setting prohibited

- Port E Control Register L1 (PECRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PE3 MD2	PE3 MD1	PE3 MD0	-	PE2 MD2	PE2 MD1	PE2 MD0	-	PE1 MD2	PE1 MD1	PE1 MD0	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value always be 0.

				always be 0.
10	PE2MD2	0	R/W	PE2 Mode
9	PE2MD1	0	R/W	Select the function of the PE2/TIOC0C/TXD0
8	PE2MD0	0	R/W	000: PE2 I/O (port)
				001: TIOC0C I/O (MTU2)
				110: TXD0 output (SCI)
				Other than above: Setting prohibited
7	—	0	R	Reserved
				This bit is always read as 0. The write value s always be 0.
6	PE1MD2	0	R/W	PE1 Mode
5	PE1MD1	0	R/W	Select the function of the PE1/TIOC0B/RXD0
4	PE1MD0	0	R/W	000: PE1 I/O (port)
				001: TIOC0B I/O (MTU2)
				110: RXD0 input (SCI)
				Other than above: Setting prohibited
3, 2	—	All 0	R	Reserved
				These bits are always read as 0. The write va should always be 0.
1	PE0MD1	0	R/W	PE0 Mode
0	PE0MD0	0	R/W	Select the function of the PE0/TIOC0A pin.
				00: PE0 I/O (port)
				01: TIOC0A I/O (MTU2)
				Other than above: Setting prohibited

				This bit is always read as 0. The write value always be 0.
14 13 12	PE15MD2 PE15MD1 PE15MD0	0 0 0	R/W R/W R/W	PE15 Mode Select the function of the PE15/TIOC4D/$\overline{\text{IR}}$ 000: PE15 I/O (port) 001: TIOC4D I/O (MTU2) 011: $\overline{\text{IRQOUT}}$ output (INTC) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
10 9 8	PE14MD2 PE14MD1 PE14MD0	0 0 0	R/W R/W R/W	PE14 Mode Select the function of the PE14/TIOC4C pin 000: PE14 I/O (port) 001: TIOC4C I/O (MTU2) Other than above: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write should always be 0.
5 4	PE13MD1 PE13MD0	0 0	R/W R/W	PE13 Mode Select the function of the PE13/TIOC4B/$\overline{\text{MR}}$ 00: PE13 I/O (port) 01: TIOC4B I/O (MTU2) 10: $\overline{\text{MRES}}$ input (INTC) Other than above: Setting prohibited

- Port E Control Register L3 (PECRL3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	PE11 MD2	PE11 MD1	PE11 MD0	-	PE10 MD2	PE10 MD1	PE10 MD0	-	PE9 MD2	PE9 MD1	PE9 MD0	-	PE8 MD2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
14	PE11MD2	0	R/W	PE11 Mode
13	PE11MD1	0	R/W	Select the function of the PE11/TIOC3D pin.
12	PE11MD0	0	R/W	000: PE11 I/O (port) 001: TIOC3D I/O (MTU2) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
10	PE10MD2	0	R/W	PE10 Mode
9	PE10MD1	0	R/W	Select the function of the PE10/TIOC3C pin.
8	PE10MD0	0	R/W	000: PE10 I/O (port) 001: TIOC3C I/O (MTU2) Other than above: Setting prohibited

3	—	0	R	Reserved This bit is always read as 0. The write value always be 0.
2	PE8MD2	0	R/W	PE8 Mode
1	PE8MD1	0	R/W	Select the function of the PE8/TIOC3A pin.
0	PE8MD0	0	R/W	000: PE8 I/O (port) 001: TIOC3A I/O (MTU2) Other than above: Setting prohibited

- Port E Control Register L2 (PECRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.

14	PE3MD2	0	R/W	PE3 Mode
13	PE3MD1	0	R/W	Select the function of the PE3/TIOC0D/SCK0
12	PE3MD0	0	R/W	000: PE3 I/O (port) 001: TIOC0D I/O (MTU2) 110: SCK0 I/O (SCI) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
10	PE2MD2	0	R/W	PE2 Mode
9	PE2MD1	0	R/W	Select the function of the PE2/TIOC0C/TXD0
8	PE2MD0	0	R/W	000: PE2 I/O (port) 001: TIOC0C I/O (MTU2) 110: TXD0 output (SCI) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
6	PE1MD2	0	R/W	PE1 Mode
5	PE1MD1	0	R/W	Select the function of the PE1/TIOC0B/RXD0
4	PE1MD0	0	R/W	000: PE1 I/O (port) 001: TIOC0B I/O (MTU2) 110: RXD0 input (SCI) Other than above: Setting prohibited

15.1.7 IRQOUT Function Control Register (IFCR)

IFCR is a 16-bit readable/writable register that is used to control the IRQOUT pin outpu is selected as the multiplexed pin function by port E control register L4 (PECRL4). Whe PECRL4 selects another function, the IFCR setting does not affect the pin function.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write v should always be 0.
1	IRQMD1	0	R/W	Port E $\overline{\text{IRQOUT}}$ Pin Function Select
0	IRQMD0	0	R/W	Select the $\overline{\text{IRQOUT}}$ pin function when bits 1 (PE15MD2 to PE15MD0) in PECRL4 are se 00: Interrupt request accept signal output Other than above: Always high-level output

functions. Table 15.6 shows the transmit forms of input functions allocated to seve
When using one of the functions shown below in multiple pins, use it with care of
polarity considering the transmit forms.

Table 15.6 Transmit Forms of Input Functions Allocated to Multiple Pins

OR Type	AND Type
SCK0 to SCK2, RXD0 to RXD2, $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, $\overline{\text{POE8}}$	IRQ0* to IRQ3

Note: * This pin is supported only by the SH7125.

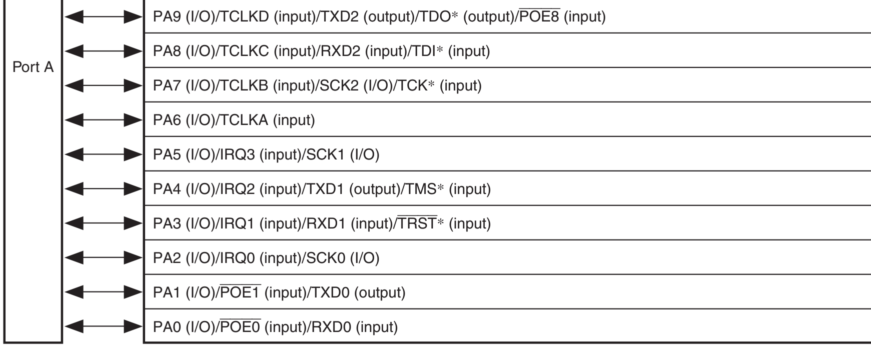
OR type: Signals input to several pins are formed as one signal through OR log
signal is transmitted into the LSI.

AND type: Signals input to several pins are formed as one signal through AND lo
the signal is transmitted into the LSI.

— When the pin function is output

Each selected pin can output the same function.

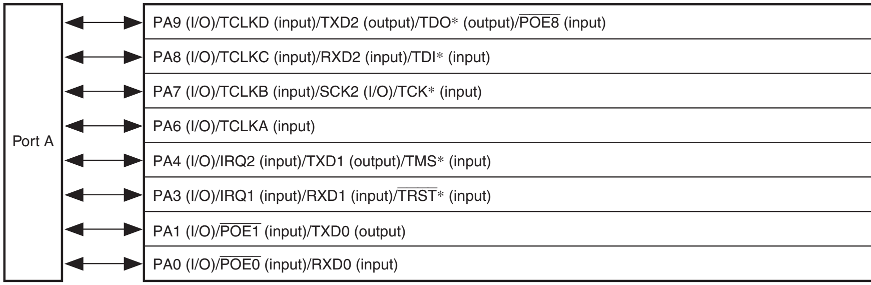
2. When the port input is switched from a low level to the IRQ edge for the pins that are multiplexed with input/output and IRQ, the corresponding edge is detected.
3. Do not set functions other than those specified in tables 15.3 and 15.4. Otherwise, cor operation cannot be guaranteed.


Port A
PA9 (I/O)/TCLKD (input)/TXD2 (output)/TDO* (output)/$\overline{\text{POE8}}$ (input)
PA8 (I/O)/TCLKC (input)/RXD2 (input)/TDI* (input)
PA7 (I/O)/TCLKB (input)/SCK2 (I/O)/TCK* (input)
PA6 (I/O)/TCLKA (input)
PA5 (I/O)/IRQ3 (input)/SCK1 (I/O)
PA4 (I/O)/IRQ2 (input)/TXD1 (output)/TMS* (input)
PA3 (I/O)/IRQ1 (input)/RXD1 (input)/$\overline{\text{TRST}}$* (input)
PA2 (I/O)/IRQ0 (input)/SCK0 (I/O)
PA1 (I/O)/$\overline{\text{POE1}}$ (input)/TXD0 (output)
PA0 (I/O)/$\overline{\text{POE0}}$ (input)/RXD0 (input)

Note: * The TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ pins are not supported on the 32 Kbyte versions (SH71251A and SH71241A) and 16 Kbyte versions (SH71250A and SH71240A).

Figure 16.1 Port A (SH7125)

Port A in the SH7124 is an input/output port with the eight pins shown in figure 16.2.


Port A
PA9 (I/O)/TCLKD (input)/TXD2 (output)/TDO* (output)/$\overline{\text{POE8}}$ (input)
PA8 (I/O)/TCLKC (input)/RXD2 (input)/TDI* (input)
PA7 (I/O)/TCLKB (input)/SCK2 (I/O)/TCK* (input)
PA6 (I/O)/TCLKA (input)
PA4 (I/O)/IRQ2 (input)/TXD1 (output)/TMS* (input)
PA3 (I/O)/IRQ1 (input)/RXD1 (input)/$\overline{\text{TRST}}$* (input)
PA1 (I/O)/$\overline{\text{POE1}}$ (input)/TXD0 (output)
PA0 (I/O)/$\overline{\text{POE0}}$ (input)/RXD0 (input)

Note: * The TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ pins are not supported on the 32 Kbyte versions (SH71251A and SH71241A) and 16 Kbyte versions (SH71250A and SH71240A).

Figure 16.2 Port A (SH7124)

Port A port register L	PAPRL	R	—	H'FFFFD11E	8,

16.1.2 Port A Data Register L (PADRL)

PADRL is a 16-bit readable/writable register that stores port A data. Bits PA15DR to PA
correspond to pins PA15 to PA0 (multiplexed functions omitted here) in the SH7125. Bi
to PA6DR, PA4DR, PA3DR, PA1DR, and PA0DR correspond to pins PA9 to PA6, PA4
PA1, and PA0, respectively (multiplexed functions omitted here) in the SH7124.

When a pin function is general output, if a value is written to PADRL, that value is outp
from the pin, and if PADRL is read, the register value is returned directly regardless of t
state.

When a pin function is general input, if PADRL is read, the pin state, not the register va
returned directly. If a value is written to PADRL, although that value is written into PA
does not affect the pin state. Table 16.2 summarizes port A data register read/write oper

13	PA13DR	0	R/W
12	PA12DR	0	R/W
11	PA11DR	0	R/W
10	PA10DR	0	R/W
9	PA9DR	0	R/W
8	PA8DR	0	R/W
7	PA7DR	0	R/W
6	PA6DR	0	R/W
5	PA5DR	0	R/W
4	PA4DR	0	R/W
3	PA3DR	0	R/W
2	PA2DR	0	R/W
1	PA1DR	0	R/W
0	PA0DR	0	R/W

9	PA9DR	0	R/W	See table 16.2.
8	PA8DR	0	R/W	
7	PA7DR	0	R/W	
6	PA6DR	0	R/W	
5	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
4	PA4DR	0	R/W	See table 16.2.
3	PA3DR	0	R/W	
2	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
1	PA1DR	0	R/W	See table 16.2.
0	PA0DR	0	R/W	

general output	state

	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	PA15PR	Pin state	R	The pin state is returned regardless of the PF These bits cannot be modified.
14	PA14PR	Pin state	R	
13	PA13PR	Pin state	R	
12	PA12PR	Pin state	R	
11	PA11PR	Pin state	R	
10	PA10PR	Pin state	R	
9	PA9PR	Pin state	R	
8	PA8PR	Pin state	R	
7	PA7PR	Pin state	R	
6	PA6PR	Pin state	R	
5	PA5PR	Pin state	R	
4	PA4PR	Pin state	R	
3	PA3PR	Pin state	R	
2	PA2PR	Pin state	R	
1	PA1PR	Pin state	R	
0	PA0PR	Pin state	R	

9	PA9PR	Pin state	R	The pin state is returned regardless of the PFC These bits cannot be modified.
8	PA8PR	Pin state	R	
7	PA7PR	Pin state	R	
6	PA6PR	Pin state	R	
5	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
4	PA4PR	Pin state	R	The pin state is returned regardless of the PFC These bits cannot be modified.
3	PA3PR	Pin state	R	
2	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
1	PA1PR	Pin state	R	The pin state is returned regardless of the PFC These bits cannot be modified.
0	PA0PR	Pin state	R	

Figure 16.3 Port B (SH7125)

Port B in the SH7124 is an input/output port with the three pins shown in figure 16.4.

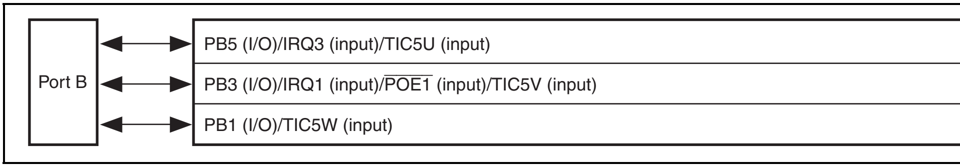

Port B
PB5 (I/O)/IRQ3 (input)/TIC5U (input)
PB3 (I/O)/IRQ1 (input)/$\overline{\text{POE1}}$ (input)/TIC5V (input)
PB1 (I/O)/TIC5W (input)

Figure 16.4 Port B (SH7124)

16.2.1 Register Descriptions

Port B is a 5-bit input/output port in the SH7125 and a 3-bit input/output port in the SH7
B has the following register. For details on register addresses and register states during e
processing, refer to section 20, List of Registers.

Table 16.3 Register Configuration

Register Name	Abbrevia- tion	R/W	Initial Value	Address	Ac
Port B data register H	PBDRH	R/W	H'0000	H'FFFFD180	8,
Port B data register L	PBDRL	R/W	H'0000	H'FFFFD182	8,
Port B port register H	PBPRH	R	—	H'FFFFD19C	8,
Port B port register L	PBPRL	R	—	H'FFFFD19E	8,

When a pin function is general input, if PBDRH or PBDRL is read, the pin state, not the r value, is returned directly. If a value is written to PBDRH or PBDRL, although that value written into PBDRH or PBDRL, it does not affect the pin state. Table 16.4 summarizes p register read/write operations.

- PBDRH (SH7125)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
0	PB16DR	0	R/W	See table 16.4.

- PBDRL (SH7125)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	PB5 DR	-	PB3 DR	PB2 DR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
5	PB5DR	0	R/W	See table 16.4.
4	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
3	PB3DR	0	R/W	See table 16.4.
2	PB2DR	0	R/W	
1	PB1DR	0	R/W	
0	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.

5	PB5DR	0	R/W	See table 16.4.
4	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
3	PB3DR	0	R/W	See table 16.4.
2	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
1	PB1DR	0	R/W	See table 16.4.
0	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.

Table 16.4 Port B Data Register (PBDR) Read/Write Operations

- PBDRH Bit 0 and PBDRL Bits 5 and 3 to 1

PBIOR	Pin Function	Read	Write
0	General input	Pin state	Can write to PBDRH and PBDRL, but it ha effect on pin state
	Other than general input	Pin state	Can write to PBDRH and PBDRL, but it ha effect on pin state
1	General output	PBDRH or PBDRL value	Value written is output from pin
	Other than general output	PBDRH or PBDRL value	Can write to PBDRH and PBDRL, but it ha effect on pin state

Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
0	PB16PR	Pin state	R	The pin state is returned regardless of the PF This bit cannot be modified.

- PBPRH (SH7124)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.

5	PB5PR	Pin state	R	The pin state is returned regardless of the PFC This bit cannot be modified.
4	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.
3	PB3PR	Pin state	R	The pin state is returned regardless of the PFC These bits cannot be modified.
2	PB2PR	Pin state	R	
1	PB1PR	Pin state	R	
0	—	0	R	Reserved This bit is always read as 0. The write value sh always be 0.

5	PB5PR	Pin state	R	The pin state is returned regardless of the PF This bit cannot be modified.
4	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
3	PB3PR	Pin state	R	The pin state is returned regardless of the PF This bit cannot be modified.
2	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.
1	PB1PR	Pin state	R	The pin state is returned regardless of the PF This bit cannot be modified.
0	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.

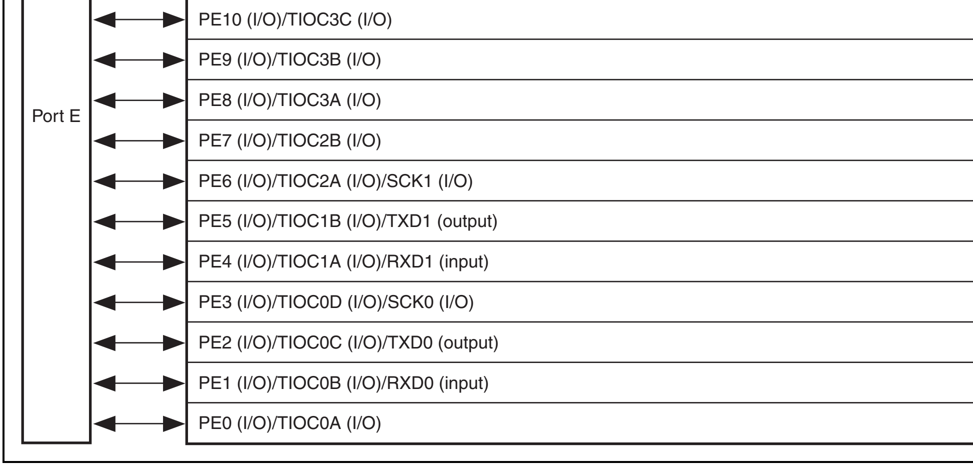

Port E
PE10 (I/O)/TIOC3C (I/O)
PE9 (I/O)/TIOC3B (I/O)
PE8 (I/O)/TIOC3A (I/O)
PE7 (I/O)/TIOC2B (I/O)
PE6 (I/O)/TIOC2A (I/O)/SCK1 (I/O)
PE5 (I/O)/TIOC1B (I/O)/TXD1 (output)
PE4 (I/O)/TIOC1A (I/O)/RXD1 (input)
PE3 (I/O)/TIOC0D (I/O)/SCK0 (I/O)
PE2 (I/O)/TIOC0C (I/O)/TXD0 (output)
PE1 (I/O)/TIOC0B (I/O)/RXD0 (input)
PE0 (I/O)/TIOC0A (I/O)

Figure 16.5 Port E (SH7125)

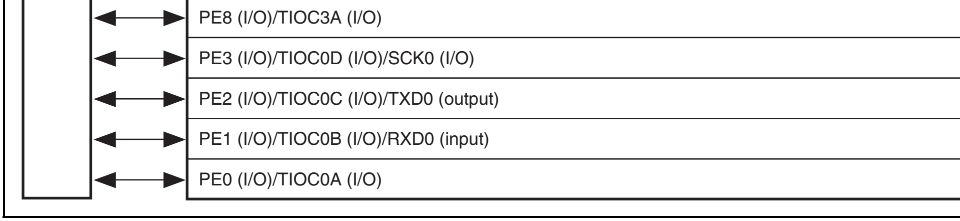

PE8 (I/O)/TIOC3A (I/O)
PE3 (I/O)/TIOC0D (I/O)/SCK0 (I/O)
PE2 (I/O)/TIOC0C (I/O)/TXD0 (output)
PE1 (I/O)/TIOC0B (I/O)/RXD0 (input)
PE0 (I/O)/TIOC0A (I/O)

Figure 16.6 Port E (SH7124)

Port E port register L	PEPRL	R	—	H'FFFFD31E	8, 1

16.3.2 Port E Data Register L (PEDRL)

PEDRL is a 16-bit readable/writable register that stores port E data. Bits PE15DR to PE0 correspond to pins PE15 to PE0 (multiplexed functions omitted here) in the SH7125. Bits PE15DR to PE8DR and PE3DR to PE0DR correspond to pins PE15 to PE8 and PE3 to P respectively (multiplexed functions omitted here) in the SH7124.

When a pin function is general output, if a value is written to PEDRL, that value is outpu from the pin, and if PEDRL is read, the register value is returned directly regardless of th state.

When a pin function is general input, if PEDRL is read, the pin state, not the register valu returned directly. If a value is written to PEDRL, although that value is written into PEDI does not affect the pin state. Table 16.6 summarizes port E data register read/write operat

13	PE13DR	0	R/W
12	PE12DR	0	R/W
11	PE11DR	0	R/W
10	PE10DR	0	R/W
9	PE9DR	0	R/W
8	PE8DR	0	R/W
7	PE7DR	0	R/W
6	PE6DR	0	R/W
5	PE5DR	0	R/W
4	PE4DR	0	R/W
3	PE3DR	0	R/W
2	PE2DR	0	R/W
1	PE1DR	0	R/W
0	PE0DR	0	R/W

13	PE13DR	0	R/W	
12	PE12DR	0	R/W	
11	PE11DR	0	R/W	
10	PE10DR	0	R/W	
9	PE9DR	0	R/W	
8	PE8DR	0	R/W	
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
3	PE3DR	0	R/W	See table 16.6.
2	PE2DR	0	R/W	
1	PE1DR	0	R/W	
0	PE0DR	0	R/W	

Table 16.6 Port E Data Register L (PEDRL) Read/Write Operations

- PEDRL Bits 15 to 0

PEIOR	Pin Function	Read	Write
0	General input	Pin state	Can write to PEDRL, but it has no effect state
	Other than general input	Pin state	Can write to PEDRL, but it has no effect state
1	General output	PEDRL value	Value written is output from pin
	Other than general output	PEDRL value	Can write to PEDRL, but it has no effect state

R/W: R R R R R R R R R R R R R R

Bit	Bit Name	Initial Value	R/W	Description
15	PE15PR	Pin state	R	The pin state is returned regardless of the PF These bits cannot be modified.
14	PE14PR	Pin state	R	
13	PE13PR	Pin state	R	
12	PE12PR	Pin state	R	
11	PE11PR	Pin state	R	
10	PE10PR	Pin state	R	
9	PE9PR	Pin state	R	
8	PE8PR	Pin state	R	
7	PE7PR	Pin state	R	
6	PE6PR	Pin state	R	
5	PE5PR	Pin state	R	
4	PE4PR	Pin state	R	
3	PE3PR	Pin state	R	
2	PE2PR	Pin state	R	
1	PE1PR	Pin state	R	
0	PE0PR	Pin state	R	

13	PE13PR	Pin state	R	
12	PE12PR	Pin state	R	
11	PE11PR	Pin state	R	
10	PE10PR	Pin state	R	
9	PE9PR	Pin state	R	
8	PE8PR	Pin state	R	
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
3	PE3PR	Pin state	R	The pin state is returned regardless of the PFC These bits cannot be modified.
2	PE2PR	Pin state	R	
1	PE1PR	Pin state	R	
0	PE0PR	Pin state	R	

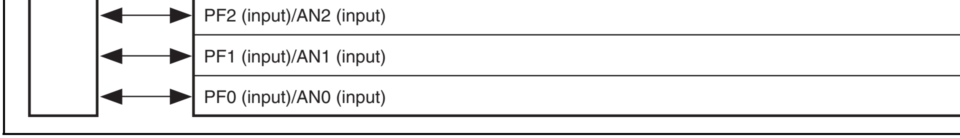


Figure 16.7 Port F (SH7125, SH7124)

16.4.1 Register Descriptions

Port F is an 8-bit input-only port in the SH7125 and SH7124. Port F has the following re
details on register addresses and register states during each processing, refer to section 2
Registers.

Table 16.7 Register Configuration

Register Name	Abbrevia-tion	R/W	Initial Value	Address	Ac
Port F data register L	PFDRL	R	—	H'FFFFD382	8,

- PFDRL (SH7125, SH7124)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	PF7 DR	PF6 DR	PF5 DR	PF4 DR	PF3 DR	PF2 DR
Initial value:	0	0	0	0	0	0	0	0	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
7	PF7DR	Pin state	R	See table 16.8.
6	PF6DR	Pin state	R	
5	PF5DR	Pin state	R	
4	PF4DR	Pin state	R	
3	PF3DR	Pin state	R	
2	PF2DR	Pin state	R	
1	PF1DR	Pin state	R	
0	PF0DR	Pin state	R	

Table 16.8 Port F Data Register L (PFDRL) Read/Write Operations

- PFDRL Bits 7 to 0

Pin Function	Read	Write
General input	Pin state	Ignored (no effect on pin state)
ANn input	1	Ignored (no effect on pin state)

SH71251A. SH71241A: 32 Kbytes

SH71250A. SH71240A: 16 Kbytes

- Two on-board programming modes and one off-board programming mode

  — On-board programming modes

  Boot Mode: This mode is a program mode that uses an on-chip SCI interface. The u can be programmed. This mode can automatically adjust the bit rate between the hos LSI.

  User Program Mode: The user MAT can be programmed by using an interface sele the user. This mode cannot be used on the 32 Kbyte and 16 Kbyte flash memory ver

  — Off-board programming mode

  This mode uses the dedicated socket adapter and PROM programmer. The user MA programmed.

- Programming/erasing interface by the download of on-chip program

  This LSI has a dedicated programming/erasing program. After downloading this pro the on-chip RAM, programming/erasing can be performed by setting the argument p The user branch is also supported.

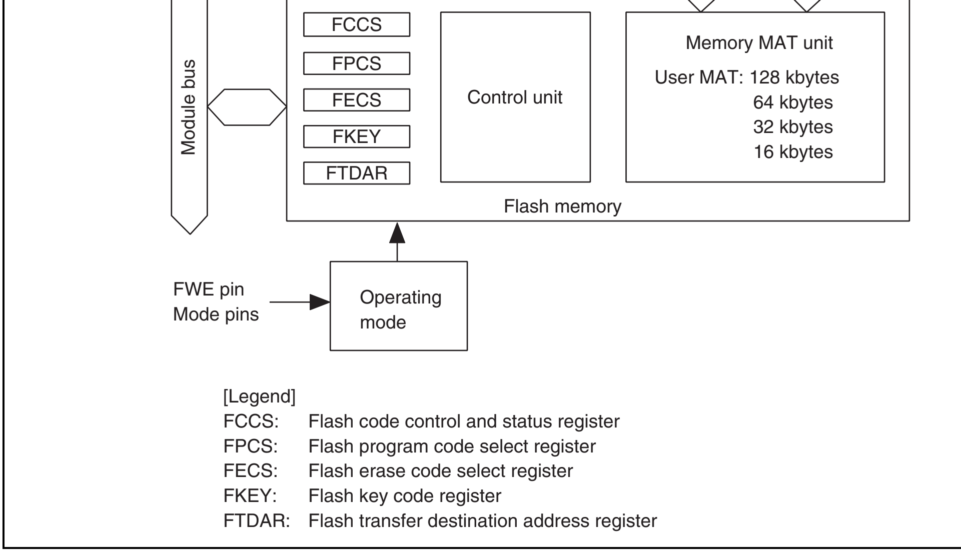
  — User branch

  The program processing is performed in 128-byte units. It consists the program puls application, verify read, and several other steps. Erasing is performed in one divided units and consists of several steps. The user processing routine can be executed betw steps, this setting for which is called the user branch addition.

- Protection modes

  There are two protection modes. Software protection by the register setting and hard protection by the FWE pin. The protection state for flash memory programming/eras set.

  When abnormalities, such as runaway of programming/erasing are detected, these m the error protection state and the programming/erasing processing is suspended.



[Legend]
FCCS: Flash code control and status register
FPCS: Flash program code select register
FECS: Flash erase code select register
FKEY: Flash key code register
FTDAR: Flash transfer destination address register

Figure 17.1 Block Diagram of Flash Memory

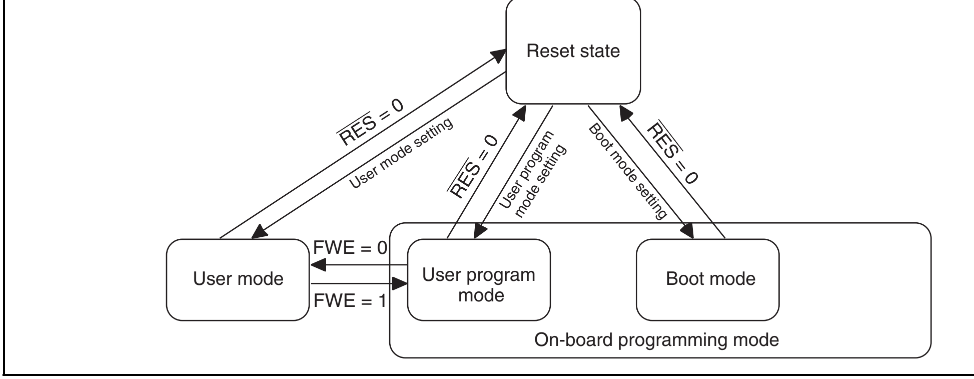


Figure 17.2 Mode Transition of Flash Memory

Table 17.1 Relationship between FWE and MD Pins and Operating Modes

Pin	Reset State	User Mode	User Program Mode	Boot Mode
$\overline{RES}$	0	1	1	1
FWE	0/1	0	1	1
MD1	0/1	1	1	0

Programming/ erasing control	Command method	Programming/erasing interface	—
All erasure	Possible (Automatic)	Possible	Possible (
Block division erasure	Possible*[1]	Possible	Impossible
Program data transfer	From host via SCI	From optional device via RAM	Via progra
User branch function	Not possible	Possible	Impossible
Reset initiation MAT	Embedded program storage MAT	User MAT	Embedded storage M
Transition to user mode	Mode setting change and reset	FWE setting change	—

Notes: 1. All-erasure is performed. After that, the specified block can be erased.
2. Cannot be used in 32-kbyte on-chip flash memory version.

- The user MAT is all erased in boot mode. Then, the user MAT can be programmed b of the command method. However, the contents of the MAT cannot be read until thi

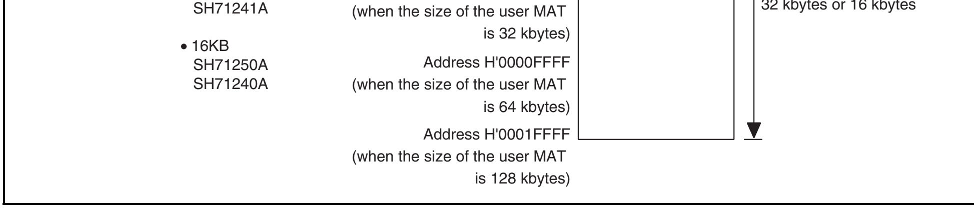


Figure 17.3 Flash Memory Configuration

17.2.5 Block Division

The user MAT is divided into 64 Kbytes (128-kbyte version: one block), 32 Kbytes (one
and 4 Kbytes (eight blocks) as shown in figure 17.4. The user MAT can be erased in this
block units and the erase-block number of EB0 to EB9 is specified when erasing. It is not
on the 32 Kbyte versions of the SH71251A and SH71241A or the 16 Kbyte versions of th
SH71250A and SH71240A.

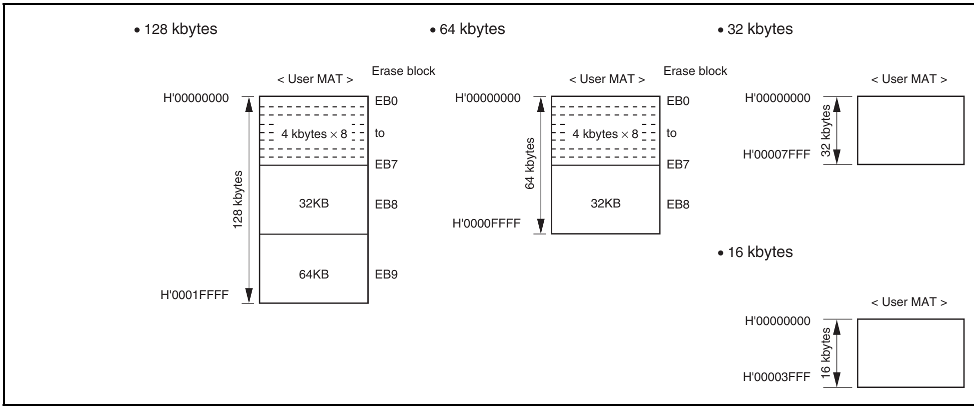


Figure 17.4 Block Division of User MAT

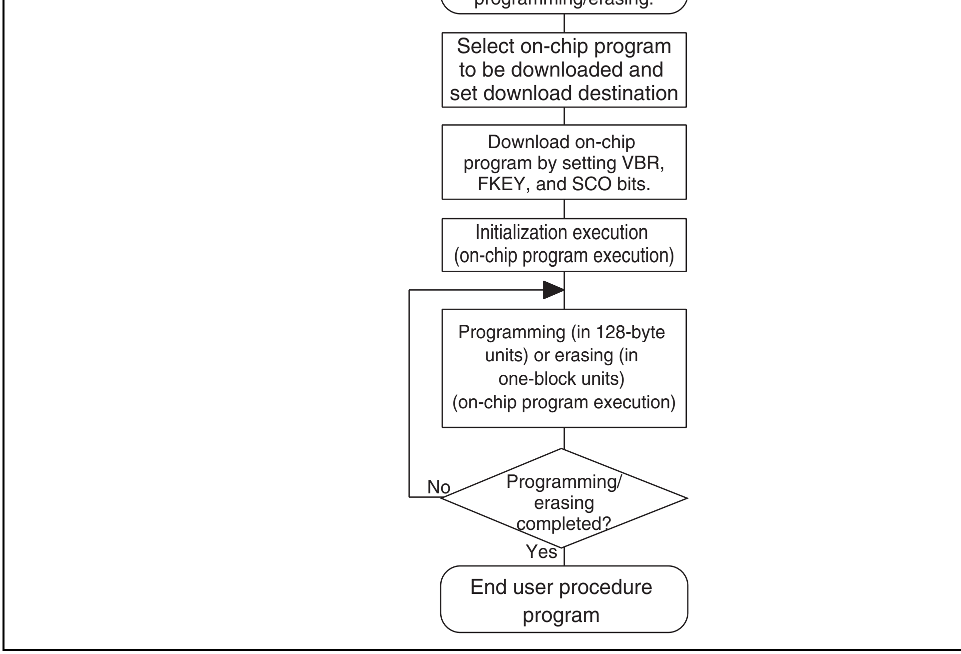

programming/erasing.
Select on-chip program to be downloaded and set download destination
Download on-chip program by setting VBR, FKEY, and SCO bits.
Initialization execution (on-chip program execution)
Programming (in 128-byte units) or erasing (in one-block units) (on-chip program execution)
Programming/ erasing completed?
No
Yes
End user procedure program

Figure 17.5 Overview of User Procedure Program

(1) Selection of On-Chip Program to be Downloaded and Setting of Download Destinat

This LSI has programming/erasing programs and they can be downloaded to the on-RAM. The on-chip program to be downloaded is selected by setting the correspondi the programming/erasing interface registers. The download destination can be specif FTDAR.

Note that VBR can be changed after download is completed.

(3) Initialization of Programming/Erasing

The operating frequency and user branch are set before execution of programming/era
The user branch destination must be in an area other than the user MAT area, which is
middle of programming and the area where the on-chip program is downloaded. Thes
are performed by using the programming/erasing interface parameters.

(4) Programming/Erasing Execution

To program or erase, the FWE pin must be brought high and user program mode must
entered.

The program data/programming destination address is specified in 128-byte units whe
programming.

The block to be erased is specified in erase-block units when erasing.

These specifications are set by using the programming/erasing interface parameters ar
chip program is initiated. The on-chip program is executed by using the JSR or BSR
instruction to perform the subroutine call of the specified address in the on-chip RAM
execution result is returned to the programming/erasing interface parameters.

The area to be programmed must be erased in advance when programming flash mem

There are limitations and notes on the interrupt processing during programming/erasin
details, see section 17.7.1, Interrupts during Programming/Erasing.

(5) When Programming/Erasing is Executed Consecutively

When the processing is not ended by the 128-byte programming or one-block erasure,
program address/data and erase-block number must be updated and consecutive
programming/erasing is required.

Since the downloaded on-chip program is left in the on-chip RAM after the processin
download and initialization are not required when the same processing is executed
consecutively.

Transmit data	TXD1 (PA4)	Output	Serial transmit data output (u boot mode)
Receive data	RXD1 (PA3)	Input	Serial receive data input (use mode)

17.4 Register Descriptions

17.4.1 Registers

The registers/parameters, which control flash memory when the on-chip flash memory i shown in table 17.4.

There are several operating modes for accessing flash memory, for example, read mode/ mode. The correspondence of operating modes and registers/parameters for use is show 17.5.

Notes: 1. The bits except the SCO bit are read-only bits. The SCO bit is a programming-
(The value, which can be read is always 0.)

2. The initial value of the FWE bit is 0 when the FWE pin goes low.
The initial value of the FWE bit is 1 when the FWE pin goes high.

3. All registers can be accessed only in bytes.

Table 17.4 (2) Parameter Configuration

Name	Abbreviation	R/W	Initial Value	Address	Ac Si
Download pass/fail result	DPFR	R/W	Undefined	On-chip RAM*	8,
Flash pass/fail result	FPFR	R/W	Undefined	R0 of CPU	8,
Flash multipurpose address area	FMPAR	R/W	Undefined	R5 of CPU	8,
Flash multipurpose data destination area	FMPDR	R/W	Undefined	R4 of CPU	8,
Flash erase block select	FEBS	R/W	Undefined	R4 of CPU	8,
Flash program and erase frequency control	FPEFEQ	R/W	Undefined	R4 of CPU	8,
Flash user branch address set parameter	FUBRA	R/W	Undefined	R5 of CPU	8,

Note: * One byte of the start address in the on-chip RAM area specified by FTDAR is v

erasing interface parameters	FPFR	—	√	√	√	—
	FPEFEQ	—	√	—	—	—
	FUBRA	—	√	—	—	—
	FMPAR	—	—	√	—	—
	FMPDR	—	—	√	—	—
	FEBS	—	—	—	√	—

	FWE	-	-	FLER	-	-	-	SCO
Initial value:	1/0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	(R)/W

Bit	Bit Name	Initial Value	R/W	Description
7	FWE	1/0	R	Flash Programming Enable Monitors the level which is input to the FWE pi performs hardware protection of the flash mem programming or erasing. The initial value is 0 c according to the FWE pin state. 0: When the FWE pin goes low (in hardware pr state) 1: When the FWE pin goes high
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.

				0: Flash memory operates normally Programming/erasing protection for flash m (error protection) is invalid. [Clearing condition] At a power-on reset 1: Indicates an error occurs during programming/erasing flash memory. Programming/erasing protection for flash m (error protection) is valid. [Setting condition] See section 17.6.3, Error Protection.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.

after setting this bit to 1.

For interrupts during download, see section 17
Interrupts during Programming/Erasing. For th
download time, see section 17.7.2, Other Note

Since this bit is cleared to 0 when download is
completed, this bit cannot be read as 1.

Download by setting the SCO bit to 1 requires
interrupt processing that performs bank switch
on-chip program storage area. Therefore, befo
issuing a download request (SCO = 1), set VB
H'84000000. Otherwise, the CPU gets out of c
Once download end is confirmed, VBR can be
to any other value.

The mode in which the FWE pin is high must b
when using the SCO function.

0: Download of the on-chip programming/erasi
program to the on-chip RAM is not execute

[Clearing condition]

When download is completed

1: Request that the on-chip programming/erasi
program is downloaded to the on-chip RAM
generated

[Setting conditions]

When all of the following conditions are satisfie
is written to this bit

- FKEY is written to H'A5
- During execution in the on-chip RAM

				These bits are always read as 0. The write va always be 0.
0	PPVS	0	R/W	Program Pulse Single Selects the programming program. 0: On-chip programming program is not selec [Clearing condition] When transfer is completed 1: On-chip programming program is selected

(3) Flash Erase Code Select Register (FECS)

FECS selects download of the on-chip erasing program.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	EPVB
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.

([illegible]) Flash Key Code Register (FKEY)

FKEY is a register for software protection that enables download of the on-chip progr
programming/erasing of flash memory. Before setting the SCO bit to 1 in order to dow
the on-chip program or executing the downloaded programming/erasing program, the
processings cannot be executed if the key code is not written.

Bit:	7	6	5	4	3	2	1	0
	K[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	K[7:0]	All 0	R/W	Key Code Only when H'A5 is written, writing to the SCO b valid. When a value other than H'A5 is written t 1 cannot be written to the SCO bit. Therefore downloading to the on-chip RAM cannot be exe Only when H'5A is written, programming/erasin flash memory can be executed. Even if the on- programming/erasing program is executed, flas memory cannot be programmed or erased whe value other than H'5A is written to FKEY. H'A5: Writing to the SCO bit is enabled (The S cannot be set by a value other than H'A5 H'5A: Programming/erasing is enabled (A valu than H'5A enables software protection st H'00: Initial value

7	TDER	0	R/W	Transfer Destination Address Setting Error This bit is set to 1 when there is an error in th download start address set by bits 6 to 0 (TD TDA0). Whether the address setting is errone is tested by checking whether the setting of T TDA0 is between the range of H'02 to H'04 af the SCO bit in FCCS to 1 and performing dov Before setting the SCO bit to 1 be sure to set FTDAR value between H'02 to H'04 as well a this bit to 0. 0: Setting of TDA6 to TDA0 is normal 1: Setting of TDER and TDA6 to TDA0 is H'0 and H'05 to H'FF and download has been a

H'04: Download start address is set to H'FFFFI

H'00, H'01, H'05 to H'7F: Setting prohibited wh
downloading by the S
with user program mo
this value is set, the T
(bit 7) is set to 1 to ab
download processing
not using user progra
setting H'00 to the TD
problem.

17.4.3 Programming/Erasing Interface Parameters

The programming/erasing interface parameters specify the operating frequency, user bran
destination address, storage place for program data, programming destination address, an
block and exchanges the processing result for the downloaded on-chip program. This para
uses the general registers of the CPU (R4, R5, and R0) or the on-chip RAM area. The init
is undefined.

At download all CPU registers are stored, and at initialization or when the on-chip progra
executed, CPU registers except for R0 are stored. The return value of the processing resul
written in R0. Since the stack area is used for storing the registers or as a work area, the s
must be saved at the processing start. (The maximum size of a stack area to be used is 12

each processing.

Table 17.6 Usable Parameters and Target Modes

Name of Parameter	Abbrevia-tion	Down-load	Initiali-zation	Pro-gram-ming	Erasure	R/W	Initial Value	A
Download pass/fail result	DPFR	√	—	—	—	R/W	Undefined	C F
Flash pass/fail result	FPFR	—	√	√	√	R/W	Undefined	F
Flash programming/ erasing frequency control	FPEFEQ	—	√	—	—	R/W	Undefined	F
Flash user branch address set	FUBRA	—	√	—	—	R/W	Undefined	F
Flash multipurpose address area	FMPAR	—	—	√	—	R/W	Undefined	F
Flash multipurpose data destination area	FMPDR	—	—	√	—	R/W	Undefined	F
Flash erase block select	FEBS	—	—	—	√	R/W	Undefined	F

Note: * One byte of start address of download destination specified by FTDAR confirmation whether the SCO bit is set to 1 is difficult, the certain determination performed by setting one byte of the start address of the on-chip RAM area specif FTDAR to a value other than the return value of download (for example, H'FF) be download start (before setting the SCO bit to 1). For the checking method of down results, see section 17.5.2 (2), Programming Procedure in User Program Mode.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	SS	FK	SF
Initial value:	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	Undefined	R/W	Unused Return 0.
2	SS	Undefined	R/W	Source Select Error Detect The on-chip program which can be downloade specified as only one type. When more than tw of the program are selected, the program is no selected, or the program is selected without ma an error occurs. 0: Download program can be selected normally 1: Download error occurs (Multi-selection or pr which is not mapped is selected)

normally or not.

0: Downloading on-chip program has ended r
(no error)

1: Downloading on-chip program has ended a
(error occurs)

(2) Programming/Erasing Initialization

The on-chip programming/erasing program to be downloaded includes the initializat program.

The specified period pulse must be applied when programming or erasing. The speci width is made by the method in which wait loop is configured by the CPU instructio operating frequency of the CPU must be set. Since the user branch function is suppo user branch destination address must be set.

The initial program is set as a parameter of the programming/erasing program which downloaded these settings.

(2.1) Flash programming/erasing frequency parameter (FPEFEQ: general register R4 of

This parameter sets the operating frequency of the CPU.

For the range of the operating frequency of this LSI, see section 21.3.1, Clock Timin

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

2. The centuplicated value is converted to the b
digit and is written to the FPEFEQ paramete
(general register R4). For example, when th
operating frequency of the CPU is 28.882 M
value is as follows.

    — The number to three decimal places of
rounded and the value is thus 28.88.

    — The formula that 28.88 × 100 = 2888 is
converted to the binary digit and B'0000
B'0100, B'1000 (H'0B48) is set to R4.

(2.2) Flash user branch address setting parameter (FUBRA: general register R5 of CPU)

This parameter sets the user branch destination address. The user program which has b
can be executed in specified processing units when programming and erasing.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	UA31	UA30	UA29	UA28	UA27	UA26	UA25	UA24	UA23	UA22	UA21	UA20	UA19	UA18
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	UA15	UA14	UA13	UA12	UA11	UA10	UA9	UA8	UA7	UA6	UA5	UA4	UA3	UA2
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

program download area and stack area must
overwritten. If CPU runaway occurs or the do
area or stack area is overwritten, the value of
memory cannot be guaranteed.

The download of the on-chip program, initializ
initiation of the programming/erasing program
be executed in the processing of the user bra
destination. Programming or erasing cannot b
guaranteed when returning from the user bra
destination. The program data which has alre
prepared must not be programmed.

Store general registers R8 to R15. General re
to R7 are available without storing them.

Moreover, the programming/erasing interface
must not be written to in the processing of the
branch destination.

After the processing of the user branch has e
programming/erasing program must be return
using the RTS instruction.

For the execution intervals of the user branch
processing, see note 2 (User Branch Process
Intervals) in section 17.7.2, Other Notes.

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	Undefined	R/W	Unused Return 0.
2	BR	Undefined	R/W	User Branch Error Detect Returns the check result whether the specified branch destination address is in the area other storage area of the programming/erasing progr which has been downloaded. 0: User branch address setting is normal 1: User branch address setting is abnormal
1	FQ	Undefined	R/W	Frequency Error Detect Returns the check result whether the specified operating frequency of the CPU is in the range supported operating frequency. 0: Setting of operating frequency is normal 1: Setting of operating frequency is abnormal
0	SF	Undefined	R/W	Success/Fail Indicates whether initialization is completed no 0: Initialization has ended normally (no error) 1: Initialization has ended abnormally (error oc

data must be in the consecutive space which can be accessed by using the MOV.
instruction of the CPU and is not the flash memory space.

When data to be programmed does not satisfy 128 bytes, the 128-byte program d
be prepared by embedding the dummy code (H'FF).

The start address of the area in which the prepared program data is stored must b
general register R4. This parameter is called FMPDR (flash multipurpose data de
area parameter).

For details on the programming procedure, see section 17.5.2, User Program Mo
in On-Chip 128-Kbyte and 64-Kbyte ROM Version).

(3.1) Flash multipurpose address area parameter (FMPAR: general register R5 of CPU)

This parameter indicates the start address of the programming destination on the use

When an address in an area other than the flash memory space is set, an error occurs

The start address of the programming destination must be at the 128-byte boundary.
boundary condition is not satisfied, an error occurs. The error occurrence is indicate
WA bit (bit 1) in FPFR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	MOA31	MOA30	MOA29	MOA28	MOA27	MOA26	MOA25	MOA24	MOA23	MOA22	MOA21	MOA20	MOA19	MOA18
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	MOA15	MOA14	MOA13	MOA12	MOA11	MOA10	MOA9	MOA8	MOA7	MOA6	MOA5	MOA4	MOA3	MOA2
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This parameter indicates the start address in the area which stores the data to be progr
in the user MAT. When the storage destination of the program data is in flash memor
error occurs. The error occurrence is indicated by the WD bit (bit 2) in FPFR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	MOD31	MOD30	MOD29	MOD28	MOD27	MOD26	MOD25	MOD24	MOD23	MOD22	MOD21	MOD20	MOD19	MOD18
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	MOD15	MOD14	MOD13	MOD12	MOD11	MOD10	MOD9	MOD8	MOD7	MOD6	MOD5	MOD4	MOD3	MOD2
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MOD31 to MOD0	Undefined	R/W	MOD31 to MOD0 Store the start address of the area which store program data for the user MAT. The consecuti byte data is programmed to the user MAT star the specified start address.

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	Undefined	R/W	Unused Return 0.
6	MD	Undefined	R/W	Programming Mode Related Setting Error De Returns the check result of whether the signa the FWE pin is high and whether the error pro state is not entered. When a low-level signal is input to the FWE p error protection state is entered, 1 is written t The input level to the FWE pin and the error p state can be confirmed with the FWE bit (bit 7 FLER bit (bit 4) in FCCS, respectively. For co enter the error protection state, see section 1 Error Protection. 0: FWE and FLER settings are normal (FWE = 0) 1: FWE = 0 or FLER = 1, and programming ca performed

				0: Programming has ended normally 1: Programming has ended abnormally (progra result is not guaranteed)
4	FK	Undefined	R/W	Flash Key Register Error Detect Returns the check result of the value of FKEY the start of the programming processing. 0: FKEY setting is normal (FKEY = H'5A) 1: FKEY setting is error (FKEY = value other th
3	—	Undefined	R/W	Unused Return 0.
2	WD	Undefined	R/W	Write Data Address Error Detect When an address in the flash memory area is s as the start address of the storage destination program data, an error occurs. 0: Setting of write data address is normal 1: Setting of write data address is abnormal
1	WA	Undefined	R/W	Write Address Error Detect When the following items are specified as the s address of the programming destination, an er occurs. • The programming destination address is ar other than flash memory • The specified address is not at the 128-byt boundary (A6 to A0 are not 0) 0: Setting of programming destination address 1: Setting of programming destination address abnormal

erasing program which is downloaded. This is set to the FEBS parameter (general re

One block is specified from the block number 0 to 15.

For details on the erasing procedure, see section 17.5.2, User Program Mode (Only i 128-Kbyte and 64-Kbyte ROM Version).

(4.1) Flash erase block select parameter (FEBS: general register R4 of CPU)

This parameter specifies the erase-block number. Several block numbers cannot be s

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	EBS[7:0]					
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Set the erase block number in the range fr
0 corresponds to the EB0 block and 8 corre
to the EB8 block. An error occurs when a n
other than 0 to 8 (H'00 to H'08) is set.

(4.2) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter returns the value of the erasing processing result.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18
	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2
	-	-	-	-	-	-	-	-	-	MD	EE	FK	EB	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	Undefined	R/W	Unused Return 0.

				enter the error protection state, see section Error Protection. 0: FWE and FLER settings are normal (FWE = 0) 1: FWE = 0 or FLER = 1, and erasure cannot performed
5	EE	Undefined	R/W	Erasure Execution Error Detect 1 is returned to this bit when the user MAT co erased or when flash-memory related register are partially changed on returning from the us processing. If this bit is set to 1, there is a high possibility user MAT is partially erased. In this case, afte removing the error factor, erase the user MAT 0: Erasure has ended normally 1: Erasure has ended abnormally (erasure res guaranteed)
4	FK	Undefined	R/W	Flash Key Register Error Detect Returns the check result of FKEY value befor the erasing processing. 0: FKEY setting is normal (FKEY = H'5A) 1: FKEY setting is error (FKEY = value other
3	EB	Undefined	R/W	Erase Block Select Error Detect Returns the check result whether the specifie block number is in the block range of the user 0: Setting of erase-block number is normal 1: Setting of erase-block number is abnormal

Boot mode executes programming/erasing user MAT by means of the control command program data transmitted from the host using the on-chip SCI. The tool for transmitting command and program data must be prepared in the host. The SCI communication mode asynchronous mode. When reset start is executed after this LSI's pin is set in boot mode program in the microcomputer is initiated. After the SCI bit rate is automatically adjuste communication with the host is executed by means of the control command method.

The system configuration diagram in boot mode is shown in figure 17.6. For details on t setting in boot mode, see table 17.1. Although NMI and other interrupts are ignored in b do not generate them.

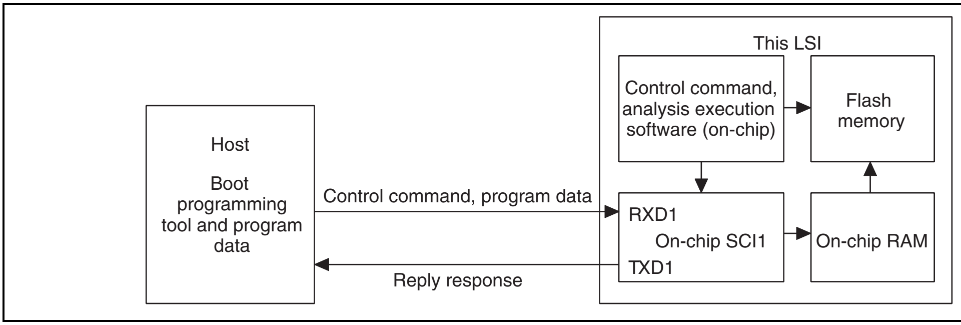

This LSI
Control command, analysis execution software (on-chip)
Flash memory
Host
Boot programming tool and program data
Control command, program data
RXD1
On-chip SCI1
TXD1
On-chip RAM
Reply response

Figure 17.6 System Configuration in Boot Mode

bps.

The system clock frequency, which can automatically adjust the transfer bit rate of th
the bit rate of this LSI is shown in table 17.7. Boot mode must be initiated in the rang
system clock. Note that the internal clock division ratio of ×1/3 is not supported in bo

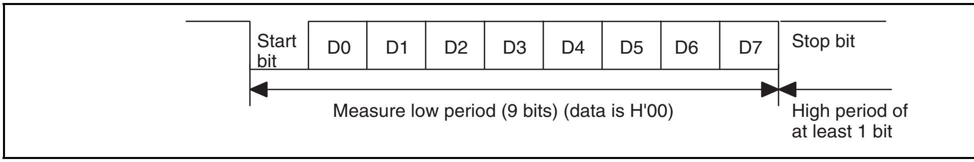

Start bit
D0
D1
D2
D3
D4
D5
D6
D7
Stop bit
Measure low period (9 bits) (data is H'00)
High period of at least 1 bit

Figure 17.7 Automatic Adjustment Operation of SCI Bit Rate

Table 17.7 Peripheral Clock (Pϕ) Frequency that Can Automatically Adjust Bit Ra This LSI

Host Bit Rate	Peripheral Clock (Pϕ) Frequency Which Can Automatically Adjust Bit Rate
9,600 bps	20 to 25 MHz
19,200 bps	20 to 25 MHz

Note: The internal clock division ratio of ×1/3 is not supported in boot mode.

supported devices, etc.

3. Automatic erasure of the entire user MAT

   After all necessary inquiries and selections have been made and the command fo
   to the programming/erasure state is sent by the host, the entire user MAT is autor
   erased.

4. Waiting for programming/erasure command

— On receiving the programming selection command, the chip waits for data to be programmed. To program data, the host transmits the programming command co followed by the address where programming should start and the data to be progr This is repeated as required while the chip is in the programming-selected state. terminate programming, H'FFFFFFFF should be transmitted as the first address c for programming. This makes the chip return to the programming/erasure comma waiting state from the programming data waiting state.

— On receiving the erasure select command, the chip waits for the block number of be erased. To erase a block, the host transmits the erasure command code follow number of the block to be erased. This is repeated as required while the chip is in erasure-selected state. To terminate erasure, H'FF should be transmitted as the bl number. This makes the chip return to the programming/erasure command waitin from the erasure block number waiting state. Erasure should only be executed wh specific block is to be reprogrammed without executing a reset-start of the chip a flash memory has been programmed in boot mode. If all desired programming is single operation, such erasure processing is not necessary because all blocks are before the chip enters the programming/erasure/other command waiting state.

— In addition to the programming and erasure commands, commands for sum chec blank checking (checking for erasure) of the user MAT, reading data from the us and acquiring current state information are provided.

Note that the command for reading from the user MAT can only read data that has been programmed after automatic erasure of the entire user MAT.

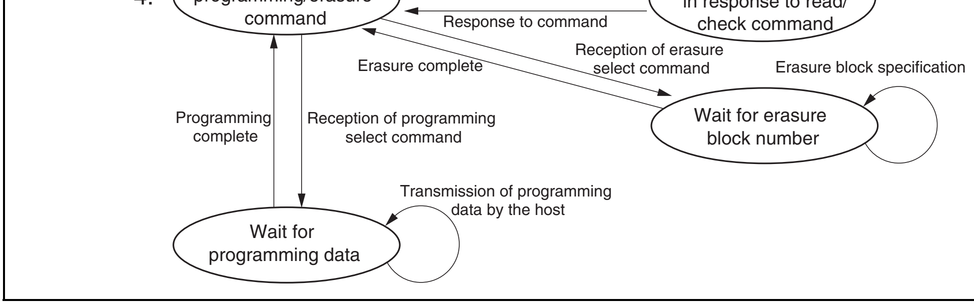


Figure 17.8 State Transitions in Boot Mode

period, which is longer than the normal 100 μs.

For details on the programming procedure, see the description in section 17.5.2 (2), Prog Procedure in User Program Mode. For details on the erasing procedure, see the descripti section 17.5.2 (3), Erasing Procedure in User Program Mode.

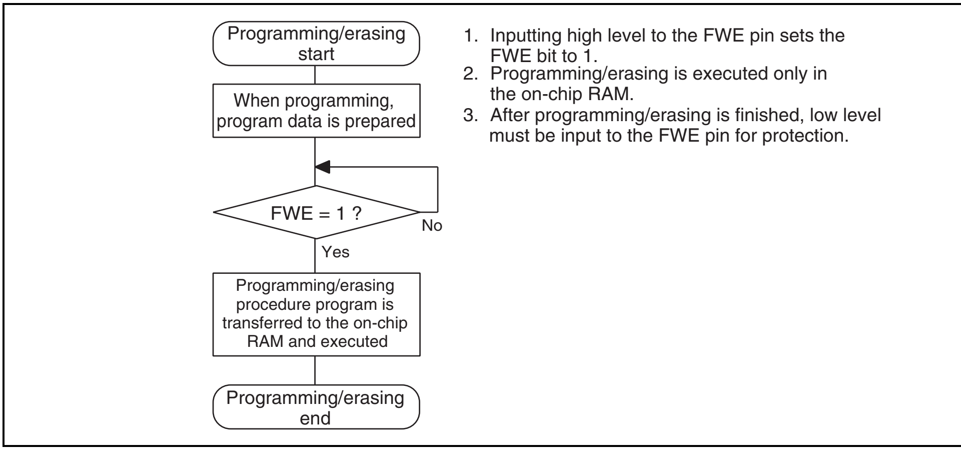

Programming/erasing start
When programming, program data is prepared
FWE = 1 ?
No
Yes
Programming/erasing procedure program is transferred to the on-chip RAM and executed
Programming/erasing end
1. Inputting high level to the FWE pin sets the FWE bit to 1.
2. Programming/erasing is executed only in the on-chip RAM.
3. After programming/erasing is finished, low level must be input to the FWE pin for protection.

Figure 17.9 Programming/Erasing Overview Flow

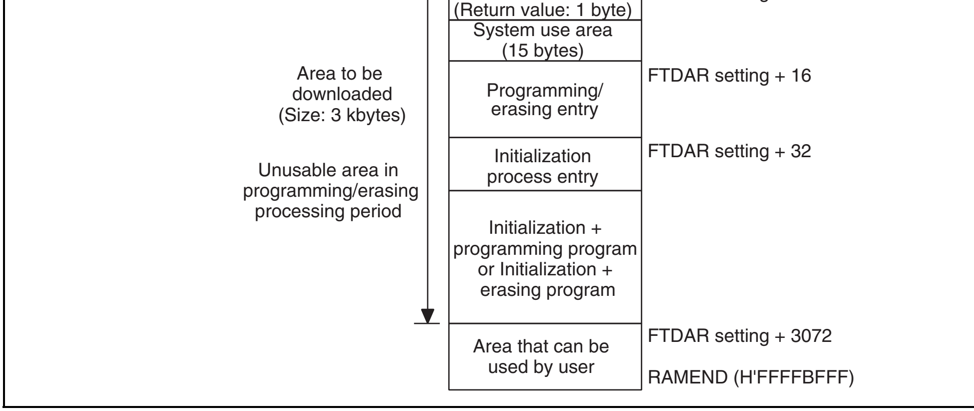

(Return value: 1 byte)
System use area (15 bytes)
FTDAR setting + 16
Area to be downloaded (Size: 3 kbytes)
Programming/ erasing entry
Unusable area in programming/erasing processing period
Initialization process entry
FTDAR setting + 32
Initialization + programming program or Initialization + erasing program
FTDAR setting + 3072
Area that can be used by user
RAMEND (H'FFFFBFFF)

Figure 17.10 RAM Map after Download

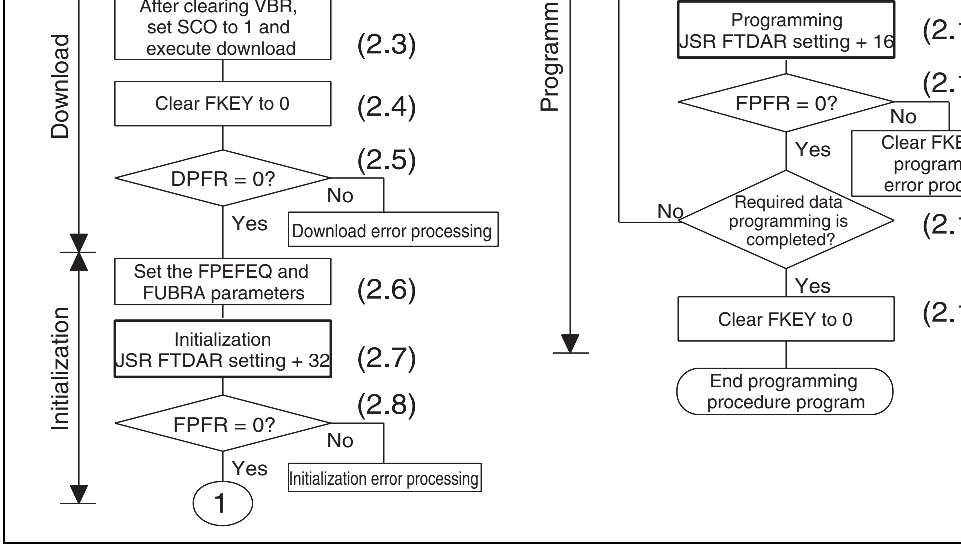

Download
After clearing VBR, set SCO to 1 and execute download
(2.3)
Clear FKEY to 0
(2.4)
DPFR = 0?
(2.5)
No
Yes
Download error processing
Initialization
Set the FPEFEQ and FUBRA parameters
(2.6)
Initialization JSR FTDAR setting + 32
(2.7)
FPFR = 0?
(2.8)
No
Yes
Initialization error processing
1
Programm
Programming JSR FTDAR setting + 16
(2.
(2.
FPFR = 0?
No
Yes
Clear FKE program error proc
No
Required data programming is completed?
(2.
Yes
Clear FKEY to 0
(2.
End programming procedure program

Figure 17.11 Programming Procedure

The details of the programming procedure are described below. The procedure progr be executed in an area other than the flash memory to be programmed. Especially the where the SCO bit in FCCS is set to 1 for downloading must be executed in the on-c

Specify 1/4 (initial value) as the frequency division ratios of an internal clock (Iϕ), a (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

After the programming/erasing program has been downloaded and the SCO bit is cle the setting of the frequency control register (FRQCR) can be changed to the desired following description assumes the area to be programmed on the user MAT is erased program data is prepared in the consecutive area. When erasing has not been execute out erasing before writing.

detect (SS) bit in the DPFR parameter.

Specify the start address of the download destination by FTDAR.

(2.2) Write H'A5 in FKEY

If H'A5 is not written to FKEY for protection, 1 cannot be written to the SCO bit for a download request.

(2.3) VBR is set to 0 and 1 is written to the SCO bit of FCCS, and then download is exec

VBR must always be set to H'84000000 before setting the SCO bit to 1.

To write 1 to the SCO bit, the following conditions must be satisfied.

- H'A5 is written to FKEY.
- The SCO bit writing is executed in the on-chip RAM.

When the SCO bit is set to 1, download is started automatically. When execution retu user procedure program, the SCO bit is cleared to 0. Therefore, the SCO bit cannot be confirmed to be 1 in the user procedure program.

The download result can be confirmed only by the return value of the DPFR paramete the SCO bit is set to 1, incorrect decision must be prevented by setting the DPFR para that is one byte of the start address of the on-chip RAM area specified by FTDAR, to other than the return value (H'FF).

When download is executed, particular interrupt processing, which is accompanied by switch as described below, is performed as an internal microcomputer processing, so need to be set to H'84000000. Four NOP instructions are executed immediately after t instructions that set the SCO bit to 1.

- The user MAT space is switched to the on-chip program storage area.
- After the selection condition of the download program and the address set in F are checked, the transfer processing is executed starting to the on-chip RAM a specified by FTDAR.
- The SCO bits in FCCS, FPCS, and FECS are cleared to 0.
- The return value is set to the DPFR parameter.

before setting the SCO bit to 1.

(2.4) FKEY is cleared to H'00 for protection.

(2.5) The value of the DPFR parameter must be checked to confirm the download result

A recommended procedure for confirming the download result is shown below.

- Check the value of the DPFR parameter (one byte of start address of the dow destination specified by FTDAR). If the value is H'00, download has been pe normally. If the value is not H'00, the source that caused download to fail can investigated by the description below.
- If the value of the DPFR parameter is the same as before downloading (e.g. H address setting of the download destination in FTDAR may be abnormal. In t confirm the setting of the TDER bit (bit 7) in FTDAR.
- If the value of the DPFR parameter is different from before downloading, che bit (bit 2) and the FK bit (bit 1) in the DPFR parameter to ensure that the dow program selection and FKEY register setting were normal, respectively.

(2.6) The operating frequency is set to the FPEFEQ parameter and the user branch destin set to the FUBRA parameter for initialization.

- The current frequency of the CPU clock is set to the FPEFEQ parameter (gen register R4). For the settable range of the FPEFEQ parameter, see section 21. Timing.
  When the frequency is set out of this range, an error is returned to the FPFR p of the initialization program and initialization is not performed. For details on frequency setting, see the description in section 17.4.3 (2.1), Flash programming/erasing frequency parameter (FPEFEQ: general register R4 of

When a programming program is downloaded, the initialization program is also down
on-chip RAM. There is an entry point of the initialization program in the area from (d
start address set by FTDAR) + 32 bytes. The subroutine is called and initialization is
by using the following steps.

```
MOV.L  #DLTOP+32,R1         ; Set entry address to R1
JSR    @R1                  ; Call initialization routine
NOP
```

- The general registers other than R0 are saved in the initialization program.
- R0 is a return value of the FPFR parameter.
- Since the stack area is used in the initialization program, a stack area of maxim
  bytes must be reserved in RAM.
- Interrupts can be accepted during the execution of the initialization program. H
  the program storage area and stack area in on-chip RAM and register values m
  be destroyed.

(2.8) The return value of the initialization program, FPFR (general register R0) is checke

(2.9) FKEY must be set to H'5A and the user MAT must be prepared for programming.

(2.10) The parameter which is required for programming is set.

The start address of the programming destination of the user MAT (FMPAR) is set to
register R5. The start address of the program data storage area (FMPDR) is set to gene
register R4.

- FMPAR setting

  FMPAR specifies the programming destination start address. When an address
  than one in the user MAT area is specified, even if the programming program
  executed, programming is not executed and an error is returned to the return va

executed by using the following steps.

```
MOV.L  #DLTOP+16,R1        ; Set entry address to R1
JSR    @R1                 ; Call programming routine
NOP
```

— The general registers other than R0 are saved in the programming program.

— R0 is a return value of the FPFR parameter.

— Since the stack area is used in the programming program, a stack area of maximu bytes must be reserved in RAM.

(2.12) The return value in the programming program, FPFR (general register R0) is chec

(2.13) Determine whether programming of the necessary data has finished.

If more than 128 bytes of data are to be programmed, specify FMPAR and FMPDR byte units, and repeat steps (2.10) to (2.13). Increment the programming destination 128 bytes and update the programming data pointer correctly. If an address which ha been programmed is written to again, not only will a programming error occur, but a memory will be damaged.

(2.14) After programming finishes, clear FKEY and specify software protection.

If this LSI is restarted by a power-on reset immediately after user MAT programmin finished, secure a reset period (period of $\overline{\text{RES}}$ = 0) that is at least as long as the norm

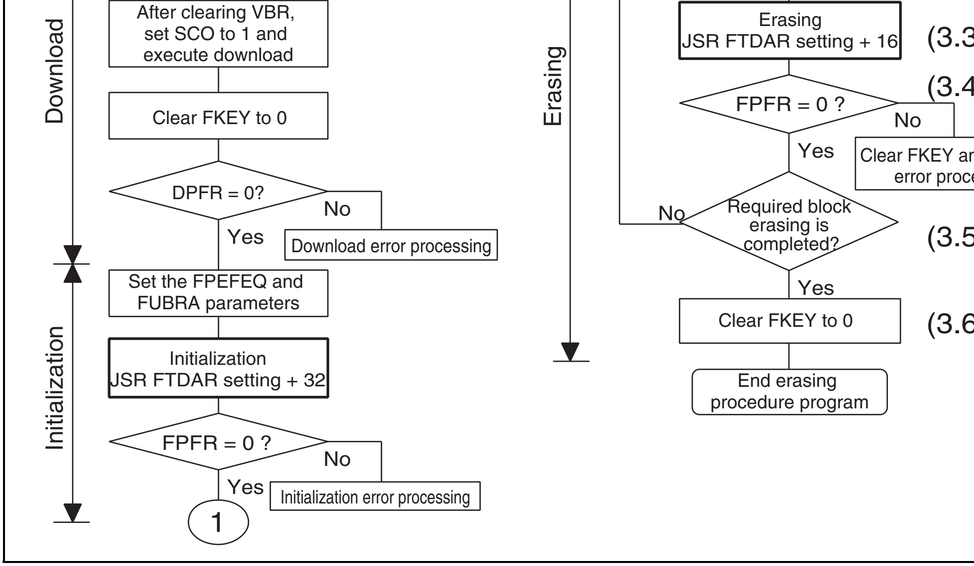

Download
After clearing VBR, set SCO to 1 and execute download
Clear FKEY to 0
DPFR = 0?
No
Yes
Download error processing
Set the FPEFEQ and FUBRA parameters
Initialization
Initialization JSR FTDAR setting + 32
FPFR = 0 ?
No
Yes
Initialization error processing
1
Erasing
Erasing JSR FTDAR setting + 16
(3.3
(3.4
FPFR = 0 ?
No
Yes
Clear FKEY ar error proce
No
Required block erasing is completed?
(3.5
Yes
Clear FKEY to 0
(3.6
End erasing procedure program

Figure 17.12 Erasing Procedure

The details of the erasing procedure are described below. The procedure program mus executed in an area other than the user MAT to be erased.

Especially the part where the SCO bit in FCCS is set to 1 for downloading must be ex on-chip RAM.

Specify 1/4 (initial value) as the frequency division ratios of an internal clock (Iϕ), a b (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

After the programming/erasing program has been downloaded and the SCO bit is clea the setting of the frequency control register (FRQCR) can be changed to the desired v the downloaded on-chip program area, see the RAM map for programming/erasing in 17.10.

same as those in the programming procedure. For details, see the description in secti
(2), Programming Procedure in User Program Mode.

(3.2) Set the FEBS parameter necessary for erasure

Set the erase block number of the user MAT in the flash erase block select paramete
general register R4). If a value other than an erase block number of the user MAT is
block is erased even though the erasing program is executed, and an error is returned
return value parameter FPFR.

(3.3) Erasure

Similar to as in programming, there is an entry point of the erasing program in the ar
(download start address set by FTDAR) + 16 bytes of on-chip RAM. The subroutine
and erasing is executed by using the following steps.

```
MOV.L  #DLTOP+16,R1        ; Set entry address to R1
JSR    @R1                 ; Call erasing routine
NOP
```

- The general registers other than R0 are saved in the erasing program.
- R0 is a return value of the FPFR parameter.
- Since the stack area is used in the erasing program, a stack area of maximum 12
  must be reserved in RAM.

(3.4) The return value in the erasing program, FPFR (general register R0) is checked.

(3.5) Determine whether erasure of the necessary blocks has finished.

If more than one block is to be erased, update the FEBS parameter and repeat steps (
(3.5). Blocks that have already been erased can be erased again.

(3.6) After erasure finishes, clear FKEY and specify software protection.

If this LSI is restarted by a power-on reset immediately after user MAT erasing has f
secure a reset period (period of $\overline{\text{RES}}$ = 0) that is at least as long as the normal 100 µs

or erase locations in a user MAT, and the error in programming/erasing is reported in the parameter.

Table 17.8 Hardware Protection

		Function to be Pro	
Item	**Description**	**Download**	**Progr Erasu**
FWE-pin protection	The input of a low-level signal on the FWE pin clears the FWE bit of FCCS and the LSI enters a programming/erasing-protected state.	—	√
Reset/standby protection	• A power-on reset (including a power-on reset by the WDT) and entry to standby mode initializes the programming/erasing interface registers and the LSI enters a programming/erasing-protected state. • Resetting by means of the $\overline{\text{RES}}$ pin after power is initially supplied will not make the LSI enter the reset state unless the $\overline{\text{RES}}$ pin is held low until oscillation has stabilized. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width that is specified in the section on AC characteristics. If the LSI is reset during programming or erasure, data in the flash memory is not guaranteed. In this case, execute erasure and then execute programming again.	√	√

SCO bit	downloading of the programming/erasing program, thus making the LSI enter a programming/erasing-protected state.		
Protection by FKEY	Downloading and programming/erasing are disabled unless the required key code is written in FKEY. Different key codes are used for downloading and for programming/erasing.	√	√

17.6.3 Error Protection

Error protection is a mechanism for aborting programming or erasure when an error occ form of the microcomputer getting out of control during programming/erasing of the fla memory or operations that are not in accordance with the established procedures for programming/erasing. Aborting programming or erasure in such cases prevents damage flash memory due to excessive programming or erasing.

If the microcomputer malfunctions during programming/erasing of the flash memory, th bit in FCCS is set to 1 and the LSI enters the error protection state, thus aborting progra erasure.

The FLER bit is set to 1 in the following conditions:

- When the relevant bank area of flash memory is read during programming/erasing (i vector read or an instruction fetch)
- When a SLEEP instruction (including software standby mode) is executed during programming/erasing

Error protection is cancelled (FLER bit is cleared) only by a power-on reset.

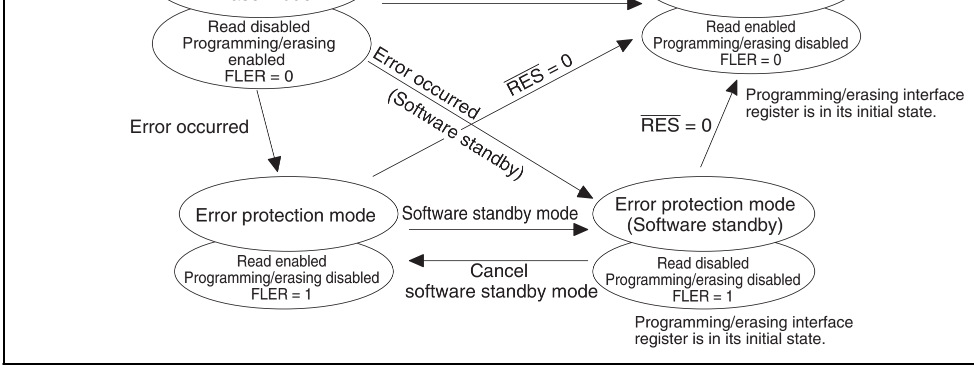

Read disabled
Programming/erasing enabled
FLER = 0
Read enabled
Programming/erasing disabled
FLER = 0
Error occurred (Software standby)
RES = 0
Programming/erasing interface register is in its initial state.
RES = 0
Error occurred
Error protection mode
Software standby mode
Error protection mode (Software standby)
Read enabled
Programming/erasing disabled
FLER = 1
Cancel software standby mode
Read disabled
Programming/erasing disabled
FLER = 1
Programming/erasing interface register is in its initial state.

Figure 17.13 Transitions to and from Error Protection State

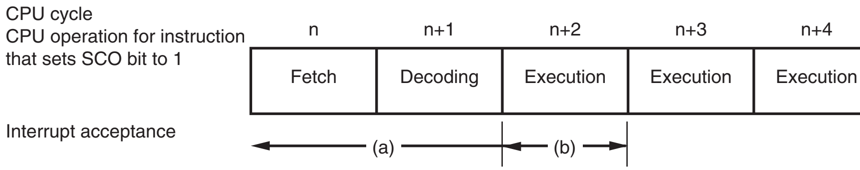
or after VBR is changed is referenced may cause an error.

Therefore, for cases where VBR setting change may conflict with interrupt occurrenc a vector table to be referenced when VBR is H'00000000 (initial value) at the start o MAT.

(1.2) SCO download request and interrupt request

Download of the on-chip programming/erasing program that is initiated by setting th in FCCS to 1 generates a particular interrupt processing accompanied by MAT switc Operation when the SCO download request and interrupt request conflicts is describ

1. Contention between SCO download request and interrupt request
   Figure 17.14 shows the timing of contention between execution of the instructio the SCO bit in FCCS to 1 and interrupt acceptance.



(a) When the interrupt is accepted at the (n + 1) cycle or before
After the interrupt processing completes, the SCO bit is set to 1 and download is executed.

(b) When the interrupt is accepted at the (n + 2) cycle or later
The interrupt will conflicts with the SCO download request. Ensure that no interrupt is generated

Figure 17.14 Timing of Contention between SCO Download Request and Interru

2. Generation of interrupt requests during downloading
   Ensure that interrupts are not generated during downloading that is initiated by th bit.

not guaranteed.

2. Do not rewrite the program data specified by the FMPDR parameter. If new progr is to provided by the interrupt processing, temporarily save the new program data another area. After confirming the completion of programming, save the new prog in the area specified by FMPDR or change the setting in FMPDR to indicated the area in which the new program data was temporarily saved.
3. Make sure the interrupt processing routine does not rewrite the contents of the flas memory related registers or data in the downloaded on-chip program area. During interrupt processing, do not simultaneously perform download of the on-chip prog an SCO request or programming/erasing.
4. At the beginning of the interrupt processing routine, save the CPU register content returning from the interrupt processing, write the saved contents in the CPU regist
5. When a transition is made to sleep mode or software standby mode in the interrup processing routine, the error protection state is entered and programming/erasing i aborted.

   If a transition is made to the reset state, the reset signal should only be released aft providing a reset input over a period longer than the normal 100 μs to reduce the c flash memory.

Table 17.10 Initiation Intervals of User Branch Processing

Processing Name	Maximum Interval
Programming	Approximately 4 ms
Erasing	Approximately 25 ms

However, when operation is done with CPU clock of 50 MHz, maximum value of th
until first user branch processing is as shown in table 17.11.

Table 17.11 Initial User Branch Processing Time

Processing Name	Max.
Programming	Approximately 4 ms
Erasing	Approximately 25 ms

3. State in which Interrupts are ignored

   In the following modes or period, interrupt requests are ignored; they are not execute
interrupt sources are not retained.

   — Boot mode

Prepare countermeasures (e.g. use of the user branch routine and periodic timer interr
WDT while taking the programming/erasing time into consideration as required.

1. Bit-rate matching state

   In this state, the boot program adjusts the bit rate to match that of the host. When the starts up in boot mode, the boot program is activated and enters the bit-rate matching which it receives commands from the host and adjusts the bit rate accordingly. After matching is complete, the boot program proceeds to the inquiry-and-selection state.

2. Inquiry-and-selection state

   In this state, the boot program responds to inquiry commands from the host. The dev mode, and bit rate are selected in this state. After making these selections, the boot p enters the programming/erasure state in response to the transition-to-programming/e state command. The boot program transfers the erasure program to RAM and execut of the user MAT before it enters the programming/erasure state.

3. Programming/erasure state

   In this state, programming/erasure are executed. The boot program transfers the prog programming/erasure to RAM in line with the command received from the host and programming/erasure. It also performs sum checking and blank checking as directed respective commands.

Figure 17.15 shows the flow of processing by the boot program.

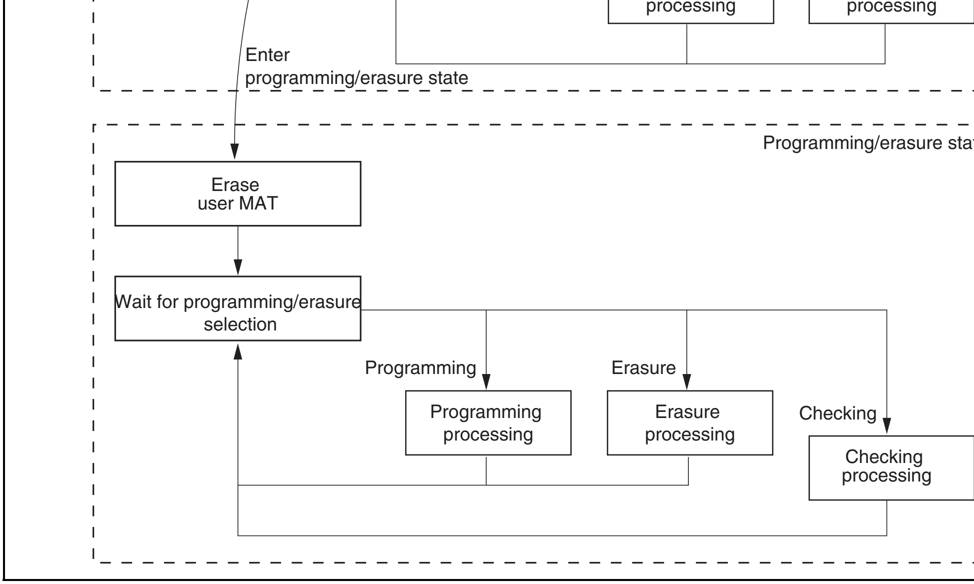


Figure 17.15 Flow of Processing by the Boot Program

- Bit-rate matching state

In bit-rate matching, the boot program measures the low-level intervals in a signal carryi data that is transmitted by the host, and calculates the bit rate from this. The bit rate can b changed by the new-bit-rate selection command. On completion of bit-rate matching, the program goes to the inquiry and selection state. The sequence of processing in bit-rate m shown in figure 17.16.

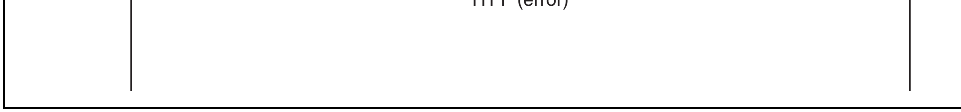


Figure 17.16 Sequence of Bit-Rate Matching

- Communications protocol

Formats in the communications protocol between the host and boot program after compl
the bit-rate matching are as follows.

1. One-character command or one-character response

   A command or response consisting of a single character used for an inquiry or the A
   indicating normal completion.

2. n-character command or n-character response

   A command or response that requires n bytes of data, which is used as a selection co
   response to an inquiry. The length of programming data is treated separately below.

3. Error response

   Response to a command in case of an error: two bytes, consisting of the error respon
   error code.

4. 128-byte programming command

   The command itself does not include data-size information. The data length is know
   response to the command for inquiring about the programming size.

5. Response to a memory reading command

   This response includes four bytes of size information.

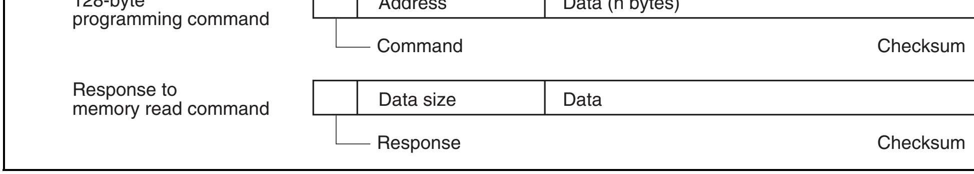


Figure 17.17 Formats in the Communications Protocol

- Command (1 byte): Inquiry, selection, programming, erasure, checking, etc.
- Response (1 byte): Response to an inquiry
- Size (one or two bytes): The length of data for transfer, excluding the command/re code, size, and checksum.
- Data (n bytes): Particular data for the command or response
- Checksum (1 byte): Set so that the total sum of byte values from the command coc checksum and change lower one byte to H'00.
- Error response (1 byte): Error response to a command
- Error code (1 byte): Indicates the type of error.
- Address (4 bytes): Address for programming
- Data (n bytes): Data to be programmed. "n" is known from the response to the con used to inquire about the programming size.
- Data size (4 bytes): Four-byte field included in the response to a memory reading command.

	devices	program names.
H'10	Device selection	Selects a device code.
H'21	Inquiry on clock modes	Requests the number of available clock modes ar respective values.
H'11	Clock-mode selection	Selects a clock mode.
H'22	Inquiry on frequency multipliers	Requests the number of clock signals for which fr multipliers and divisors are selectable, the numbe multiplier and divisor settings for the respective cl the values of the multipliers and divisors.
H'23	Inquiry on operating frequency	Requests the minimum and maximum values for frequency of the main clock and peripheral clock.
H'25	Inquiry on user MATs	Requests the number of user MAT areas along w start and end addresses.
H'26	Inquiry on erasure blocks	Requests the number of erasure blocks along wit start and end addresses.
H'27	Inquiry on programming size	Requests the unit of data for programming.
H'3F	New bit rate selection	Selects a new bit rate.
H'40	Transition to programming/erasure state	On receiving this command, the boot program era user MAT and enters the programming/erasure st
H'4F	Inquiry on boot program state	Requests information on the current state of boot processing.

The selection commands should be sent by the host in this order: device selection (H'10) mode selection (H'11), new bit rate selection (H'3F). These commands are mandatory. If selection command is sent two or more times, the command that is sent last is effective.

Command	H'20

— Command H'20 (1 byte): Inquiry on supported devices

Response	H'30	Size	No. of devices	
	Number of characters	Device code		Product name
	…			
	SUM			

— Response H'30 (1 byte): Response to the inquiry on supported devices

— Size (1 byte): The length of data for transfer excluding the command code, this fie and the checksum. Here, it is the total number of bytes taken up by the number of number of characters, device code, and product name fields.

— Number of devices (1 byte): The number of device models supported by the boot p embedded in the microcomputer.

— Number of characters (1 byte): The number of characters in the device code and p name fields.

— Device code (4 bytes): Device code of a supported device (ASCII encoded)

— Product name (n bytes): Product code of the boot program (ASCII encoded)

— SUM (1 byte): Checksum
This is set so that the total sum of all bytes from the command code to the checksu H'00.

supported devices (ASCII encoded)

— SUM (1 byte): Checksum

Response	H'06

— Response H'06 (1 byte): Response to device selection
This is the ACK code and is returned when the specified device code matches on
supported devices.

Error response	H'90	ERROR

— Error response H'90 (1 byte): Error response to device selection

— ERROR (1 byte): Error code
H'11: Sum-check error
H'21: Non-matching device code

(3) Inquiry on clock modes

In response to the inquiry on clock modes, the boot program returns the number of avail
modes.

Command	H'21

— Command H'21 (1 byte): Inquiry on clock modes

Response	H'31	Size	Mode	…	SUM

Command	H'11	Size	Mode	SUM

- Command H'11 (1 byte): Clock mode selection
- Size (1 byte): Number of characters in the clock-mode field (fixed at 1)
- Mode (1 byte): A clock mode returned in response to the inquiry on clock modes
- SUM (1 byte): Checksum

Response	H'06

- Response H'06 (1 byte): Response to clock mode selection
  This is the ACK code and is returned when the specified clock-mode matches one
  available clock modes.

Error response	H'91	ERROR

- Error response H'91 (1 byte): Error response to clock mode selection
- ERROR (1 byte): Error code
  H'11: Sum-check error
  H'22: Non-matching clock mode

No. of multipliers	Multiplier	…				
…						
SUM						

— Response H'32 (1 byte): Response to the inquiry on frequency multipliers

— Size (1 byte): The total length of the number of frequency types, number of mult
multiplier fields.

— Number of frequency types (1 byte): The number of operating clocks for which n
can be selected
(for example, if frequency multiplier settings can be made for the frequencies of
and peripheral operating clocks, the value should be H'02).

— Number of multipliers (1 byte): The number of multipliers selectable for the oper
frequency of the main or peripheral modules

— Multiplier (1 byte):
Multiplier: Numerical value in the case of frequency multiplication (e.g. H'04 fo
Divisor: Two’s complement negative numerical value in the case of frequency di
(e.g. H'FE [-2] for ×1/2)
As many multiplier fields are included as there are multipliers or divisors, and
combinations of the number of frequency types are repeated as many times as the
operating clocks.

— SUM (1 byte): Checksum

...	
SUM	

- — Response H'33 (1 byte): Response to the inquiry on operating frequency
- — Size (1 byte): The total length of the number of frequency types, and maximum an minimum values of operating frequency fields.
- — Number of frequency types (1 byte): The number of operating clock frequencies r within the device.

  For example, the value two indicates main and peripheral operating clock frequen
- — Minimum value of operating frequency (2 bytes): The minimum frequency of a fr multiplied or -divided clock signal.

  The value in this field and in the maximum value field is the frequency in MHz to decimal places, multiplied by 100 (for example, if the frequency is 20.00 MHz, th multiplied by 100 is 2000, so H'07D0 is returned here).
- — Maximum value of operating frequency (2 bytes): The maximum frequency of a f multiplied or -divided clock signal.

  As many pairs of minimum values are included as there are frequency types.
- — SUM (1 byte): Checksum

…	
SUM	

— Response H'35 (1 byte): Response to the inquiry on user MATs

— Size (1 byte): The total length of the number of areas and first and last address fi

— Number of areas (1 byte): The number of user MAT areas.
H'01 is returned if the entire user MAT area is continuous.

— First address of the area (4 bytes)

— Last address of the area (4 bytes)
As many pairs of first and last address field are included as there are areas.

— SUM (1 byte): Checksum

(8) Inquiry on erasure blocks

In response to the inquiry on erasure blocks, the boot program returns the number of era blocks in the user MAT and the addresses where each block starts and ends.

Command	H'26

— Command H'26 (1 byte): Inquiry on erasure blocks

Response	H'36	Size	No. of blocks	
	First address of the block			Last address of the block
	…			
	SUM			

In response to the inquiry on programming size, the boot program returns the size, in byt
unit for programming.

Command	H'27

- — Command H'27 (1 byte): Inquiry on programming size

Response	H'37	Size	Programming size	SUM

- — Response H'37 (1 byte): Response to the inquiry on programming size
- — Size (1 byte): The number of characters in the programming size field (fixed at 2)
- — Programming size (2 bytes): The size of the unit for programming
  This is the unit for the reception of data to be programmed.
- — SUM (1 byte): Checksum

(10) New bit rate selection

In response to the new-bit-rate selection command, the boot program changes the bit rate the new bit rate and, if the setting was successful, responds to the ACK sent by the host b returning another ACK at the new bit rate.

The new-bit-rate selection command should be sent after clock-mode selection.

Command	H'3F	Size	Bit rate	Input frequency
	No. of multipliers	Multiplier 1	Multiplier 2	
	SUM			

— Number of multipliers (1 byte): The number of selectable frequency multipliers a divisors for the device.

This is normally 2, which indicates the main operating frequency and the operati frequency of the peripheral modules.

— Multiplier 1 (1 byte): Multiplier or divisor for the main operating frequency

Multiplier: Numerical value of the frequency multiplier (e.g. H'04 for ×4)

Divisor: Two’s complement negative numerical value in the case of frequency di (e.g. H'FE [-2] for ×1/2)

— Multiplier 2 (1 byte): Multiplier or divisor for the peripheral operating frequency

Multiplier: Numerical value of the frequency multiplier (e.g. H'04 for ×4)

Divisor: Two’s complement negative numerical value in the case of frequency di (e.g. H'FE [-2] for ×1/2)

— SUM (1 byte): Checksum

Response	H'06

— Response H'06 (1 byte): Response to the new-bit-rate selection command

This is the ACK code and is returned if the specified bit rate has been selected.

Error response	H'BF	ERROR

— Error response H'BF (1 byte): Error response to new bit rate selection

— ERROR (1 byte): Error code

H'11: Sum-check error

H'24: Bit rate selection error (the specified bit rate is not selectable).

H'25: Input frequency error (the specified input frequency is not within the range minimum to the maximum value).

The value of the received multiplier is checked to see if it matches a multiplier or divi is available for the selected clock mode of the selected device. A value that does not r available ratio generates a frequency multiplier error.

3. Operating frequency

   The operating frequency is calculated from the received input frequency and the frequ multiplier or divisor. The input frequency is the frequency of the clock signal supplied LSI, while the operating frequency is the frequency at which the LSI is actually driven following formulae are used for this calculation.

   Operating frequency = input frequency × multiplier, or

   Operating frequency = input frequency / divisor

   The calculated operating frequency is checked to see if it is within the range of the mi and maximum values of the operating frequency for the selected clock mode of the se device. A value outside the range generates an operating frequency error.

4. Bit rate

   From the peripheral operating frequency (Pϕ) and the bit rate (B), the value (= n) of th select bits (CKS) in the serial mode register (SCSMR) and the value (= N) of the bit r register (SCBRR) are calculated, after which the error in the bit rate is calculated. Thi checked to see if it is smaller than 4%. A result greater than or equal to 4% generates selection error. The following formula is use to calculate the error.

$$\text{Error (\%)} = \left\{ \left[\frac{P\phi \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} \right] - 1 \right\} \times 100$$

— Response H'06 (1 byte): The ACK code transferred in response to acknowledgen new bit rate

The sequence of new bit rate selection is shown in figure 17.18.

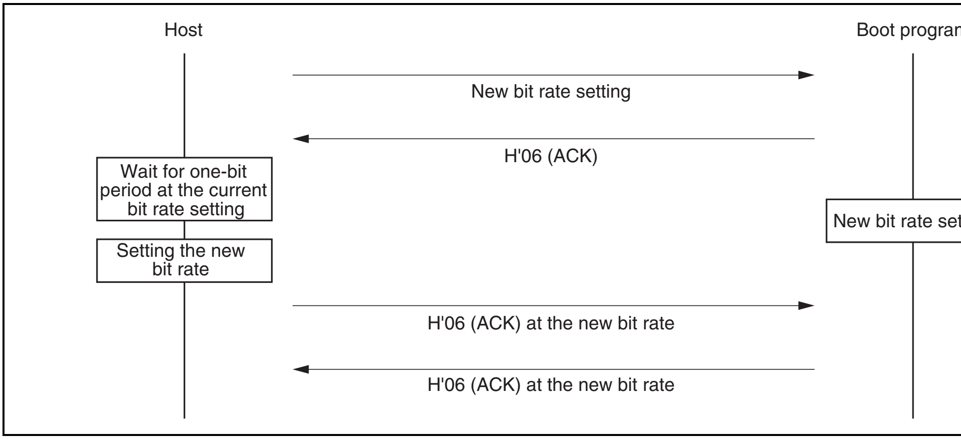

Host
Boot progran
New bit rate setting
H'06 (ACK)
Wait for one-bit period at the current bit rate setting
New bit rate set
Setting the new bit rate
H'06 (ACK) at the new bit rate
H'06 (ACK) at the new bit rate

Figure 17.18 Sequence of New Bit Rate Selection

Command	H'40

— Command H'40 (1 byte): Transition to programming/erasure state

Response	H'06

— Response H'06 (1 byte): Response to the transition-to-programming/erasure state c
This is returned as ACK when erasure of the user MAT has succeeded after transf
erasure program.

Error response	H'C0	H'51

— Error response H'C0 (1 byte): Error response to the transition-to-programming/era
command

— ERROR (1 byte): Error code

H'51: Erasure error (Erasure did not succeed because of an error.)

— Command H'xx (1 byte): Received command

- Order of Commands

In the inquiry-and-selection state, commands should be sent in the following order.

1. Send the inquiry on supported devices command (H'20) to get the list of supported d
2. Select a device from the returned device information, and send the device selection c (H'10) to select that device.
3. Send the inquiry on clock mode command (H'21) to get the available clock modes.
4. Select a clock mode from among the returned clock modes, and send the clock-mode command (H'11).
5. After selection of the device and clock mode, send the commands to inquire about fr multipliers (H'22) and operating frequencies (H'23) to get the information required t new bit rate.
6. Taking into account the returned information on the frequency multipliers and opera frequencies, send a new-bit-rate selection command (H'3F).
7. After the device and clock mode have been selected, get the information required for programming and erasure of the user MAT by sending the commands to inquire abo MAT (H'25), erasure block (H'26), and programming size (H'27).
8. After making all necessary inquiries and the new bit rate selection, send the transitio programming/erasure state command (H'40) to place the boot program in the programming/erasure state.

H'43	Selection of user MAT programming	Selects transfer of the program for user MAT prog
H'50	128-byte programming	Executes 128-byte programming.
H'48	Erasure selection	Selects transfer of the erasure program.
H'58	Block erasure	Executes erasure of the specified block.
H'52	Memory read	Reads from memory.
H'4B	Sum checking of user MAT	Executes sum checking of the user MAT.
H'4D	Blank checking of user MAT	Executes blank checking of the user MAT.
H'4F	Inquiry on boot program state	Requests information on the state of boot processi

- Programming

Programming is performed by issuing a programming-selection command and the 128-by programming command.

Firstly, the host issues the programming-selection command to select the MAT to be prog and programming by the method.

Next, the host issues a 128-byte programming command. 128 bytes of data for programm the method selected by the preceding programming selection command are expected to fo command. To program more than 128 bytes, repeatedly issue 128-byte programming com To terminate programming, the host should send another 128-byte programming comma the address H'FFFFFFFF. On completion of programming, the boot program waits for the programming/erasure selection command.

To then program the other MAT, start by sending the programming select command.

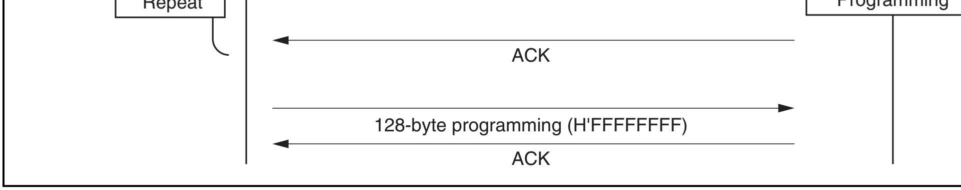


Figure 17.19 Sequence of Programming

(1) Selection of user MAT programming

In response to the command for selecting programming of the user MAT, the boot progr
transfers the corresponding flash-writing program, i.e. the program for writing to the use

Command	H'43

— Command H'43 (1 byte): Selects programming of the user MAT.

Response	H'06

— Response H'06 (1 byte): Response to selection of user MAT programming
This ACK code is returned after transfer of the program that performs writing to
MAT.

Error response	H'C3	ERROR

— Error response H'C3 (1 byte): Error response to selection of user MAT programm

…						
SUM						

- Command H'50 (1 byte): 128-byte programming
- Address for programming (4 bytes): Address where programming starts
  Specify an address on a 128-byte boundary.
  [Example] H'00, H01, H'00, H'00: H'00010000
- Programming data (n bytes): Data for programming
  The length of the programming data is the size returned in response to the progran
  size inquiry command.
- SUM (1 byte): Checksum

Response	H'06

- Response H'06 (1 byte): Response to 128-byte programming
  The ACK code is returned on completion of the requested programming.

Error response	H'D0	ERROR

- Error response H'D0 (1 byte): Error response to 128-byte programming
- ERROR (1 byte): Error code
  H'11: Sum-check error
  H'2A: Address error (the address is not within the range for the selected MAT)
  H'53: Programming error (programming failed because of an error in programmin

— Command H'50 (1 byte): 128-byte programming

— Address for programming (4 bytes): Terminating code (H'FF, H'FF, H'FF, H'FF)

— SUM (1 byte): Checksum

Response	H'06

— Response H'06 (1 byte): Response to 128-byte programming
This ACK code is returned on completion of the requested programming.

Error response	H'D0	ERROR

— Error response H'D0 (1 byte): Error response to 128-byte programming

— ERROR (1 byte): Error code
H'11: Sum-check error
H'53: Programming error

in figure 17.20.

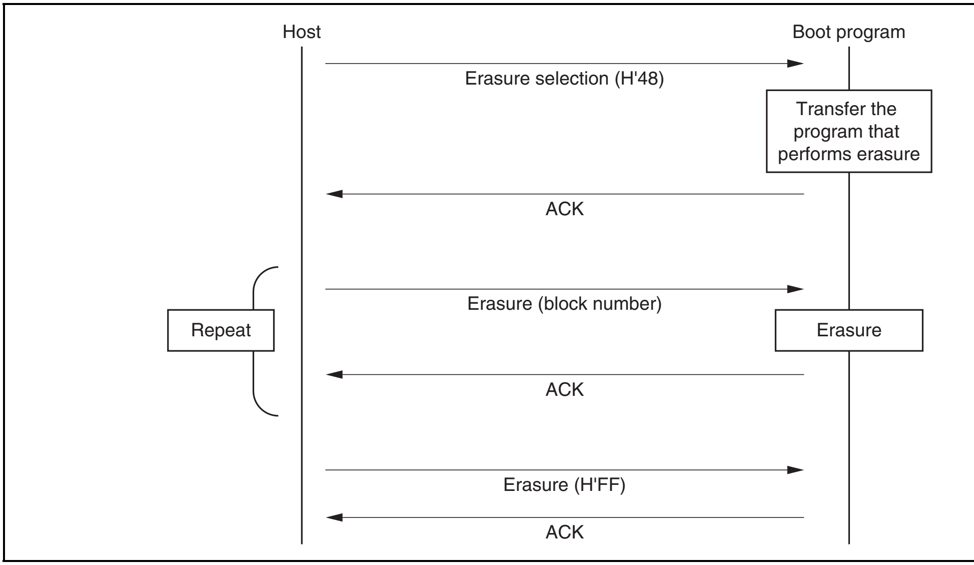


Figure 17.20 Sequence of Erasure

— Response H'06 (1 byte): Response to selection of erasure
This ACK code is returned after transfer of the program that performs erasure.

Error response	H'C8	ERROR

— Error response H'C8 (1 byte): Error response to selection of erasure

— ERROR (1 byte): Error code
H'54: Error in selection processing (processing was not completed because of a tr
error.)

(2) Block erasure

In response to the block erasure command, the boot program erases the data in a specifie
the user MAT.

Command	H'58	Size	Block number	SUM

— Command H'58 (1 byte): Erasure of a block

— Size (1 byte): The number of characters in the block number field (fixed at 1)

— Block number (1 byte): Block number of the block to be erased

— SUM (1 byte): Checksum

Response	H'06

— Response H'06 (1 byte): Response to the block erasure command
This ACK code is returned when the block has been erased.

processing and waits for the next programming/erasure selection command.

Command	H'58	Size	Block number	SUM

- Command H'58 (1 byte): Erasure of a block
- Size (1 byte): The number of characters in the block number field (fixed at 1)
- Block number (1 byte): H'FF (erasure terminating code)
- SUM (1 byte): Checksum

Response	H'06

- Response H'06 (1 byte): ACK code to indicate response to the request for terminat erasure

To perform erasure again after having issued the command with the block number specifi H'FF, execute the process from the selection of erasure.

- Memory read

In response to the memory read command, the boot program returns the data from the spe address.

Command	H'52	Size	Area	First address for reading
	Amount to read			SUM

- Command H'52 (1 byte): Memory read
- Size (1 byte): The total length of the area, address for reading, and amount to read (fixed value of 9)

— Response H'52 (1 byte): Response to the memory read command

— Amount to read (4 bytes): The amount to read as specified in the memory read co

— Data (n bytes): The specified amount of data read out from the specified address

— SUM (1 byte): Checksum

Error response	H'D2	ERROR

— Error response H'D2 (1 byte): Error response to memory read command

— ERROR (1 byte): Error code
H'11: Sum-check error
H'2A: Address error (the address specified for reading is beyond the range of the
H'2B: Size error (the specified amount is greater than the size of the MAT,
the last address for reading as calculated from the specified address for the start o
and the amount to read is beyond the MAT area, or "0" was specified as the amou
read)

— Response H'5B (1 byte): Response to sum checking of the user MAT

— Size (1 byte): The number of characters in the checksum for the MAT (fixed to 4)

— Checksum for the MAT (4 bytes): Result of checksum calculation for the user MA
the total of all data in the MAT, in byte units.

— SUM (1 byte): Checksum (for the transmitted data)

- Blank checking of the user MAT

In response to the command for blank checking of the user MAT, the boot program check
if the whole of the user MAT is blank; the value returned indicates the result.

Command	H'4D

— Command H'4D (1 byte): Blank checking of the user MAT

Response	H'06

— Response H'06 (1 byte): Response to blank checking of the user MAT
The ACK code is returned when the whole area is blank (all bytes are H'FF).

Error response	H'CD	H'52

— Error response H'CD (1 byte): Error response to blank checking of the user MAT

— Error code H'52 (1 byte): Non-erased error

— Response H'5F (1 byte): Response to the inquiry regarding boot-program state

— Size (1 byte): The number of characters in STATUS and ERROR (fixed at 2)

— STATUS (1 byte): State of the standard boot program
See table 17.14, Status Codes.

— ERROR (1 byte): Error state (indicates whether the program is in normal operati
error has occurred)
ERROR = 0: Normal
ERROR ≠ 0: Error
See table 17.15, Error Codes.

— SUM (1 byte): Checksum

Table 17.14 Status Codes

Code	Description
H'11	Waiting for device selection
H'12	Waiting for clock-mode selection
H'13	Waiting for bit-rate selection
H'1F	Waiting for transition to programming/erasure status (bit-rate selection
H'31	Erasing the user MAT
H'3F	Waiting for programming/erasure selection (erasure complete)
H'4F	Waiting to receive data for programming (programming complete)
H'5F	Waiting for erasure block specification (erasure complete)

H'27	Operating frequency error
H'29	Block number error
H'2A	Address error
H'2B	Data length error (size error)
H'51	Erasure error
H'52	Non-erased error
H'53	Programming error
H'54	Selection processing error
H'80	Command error
H'FF	Bit-rate matching acknowledge error

17.8.2 Areas for Storage of the Procedural Program and Data for Programming

In the descriptions in the previous section, storable areas for the programming/erasing pro
programs and program data are assumed to be in on-chip RAM. However, the procedure
and data can be executed in other areas as long as the following conditions are satisfied.

1. The on-chip programming/erasing program is downloaded from the address set by FT
   on-chip RAM, therefore, this area is not available for use.
2. The on-chip programming/erasing program will use 128 bytes or more as a stack. Ma
   this area is reserved.
3. Since download by setting the SCO bit to 1 will cause the MATs to be switched, it sh
   executed in on-chip RAM.
4. The flash memory is accessible until the start of programming or erasing, that is, until
   result of downloading has been decided. When in a mode in which the external addres
   is not accessible, such as single-chip mode, the required procedure programs, interrup

Transitions to the reset state during programming/erasing are inhibited. When the res is accidentally input to the LSI, a longer period in the reset state than usual (100 μs) before the reset signal is released.

7. When the program data storage area indicated by the FMPDR parameter in the progr processing is within the flash memory area, an error will occur. Therefore, temporari the program data to on-chip RAM to change the address set in FMPDR to an address than flash memory.

Tables 17.16 and 17.17 show the areas in which the program data can be stored and exec according to the operation type and mode.

Table 17.16 Executable MAT

	Initiated Mode
Operation	**User Program Mode**
Programming	Table 17.17 (1)
Erasing	Table 17.17 (2)

	Writing 1 to SCO in FCCS (download)	√	X		√
	Key register clearing	√	√	√	
	Deciding download result	√	√	√	
	Download error processing	√	√	√	
	Setting initialization parameters	√	√	√	
Pro-gramming procedure	Initialization	√	X	√	
	Deciding initialization result	√	√	√	
	Initialization error processing	√	√	√	
	Interrupt processing routine	√	X	√	
	Writing H'5A to key register	√	√	√	
	Setting programming parameters	√	X	√	
	Programming	√	X	√	
	Deciding programming result	√	X	√	
	Programming error processing	√	X	√	
	Key register clearing	√	X	√	

Note: * If the data has been transferred to on-chip RAM in advance, this area can be u

	(download)			
	Key register clearing	√	√	√
	Deciding download result	√	√	√
	Download error processing	√	√	√
	Setting initialization parameters	√	√	√
	Initialization	√	X	√
Erasing procedure	Deciding initialization result	√	√	√
	Initialization error processing	√	√	√
	Interrupt processing routine	√	X	√
	Writing H'5A to key register	√	√	√
	Setting erasure parameters	√	X	√
	Erasure	√	X	√
	Deciding erasure result	√	X	√
	Erasing error processing	√	X	√
	Key register clearing	√	X	√

register (RAMCR). For details on the RAM control register (RAMCR), refer to section RAM Control Register (RAMCR).

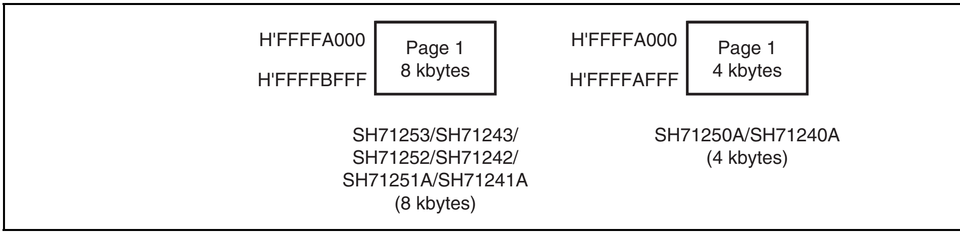


Figure 18.1 On-chip RAM Addresses

When an address error in write access to the on-chip RAM occurs, the contents of the on-
RAM may be corrupted.

18.1.3 Initial Values in RAM

After power has been supplied, initial values in RAM remain undefined until RAM is wri

This LSI has the following power-down modes.

- Sleep mode
- Software standby mode
- Module standby mode

Table 19.1 shows the methods to make a transition from the program execution state, as the CPU and peripheral module states in each mode and the procedures for canceling ea

standby	instruction with STBY bit in STBCR1 and STBYMD bit in STBCR6 set to 1.				(contents retained)		IRQ • Power-on the $\overline{\text{RES}}$
Module standby	Set MSTP bits in STBCR2 to STBCR5 to 1.	Runs	Runs	Held	Specified module halts (contents retained)	Specified module halts	• Clear MS • Power-on modules MSTP bit initial valu

Note: For details on the states of on-chip peripheral module registers in each mode, refe section 20.3, Register States in Each Operating Mode. For details on the pin states mode, refer to appendix A, Pin States.

19.3 Register Descriptions

There are following registers used for the power-down modes. For details on the address these registers and the states of these registers in each processing state, see section 20, L Registers.

Table 19.3 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Ac
Standby control register 1	STBCR1	R/W	H'00	H'FFFFE802	8
Standby control register 2	STBCR2	R/W	H'38	H'FFFFE804	8
Standby control register 3	STBCR3	R/W	H'FF	H'FFFFE806	8
Standby control register 4	STBCR4	R/W	H'FF	H'FFFFE808	8
Standby control register 5	STBCR5	R/W	H'03	H'FFFFE80A	8
Standby control register 6	STBCR6	R/W	H'00	H'FFFFE80C	8
RAM control register	RAMCR	R/W	H'10	H'FFFFE880	8

7	STBY	0	R/W	Standby Specifies transition to software standby mo 0: Executing SLEEP instruction makes this sleep mode 1: Executing SLEEP instruction makes this software standby mode
6 to 0	—	All 0	R	Reserved These bits are always read as 0. The write should always be 0.

Bit	Bit Name	Value	R/W	Description
7	MSTP7	0	R/W	Module Stop Bit 7 When this bit is set to 1, the supply of the the RAM is halted. 0: RAM operates 1: Clock supply to RAM halted
6	—	0	R/W	Reserved This bit is always read as 0. The write valu always be 0.
5 to 3	—	All 1	R/W	Reserved These bits are always read as 1. The write should always be 1.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write should always be 0.

Bit	Bit Name	Value	R/W	Description
7, 6	—	All 1	R/W	Reserved These bits are always read as 1. The write valu always be 1.
5	MSTP13	1	R/W	Module Stop Bit 13 When this bit is set to 1, the supply of the clock SCI_2 is halted. 0: SCI_2 operates 1: Clock supply to SCI_2 halted
4	MSTP12	1	R/W	Module Stop Bit 12 When this bit is set to 1, the supply of the clock SCI_1 is halted. 0: SCI_1 operates 1: Clock supply to SCI_1 halted
3	MSTP11	1	R/W	Module Stop Bit 11 When this bit is set to 1, the supply of the clock SCI_0 is halted. 0: SCI_0 operates 1: Clock supply to SCI_0 halted
2 to 0	—	All 1	R/W	Reserved These bits are always read as 1. The write valu always be 1.

Bit	Bit Name	Value	R/W	Description
7	—	1	R/W	Reserved This bit is always read as 1. The write value s always be 1.
6	MSTP22	1	R/W	Module Stop Bit 22 When this bit is set to 1, the supply of the cloc MTU2 is halted. 0: MTU2 operates 1: Clock supply to MTU2 halted
5	MSTP21	1	R/W	Module Stop Bit 21 When this bit is set to 1, the supply of the cloc CMT is halted. 0: CMT operates 1: Clock supply to CMT halted
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write va always be 1.
2	—	1	R/W	Reserved This bit is always read as 1. The write value s always be 1.
1	MSTP17	1	R/W	Module Stop Bit 17 When this bit is set to 1, the supply of the cloc A/D_1 is halted. 0: A/D_1 operates 1: Clock supply to A/D_1 halted

STBCR5 is an 8-bit readable/writable register that controls the operation of modules in po
down mode.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	MSTP[25:24]	
Initial value:	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
1, 0	MSTP[25:24]	11	R/W	Module Stop Bit 25 and 24 When either or both of these bits are set to 1, t supply of the clock to the UBC is halted. 00: UBC operates 01: Setting prohibited 10: Setting prohibited 11: Clock supply to UBC halted

Note: Write an initial value of "11" when programming the 32 Kbyte (SH71251A and SH7 and 16 Kbyte (SH71250A and SH71240A) versions.

7	UBCRST	0	R/W	UBC Software Reset Resetting the PC trace unit of UBC is controll software. Clearing this bit to 0 puts the PC trace unit of module into the power-on reset state. 0: Puts the PC trace unit of UBC into the rese 1: Releases reset in the PC trace unit of UBC This bit is not supported on 32 Kbyte versions (SH71251A, SH71241A) and 16 Kbyte versio (SH71250A, SH71240A). These bits are always read as 0. The write va always be 0.
6	HIZ	0	R/W	Port High-Impedance In software standby mode, this bit selects whe pin state is retained or changed to high-impec 0: In software standby mode, the pin state is 1: In software standby mode, the pin state is to high-impedance
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write va always be 0.
1	STBYMD	0	R/W	Software Standby Mode Select If this bit is set to 1, executing SLEEP instruct the STBY bit in STBCR1 is 1 and makes trans software standby mode. 0: Setting prohibited 1: Makes transition to software standby mode
0	—	0	R	Reserved This bit is always read as 0. The write value s always be 0.

Bit	Bit Name	Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.
4	RAME	1	R/W	RAM Enable This bit enables/disables the on-chip RAM. 0: On-chip RAM disabled 1: On-chip RAM enabled When this bit is cleared to 0, the access to the RAM is disabled. In this case, an undefined va returned when reading or fetching the data or instruction from the on-chip RAM, and writing t chip RAM is ignored. When RAME is cleared to 0 to disable the on-c RAM, an instruction to access the on-chip RAM not be set next to the instruction to write RAMC such an instruction is set, normal access is not guaranteed. When RAME is set to 1 to enable the on-chip F instruction to read RAMCR should be set next instruction to write to RAMCR. If an instruction access the on-chip RAM is set next to the instr write to RAMCR, normal access is not guarant
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write valu always be 0.

Sleep mode is canceled by a reset.

(1) Canceling with Reset

Sleep mode is canceled by a power-on reset with the $\overline{\text{RES}}$ pin, a manual reset with the $\overline{\text{M}}$
or an internal power-on/manual reset by WDT. Do not cancel sleep mode with an interru

chip peripheral module registers in software standby mode, refer to section 20.3, Register
Each Operating Mode. For details on the pin states in software standby mode, refer to app
Pin States.

The procedure for switching to software standby mode is as follows:

1. Clear the TME bit in the timer control register (WTCSR) of the WDT to 0 to stop the
2. Set the timer counter (WTCNT) of the WDT to 0 and bits CKS2 to CKS0 in WTCSR appropriate values to secure the specified oscillation settling time.
3. After setting the STBY bit in STBCR1 and the STBYMD bit in STBCR6 to 1, execut SLEEP instruction.
4. Software standby mode is entered and the clocks within this LSI are halted.

When the priority level of an IRQ interrupt is lower than the interrupt mask level set in t register (SR) of the CPU, an interrupt request is not accepted preventing software standb from being canceled.

When falling-edge detection is selected for the NMI pin, drive the NMI pin high before transition to software standby mode. When rising-edge detection is selected for the NMI the NMI pin low before making a transition to software standby mode.

Similarly, when falling-edge detection is selected for the IRQ pin, drive the IRQ pin hig making a transition to software standby mode. When rising-edge detection is selected fo pin, drive the IRQ pin low before making a transition to software standby mode.

(2) Canceling with Power-on Reset

Software standby mode is canceled by a power-on reset with the $\overline{\text{RES}}$ pin. Keep the $\overline{\text{RES}}$ until the clock oscillation settles.

(3) Canceling with Manual Reset

Note that software standby mode cannot be canceled with a manual reset in this LSI.

mode, refer to section 20.3, Register States in Each Operating Mode.

19.6.2 Canceling Module Standby Function

The module standby function can be canceled by clearing the MSTP bits in STBCR2 to S to 0. The module standby function can be canceled by a power-on reset for modules whos bit has an initial value of 0.

19.7 Usage Note

19.7.1 Current Consumption while Waiting for Oscillation to be Stabilized

The current consumption while waiting for oscillation to be stabilized is higher than that oscillation is stabilized.

19.7.2 Executing the SLEEP Instruction

Apply either of the following measures before executing the SLEEP instruction to initiate transition to sleep mode or software standby mode.

Measure A: Stop the generation of interrupts from on-chip peripheral modules, IRQ inter the NMI interrupt before executing the SLEEP instruction.

Measure B: Change the value in FRQCR to the initial value, H’36DB, and then dummy-r FRQCR twice before executing the SLEEP instruction.

- The numbers of access cycles are given.

2. Register Bit Table

- Bit configurations are shown in the order of the register address table.
- As for reserved bits, the bit name column is indicated with —.
- As for the blank column of the bit names, the whole register is allocated to the count
- As for 16- or 32-bit registers, bits are indicated from the MSB.

3. Register State in Each Operating Mode

- Register states are listed in the order of the register address table.
- Register states in the basic operating mode are shown. As for modules including thei states such as reset, see the sections of those modules.

Serial mode register_0	SCSMR_0	8	H'FFFFC000	SCI	8	Pϕ refere
Bit rate register_0	SCBRR_0	8	H'FFFFC002	(Channel 0)	8	B: 2
Serial control register_0	SCSCR_0	8	H'FFFFC004		8	
Transmit data register_0	SCTDR_0	8	H'FFFFC006		8	
Serial status register_0	SCSSR_0	8	H'FFFFC008		8	
Receive data register_0	SCRDR_0	8	H'FFFFC00A		8	
Serial direction control register_0	SCSDCR_0	8	H'FFFFC00C		8	
Serial port register_0	SCSPTR_0	8	H'FFFFC00E		8	
Serial mode register_1	SCSMR_1	8	H'FFFFC080	SCI	8	Pϕ refere
Bit rate register_1	SCBRR_1	8	H'FFFFC082	(Channel 1)	8	B: 2
Serial control register_1	SCSCR_1	8	H'FFFFC084		8	
Transmit data register_1	SCTDR_1	8	H'FFFFC086		8	
Serial status register_1	SCSSR_1	8	H'FFFFC088		8	
Receive data register_1	SCRDR_1	8	H'FFFFC08A		8	
Serial direction control register_1	SCSDCR_1	8	H'FFFFC08C		8	
Serial port register_1	SCSPTR_1	8	H'FFFFC08E		8	
Serial mode register_2	SCSMR_2	8	H'FFFFC100	SCI	8	Pϕ refere
Bit rate register_2	SCBRR_2	8	H'FFFFC102	(Channel 2)	8	B: 2
Serial control register_2	SCSCR_2	8	H'FFFFC104		8	
Transmit data register_2	SCTDR_2	8	H'FFFFC106		8	
Serial status register_2	SCSSR_2	8	H'FFFFC108		8	
Receive data register_2	SCRDR_2	8	H'FFFFC10A		8	
Serial direction control register_2	SCSDCR_2	8	H'FFFFC10C		8	
Serial port register_2	SCSPTR_2	8	H'FFFFC10E		8	

Timer I/O control register L_4	TIORL_4	8	H'FFFFC207		8
Timer interrupt enable register_3	TIER_3	8	H'FFFFC208		8, 16
Timer interrupt enable register_4	TIER_4	8	H'FFFFC209		8
Timer output master enable register	TOER	8	H'FFFFC20A		8
Timer gate control register	TGCR	8	H'FFFFC20D		8
Timer output control register 1	TOCR1	8	H'FFFFC20E		8, 16
Timer output control register 2	TOCR2	8	H'FFFFC20F		8
Timer counter_3	TCNT_3	16	H'FFFFC210		16, 32
Timer counter_4	TCNT_4	16	H'FFFFC212		16
Timer cycle data register	TCDR	16	H'FFFFC214		16, 32
Timer dead time data register	TDDR	16	H'FFFFC216		16
Timer general register A_3	TGRA_3	16	H'FFFFC218		16, 32
Timer general register B_3	TGRB_3	16	H'FFFFC21A		16
Timer general register A_4	TGRA_4	16	H'FFFFC21C		16, 32
Timer general register B_4	TGRB_4	16	H'FFFFC21E		16
Timer sub-counter	TCNTS	16	H'FFFFC220		16, 32
Timer cycle buffer register	TCBR	16	H'FFFFC222		16
Timer general register C_3	TGRC_3	16	H'FFFFC224		16, 32
Timer general register D_3	TGRD_3	16	H'FFFFC226		16
Timer general register C_4	TGRC_4	16	H'FFFFC228		16, 32
Timer general register D_4	TGRD_4	16	H'FFFFC22A		16
Timer status register_3	TSR_3	8	H'FFFFC22C		8, 16
Timer status register_4	TSR_4	8	H'FFFFC22D		8
Timer interrupt skipping set register	TITCR	8	H'FFFFC230		8, 16

Timer A/D converter start request control register	TADCR	16	H'FFFFC240	16
Timer A/D converter start request cycle set register A_4	TADCORA_4	16	H'FFFFC244	16, 32
Timer A/D converter start request cycle set register B_4	TADCORB_4	16	H'FFFFC246	16
Timer A/D converter start request cycle set buffer register A_4	TADCOBRA_4	16	H'FFFFC248	16, 32
Timer A/D converter start request cycle set buffer register B_4	TADCOBRB_4	16	H'FFFFC24A	16
Timer waveform control register	TWCR	8	H'FFFFC260	8
Timer start register	TSTR	8	H'FFFFC280	8, 16
Timer synchronous register	TSYR	8	H'FFFFC281	8
Timer read/write enable register	TRWER	8	H'FFFFC284	8
Timer control register_0	TCR_0	8	H'FFFFC300	8, 16, 32
Timer mode register_0	TMDR_0	8	H'FFFFC301	8
Timer I/O control register H_0	TIORH_0	8	H'FFFFC302	8, 16
Timer I/O control register L_0	TIORL_0	8	H'FFFFC303	8
Timer interrupt enable register_0	TIER_0	8	H'FFFFC304	8, 16, 32
Timer status register_0	TSR_0	8	H'FFFFC305	8
Timer counter_0	TCNT_0	16	H'FFFFC306	16
Timer general register A_0	TGRA_0	16	H'FFFFC308	16, 32
Timer general register B_0	TGRB_0	16	H'FFFFC30A	16

Timer control register_1	TCR_1	8	H'FFFFC380		8, 16
Timer mode register_1	TMDR_1	8	H'FFFFC381		8
Timer I/O control register_1	TIOR_1	8	H'FFFFC382		8
Timer interrupt enable register_1	TIER_1	8	H'FFFFC384		8, 16, 32
Timer status register_1	TSR_1	8	H'FFFFC385		8
Timer counter_1	TCNT_1	16	H'FFFFC386		16
Timer general register A_1	TGRA_1	16	H'FFFFC388		16, 32
Timer general register B_1	TGRB_1	16	H'FFFFC38A		16
Timer input capture control register	TICCR	8	H'FFFFC390		8
Timer control register_2	TCR_2	8	H'FFFFC400		8, 16
Timer mode register_2	TMDR_2	8	H'FFFFC401		8
Timer I/O control register_2	TIOR_2	8	H'FFFFC402		8
Timer interrupt enable register_2	TIER_2	8	H'FFFFC404		8, 16, 32
Timer status register_2	TSR_2	8	H'FFFFC405		8
Timer counter_2	TCNT_2	16	H'FFFFC406		16
Timer general register A_2	TGRA_2	16	H'FFFFC408		16, 32
Timer general register B_2	TGRB_2	16	H'FFFFC40A		16
Timer counter U_5	TCNTU_5	16	H'FFFFC480		16, 32
Timer general register U_5	TGRU_5	16	H'FFFFC482		16
Timer control register U_5	TCRU_5	8	H'FFFFC484		8
Timer I/O control register U_5	TIORU_5	8	H'FFFFC486		8
Timer counter V_5	TCNTV_5	16	H'FFFFC490		16, 32
Timer general register V_5	TGRV_5	16	H'FFFFC492		16

Timer interrupt enable register_5	TIER_5	8	H'FFFFC4B2		8	
Timer start register_5	TSTR_5	8	H'FFFFC4B4		8	
Timer compare match clear register	TCNTCMPCLR	8	H'FFFFC4B6		8	
A/D data register 0	ADDR0	16	H'FFFFC900	A/D	16	Pφ refer
A/D data register 1	ADDR1	16	H'FFFFC902	(Channel 0)	16	B: 2, W:
A/D data register 2	ADDR2	16	H'FFFFC904		16	
A/D data register 3	ADDR3	16	H'FFFFC906		16	
A/D control/status register_0	ADCSR_0	16	H'FFFFC910		16	
A/D control register_0	ADCR_0	16	H'FFFFC912		16	
A/D data register 4	ADDR4	16	H'FFFFC980	A/D	16	Pφ refer
A/D data register 5	ADDR5	16	H'FFFFC982	(Channel 1)	16	B: 2, W:
A/D data register 6	ADDR6	16	H'FFFFC984		16	
A/D data register 7	ADDR7	16	H'FFFFC986		16	
A/D control/status register_1	ADCSR_1	16	H'FFFFC990		16	
A/D control register_1	ADCR_1	16	H'FFFFC992		16	
Flash code control/status register	FCCS	8	H'FFFFCC00	FLASH	8	Pφ refer
Flash program code select register	FPCS	8	H'FFFFCC01		8	B: 5
Flash erase code select register	FECS	8	H'FFFFCC02		8	
Flash key code register	FKEY	8	H'FFFFCC04		8	
Flash transfer destination address register	FTDAR	8	H'FFFFCC06		8	

Compare match constant register_1	CMCOR_1	16	H'FFFFCE0C		8, 16, 32	
Input level control/status register 1	ICSR1	16	H'FFFFD000	POE	8, 16, 32	Pφ refe
Output level control/status register 1	OCSR1	16	H'FFFFD002		8, 16	B: 2, W
Input level control/status register 3	ICSR3	16	H'FFFFD008		8, 16	
Software port output enable register	SPOER	8	H'FFFFD00A		8	
Port output enable control register 1	POECR1	8	H'FFFFD00B		8	
Port output enable control register 2	POECR2	16	H'FFFFD00C		8, 16	
Port A data register L	PADRL	16	H'FFFFD102	I/O	8, 16	Pφ refe
Port A I/O register L	PAIORL	16	H'FFFFD106	PFC	8, 16	B: 2, W
Port A control register L4	PACRL4	16	H'FFFFD110		8, 16, 32	
Port A control register L3	PACRL3	16	H'FFFFD112		8, 16	
Port A control register L2	PACRL2	16	H'FFFFD114		8, 16, 32	
Port A control register L1	PACRL1	16	H'FFFFD116		8, 16	
Port A port register L	PAPRL	16	H'FFFFD11E	I/O	8, 16	
Port B data register H	PBDRH	16	H'FFFFD180		8, 16, 32	
Port B data register L	PBDRL	16	H'FFFFD182		8, 16	
Port B I/O register H	PBIORH	16	H'FFFFD184	PFC	8, 16, 32	
Port B I/O register L	PBIORL	16	H'FFFFD186		8, 16	
Port B control register H1	PBCRH1	16	H'FFFFD18E		8, 16	
Port B control register L2	PBCRL2	16	H'FFFFD194		8, 16, 32	
Port B control register L1	PBCRL1	16	H'FFFFD196		8, 16	
Port B port register H	PBPRH	16	H'FFFFD19C	I/O	8, 16, 32	
Port B port register L	PBPRL	16	H'FFFFD19E		8, 16	
Port E data register L	PEDRL	16	H'FFFFD302		8, 16	

Port F data register L	PFDRL	16	H'FFFFD382	I/O	8, 16	
Frequency control register	FRQCR	16	H'FFFFE800	CPG	16	Pϕ refer W: 2
Standby control register 1	STBCR1	8	H'FFFFE802	Power-down modes	8	Pϕ refer B: 2
Standby control register 2	STBCR2	8	H'FFFFE804		8	
Standby control register 3	STBCR3	8	H'FFFFE806		8	
Standby control register 4	STBCR4	8	H'FFFFE808		8	
Standby control register 5	STBCR5	8	H'FFFFE80A		8	
Standby control register 6	STBCR6	8	H'FFFFE80C		8	
Watchdog timer counter	WTCNT	8	H'FFFFE810	WDT *1: Read *2: Write	8*1, 16*2	Pϕ refer B: 2*1, W
Watchdog timer control/status register	WTCSR	8	H'FFFFE812		8*1, 16*2	
Oscillation stop detection control register	OSCCR	8	H'FFFFE814	CPG	8	Pϕ refer B: 2
RAM control register	RAMCR	8	H'FFFFE880	Power-down modes	8	Pϕ refer B: 2
A/D trigger select register_0	ADTSR_0	16	H'FFFFE890	A/D	8, 16	Pϕ refer B: 2, W:
Interrupt control register 0	ICR0	16	H'FFFFE900	INTC	8, 16	Pϕ refer B: 2, W:
IRQ control register	IRQCR	16	H'FFFFE902		8, 16	
IRQ status register	IRQSR	16	H'FFFFE904		8, 16	
Interrupt priority register A	IPRA	16	H'FFFFE906		8, 16	
Interrupt priority register B	IPRB	16	H'FFFFE908		8, 16	
Interrupt priority register C	IPRC	16	H'FFFFE980		16	

Interrupt priority register L	IPRL	16	H'FFFFE992		16	
Interrupt priority register M	IPRM	16	H'FFFFE994		16	
Break address register A*	BARA	32	H'FFFFF300	UBC	32	Bϕ refe
Break address mask register A*	BAMRA	32	H'FFFFF304		32	B: 2, W
Break bus cycle register A*	BBRA	16	H'FFFFF308		16	
Break data register A*	BDRA	32	H'FFFFF310		32	
Break data mask register A*	BDMRA	32	H'FFFFF314		32	
Break address register B*	BARB	32	H'FFFFF320		32	
Break address mask register B*	BAMRB	32	H'FFFFF324		32	
Break bus cycle register B*	BBRB	16	H'FFFFF328		16	
Break data register B*	BDRB	32	H'FFFFF330		32	
Break data mask register B*	BDMRB	32	H'FFFFF334		32	
Break control register*	BRCR	32	H'FFFFF3C0		32	
Branch source register*	BRSR	32	H'FFFFF3D0		32	
Branch destination register*	BRDR	32	H'FFFFF3D4		32	
Execution times break register*	BETR	16	H'FFFFF3DC		16	

Note: * The UBC registers are not supported on 32 Kbyte versions (SH71251A, SH7
and 16 Kbyte versions (SH71250A, SH71240A).

SCSCR_0	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]		
SCTDR_0									
SCSSR_0	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SCRDR_0									
SCSDCR_0	—	—	—	—	DIR	—	—	—	
SCSPTR_0	EIO	—	—	—	SPB1IO	SPB1DT	SPB0IO	SPB0DT	
SCSMR_1	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS[1:0]		SC
SCBRR_1									(Ch
SCSCR_1	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]		
SCTDR_1									
SCSSR_1	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SCRDR_1									
SCSDCR_1	—	—	—	—	DIR	—	—	—	
SCSPTR_1	EIO	—	—	—	SPB1IO	SPB1DT	SPB0IO	SPB0DT	
SCSMR_2	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS[1:0]		SC
SCBRR_2									(Ch
SCSCR_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]		
SCTDR_2									
SCSSR_2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SCRDR_2									
SCSDCR_2	—	—	—	—	DIR	—	—	—	
SCSPTR_2	EIO	—	—	—	SPB1IO	SPB1DT	SPB0IO	SPB0DT	

TIORL_4	IOD[3:0]				IOC[3:0]			
TIER_3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
TIER_4	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
TOER	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
TGCR	—	BDC	N	P	FB	WF	VF	UF
TOCR1	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
TOCR2	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
TCNT_3								
TCNT_4								
TCDR								
TDDR								
TGRA_3								
TGRB_3								
TGRA_4								
TGRB_4								

TGRC_4								
TGRD_4								
TSR_3	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
TSR_4	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
TITCR	T3AEN	3ACOR[2:0]			T4VEN	4VCOR[2:0]		
TITCNT	—	3ACNT[2:0]			—	4VCNT[2:0]		
TBTER	—	—	—	—	—	—	BTE[1:0]	
TDER	—	—	—	—	—	—	—	TDER
TOLBR	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
TBTM_3	—	—	—	—	—	—	TTSB	TTSA
TBTM_4	—	—	—	—	—	—	TTSB	TTSA
TADCR	BF[1:0]		—	—	—	—	—	—
	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
TADCORA_4								
TADCORB_4								
TADCOBRA_4								
TADCOBRB_4								

TIORL_0	IOD[3:0]				IOC[3:0]			
TIER_0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
TSR_0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
TCNT_0								
TGRA_0								
TGRB_0								
TGRC_0								
TGRD_0								
TGRE_0								
TGRF_0								
TIER2_0	TTGE2	—	—	—	—	—	TGIEF	TGIEE
TSR2_0	—	—	—	—	—	—	TGFF	TGFE
TBTM_0	—	—	—	—	—	TTSE	TTSB	TTSA
TCR_1	—	CCLR[1:0]		CKEG[1:0]		TPSC[2:0]		
TMDR_1	—	—	—	—	MD[3:0]			
TIOR_1	IOB[3:0]				IOA[3:0]			

TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE
TCR_2	—	CCLR[1:0]		CKEG[1:0]		TPSC[2:0]		
TMDR_2	—	—	—	—	MD[3:0]			
TIOR_2	IOB[3:0]				IOA[3:0]			
TIER_2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
TSR_2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
TCNT_2								
TGRA_2								
TGRB_2								
TCNTU_5								
TGRU_5								
TCRU_5	—	—	—	—	—	—	TPSC[1:0]	
TIORU_5	—	—	—	IOC[4:0]				
TCNTV_5								
TGRV_5								
TCRV_5	—	—	—	—	—	—	TPSC[1:0]	

TSR_5	—	—	—	—	—	CMFU5	CMFV5	CMFW5	
TIER_5	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W	
TSTR_5	—	—	—	—	—	CSTU5	CSTV5	CSTW5	
TCNTCMPCLR	—	—	—	—	—	CMPCLR5U	CMPCLR5V	CMPCLR5W	
ADDR0	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A
	AD1	AD0	—	—	—	—	—	—	
ADDR1	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR2	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR3	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADCSR_0	ADF	ADIE	—	—	TRGE	—	CONADF	STC	
	CKSL[1:0]		ADM[1:0]		ADCS	CH[2:0]			
ADCR_0	—	—	ADST	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
ADDR4	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A
	AD1	AD0	—	—	—	—	—	—	
ADDR5	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR6	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR7	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	

FKEY	K[7:0]								
FTDAR	TDER	TDA[6:0]							
CMSTR	—	—	—	—	—	—	—	—	CM
	—	—	—	—	—	—	STR1	STR0	
CMCSR_0	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS[1:0]		
CMCNT_0									
CMCOR_0									
CMCSR_1	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS[1:0]		
CMCNT_1									
CMCOR_1									
ICSR1	POE3F	—	POE1F	POE0F	—	—	—	PIE1	PO
	POE3M[1:0]		—	—	POE1M[1:0]		POE0M[1:0]		
OCSR1	OSF1	—	—	—	—	—	OCE1	OIE1	
	—	—	—	—	—	—	—	—	
ICSR3	—	—	—	POE8F	—	—	POE8E	PIE3	
	—	—	—	—	—	—	POE8M[1:0]		
SPOER	—	—	—	—	—	—	MTU2CH0HIZ	MTU2CH34HIZ	

PAIORL (SH7125)	PA15IOR	PA14IOR	PA13IOR	PA12IOR	PA11IOR	PA10IOR	PA9IOR	PA8IOR	P
	PA7IOR	PA6IOR	PA5IOR	PA4IOR	PA3IOR	PA2IOR	PA1IOR	PA0IOR	
PAIORL (SH7124)	—	—	—	—	—	—	PA9IOR	PA8IOR	
	PA7IOR	PA6IOR	—	PA4IOR	PA3IOR	—	PA1IOR	PA0IOR	
PACRL4 (SH7125)	—	PA15MD2	PA15MD1	PA15MD0	—	PA14MD2	PA14MD1	PA14MD0	
	—	PA13MD2	PA13MD1	PA13MD0	—	PA12MD2	PA12MD1	PA12MD0	
PACRL4 (SH7124)	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
PACRL3 (SH7125)	—	PA11MD2	PA11MD1	PA11MD0	—	PA10MD2	PA10MD1	PA10MD0	
	—	PA9MD2	PA9MD1	PA9MD0	—	PA8MD2	PA8MD1	PA8MD0	
PACRL3 (SH7124)	—	—	—	—	—	—	—	—	
	—	PA9MD2	PA9MD1	PA9MD0	—	PA8MD2	PA8MD1	PA8MD0	
PACRL2 (SH7125)	—	PA7MD2	PA7MD1	PA7MD0	—	PA6MD2	PA6MD1	PA6MD0	
	—	PA5MD2	PA5MD1	PA5MD0	—	PA4MD2	PA4MD1	PA4MD0	
PACRL2 (SH7124)	—	PA7MD2	PA7MD1	PA7MD0	—	PA6MD2	PA6MD1	PA6MD0	
	—	—	—	—	—	PA4MD2	PA4MD1	PA4MD0	
PACRL1 (SH7125)	—	PA3MD2	PA3MD1	PA3MD0	—	PA2MD2	PA2MD1	PA2MD0	
	—	PA1MD2	PA1MD1	PA1MD0	—	PA0MD2	PA0MD1	PA0MD0	
PACRL1 (SH7124)	—	PA3MD2	PA3MD1	PA3MD0	—	—	—	—	
	—	PA1MD2	PA1MD1	PA1MD0	—	PA0MD2	PA0MD1	PA0MD0	
PAPRL (SH7125)	PA15PR	PA14PR	PA13PR	PA12PR	PA11PR	PA10PR	PA9PR	PA8PR	I/
	PA7PR	PA6PR	PA5PR	PA4PR	PA3PR	PA2PR	PA1PR	PA0PR	
PAPRL (SH7124)	—	—	—	—	—	—	PA9PR	PA8PR	
	PA7PR	PA6PR	—	PA4PR	PA3PR	—	PA1PR	PA0PR	

	—	—	PB5DR	—	PB3DR	—	PB1DR	—
PBIORH (SH7125)	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	PB16IOR
PBIORH (SH7124)	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
PBIORL (SH7125)	—	—	—	—	—	—	—	—
	—	—	PB5IOR	—	PB3IOR	PB2IOR	PB1IOR	—
PBIORL (SH7124)	—	—	—	—	—	—	—	—
	—	—	PB5IOR	—	PB3IOR	—	PB1IOR	—
PBCRH1 (SH7125)	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	PB16MD
PBCRH1 (SH7124)	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
PBCRL2 (SH7125)	—	—	—	—	—	—	—	—
	—	PB5MD2	PB5MD1	PB5MD0	—	—	—	—
PBCRL2 (SH7124)	—	—	—	—	—	—	—	—
	—	PB5MD2	PB5MD1	PB5MD0	—	—	—	—
PBCRL1 (SH7125)	—	PB3MD2	PB3MD1	PB3MD0	—	PB2MD2	PB2MD1	PB2MD0
	—	PB1MD2	PB1MD1	PB1MD0	—	—	—	—
PBCRL1 (SH7124)	—	PB3MD2	PB3MD1	PB3MD0	—	—	—	—
	—	PB1MD2	PB1MD1	PB1MD0	—	—	—	—

	—	—	PB5PR	—	PB3PR	—	PB1PR	—	
PEDRL (SH7125)	PE15DR	PE14DR	PE13DR	PE12DR	PE11DR	PE10DR	PE9DR	PE8DR	
	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR	
PEDRL (SH7124)	PE15DR	PE14DR	PE13DR	PE12DR	PE11DR	PE10DR	PE9DR	PE8DR	
	—	—	—	—	PE3DR	PE2DR	PE1DR	PE0DR	
PEIORL (SH7125)	PE15IOR	PE14IOR	PE13IOR	PE12IOR	PE11IOR	PE10IOR	PE9IOR	PE8IOR	P
	PE7IOR	PE6IOR	PE5IOR	PE4IOR	PE3IOR	PE2IOR	PE1IOR	PE0IOR	
PEIORL (SH7124)	PE15IOR	PE14IOR	PE13IOR	PE12IOR	PE11IOR	PE10IOR	PE9IOR	PE8IOR	
	—	—	—	—	PE3IOR	PE2IOR	PE1IOR	PE0IOR	
PECRL4	—	PE15MD2	PE15MD1	PE15MD0	—	PE14MD2	PE14MD1	PE14MD0	
	—	—	PE13MD1	PE13MD0	—	PE12MD2	PE12MD1	PE12MD0	
PECRL3	—	PE11MD2	PE11MD1	PE11MD0	—	PE10MD2	PE10MD1	PE10MD0	
	—	PE9MD2	PE9MD1	PE9MD0	—	PE8MD2	PE8MD1	PE8MD0	
PECRL2 (SH7125)	—	PE7MD2	PE7MD1	PE7MD0	—	PE6MD2	PE6MD1	PE6MD0	
	—	PE5MD2	PE5MD1	PE5MD0	—	PE4MD2	PE4MD1	PE4MD0	
PECRL2 (SH7124)	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
PECRL1	—	PE3MD2	PE3MD1	PE3MD0	—	PE2MD2	PE2MD1	PE2MD0	
	—	PE1MD2	PE1MD1	PE1MD0	—	—	PE0MD1	PE0MD0	
PEPRL (SH7125)	PE15PR	PE14PR	PE13PR	PE12PR	PE11PR	PE10PR	PE9PR	PE8PR	I/
	PE7PR	PE6PR	PE5PR	PE4PR	PE3PR	PE2PR	PE1PR	PE0PR	
PEPRL (SH7124)	PE15PR	PE14PR	PE13PR	PE12PR	PE11PR	PE10PR	PE9PR	PE8PR	
	—	—	—	—	PE3PR	PE2PR	PE1PR	PE0PR	

STBCR2	MSTP7	—	—	—	—	—	—	—	
STBCR3	—	—	MSTP13	MSTP12	MSTP11	—	—	—	
STBCR4	—	MSTP22	MSTP21	—	—	—	MSTP17	MSTP16	
STBCR5	—	—	—	—	—	—	MSTP[25:24]		
STBCR6	UBCRST	HIZ	—	—	—	—	STBYMD	—	
WTCNT									WD
WTCSR	TME	WT/IT	RSTS	WOVF	IOVF	CKS[2:0]			
OSCCR	—	—	—	—	—	OSCSTOP	—	OSCERS	CP
RAMCR	—	—	—	RAME	—	—	—	—	Po mo
ADTSR_0	TRG11S[3:0]				TRG01S[3:0]				A/D
	TRG1S[3:0]				TRG0S[3:0]				
ICR0	NMIL	—	—	—	—	—	—	NMIE	INT
	—	—	—	—	—	—	—	—	
IRQCR	—	—	—	—	—	—	—	—	
	IRQ31S	IRQ30S	IRQ21S	IRQ20S	IRQ11S	IRQ10S	IRQ01S	IRQ00S	
IRQSR	—	—	—	—	IRQ3L	IRQ2L	IRQ1L	IRQ0L	
	—	—	—	—	IRQ3F	IRQ2F	IRQ1F	IRQ0F	
IPRA	IRQ0	IRQ0	IRQ0	IRQ0	IRQ1	IRQ1	IRQ1	IRQ1	
	IRQ2	IRQ2	IRQ2	IRQ2	IRQ3	IRQ3	IRQ3	IRQ3	
IPRB	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
IPRC	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	

	—	—	—	—	—	—	—	—	
IPRI	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
IPRJ	CMT_0	CMT_0	CMT_0	CMT_0	CMT_1	CMT_1	CMT_1	CMT_1	
	—	—	—	—	WDT	WDT	WDT	WDT	
IPRK	A/D_0,1	A/D_0,1	A/D_0,1	A/D_0,1	—	—	—	—	
	—	—	—	—	—	—	—	—	
IPRL	SCI_0	SCI_0	SCI_0	SCI_0	SCI_1	SCI_1	SCI_1	SCI_1	
	SCI_2	SCI_2	SCI_2	SCI_2	—	—	—	—	
IPRM	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
BARA	BAA31	BAA30	BAA29	BAA28	BAA27	BAA26	BAA25	BAA24	U
	BAA23	BAA22	BAA21	BAA20	BAA19	BAA18	BAA17	BAA16	
	BAA15	BAA14	BAA13	BAA12	BAA11	BAA10	BAA9	BAA8	
	BAA7	BAA6	BAA5	BAA4	BAA3	BAA2	BAA1	BAA0	
BAMRA	BAMA31	BAMA30	BAMA29	BAMA28	BAMA27	BAMA26	BAMA25	BAMA24	
	BAMA23	BAMA22	BAMA21	BAMA20	BAMA19	BAMA18	BAMA17	BAMA16	
	BAMA15	BAMA14	BAMA13	BAMA12	BAMA11	BAMA10	BAMA9	BAMA8	
	BAMA7	BAMA6	BAMA5	BAMA4	BAMA3	BAMA2	BAMA1	BAMA0	
BBRA	—	—	—	—	—	CPA[2:0]			
	CDA[1:0]		IDA[1:0]		RWA[1:0]		SZA[1:0]		

	BDMA7	BDMA6	BDMA5	BDMA4	BDMA3	BDMA2	BDMA1	BDMA0
BARB	BAB31	BAB30	BAB29	BAB28	BAB27	BAB26	BAB25	BAB24
	BAB23	BAB22	BAB21	BAB20	BAB19	BAB18	BAB17	BAB16
	BAB15	BAB14	BAB13	BAB12	BAB11	BAB10	BAB9	BAB8
	BAB7	BAB6	BAB5	BAB4	BAB3	BAB2	BAB1	BAB0
BAMRB	BAMB31	BAMB30	BAMB29	BAMB28	BAMB27	BAMB26	BAMB25	BAMB24
	BAMB23	BAMB22	BAMB21	BAMB20	BAMB19	BAMB18	BAMB17	BAMB16
	BAMB15	BAMB14	BAMB13	BAMB12	BAMB11	BAMB10	BAMB9	BAMB8
	BAMB7	BAMB6	BAMB5	BAMB4	BAMB3	BAMB2	BAMB1	BAMB0
BBRB	—	—	—	—	—	CPB[2:0]		
	CDB[1:0]		IDB[1:0]		RWB[1:0]		SZB[1:0]	
BDRB	BDB31	BDB30	BDB29	BDB28	BDB27	BDB26	BDB25	BDB24
	BDB23	BDB22	BDB21	BDB20	BDB19	BDB18	BDB17	BDB16
	BDB15	BDB14	BDB13	BDB12	BDB11	BDB10	BDB9	BDB8
	BDB7	BDB6	BDB5	BDB4	BDB3	BDB2	BDB1	BDB0
BDMRB	BDMB31	BDMB30	BDMB29	BDMB28	BDMB27	BDMB26	BDMB25	BDMB24
	BDMB23	BDMB22	BDMB21	BDMB20	BDMB19	BDMB18	BDMB17	BDMB16
	BDMB15	BDMB14	BDMB13	BDMB12	BDMB11	BDMB10	BDMB9	BDMB8
	BDMB7	BDMB6	BDMB5	BDMB4	BDMB3	BDMB2	BDMB1	BDMB0
BRCR	—	—	—	—	—	—	—	—
	—	—	—	—	UBIDB	—	UBIDA	—
	SCMFCA	SCMFCB	SCMFDA	SCMFDB	PCTE	PCBA	—	—
	DBEA	PCBB	DBEB	—	SEQ	—	—	ETBE

	BDA7	BDA6	BDA5	BDA4	BDA3	BDA2	BDA1	BDA0
BETR	—	—	—	—	BET[11:8]			
	BET[7:0]							

Note: * The UBC registers are not supported on 32 Kbyte versions (SH71251A, SH7 and 16 Kbyte versions (SH71250A, SH71240A).

SCRDR_0	Initialized	Retained	Initialized	Initialized	Retained	
SCSDCR_0	Initialized	Retained	Initialized	Initialized	Retained	
SCSPTR_0	Initialized	Retained	Initialized	Initialized	Retained	
SCSMR_1	Initialized	Retained	Initialized	Initialized	Retained	SCI (Ch
SCBRR_1	Initialized	Retained	Initialized	Initialized	Retained	
SCSCR_1	Initialized	Retained	Initialized	Initialized	Retained	
SCTDR_1	Initialized	Retained	Initialized	Initialized	Retained	
SCSSR_1	Initialized	Retained	Initialized	Initialized	Retained	
SCRDR_1	Initialized	Retained	Initialized	Initialized	Retained	
SCSDCR_1	Initialized	Retained	Initialized	Initialized	Retained	
SCSPTR_1	Initialized	Retained	Initialized	Initialized	Retained	
SCSMR_2	Initialized	Retained	Initialized	Initialized	Retained	SCI (Ch
SCBRR_2	Initialized	Retained	Initialized	Initialized	Retained	
SCSCR_2	Initialized	Retained	Initialized	Initialized	Retained	
SCTDR_2	Initialized	Retained	Initialized	Initialized	Retained	
SCSSR_2	Initialized	Retained	Initialized	Initialized	Retained	
SCRDR_2	Initialized	Retained	Initialized	Initialized	Retained	
SCSDCR_2	Initialized	Retained	Initialized	Initialized	Retained	
SCSPTR_2	Initialized	Retained	Initialized	Initialized	Retained	
TCR_3	Initialized	Retained	Initialized	Initialized	Retained	MTU
TCR_4	Initialized	Retained	Initialized	Initialized	Retained	
TMDR_3	Initialized	Retained	Initialized	Initialized	Retained	
TMDR_4	Initialized	Retained	Initialized	Initialized	Retained	
TIORH_3	Initialized	Retained	Initialized	Initialized	Retained	

TOCR1	Initialized	Retained	Initialized	Initialized	Retained
TOCR2	Initialized	Retained	Initialized	Initialized	Retained
TCNT_3	Initialized	Retained	Initialized	Initialized	Retained
TCNT_4	Initialized	Retained	Initialized	Initialized	Retained
TCDR	Initialized	Retained	Initialized	Initialized	Retained
TDDR	Initialized	Retained	Initialized	Initialized	Retained
TGRA_3	Initialized	Retained	Initialized	Initialized	Retained
TGRB_3	Initialized	Retained	Initialized	Initialized	Retained
TGRA_4	Initialized	Retained	Initialized	Initialized	Retained
TGRB_4	Initialized	Retained	Initialized	Initialized	Retained
TCNTS	Initialized	Retained	Initialized	Initialized	Retained
TCBR	Initialized	Retained	Initialized	Initialized	Retained
TGRC_3	Initialized	Retained	Initialized	Initialized	Retained
TGRD_3	Initialized	Retained	Initialized	Initialized	Retained
TGRC_4	Initialized	Retained	Initialized	Initialized	Retained
TGRD_4	Initialized	Retained	Initialized	Initialized	Retained
TSR_3	Initialized	Retained	Initialized	Initialized	Retained
TSR_4	Initialized	Retained	Initialized	Initialized	Retained
TITCR	Initialized	Retained	Initialized	Initialized	Retained
TITCNT	Initialized	Retained	Initialized	Initialized	Retained
TBTER	Initialized	Retained	Initialized	Initialized	Retained
TDER	Initialized	Retained	Initialized	Initialized	Retained
TOLBR	Initialized	Retained	Initialized	Initialized	Retained
TBTM_3	Initialized	Retained	Initialized	Initialized	Retained

TSTR	Initialized	Retained	Initialized	Initialized	Retained
TSYR	Initialized	Retained	Initialized	Initialized	Retained
TRWER	Initialized	Retained	Initialized	Initialized	Retained
TCR_0	Initialized	Retained	Initialized	Initialized	Retained
TMDR_0	Initialized	Retained	Initialized	Initialized	Retained
TIORH_0	Initialized	Retained	Initialized	Initialized	Retained
TIORL_0	Initialized	Retained	Initialized	Initialized	Retained
TIER_0	Initialized	Retained	Initialized	Initialized	Retained
TSR_0	Initialized	Retained	Initialized	Initialized	Retained
TCNT_0	Initialized	Retained	Initialized	Initialized	Retained
TGRA_0	Initialized	Retained	Initialized	Initialized	Retained
TGRB_0	Initialized	Retained	Initialized	Initialized	Retained
TGRC_0	Initialized	Retained	Initialized	Initialized	Retained
TGRD_0	Initialized	Retained	Initialized	Initialized	Retained
TGRE_0	Initialized	Retained	Initialized	Initialized	Retained
TGRF_0	Initialized	Retained	Initialized	Initialized	Retained
TIER2_0	Initialized	Retained	Initialized	Initialized	Retained
TSR2_0	Initialized	Retained	Initialized	Initialized	Retained
TBTM_0	Initialized	Retained	Initialized	Initialized	Retained
TCR_1	Initialized	Retained	Initialized	Initialized	Retained
TMDR_1	Initialized	Retained	Initialized	Initialized	Retained
TIOR_1	Initialized	Retained	Initialized	Initialized	Retained
TIER_1	Initialized	Retained	Initialized	Initialized	Retained

TIOR_2	Initialized	Retained	Initialized	Initialized	Retained
TIER_2	Initialized	Retained	Initialized	Initialized	Retained
TSR_2	Initialized	Retained	Initialized	Initialized	Retained
TCNT_2	Initialized	Retained	Initialized	Initialized	Retained
TGRA_2	Initialized	Retained	Initialized	Initialized	Retained
TGRB_2	Initialized	Retained	Initialized	Initialized	Retained
TCNTU_5	Initialized	Retained	Initialized	Initialized	Retained
TGRU_5	Initialized	Retained	Initialized	Initialized	Retained
TCRU_5	Initialized	Retained	Initialized	Initialized	Retained
TIORU_5	Initialized	Retained	Initialized	Initialized	Retained
TCNTV_5	Initialized	Retained	Initialized	Initialized	Retained
TGRV_5	Initialized	Retained	Initialized	Initialized	Retained
TCRV_5	Initialized	Retained	Initialized	Initialized	Retained
TIORV_5	Initialized	Retained	Initialized	Initialized	Retained
TCNTW_5	Initialized	Retained	Initialized	Initialized	Retained
TGRW_5	Initialized	Retained	Initialized	Initialized	Retained
TCRW_5	Initialized	Retained	Initialized	Initialized	Retained
TIORW_5	Initialized	Retained	Initialized	Initialized	Retained
TSR_5	Initialized	Retained	Initialized	Initialized	Retained
TIER_5	Initialized	Retained	Initialized	Initialized	Retained
TSTR5	Initialized	Retained	Initialized	Initialized	Retained
TCNTCMPCLR	Initialized	Retained	Initialized	Initialized	Retained

ADDR5	Initialized	Retained	Initialized	Initialized	Retained	
ADDR6	Initialized	Retained	Initialized	Initialized	Retained	
ADDR7	Initialized	Retained	Initialized	Initialized	Retained	
ADCSR_1	Initialized	Retained	Initialized	Initialized	Retained	
ADCR_1	Initialized	Retained	Initialized	Initialized	Retained	
FCCS	Initialized	Retained	Initialized	Initialized	Retained	FLA
FPCS	Initialized	Retained	Initialized	Initialized	Retained	
FECS	Initialized	Retained	Initialized	Initialized	Retained	
FKEY	Initialized	Retained	Initialized	Initialized	Retained	
FTDAR	Initialized	Retained	Initialized	Initialized	Retained	
CMSTR	Initialized	Retained	Initialized	Initialized	Retained	CMT
CMCSR_0	Initialized	Retained	Initialized	Initialized	Retained	
CMCNT_0	Initialized	Retained	Initialized	Initialized	Retained	
CMCOR_0	Initialized	Retained	Initialized	Initialized	Retained	
CMCSR_1	Initialized	Retained	Initialized	Initialized	Retained	
CMCNT_1	Initialized	Retained	Initialized	Initialized	Retained	
CMCOR_1	Initialized	Retained	Initialized	Initialized	Retained	
ICSR1	Initialized	Retained	Retained	—	Retained	POE
OCSR1	Initialized	Retained	Retained	—	Retained	
ICSR3	Initialized	Retained	Retained	—	Retained	
SPOER	Initialized	Retained	Retained	—	Retained	
POECR1	Initialized	Retained	Retained	—	Retained	
POECR2	Initialized	Retained	Retained	—	Retained	

PBDRH	Initialized	Retained	Retained	—	Retained	
PBDRL	Initialized	Retained	Retained	—	Retained	
PBIORH	Initialized	Retained	Retained	—	Retained	PF
PBIORL	Initialized	Retained	Retained	—	Retained	
PBCRH1	Initialized	Retained	Retained	—	Retained	
PBCRL2	Initialized	Retained	Retained	—	Retained	
PBCRL1	Initialized	Retained	Retained	—	Retained	
PBPRH	Initialized	Retained	Retained	—	Retained	I/C
PBPRL	Initialized	Retained	Retained	—	Retained	
PEDRL	Initialized	Retained	Retained	—	Retained	
PEIORL	Initialized	Retained	Retained	—	Retained	PF
PECRL4	Initialized	Retained	Retained	—	Retained	
PECRL3	Initialized	Retained	Retained	—	Retained	
PECRL2	Initialized	Retained	Retained	—	Retained	
PECRL1	Initialized	Retained	Retained	—	Retained	
PEPRL	Initialized	Retained	Retained	—	Retained	I/C
IFCR	Initialized	Retained	Retained	—	Retained	PF
PFDRL	Initialized	Retained	Retained	—	Retained	I/C
FRQCR	Initialized*[1]	Retained	Retained	—	Retained	CF
STBCR1	Initialized	Retained	Retained	—	Retained	Po m
STBCR2	Initialized	Retained	Retained	—	Retained	
STBCR3	Initialized	Retained	Retained	—	Retained	
STBCR4	Initialized	Retained	Retained	—	Retained	

ICR0	Initialized	Initialized	Retained	—	Retained	INTC
IRQCR	Initialized	Initialized	Retained	—	Retained	
IRQSR	Initialized	Initialized	Retained	—	Retained	
IPRA	Initialized	Initialized	Retained	—	Retained	
IPRB	Initialized	Initialized	Retained	—	Retained	
IPRC	Initialized	Initialized	Retained	—	Retained	
IPRD	Initialized	Initialized	Retained	—	Retained	
IPRE	Initialized	Initialized	Retained	—	Retained	
IPRF	Initialized	Initialized	Retained	—	Retained	
IPRH	Initialized	Initialized	Retained	—	Retained	
IPRI	Initialized	Initialized	Retained	—	Retained	
IPRJ	Initialized	Initialized	Retained	—	Retained	
IPRK	Initialized	Initialized	Retained	—	Retained	
IPRL	Initialized	Initialized	Retained	—	Retained	
IPRM	Initialized	Initialized	Retained	—	Retained	
BARA	Initialized	Retained	Retained	Initialized	Retained	UBC
BAMRA	Initialized	Retained	Retained	Initialized	Retained	
BBRA	Initialized	Retained	Retained	Initialized	Retained	
BDRA	Initialized	Retained	Retained	Initialized	Retained	
BDMRA	Initialized	Retained	Retained	Initialized	Retained	
BARB	Initialized	Retained	Retained	Initialized	Retained	
BAMRB	Initialized	Retained	Retained	Initialized	Retained	
BBRB	Initialized	Retained	Retained	Initialized	Retained	

3. The OSCSTOP bit is initialized.
4. The UBC register is not supported on the 32 Kbyte (SH71251A and SH71241 Kbyte (SH71250A and SH71240A) versions.

Item		Symbol	Value
Power supply voltage		V_{CC}	–0.3 to + 7.0
Input voltage (except analog input)		V_{in}	–0.3 to V_{CC} + 0.3
Analog power supply voltage		AV_{CC}	–0.3 to + 7.0
Analog input voltage		V_{an}	–0.3 to AV_{CC} + 0.3
Operating temperature	Consumer specifications	T_{opr}	–20 to + 85
	Industrial specifications		–40 to + 85
Storage temperature		T_{stg}	–55 to + 125

[Operating Precautions]

Operating the LSI in excess of the absolute maximum ratings may result in permanent da

Input high-level voltage (other than Schmitt trigger input voltage)	$\overline{RES}$, $\overline{MRES}$, NMI, FWE, MD1, $\overline{ASEMD0}$, EXTAL	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	Analog ports		2.2	—	AV_{CC} + 0.3	V	
	Other input pins		2.2	—	V_{CC} + 0.3	V	
Input low-level voltage (other than Schmitt trigger input voltage)	$\overline{RES}$, $\overline{MRES}$, NMI, FWE, MD1, $\overline{ASEMD0}$, EXTAL	V_{IL}	–0.3	—	0.5	V	
	Other input pins		–0.3	—	0.8	V	
Schmitt trigger input voltage	IRQ3 to IRQ0, $\overline{POE8}$, $\overline{POE3}$, $\overline{POE1}$, $\overline{POE0}$, TCLKA to TCLKD, TIOC0A to TIOC0D, TIOC1A, TIOC1B, TIOC2A, TIOC2B, TIOC3A to TIOC3D, TIOC4A to TIOC4D, TIC5U, TIC5V, TIC5WS, SCK0 to SCK3, RXD0 to RXD3	V_{T+}	V_{CC} – 0.5	—	—	V	
		V_{T-}	—	—	1.0	V	
		V_{T+}–V_{T-}	0.4	—	—	V	V_{CC} = 5.5 V
Input leak current	All input pins (except $\overline{ASEMD0}$)	$\| I_{in} \|$	—	—	1.0	μA	
Input pull-up MOS current	$\overline{ASEMD0}$, $\overline{POE3}$	$-I_{pu}$	—	—	800	μA	V_{in} =
Tri-state leakage current (OFF state)	Ports A, B, E	$\| I_{tsi} \|$	—	—	1.0	μA	

			—	—	0.6	V	I_{OL} = 10 mA, V_{CC} = 4.5 V t
			—	—	0.44	V	I_{OL} = 8 mA, V_{CC} = 4.5 V t
	All other output pins		—	—	0.4	V	I_{OL} = 1.6 mA
Input capacitance	All input pins	C_{in}	—	—	20	pF	V_{in} = 0 V f = 1 MHz Ta = 25°C
Supply current	Normal operation	I_{CC}	—	52	70	mA	Iϕ = 50 MHz (SH7125, SH
			—	35	50	mA	Iϕ = 50 MHz (SH71251A, SH71250A,
	Sleep		—	33	50	mA	Iϕ = 50 MHz (SH7125, SH
			—	22	30	mA	Iϕ = 50 MHz (SH71251A, SH71250A,
	Software standby		—	—	5	mA	T_a ≤ 50°C
			—	—	15	mA	50°C < T_a
Analog power supply current	During A/D conversion	AI_{CC}	—	3	5	mA	The value pe
	Waiting for A/D conversion		—	—	2	mA	The value pe
	Standby		—	—	15	μA	

[Operating Precautions]

1. When the A/D converter is not used, do not leave the AV_{CC} and AV_{SS} pins ope
2. The supply current was measured when V_{IH} (Min.) = V_{CC} - 0.5 V, V_{IL} (Max.) = 0 all output pins unloaded.

Permissible current in high-level output (total)	$\Sigma -I_{OH}$	—	—	25

[Operating Precautions]

To assure LSI reliability, do not exceed the output values listed in table 21.3.

Note: * I_{OL} = 15 mA (Max.)/$-I_{OH}$ = 5 mA (Max.) for pins PE9 and PE11 to PE15. Howeve least three pins are permitted to have simultaneously $I_{OL}/-I_{OH} > 2.0$ mA among pins.

21.3 AC Characteristics

Signals input to this LSI are basically handled as signals in synchronization with a clock. setup and hold times for input pins must be followed.

Table 21.4 Maximum Operating Frequency

Conditions: $V_{CC} = AV_{CC}$ = 4.0 V to 5.5 V, $V_{SS} = PLLV_{SS} = AV_{SS}$ = 0 V,
T_a = –20 to +85°C (consumer specifications),
T_a = –40 to +85°C (industrial specifications)

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	CPU (Iϕ)	f	10	—	50	MHz
	Peripheral module (Pϕ)		10	—	40	

EXTAL clock input cycle time	t_{EXcyc}	80	100	ns	
EXTAL clock input low pulse width	t_{EXL}	20	—	ns	
EXTAL clock input high pulse width	t_{EXH}	20	—	ns	
EXTAL clock input rising time	t_{EXr}	—	5	ns	
EXTAL clock input falling time	t_{EXf}	—	5	ns	
CK (Bϕ) clock frequency (reference values)	f_{OP}	10	40	MHz	*
CK (Bϕ) clock cycle time (reference values)	t_{cyc}	25	100	ns	
Power-on oscillation stabilization time	t_{OSC1}	10	—	ms	Figure
Oscillation stabilization time on return from standby 1	t_{OSC2}	10	—	ms	Figure
Oscillation stabilization time on return from standby 2	t_{OSC3}	10	—	ms	Figure

Note: * Depends on the frequency control register (FRQCR).

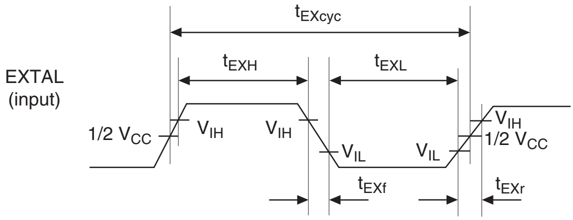
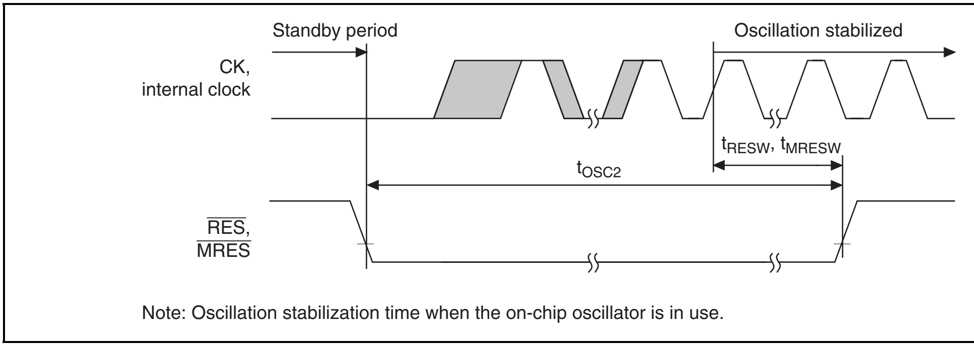
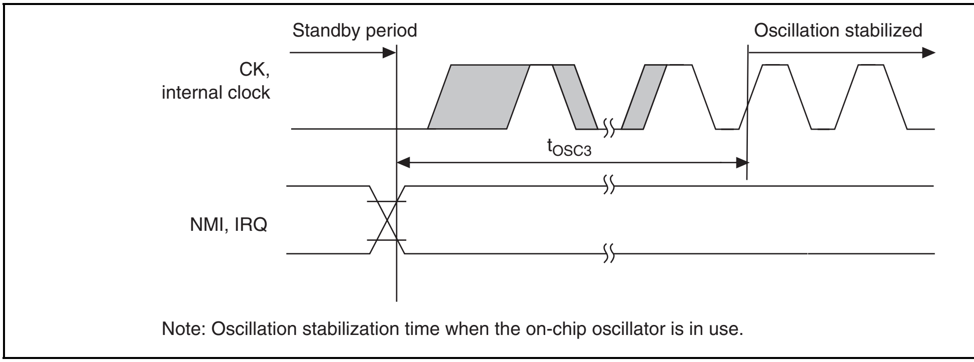


Figure 21.1 Timing of EXTAL Input Clock Signal



Note: Oscillation stabilization time when the on-chip oscillator is in use.

Figure 21.3 Oscillation Stabilization Time on Return from Standby (Return by



Note: Oscillation stabilization time when the on-chip oscillator is in use.

Figure 21.4 Oscillation Stabilization Time on Return from Standby (Return by NMI or IRQ)

$\overline{\text{RES}}$ hold time (reference values)	t_{RESH}	15	—	ns	
$\overline{\text{MRES}}$ pulse width	t_{MRESW}	20*3	—	t_{Bcyc}*4	
$\overline{\text{MRES}}$ setup time*1 (reference values)	t_{MRESS}	25	—	ns	
$\overline{\text{MRES}}$ hold time (reference values)	t_{MRESH}	15	—	ns	
MD1, FWE setup time	t_{MDS}	20	—	t_{Bcyc}*4	Figure 21
NMI setup time*1 (reference values)	t_{NMIS}	60	—	ns	Figure 21
NMI hold time (reference values)	t_{NMIH}	10	—	ns	
IRQ3 to IRQ0 setup time*1 (reference values)	t_{IRQS}	35	—	ns	
IRQ3 to IRQ0 hold time (reference values)	t_{IRQH}	35	—	ns	
$\overline{\text{IRQOUT}}$ output delay time (reference values)	t_{IRQOD}	—	100	ns	Figure 21

Notes: 1. The $\overline{\text{RES}}$, $\overline{\text{MRES}}$, NMI, and IRQ3 to IRQ0 signals are asynchronous signals. setup time is satisfied, change of signal level is detected at the rising edge of If not, the detection is delayed until the rising edge of the clock.

2. In standby mode, $t_{RESW} = t_{OSC2}$ (10 ms).

3. In standby mode, $t_{MRESW} = t_{OSC2}$ (10 ms).

4. t_{Bcyc} indicates the bus clock cycle time (Bϕ = CK).

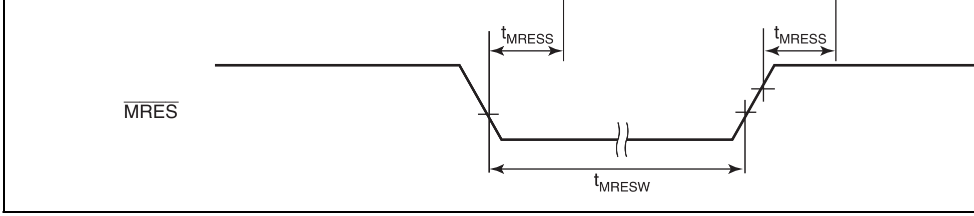


Figure 21.5 Reset Input Timing

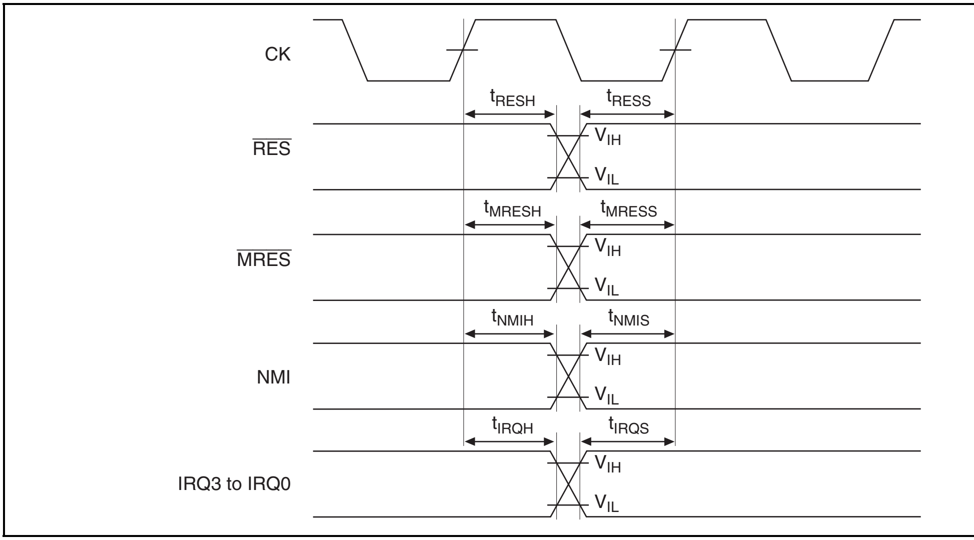


Figure 21.6 Interrupt Signal Input Timing

(reference values)					
Input capture input setup time (reference values)	t_{TICS}	20	—	ns	
Input capture input pulse width (single edge)	$t_{TICWH/L}$	1.5	—	t_{MPcyc}	
Input capture input pulse width (both edges)	$t_{TICWH/L}$	2.5	—	t_{MPcyc}	
Timer input setup time (reference values)	t_{TCKS}	20	—	ns	Figur
Timer clock pulse width (single edge)	$t_{TCKWH/L}$	1.5	—	t_{MPcyc}	
Timer clock pulse width (both edges)	$t_{TCKWH/L}$	2.5	—	t_{MPcyc}	
Timer clock pulse width (phase counting mode)	$t_{TCKWH/L}$	2.5	—	t_{MPcyc}	

Note: t_{MPcyc} indicates the MTU2 clock (MPϕ) cycle.

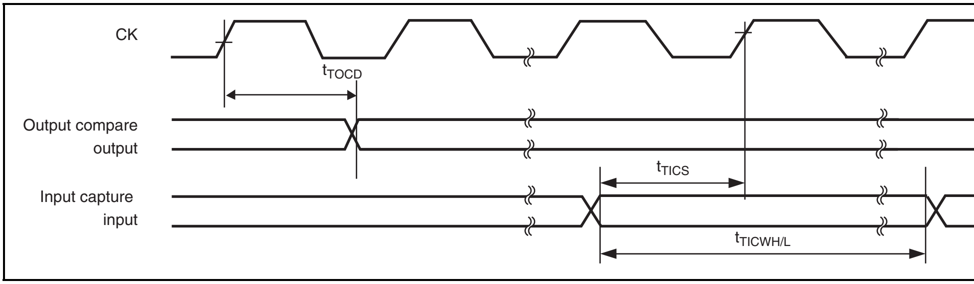


Figure 21.8 MTU2 Input/Output Timing

(reference values)				
Port input low pulse width	t_{PRWL}	2	—	t_{Pcyc}
Port input high pulse width	t_{PRWH}	2	—	t_{Pcyc}

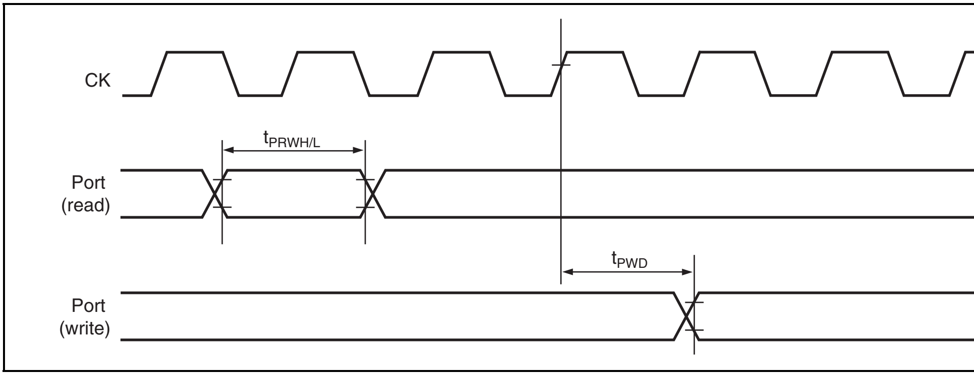


Figure 21.10 I/O Port Input/Output Timing

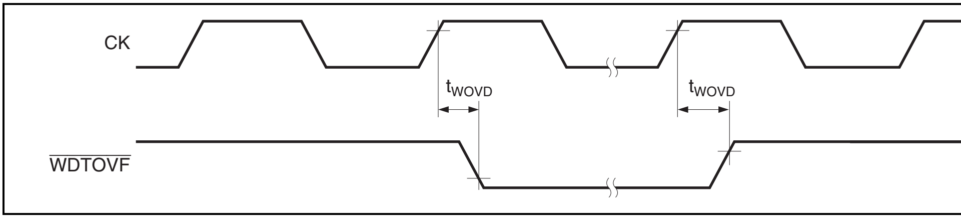


Figure 21.11 WDT Timing

Input clock cycle (clock synchronous)		t_{scyc}	6	—	t_{pcyc}	
Input clock pulse width		t_{sckw}	0.4	0.6	t_{scyc}	
Input clock rising time		t_{sckr}	—	1.5	t_{pcyc}	
Input clock falling time		t_{sckf}	—	1.5	t_{pcyc}	
Transmit data delay time	Asynchronous	t_{TXD}	—	4 t_{pcyc} + 10	ns	F 2
Receive data setup time		t_{RXS}	4 t_{pcyc}	—	ns	
Receive data hold time		t_{RXH}	4 t_{pcyc}	—	ns	
Transmit data delay time	Clock synchronous	t_{TXD}	—	3 t_{pcyc} + 10	ns	
Receive data setup time		t_{RXS}	2 t_{pcyc} + 50	—	ns	
Receive data hold time		t_{RXH}	2 t_{pcyc}	—	ns	

Note: t_{pcyc} indicates the peripheral clock (Pϕ) cycle.

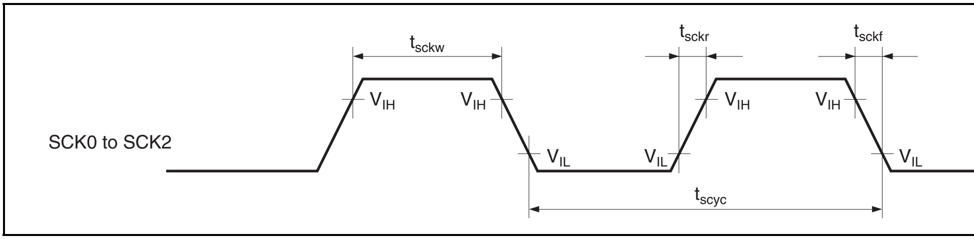
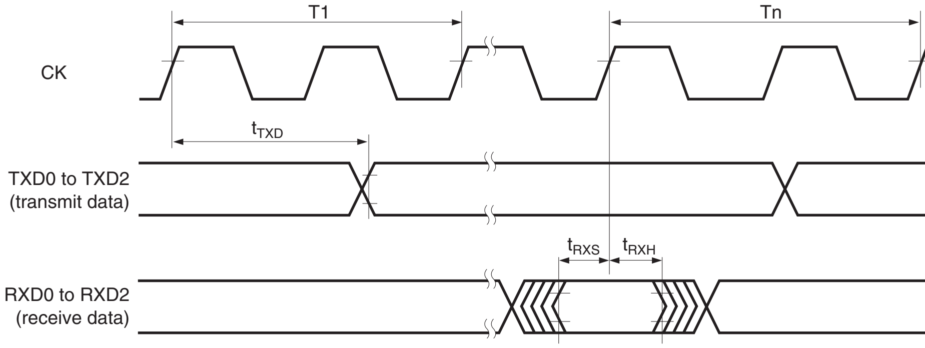


Figure 21.12 Input Clock Timing

SCI input/output timing (clock synchronous mode)



SCI input/output timing (asynchronous mode)

Figure 21.13 SCI Input/Output Timing

(reference values)				
$\overline{\text{POE}}$ input pulse width	t_{POEW}	1.5	—	t_{pcyc}

Note: t_{pcyc} indicates the peripheral clock (Pϕ) cycle.

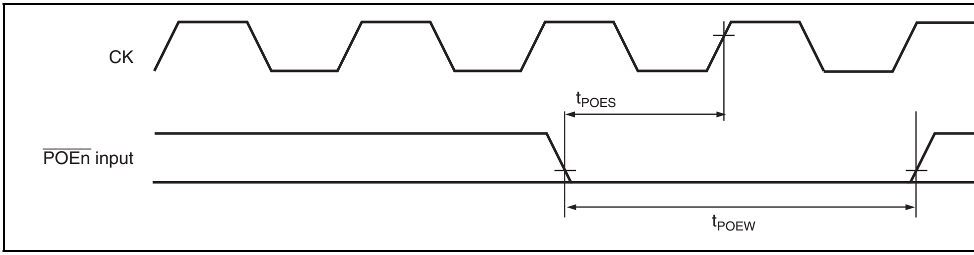


Figure 21.14 $\overline{\text{POE}}$ Input Timing

delay time (reference values)

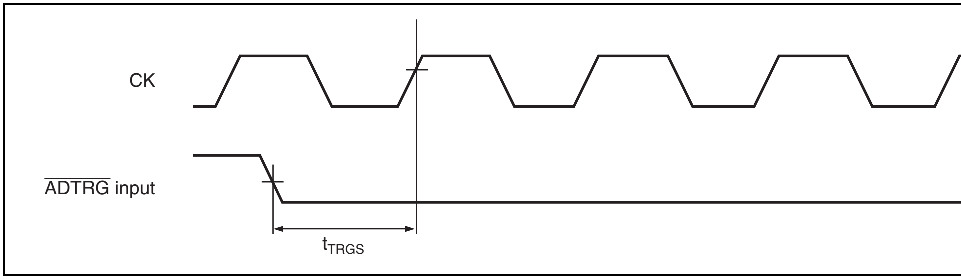
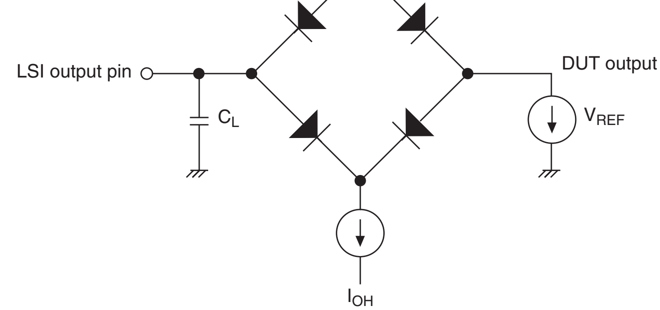


Figure 21.15 External Trigger Input Timing



Notes: 1. C_L is the total value that includes the capacitance of the measurement instrument and is set as follows for the respective pins.
30pF: All other output pins
2. I_{OL} = 1.6 mA and I_{OH} = -200 mA in the test conditions.

Figure 21.16 Output Load Circuit

Analog input capacitance	—	—	20
Permitted analog signal source impedance	—	—	1*[2]/3*[1]
Non-linear error	—	—	±3.0*[1]/±5.0*[2]
Offset error	—	—	±3.0*[1]/±5.0*[2]
Full-scale error	—	—	±3.0*[1]/±5.0*[2]
Quantization error	—	—	±0.5
Absolute error	—	—	±4.0*[1]/±6.0*[2]

Notes: 1. It is assumed that A/D conversion time ≥ 4.0 μs.

2. It is assumed that A/D conversion time < 4.0 μs.

					block
		—	300	800	ms/32 block
		—	600	1500	ms/64 block
Programming time (total) *1*2*4	Σ t_P	—	1.2	3	s/128 K
		—	0.6	1.5	s/64 K
Erase time (total) *1*2*4	Σ t_E	—	1.3	3.5	s/128 K
		—	0.7	2	s/64 K
Programming and erase time (total) *1*2*4	Σ t_{PE}	—	2.5	6.5	s/128 K
		—	1.3	3.5	s/64 K
Reprogramming count	N_{WEC}	100*3	—	—	Times

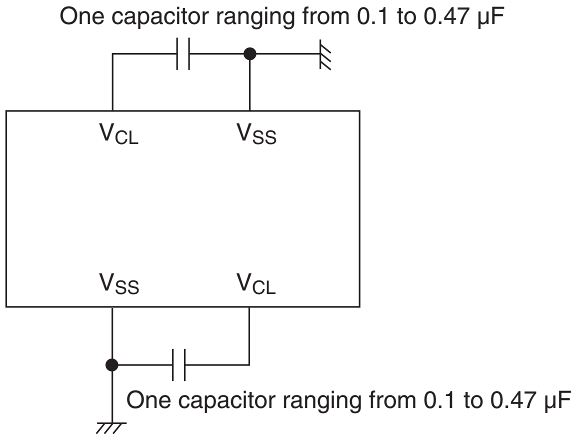
Notes: 1. Programming/erasure time is data-dependent.

2. Programming/erasure time does not include data transfer time.

3. Minimum number to guarantee all the characteristics after reprogramming. (Gu within the range from 1 to min. value)

4. Characteristics when reprogramming is performed within the specified number including min. value.

External power-supply
stabilizing capacitor


One capacitor ranging from 0.1 to 0.47 μF
V_{CL}
V_{SS}
V_{SS}
V_{CL}
One capacitor ranging from 0.1 to 0.47 μF

Note: Do not apply any power supply voltage to the V_{CL} pin.
Use multilayer ceramic capacitors (one capacitor ranging from 0.1 to 0.47 μF for each V_{CL} pin), which should be located near the pin.

Figure 21.17 Connection of V_{CL} Capacitor

		Reset State		Power-Down State			
Type	**Pin Name**	**Power-On**	**Manual**	**Software Standby**	**Sleep**	**Oscillation Stop Detected**	**PO Us**
Clock	XTAL	O	O	L	O	O	O
	EXTAL	I	I	I	I	I	I
System control	RES	I	I	I	I	I	I
	MRES	Z	I	Z	I	Z	I
	WDTOVF	O*[2]	O	O	O	O	O
Operating mode control	MD1	I	I	I	I	I	I
	ASEMD0	I*[3]	I*[3]	I*[3]	I*[3]	I*[3]	I*
	FWE	I	I	I	I	I	I
Interrupt	NMI	I	I	I	I	I	I
	IRQ0 to IRQ3	Z	I	I	I	I	I
	IRQOUT	Z	O	Z	O	Z	O
MTU2	TCLKA to TCLKD	Z	I	Z	I	I	I
	TIOC0A to TIOC0D	Z	I/O	K*[1]	I/O	I/O	Z
	TIOC1A, TIOC1B	Z	I/O	K*[1]	I/O	I/O	I/C
	TIOC2A, TIOC2B	Z	I/O	K*[1]	I/O	I/O	I/C
	TIOC3A, TIOC3C	Z	I/O	K*[1]	I/O	I/O	I/C
	TIOC3B, TIOC3D	Z	I/O	Z	I/O	Z	Z
MTU2	TIOC4A to TIOC4D	Z	I/O	Z	I/O	Z	Z
	TIC5U, TIC5V, TIC5W	Z	I	Z	I	I	I
POE	POE0, POE1, POE8	Z	I	Z	I	I	I
	POE3	I*[3]	I*[3]	Z	I*[3]	I*[3]	I*

I/O Ports	PA0 to PA15	Z	I/O	K*1	I/O	I/O	I/O
	PB1 to PB3, PB5, PB16	Z	I/O	K*1	I/O	I/O	I/O
	PE0 to PE3	Z	I/O	K*1	I/O	I/O	Z
	PE4 to PE8, PE10	Z	I/O	K*1	I/O	I/O	I/O
	PE9, PE11 to PE15	Z	I/O	Z	I/O	Z	Z
	PF0 to PF7	Z	I	Z	I	I	I

[Legend]

I:	Input
O:	Output
H:	High-level output
L:	Low-level output
Z:	High-impedance
K:	Input pins become high-impedance, and output pins retain their state.

Notes: 1. Output pins become high-impedance when the HIZ bit in standby control regis (STBCR6) is set to 1.

2. Becomes input during a power-on reset. Pull-up to prevent erroneous operatio down with a resistance of at least 1 MΩ as required.

3. Pulled-up inside the LSI when there is no input.

	$\overline{\text{WDTOVF}}$	O*2	O	O	O	O	O
Operating mode control	MD1	I	I	I	I	I	I
	$\overline{\text{ASEMD0}}$	I*3	I*3	I*3	I*3	I*3	I*3
	FWE	I	I	I	I	I	I
Interrupt	NMI	I	I	I	I	I	I
	IRQ1 to IRQ3	Z	I	I	I	I	I
	$\overline{\text{IRQOUT}}$	Z	O	Z	O	Z	O
MTU2	TCLKA to TCLKD	Z	I	Z	I	I	I
	TIOC0A to TIOC0D	Z	I/O	K*1	I/O	I/O	Z
	TIOC3A, TIOC3C	Z	I/O	K*1	I/O	I/O	I/O
	TIOC3B, TIOC3D	Z	I/O	Z	I/O	Z	Z
	TIOC4A to TIOC4D	Z	I/O	Z	I/O	Z	Z
	TIC5U, TIC5V, TIC5W	Z	I	Z	I	I	I
POE	$\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE8}}$	Z	I	Z	I	I	I
SCI	SCK0, SCK2	Z	I/O	Z	I/O	I/O	I/O
	RXD0 to RXD2	Z	I	Z	I	I	I
	TXD0 to TXD2	Z	O	O*1	O	O	O
A/D Converter	AN0 to AN7	Z	I	Z	I	I	I

PF0 to PF7	Z	I	Z	I	I	I

[Legend]

I: Input

O: Output

H: High-level output

L: Low-level output

Z: High-impedance

K: Input pins become high-impedance, and output pins retain their state.

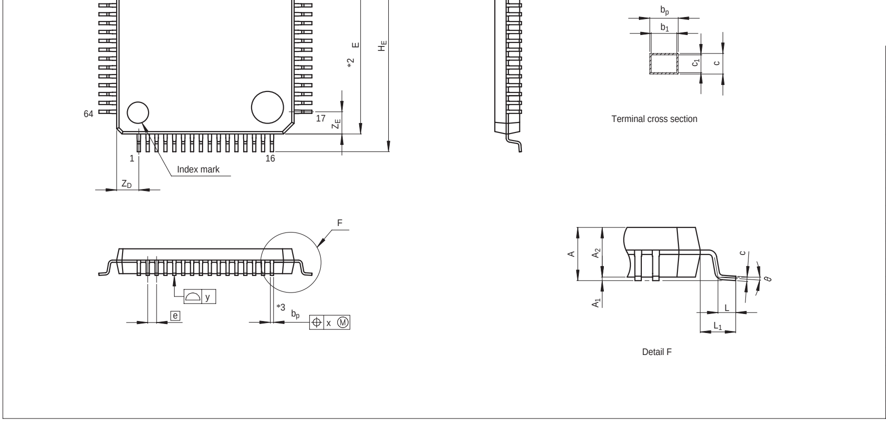
Notes: 1. Output pins become high-impedance when the HIZ bit in standby control regis (STBCR6) is set to 1.

2. Becomes input during a power-on reset. Pull-up to prevent erroneous operatio down with a resistance of at least 1 MΩ as required.

3. Pulled-up inside the LSI when there is no input.

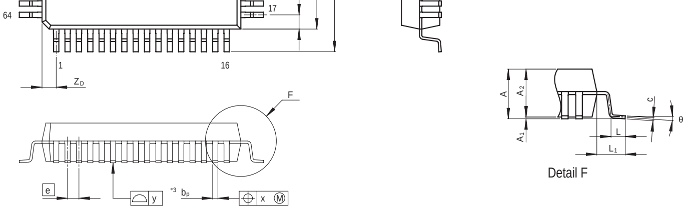
	Flash memory version (on-chip 64-kbyte)	Consumer product	R5F71252N50FP	LQFP-64 (FP-6
		Industrial product	R5F71252D50FP	
		Consumer product	R5F71252N50FA	QFP-64 (FP-64
		Industrial product	R5F71252D50FA	
		Consumer product	R5F71252N50NP	VQFN-64 (TNF
		Industrial product	R5F71252D50NP	
	Flash memory version (on-chip 32-kbyte)	Consumer product	R5F71251AN50FA	QFP-64 (FP-64
		Industrial product	R5F71251AD50FA	
		Consumer product	R5F71251AN50FP	LQFP-64 (FP-6
		Industrial product	R5F71251AD50FP	
		Consumer product	R5F71251AN50NP	VQFN-64 (TNF
		Industrial product	R5F71251AD50NP	
	Flash memory version (on-chip 16-kbyte)	Consumer product	R5F71250AN50FA	QFP-64 (FP-64
		Industrial product	R5F71250AD50FA	
		Consumer product	R5F71250AN50FP	LQFP-64 (FP-6
		Industrial product	R5F71250AD50FP	
		Consumer product	R5F71250AN50NP	VQFN-64 (TNF
		Industrial product	R5F71250AD50NP	
SH7124	Flash memory version (on-chip 128-kbyte)	Consumer product	R5F71243N50FP	LQFP-48 (FP-4
		Industrial product	R5F71243D50FP	
		Consumer product	R5F71243N50NP	VQFN-52
		Industrial product	R5F71243D50NP	

	Flash memory version (on-chip 16-kbyte)	Consumer product	R5F71240AN50FP	LQFP-48 (FP-48
		Industrial product	R5F71240AD50FP	
		Consumer product	R5F71240AN50NP	VQFN-52
		Industrial product	R5F71240AD50NP	



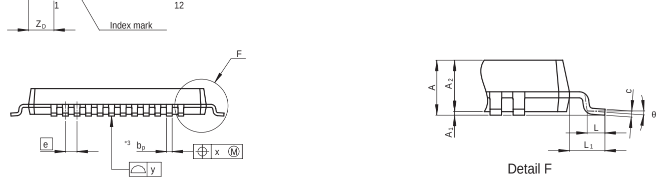
Reference Symbol	D
D	
E	
A_2	-
H_D	1
H_E	1
A	-
A_1	0
b_p	0
b_1	-
c	0
c_1	-
θ	
e	-
x	-
y	-
Z_D	-
Z_E	-
L	0
L_1	-

Figure C.1 LQFP-64



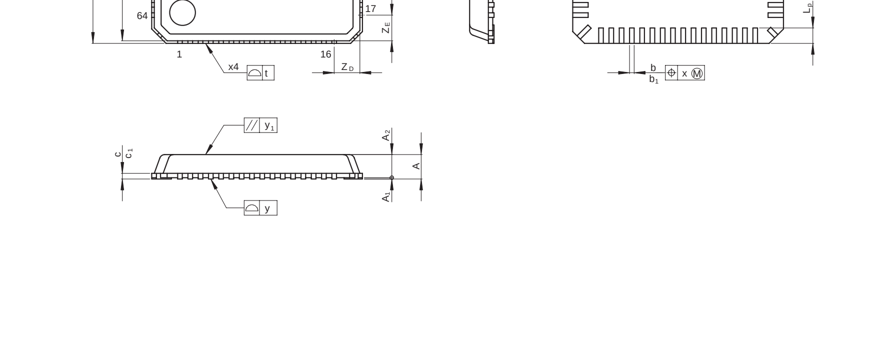
E	—
A_2	—
H_D	17
H_E	17
A	—
A_1	0.0
b_p	0.2
b_1	—
c	0.1
c_1	—
θ	0
$\boxed{e}$	—
x	—
y	—
Z_D	—
Z_E	—
L	0.
L_1	—

Figure C.2 QFP-64



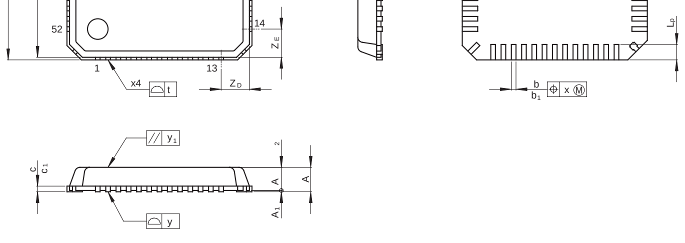
E	-
A_2	-
H_D	1
H_E	1
A	-
A_1	0
b_p	0
b_1	-
c	0
c_1	-
θ	
e	-
x	-
y	-
Z_D	-
Z_E	-
L	
L_1	-

Figure C.3 LQFP-48



D	—
E	—
A_2	—
A	—
A_1	0.00
b	0.13
b_1	—
$\boxed{e}$	—
L_p	0.50
x	—
y	—
y_1	—
t	—
H_D	—
H_E	—
Z_D	—
Z_E	—
c	0.17
c_1	—

Figure C.4 VQFN-64



D	–
E	–
A_2	–
A	–
A_1	0.(
b	0
b_1	–
$\boxed{e}$	–
L_p	0
x	–
y	–
y_1	–
t	–
H_D	–
H_E	–
Z_D	–
Z_E	–
c	0
c_1	–

Figure C.5 VQFN-52

3 Table amended

Items	Specification
User debugging interface (H-UDI)*	• E10A emulator support

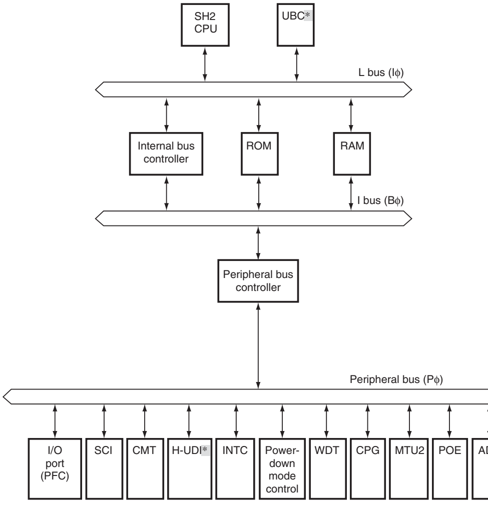
5 Note added

Note: * The 32 Kbyte (SH71251A and SH712
16 Kbyte (SH71250A and SH71240A
are not supported.

1.2 Block Diagram

Figure 1.1 Block Diagram

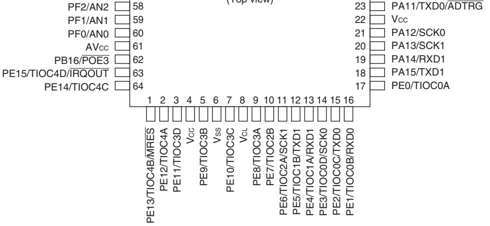
6 Figure amended



[Legend]

ROM:	On-chip ROM	PFC:	Pin function controller
RAM:	On-chip RAM	MTU2:	Multi-function timer pulse unit 2
UBC*:	User break controller	POE:	Port output enable
H-UDI*:	User debugging interface	SCI:	Serial communication interface
INTC:	Interrupt controller	CMT:	Compare match timer
CPG:	Clock pulse generator	ADC:	A/D converter
WDT:	Watchdog timer		
CPU:	Central processing unit		

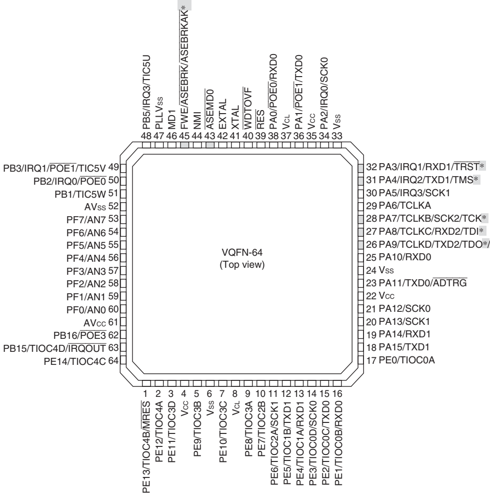
Note: * The 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versi



□ Pins for the system development tool.
When these pins are used for an on-chip
debugger, they are not available.

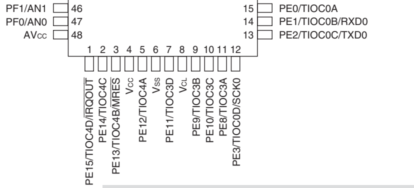
Note: * Pins ASEBRK, ASEBRKAK, TRST, TMS, TCK, TDI, and IDO a
on the 32 Kbyte version (SH71251A) and 16 Kbyte version (SH

Figure 1.2 (2) Pin Assignments of SH7125	8	Figure amended



□ Pins for the system development tool.
When these pins are used for an on-chip
debugger, they are not available.

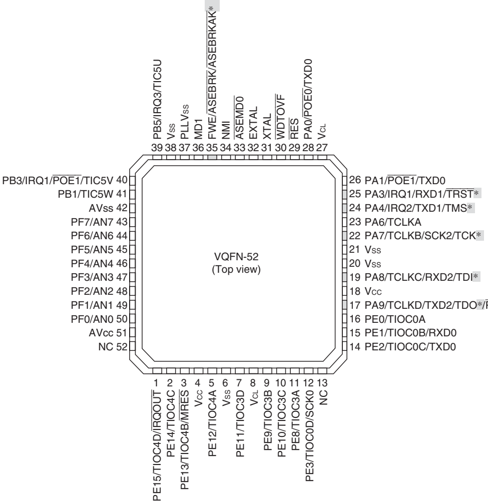
Note: * Pins ASEBRK, ASEBRKAK, TRST, TMS, TCK, TDI, and IDO a
on the 32 Kbyte version (SH71251A) and 16 Kbyte version (SH



□ Pins for the system development tool. When these pins are used for an on-chip debugger, they are not available.

Note: * Pins ASEBRK, ASEBRKAK, TRST, TMS, TCK, TDI, and ID
on the 32 Kbyte version (SH71241A) and 16 Kbyte version

Figure 1.3 (2) Pin Assignments of SH7124	10	Figure amended



□ Pins for the system development tool. When these pins are used for an on-chip debugger, they are not available.

Note: * Pins ASEBRK, ASEBRKAK, TRST, TMS, TCK, TDI, and I
on the 32 Kbyte version (SH71241A) and 16 Kbyte versio

				ground (0 V) correctl
User debugging interface (H-UDI)*1	TCK	I	Test clock	Test-clock input pin
	TMS	I	Test mode select	Inputs the test-mode
	TDI	I	Test data input	Serial input pin for ins data
	TDO	O	Test data output	Serial output pin for i data
	TRST	I	Test reset	Initialization-signal in

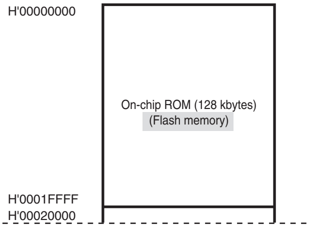
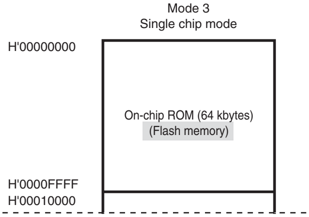
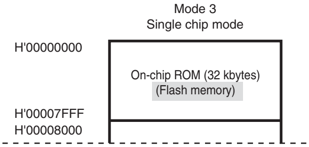
15 Table amended

Classification	Symbol	I/O	Name	Function
E10A interface	ASEMD0*2	I	ASE mode	Sets the ASE mode. When a low-level sig this pin, the MCU ent When a high-level sig MCU enters normal r operation mode or or memory programmin Emulator-specific fun available in ASE moc signal is input, this pi internally. If only normal mode v up the pin by connec
	ASEBRK*2	I	Break request	E10A emulator break
	ASEBRKAK*2	O	Break mode acknowledge	Indicates that the E1(entered its break moc

15 Note added

Notes: *1 This pin function is not supported o Kbyte (SH71250A and SH71240A) Kbyte (SH71251A and SH71241A)

*2 On 32 Kbyte versions (SH71251A, SH71241A) and 16 Kbyte versions (SH71250A, SH71240A), connect A to V_{CC} via a resistor and fix it high. N these versions do not support ASEE ASEBRKAK.

SH7125, SH7124 (128 Kbytes Flash Memory Version)		 H'00000000 On-chip ROM (128 kbytes) (Flash memory) H'0001FFFF H'00020000
Figure 3.2 Address Map in SH7125, SH7124 (64 Kbytes Flash Memory Version)	52	Figure amended  Mode 3 Single chip mode H'00000000 On-chip ROM (64 kbytes) (Flash memory) H'0000FFFF H'00010000
Figure 3.3 Address Map in SH71251A and SH71241A (32 Kbytes Flash Memory Version)	53	Figure amended  Mode 3 Single chip mode H'00000000 On-chip ROM (32 kbytes) (Flash memory) H'00007FFF H'00008000
Figure 3.4 Address Map in SH71250A and SH71240A (16 Kbytes Flash Memory Version)	54	Figure added

Note added

Note: * The UBC is not supported on 32 Kb
versions (SH71251A, SH71241A) a
Kbyte versions (SH71250A, SH712

5.1.1 Types of Exception Handling and Priority

Table 5.1 Types of Exceptions and Priority

73

Table amended

Exception	Exception Source
Interrupt	User break (break before instruction execution)*3
Interrupt	User break (break after instruction execution or operand b
	NMI
	IRQ
	On-chip peripheral modules

Note added

Notes: 3. The user break interrupt is not gene
the 32 Kbyte (SH71251A and SH71
and 16 Kbyte (SH71250A and SH71
versions.

5.1.3 Exception Handling Vector Table

Table 5.3 Vector Numbers and Vector Table Address Offsets

75

Table amended

Exception Handling Source		Vector Number	Vector Table Addre
Interrupt	NMI	11	H'0000002C to H'00
	User break*1	12	H'00000030 to H'00

76

Note added

Notes: 1. Reserved on the 32 Kbyte (SH7125
SH71241A) and 16 Kbyte (SH7125
SH71240A) versions.

5.4.1 Interrupt Sources

Table 5.7 Interrupt Sources

81

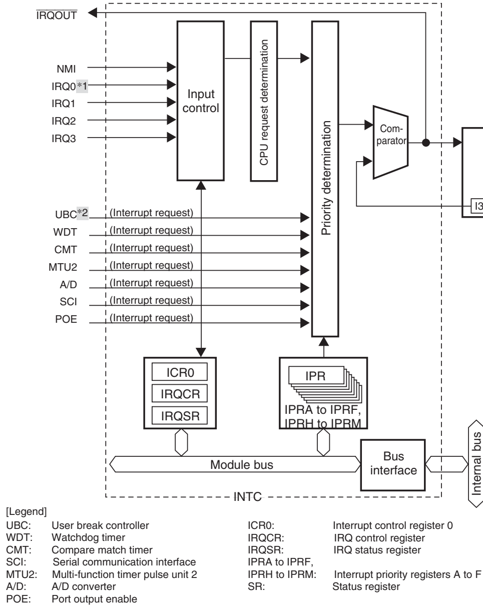
Table amended

Type	Request Source
User break*	User break controller (UBC)

Note: The user break interrupt is not gen
the 32 Kbyte (SH71251A and SH7
and 16 Kbyte (SH71250A and SH7
versions.

6.1 Features — 92 — Figure amended

Figure 6.1 Block Diagram of INTC



Note: *1 Supported only by the SH7125.
*2 The 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versio

6.4.3 User Break Interrupt* — 105 — Note added

Note: * The user break interrupt is not gen
the 32 Kbyte (SH71251A and SH7
and 16 Kbyte (SH71250A and SH7
versions.

Table 8.1 Address Map

Address	Type of Memory	Size 128 Kbytes Version	64 Kbytes Version	32 Kbytes Version	16 Ver
H'00000000 to H'00003FFF	On-chip FLASH	128 Kbytes	64 Kbytes	32 Kbytes	16
H'00004000 to H'00007FFF					Res
H'00008000 to H'0000FFFF				Reserved	
H'00010000 to H'0001FFFF			Reserved		
H'00020000 to H'FFFF9FFF	Reserved				
H'FFFFA000 to H'FFFFAFFF	On-chip RAM	8 Kbytes	8 Kbytes	8 Kbytes	8 K
H'FFFFB000 to H'FFFFBFFF					Res
H'FFFFC000 to H'FFFFFFFF	On-chip peripheral I/O	128 Kbytes	64 Kbytes	64 Kbytes	64

9.7.22 Simultaneous Capture of TCNT_1 and TCNT_2 in Cascade Connection — 349

Description amended

The MTU2 has a new function that allows simu capture of TCNT_1 and TCNT_2 with a single i capture input as the trigger. This function allows of the 32-bit counter such that TCNT_1 and TC are captured at the same time.

See section 9.3.8, Timer Input Capture Control (TICCR), for details.

10.5 Interrupt — 401

Table 10.5 Interrupt Sources and Conditions

Table amended

Name	Interrupt Source	Interrupt Flag	Condition
OEI3	Output enable interrupt 3	POE8F	PIE3 • POE8F

11.5.1 Overflow — 412

Title added

11.5.2 $\overline{\text{WDTOVF}}$ Signal Connection — 412

Newly added

12.3 Register Descriptions — 416

Table amended

Chan-nel	Register Name	Abbrevia-tion	R/W	Initial Value	Address
0	Serial port register_0	SCSPTR_0	R/W	H'0x	H'FFFFC0
1	Serial port register_1	SCSPTR_1	R/W	H'0x	H'FFFFC0
2	Serial port register_2	SCSPTR_2	R/W	H'0x	H'FFFFC1

output is enabled, the SPB1DT bit val
through the SCK pin.

0: Low level is output

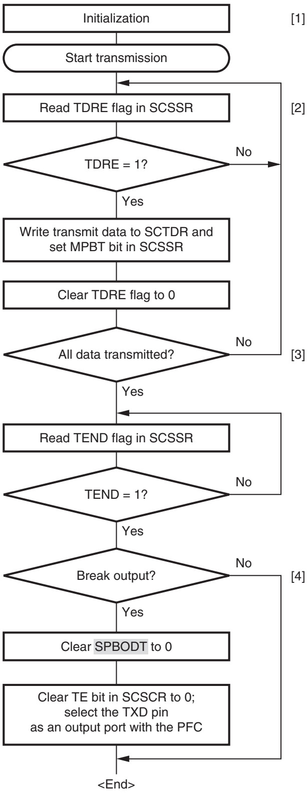
1: High level is output

12.4.5 Multiprocessor Serial Data Transmission

Figure 12.16 Sample Multiprocessor Serial Transmission Flowchart

467

Figure amended



[1] SCI initialization:
Set the TXD pin us
After the TE bit is s
for one frame, and
enabled. However,
transmitted.

[2] SCI status check a
write:
Read SCSSR and
TDRE flag is set to
transmit data to SC
MPBT bit in SCSS
clear the TDRE fla

After initializing the
is written to SCTDI
transmit the ID, da
transferred, and th
set to 1. The MPB
because the ID is
the TXD pin at this
TDRE flag is set to
following the ID is
clear the MPBT bit

[3] Serial transmission
procedure:

To continue serial
sure to read 1 from
confirm that writing
write data to SCTD
the TDRE flag to 0

[4] Break output at the
transmission:
To output a break
transmission, first
bit in the serial por
(SCSPTR) to 0, the
in SCSCR to 0 and
select the TXD pin

	PA7 I/O (port)	TCLKB input (MTU2)	SCK2 I/O (SCI)	TCK input (H-UDI)*2	
	PA8 I/O (port)	TCLKC input (MTU2)	RXD2 input (SCI)	TDI input (H-UDI)*2	
	PA9 I/O (port)	TCLKD input (MTU2)	TXD2 output (SCI)	$\overline{\text{POE8}}$ input (POE)	T

516 Note added

Notes: 1. During A/D conversion, the AN inpu
is enabled.

2. These functions ($\overline{\text{TRST}}$, TMS, TCK,
TDO) are not supported on the 32 K
versions (SH71251A and SH71241
Kbyte versions (SH71250A and SH

Table 15.2 SH7124 Multiplexed Pins

517 Table amended

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	F (
A	PA0 I/O (port)	$\overline{\text{POE0}}$ input (POE)	RXD0 input (SCI)		
	PA1 I/O (port)	$\overline{\text{POE1}}$ input (POE)	TXD0 output (SCI)		
	PA3 I/O (port)	IRQ1 input (INTC)	RXD1 input (SCI)	$\overline{\text{TRST}}$ input (H-UDI)*2	
	PA4 I/O (port)	IRQ2 input (INTC)	TXD1 output (SCI)	TMS input (H-UDI)*2	
	PA6 I/O (port)	TCLKA input (MTU2)			
	PA7 I/O (port)	TCLKB input (MTU2)	SCK2 I/O (SCI)	TCK input (H-UDI)*2	
	PA8 I/O (port)	TCLKC input (MTU2)	RXD2 input (SCI)	TDI input (H-UDI)*2	
	PA9 I/O (port)	TCLKD input (MTU2)	TXD2 output (SCI)	$\overline{\text{POE8}}$ input (POE)	T

518 Note added

Notes: 1. During A/D conversion, the AN inpu
is enabled.

2. These functions ($\overline{\text{TRST}}$, TMS, TCK,
TDO) are not supported on the 32 K
versions (SH71251A and SH71241
Kbyte versions (SH71250A and SH

Notes: 1. Fixed to TMS, TRST, TDI, TDO, T
ASEBRKAK/ASEBRK when using
(in ASEMD0 = low).

2. E10A cannot be used on the 32 Kb
(SH71251A and SH71241A) and 1
(SH71250A and SH71240A) versi

Table 15.4 SH7124 Pin Functions in Each Operating Mode

521 Table amended

	Pin Name	
	Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities
33	FWE/(ASEBRKAK/ ASEBRK*1)	FWE
23	PA3/(TRST*1)	PA3/IRQ1/RXD1

522 Table amended

	Pin Name	
	Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities
22	PA4/(TMS*1)	PA4/IRQ2/TXD1
21	PA6	PA6/TCLKA
20	PA7/(TCK*1)	PA7/TCLKB/SCK2
18	PA8/(TDI*1)	PA8/TCLKC/RXD2
16	PA9/(TDO*1)	PA9/TCLKD/TXD2/POE8

Note added

Notes: 1. Fixed to TMS, TRST, TDI, TDO, T
ASEBRKAK/ASEBRK when using
(in ASEMD0 = low).

2. E10A cannot be used on the 32 Kb
(SH71251A and SH71241A) and 1
(SH71250A and SH71240A) versi

0	PA8MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = is fixed to TDI input. 000: PA8 I/O (port) 001: TCLKC input (MTU2) 110: RXD2 input (SCI) Other than above: Setting prohibited

Note added

Note: * E10A cannot be used on the 32 Kby
(SH71251A and SH71241A) and 16
(SH71250A and SH71240A) versio

- Port A Control Register L2 (PACRL2)

528 Table amended

Bit	Bit Name	Initial Value	R/W	Description
14	PA7MD2	0	R/W	PA7 Mode
13	PA7MD1	0	R/W	Select the function of the PA7/TCLKB
12	PA7MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = is fixed to TCK input. 000: PA7 I/O (port) 001: TCLKB input (MTU2) 110: SCK2 I/O (SCI) Other than above: Setting prohibited

529 Table amended

Bit	Bit Name	Initial Value	R/W	Description
2	PA4MD2	0	R/W	PA4 Mode
1	PA4MD1	0	R/W	Select the function of the PA4/IRQ2/T
0	PA4MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = is fixed to TCK input. 000: PA4 I/O (port) 001: TXD1 output (SCI) 111: IRQ2 input (INTC) Other than above: Setting prohibited

Note added

Note: * E10A cannot be used on the 32 Kby
(SH71251A and SH71241A) and 16
(SH71250A and SH71240A) versio

(SH71251A and SH71241A) and 1
(SH71250A and SH71240A) versi

- Port A Control Register L3 (PACRL3)

531 Table amended

Bit	Bit Name	Initial Value	R/W	Description
6	PA9MD2	0	R/W	PA9 Mode
5	PA9MD1	0	R/W	Select the function of the PA9/TCLKD/TXD2/TDO/$\overline{\text{POE8}}$ pin. is in use ($\overline{\text{ASEMD0}}$ = low), function output. 000: PA9 I/O (port) 001: TCLKD input (MTU2) 110: TXD2 output (SCI) 111: $\overline{\text{POE8}}$ input (POE) Other than above: Setting prohibited
4	PA9MD0	0	R/W	

532 Table amended

Bit	Bit Name	Initial Value	R/W	Description
2	PA8MD2	0	R/W	PA8 Mode
1	PA8MD1	0	R/W	Select the function of the PA8/TCLK When the E10A* is in use ($\overline{\text{ASEMD}}$ is fixed to TDI input. 000: PA8 I/O (port) 001: TCLKC input (MTU2) 110: RXD2 input (SCI) Other than above: Setting prohibited
0	PA8MD0	0	R/W	

Note added

Note: * E10A cannot be used on the 32 Kb
(SH71251A and SH71241A) and 1
(SH71250A and SH71240A) versi

Bit	Bit Name	Value	R/W	Description
2	PA4MD2	0	R/W	PA4 Mode
1	PA4MD1	0	R/W	Select the function of the PA4/IRQ2/T
0	PA4MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = is fixed to TMS input. 000: PA4 I/O (port) 001: TXD1 output (SCI) 111: IRQ2 input (INTC) Other than above: Setting prohibited

- Port A Control Register L2 (PACRL2)

533

Note added

Note: * E10A cannot be used on the 32 Kby
(SH71251A and SH71241A) and 16
(SH71250A and SH71240A) versio

- Port A Control Register L1 (PACRL1)

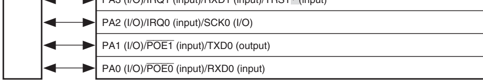
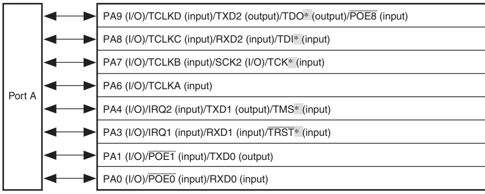
534

Table amended

Bit	Bit Name	Initial Value	R/W	Description
14	PA3MD2	0	R/W	PA3 Mode
13	PA3MD1	0	R/W	Select the function of the PA3/IRQ1/R
12	PA3MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = is fixed to $\overline{\text{TRST}}$ input. 000: PA3 I/O (port) 001: RXD1 input (SCI) 111: IRQ1 input (INTC) Other than above: Setting prohibited

Note added

Note: * E10A cannot be used on the 32 Kby
(SH71251A and SH71241A) and 16
(SH71250A and SH71240A) versio

		 PA3 (I/O)/IRQ1 (input)/RXD1 (input)/TRST* (input) PA2 (I/O)/IRQ0 (input)/SCK0 (I/O) PA1 (I/O)/POE1 (input)/TXD0 (output) PA0 (I/O)/POE0 (input)/RXD0 (input) Note: * The TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ pins are not supported on the 32 Kbyte (SH71251A and SH7 16 Kbyte (SH71250A and SH71240A) versions.
Figure 16.2 Port A (SH7124)	554	Figure amended  Port A PA9 (I/O)/TCLKD (input)/TXD2 (output)/TDO* (output)/POE8 (input) PA8 (I/O)/TCLKC (input)/RXD2 (input)/TDI* (input) PA7 (I/O)/TCLKB (input)/SCK2 (I/O)/TCK* (input) PA6 (I/O)/TCLKA (input) PA4 (I/O)/IRQ2 (input)/TXD1 (output)/TMS* (input) PA3 (I/O)/IRQ1 (input)/RXD1 (input)/TRST* (input) PA1 (I/O)/POE1 (input)/TXD0 (output) PA0 (I/O)/POE0 (input)/RXD0 (input) Note: * The TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ pins are not supported on the 32 Kbyte (SH71251A and SH 16 Kbyte (SH71250A and SH71240A) versions.
16.5 Usage Notes 16.5.1 Handling of Unused Pins	577	Newly added
17. Flash Memory (ROM)	579	Description amended This LSI has 128-Kbyte, 64-Kbyte, 32-Kbyte, o Kbyte on-chip flash memory. The flash memor following features.

<table>
<tr><th></th><th></th><th></th></tr>
<tr><td></td><td></td><td>

Boot Mode: This mode is a program mode an on-chip SCI interface. The user MAT car programmed. This mode can automatically the bit rate between the host and this LSI.

User Program Mode: The user MAT can b programmed by using an interface selected user. This mode cannot be used on the 32 l and 16 Kbyte flash memory versions.

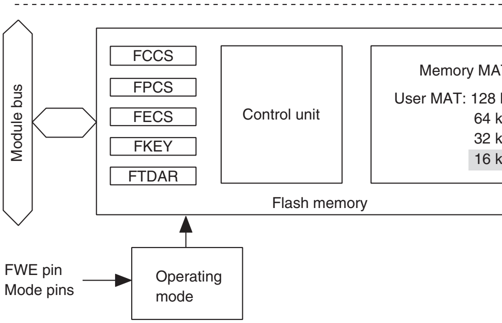
</td></tr>
<tr><td>

17.2.1 Block Diagram

Figure 17.1 Block Diagram of Flash Memory

</td><td>584</td><td>

Figure amended



</td></tr>
<tr><td>

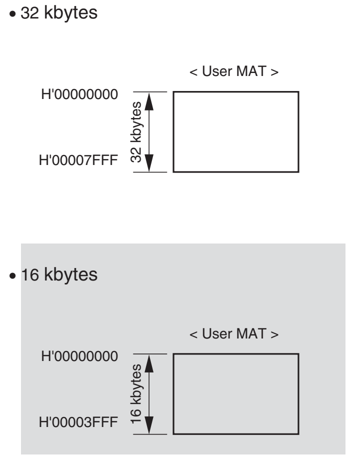
17.2.4 Flash Memory Configuration

</td><td>584</td><td>

Description amended

This LSI's flash memory is configured by the 12 64-Kbyte, 32-Kbyte, or 16-Kbyte user MAT.

</td></tr>
</table>

		is 128 kbytes)
17.2.5 Block Division	584	Description amended It is not divided on the 32 Kbyte versions of th SH71251A and SH71241A or the 16 Kbyte ve the SH71250A and SH71240A.
Figure 17.4 Block Division of User MAT	584	Figure amended  • 32 kbytes < User MAT > H'00000000 32 kbytes H'00007FFF • 16 kbytes < User MAT > H'00000000 16 kbytes H'00003FFF
17.9 Off-Board Programming Mode	662	Description amended A PROM programmer can be used to perform programming/erasing via a socket adapter. Us PROM programmer that supports the propriet Renesas specification. Note that before using a PROM programmer t the MCU, the MAT should initially be erased c

Note: Write an initial value of "1" when progr
the 32 Kbyte (SH71251A and SH71241
16 Kbyte (SH71250A and SH71240A) v

19.3.6 Standby Control Register 6 (STBCR6) 673

Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	UBCRST	0	R/W	UBC Software Reset Resetting the PC trace unit of UBC is co software. Clearing this bit to 0 puts the PC trace u module into the power-on reset state. 0: Puts the PC trace unit of UBC into the 1: Releases reset in the PC trace unit of This bit is not supported on 32 Kbyte ve (SH71251A, SH71241A) and 16 Kbyte v (SH71250A, SH71240A). These bits are always read as 0. The wr always be 0.

20.1 Register Address Table (In the Order from Lower Addresses) 687

Table amended

Register Name	Abbreviation	Number of Bits	Address	Module	Access Size
Break address register A*	BARA	32	H'FFFFF300	UBC	32
Break address mask register A*	BAMRA	32	H'FFFFF304		32
Break bus cycle register A*	BBRA	16	H'FFFFF308		16
Break data register A*	BDRA	32	H'FFFFF310		32
Break data mask register A*	BDMRA	32	H'FFFFF314		32
Break address register B*	BARB	32	H'FFFFF320		32
Break address mask register B*	BAMRB	32	H'FFFFF324		32
Break bus cycle register B*	BBRB	16	H'FFFFF328		16
Break data register B*	BDRB	32	H'FFFFF330		32
Break data mask register B*	BDMRB	32	H'FFFFF334		32
Break control register*	BRCR	32	H'FFFFF3C0		32
Branch source register*	BRSR	32	H'FFFFF3D0		32
Branch destination register*	BRDR	32	H'FFFFF3D4		32
Execution times break register*	BETR	16	H'FFFFF3DC		16

Note added

Note: * The UBC registers are not supporte
Kbyte versions (SH71251A, SH712
16 Kbyte versions (SH71250A, SH7

Abbreviation	31/23/15/7	30/22/14/6	29/21/13/5	28/20/12/4	27/19/11/3	26/18/10/2	25/17/9/1	24/1
BRSR	SVF				BSA27	BSA26	BSA25	B

Note added

Note: * The UBC registers are not support
Kbyte versions (SH71251A, SH71
16 Kbyte versions (SH71250A, SH

20.3 Register States in Each Operating Mode

708 Table amended

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Module Standby	Sleep
BARA	Initialized	Retained	Retained	Initialized	Retained

709 Table amended

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Module Standby	Sleep
BDRB	Initialized	Retained	Retained	Initialized	Retained

Note added

Notes: 4. The UBC registers are not support
Kbyte versions (SH71251A, SH71
16 Kbyte versions (SH71250A, SH

B. Product Code Lineup 737 Table amended

Product Type			Product Code	Package
SH7125	Flash memory version (on-chip 64-kbyte)	Consumer product	R5F71252N50NP	VQFN-64
		Industrial product	R5F71252D50NP	
	Flash memory version (on-chip 32-kbyte)	Consumer product	R5F71251AN50FA	QFP-64
		Industrial product	R5F71251AD50FA	
		Consumer product	R5F71251AN50FP	LQFP-64
		Industrial product	R5F71251AD50FP	
		Consumer product	R5F71251AN50NP	VQFN-64
		Industrial product	R5F71251AD50NP	
	Flash memory version (on-chip 16-kbyte)	Consumer product	R5F71250AN50FA	QFP-64
		Industrial product	R5F71250AD50FA	
		Consumer product	R5F71250AN50FP	LQFP-64
		Industrial product	R5F71250AD50FP	
		Consumer product	R5F71250AN50NP	VQFN-64
		Industrial product	R5F71250AD50NP	
SH7124	Flash memory version (on-chip 128-kbyte)	Consumer product	R5F71243N50NP	VQFN-52
		Industrial product	R5F71243D50NP	

738 Table amended

Product Type			Product Code	Package
SH7124	Flash memory version (on-chip 16-kbyte)	Consumer product	R5F71240AN50FP	LQFP-48
		Industrial product	R5F71240AD50FP	
		Consumer product	R5F71240AN50NP	VQFN-52
		Industrial product	R5F71240AD50NP	

Renesas 32-Bit RISC Microcomputer
Hardware Manual
SH7125 Group, SH7124 Group

Publication Date:	Rev.1.00, March 25, 2005
	Rev.5.00, March 6, 2009
Published by:	Sales Strategic Planning Div.
	Renesas Technology Corp.
Edited by:	Customer Support Department
	Global Strategic Communication Div.
	Renesas Solutions Corp.

RenesasTechnology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, J

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