


| | | | |
|----------------------|------------|-------------------|-------------|
| MCOT22005A1V-EBM | 2 x 20 | Euro/Jap/Cyrillic | OLED Module |
| Specification | | | |
| Version: 1 | | Date: 23/10/2017 | |
| Revision | | | |
| 1 | 20/10/2017 | First Issue. | |

| Display Features | |  | |
|-----------------------|-------------------------------|--|------------------|
| Character Count | 2 x 20 | | |
| Appearance | Blue on Black | | |
| Logic Voltage | 5V | | |
| Interface | Parallel / SPI / I2C | | |
| Font Set | English / Japanese / Cyrillic | | |
| Character Height | 5.57 | | |
| Module Size | 84.50 x 19.28 x 2.05 mm | | |
| Operating Temperature | -40°C ~ +80°C | | |
| Construction | TAB | Box Quantity | Weight / Display |
| | | --- | --- |

* - For full design functionality, please use this specification in conjunction with the SSD1311 specification.(Provided Separately)

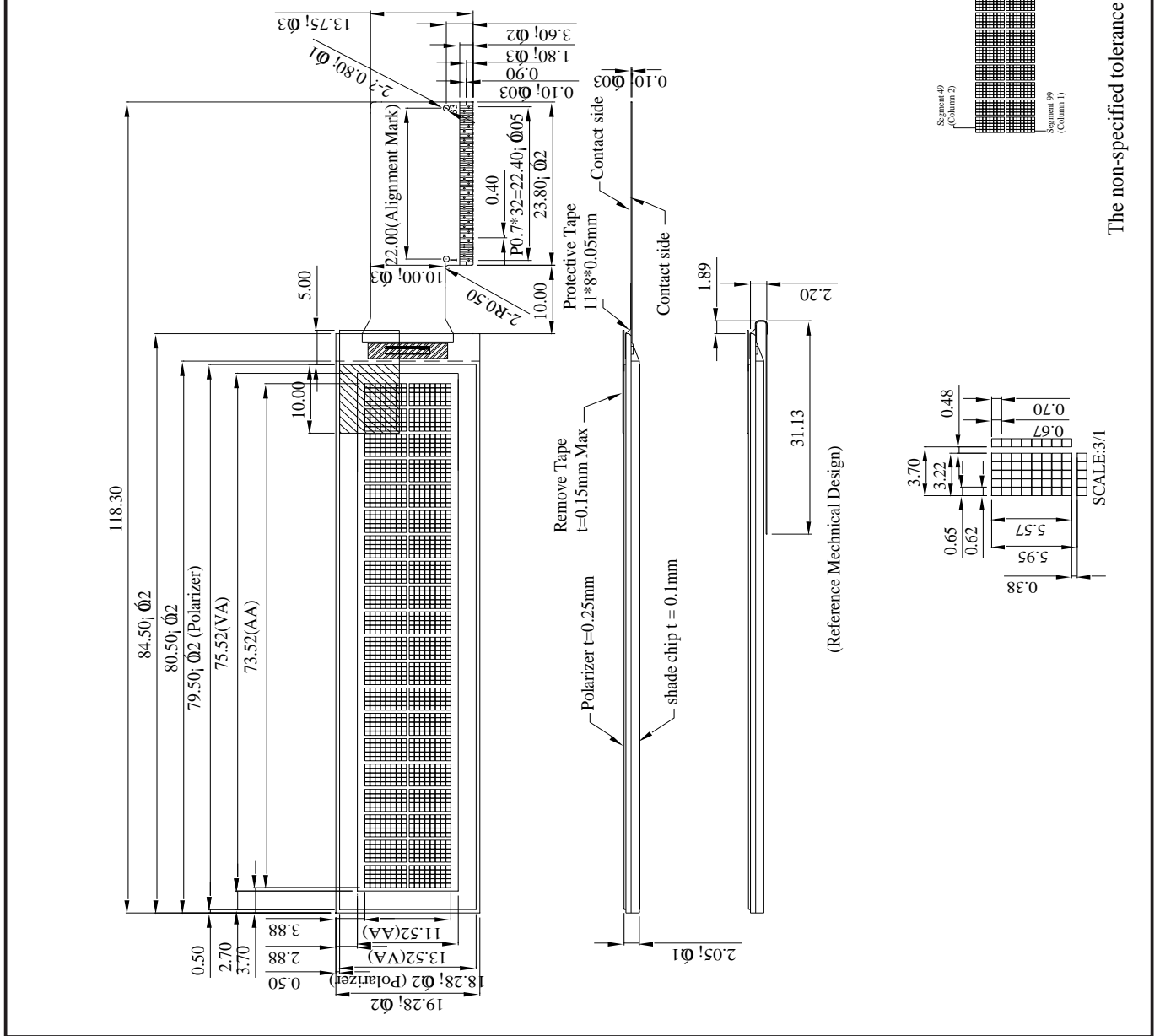
| Display Accessories | |
|---------------------|---|
| Part Number | Description |
| MPBV4-Iss2 | Direct solder-to-2mm pitch DIL pinout interface board. Compatible with: 0.7, 0.8, 0.845 and 1mm pitch pads. |
| MCIB-13 V2 | Direct solder OLED character interface board. Used in conjunction with MCIB-12 and UC32. |
| | |

| Optional Variants | |
|---|---------|
| Appearance | Voltage |
| White on Black Green on Black Yellow on Black | |
| Interface | |
| | |

Mechanical Specifications

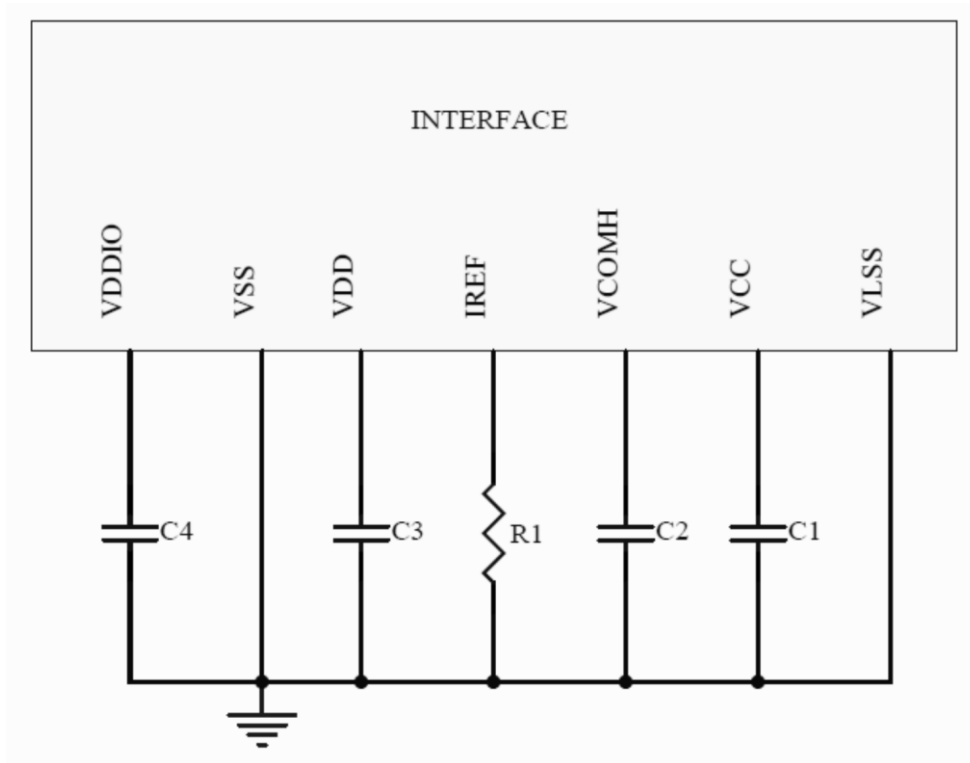
| | | | | | |
|----------------|--|----------|-----------------|-------------|--------------|
| Module Size | 84.50 x 19.28 x 2.05 (Without Backlight) | | | | W x H x D mm |
| Active Area | 73.52 x 11.52 | W x H mm | Hole-to-Hole | --- | W x H mm |
| Character Size | 3.22 x 5.57 | W x H mm | Character Pitch | 3.70 x 5.95 | W x H mm |
| Dot Size | 0.62 x 0.67 | W x H mm | Dot Pitch | 0.65 x 0.70 | W x H mm |

| Pin No. | Symbol | Pin No. | Symbol |
|---------|-----------|---------|--------|
| 1 | NC | 18 | D0 |
| 2 | VSL | 19 | D1 |
| 3 | VSS | 20 | D2 |
| 4 | REGVDD | 21 | D3 |
| 5 | SHLC | 22 | D4 |
| 6 | SHLS | 23 | D5 |
| 7 | VDD | 24 | D6 |
| 8 | VDDIO | 25 | D7 |
| 9 | BS0 | 26 | IREF |
| 10 | BS1 | 27 | ROM0 |
| 11 | BS2 | 28 | ROM1 |
| 12 | GPIO | 29 | OPR0 |
| 13 | CS# | 30 | OPR1 |
| 14 | RES# | 31 | VCOMH |
| 15 | D/C# | 32 | VCC |
| 16 | R/W#(WR#) | 33 | NC |
| 17 | E(RD#) | | |



| | | | |
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Block Diagram and Application Recommendation



C1, C2: 4.7uF (1)

C3, C4: 1.0uF (1) place close to IC VDDIO / VDD and VSS pins on PCB

Voltage at IREF = VCC – 4.5V. For VCC = 10V, IREF = 15uA:

$R1 = (\text{Voltage at IREF} - \text{VSS}) / \text{IREF}$

$(10-4.5)\text{V} / 15\mu\text{A}$
 = 366KΩ

Note

(1) The capacitor value is recommended value. Select appropriate value against module application.

*For more information, please refer to Application Note provided by Midas.

| | | | |
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Pin Layout

| Pin | Symbol | Description | | | | | | | | | | | | | | | | | | |
|---------|-------------------------|--|---------|--------------------|-----|------------------------|-----|-------------------------|-----|------------------|-----|---------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|
| 1 | NC | No connection | | | | | | | | | | | | | | | | | | |
| 2 | VSL | This is segment voltage (output low level) reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, connect with resistor and diode to ground (details depend on application). | | | | | | | | | | | | | | | | | | |
| 3 | VSS | Ground pin. It must be connected to external ground. | | | | | | | | | | | | | | | | | | |
| 4 | REGVDD | Internal VDD regulator selection pin in 5V I/O application mode. When this pin is pulled HIGH, internal VDD regulator is enabled (5V I/O application). When this pin is pulled LOW, internal VDD regulator is disabled (Low voltage I/O application). | | | | | | | | | | | | | | | | | | |
| 5 | SHLC | This pin is used to determine the Common output scanning direction. COM scan direction <table border="1" style="width: 100%;"> <tr> <th>SHLC</th> <th>COM scan direction</th> </tr> <tr> <td>1</td> <td>COM0 to COM31 (Normal)</td> </tr> <tr> <td>0</td> <td>COM31 to COM0 (Reverse)</td> </tr> </table> <p>(1) 0 s connected to VSS (2) 1 s connected to VDDIO</p> | SHLC | COM scan direction | 1 | COM0 to COM31 (Normal) | 0 | COM31 to COM0 (Reverse) | | | | | | | | | | | | |
| SHLC | COM scan direction | | | | | | | | | | | | | | | | | | | |
| 1 | COM0 to COM31 (Normal) | | | | | | | | | | | | | | | | | | | |
| 0 | COM31 to COM0 (Reverse) | | | | | | | | | | | | | | | | | | | |
| 6 | SHLS | This pin is used to change the mapping between the display data column address and the Segment driver. SEG scan direction <table border="1" style="width: 100%;"> <tr> <th>SHLS</th> <th>SEG direction</th> </tr> <tr> <td>1</td> <td>SEG0 to SEG99 (Normal)</td> </tr> <tr> <td>0</td> <td>SEG99 to SEG0 (Reverse)</td> </tr> </table> <p>(1) 0 s connected to VSS (2) 1 s connected to VDDIO</p> | SHLS | SEG direction | 1 | SEG0 to SEG99 (Normal) | 0 | SEG99 to SEG0 (Reverse) | | | | | | | | | | | | |
| SHLS | SEG direction | | | | | | | | | | | | | | | | | | | |
| 1 | SEG0 to SEG99 (Normal) | | | | | | | | | | | | | | | | | | | |
| 0 | SEG99 to SEG0 (Reverse) | | | | | | | | | | | | | | | | | | | |
| 7 | VDD | Power Supply For Core Logic Operation. VDD can be supplied externally or regulated internally. In LV IO application (internal VDD is disabled), this is a power input pin. In 5V IO application (internal VDD is enabled), VDD is regulated internally from VDDIO. A capacitor should be connected between VDD and VSS under all circumstances. | | | | | | | | | | | | | | | | | | |
| 8 | VDDIO | Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source. | | | | | | | | | | | | | | | | | | |
| 9 | BS0 | MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select. | | | | | | | | | | | | | | | | | | |
| 10 | BS1 | Bus Interface selection | | | | | | | | | | | | | | | | | | |
| 11 | BS2 | <table border="1" style="width: 100%;"> <tr> <th>BS[2:0]</th> <th>Interface</th> </tr> <tr> <td>000</td> <td>Serial Interface</td> </tr> <tr> <td>001</td> <td>Invalid</td> </tr> <tr> <td>010</td> <td>I²C</td> </tr> <tr> <td>011</td> <td>Invalid</td> </tr> <tr> <td>100</td> <td>8-bit 6800 parallel</td> </tr> <tr> <td>101</td> <td>4-bit 6800 parallel</td> </tr> <tr> <td>110</td> <td>8-bit 8080 parallel</td> </tr> <tr> <td>111</td> <td>4-bit 8080 parallel</td> </tr> </table> <p>(1) 0 s connected to VSS (2) 1 s connected to VDDIO</p> | BS[2:0] | Interface | 000 | Serial Interface | 001 | Invalid | 010 | I ² C | 011 | Invalid | 100 | 8-bit 6800 parallel | 101 | 4-bit 6800 parallel | 110 | 8-bit 8080 parallel | 111 | 4-bit 8080 parallel |
| BS[2:0] | Interface | | | | | | | | | | | | | | | | | | | |
| 000 | Serial Interface | | | | | | | | | | | | | | | | | | | |
| 001 | Invalid | | | | | | | | | | | | | | | | | | | |
| 010 | I ² C | | | | | | | | | | | | | | | | | | | |
| 011 | Invalid | | | | | | | | | | | | | | | | | | | |
| 100 | 8-bit 6800 parallel | | | | | | | | | | | | | | | | | | | |
| 101 | 4-bit 6800 parallel | | | | | | | | | | | | | | | | | | | |
| 110 | 8-bit 8080 parallel | | | | | | | | | | | | | | | | | | | |
| 111 | 4-bit 8080 parallel | | | | | | | | | | | | | | | | | | | |
| 12 | GPIO | GPIO pin. Details refer to OLED command DCh. | | | | | | | | | | | | | | | | | | |
| 13 | CS# | Chip Select Input Connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW). In I2C mode, this pin must be connected to VSS. | | | | | | | | | | | | | | | | | | |
| 14 | RES# | Reset Signal Input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation. | | | | | | | | | | | | | | | | | | |

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| 15 | D/C# | Data/Command Control Pin Connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I2C mode, this pin acts as SA0 for slave address selection. When serial interface is selected, this pin must be connected to VSS. | | | | | | | | | | | | | | | | | | | | |
|-------|-----------|--|-------|------|-------|-------|---|---|-----|---|---|---|-----|---|---|---|-------------------------------|---|---|---|-----|---|
| 16 | R/W#(WR#) | Read / Write Control Input Pin Connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS. | | | | | | | | | | | | | | | | | | | | |
| 17 | E(RD#) | MCU Interface Input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS. | | | | | | | | | | | | | | | | | | | | |
| 18-25 | D0~D7 | Bi-directional Data Bus Connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL. | | | | | | | | | | | | | | | | | | | | |
| 26 | IREF | Segment Output Current Reference pin. IREF is supplied externally. A resistor should be connected between this pin and VSS to maintain current of around 15uA. | | | | | | | | | | | | | | | | | | | | |
| 27 | ROM0 | These pins are used to select Character ROM; select appropriate logic setting as described in the following table. ROM1 and ROM0 are pin select as shown in below table: Character ROM selection | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>ROM1</th> <th>ROM0</th> <th>ROM</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>A</td> </tr> <tr> <td>0</td> <td>1</td> <td>B</td> </tr> <tr> <td>1</td> <td>0</td> <td>C</td> </tr> <tr> <td>1</td> <td>1</td> <td>S/W selectable⁽³⁾</td> </tr> </tbody> </table> | ROM1 | ROM0 | ROM | 0 | 0 | A | 0 | 1 | B | 1 | 0 | C | 1 | 1 | S/W selectable ⁽³⁾ | | | | | |
| ROM1 | ROM0 | ROM | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | A | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | B | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | C | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | S/W selectable ⁽³⁾ | | | | | | | | | | | | | | | | | | | | |
| 28 | ROM1 | Note (1) 0 is connected to VSS (2) 1 is connected to VDDIO | | | | | | | | | | | | | | | | | | | | |
| 29 | OPR0 | This pin is used to select the character number of character generator. Character RAM selection | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>OPR1</th> <th>OPR0</th> <th>CGROM</th> <th>CGRAM</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>256</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>248</td> <td>8</td> </tr> <tr> <td>1</td> <td>0</td> <td>250</td> <td>6</td> </tr> <tr> <td>0</td> <td>0</td> <td>240</td> <td>8</td> </tr> </tbody> </table> | OPR1 | OPR0 | CGROM | CGRAM | 1 | 1 | 256 | 0 | 0 | 1 | 248 | 8 | 1 | 0 | 250 | 6 | 0 | 0 | 240 | 8 |
| OPR1 | OPR0 | CGROM | CGRAM | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 256 | 0 | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 248 | 8 | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 250 | 6 | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 240 | 8 | | | | | | | | | | | | | | | | | | | |
| 30 | OPR1 | Note (1) 0 is connected to VSS (2) 1 is connected to VDDIO | | | | | | | | | | | | | | | | | | | | |
| 31 | VCOMH | COM signal deselected voltage level. A capacitor should be connected between this pin and VSS. No external power supply can connect to this pin. | | | | | | | | | | | | | | | | | | | | |
| 32 | VCC | Power Supply for Panel Driving Voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source. | | | | | | | | | | | | | | | | | | | | |
| 33 | NC | No connection. | | | | | | | | | | | | | | | | | | | | |

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Font Map

| Upper 4bit Lower 4bit | LLLL | LLLH | LLHL | LLHH | LHLL | LHLH | LHHL | LHHH | HLLL | HLLH | HLHL | HLHH | HHLL | HHLH | HHHL | HHHH |
|--------------------------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| LLLL | CG RAM (1) | | | | | | | | | | | | | | | |
| LLLH | (2) | | | | | | | | | | | | | | | |
| LLHL | (3) | | | | | | | | | | | | | | | |
| LLHH | (4) | | | | | | | | | | | | | | | |
| LHLL | (5) | | | | | | | | | | | | | | | |
| LHLH | (6) | | | | | | | | | | | | | | | |
| LHHL | (7) | | | | | | | | | | | | | | | |
| LHHH | (8) | | | | | | | | | | | | | | | |
| HLLL | (1) | | | | | | | | | | | | | | | |
| HLLH | (2) | | | | | | | | | | | | | | | |
| HLHL | (3) | | | | | | | | | | | | | | | |
| HLHH | (4) | | | | | | | | | | | | | | | |
| HHLL | (5) | | | | | | | | | | | | | | | |
| HHLH | (6) | | | | | | | | | | | | | | | |
| HHHL | (7) | | | | | | | | | | | | | | | |
| HHHH | (8) | | | | | | | | | | | | | | | |

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| Upper 4bit Lower 4bit | LLLL | LLLH | LLHL | LLHH | LHLL | LHLH | LHHL | LHHH | HLLL | HLLH | HLHL | HLHH | HHLL | HHLH | HHHL | HHHH |
|--------------------------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| LLLL | CG RAM (1) | | | | | | | | | | | | | | | |
| LLLH | (2) | | | | | | | | | | | | | | | |
| LLHL | (3) | | | | | | | | | | | | | | | |
| LLHH | (4) | | | | | | | | | | | | | | | |
| LHLL | (5) | | | | | | | | | | | | | | | |
| LHLH | (6) | | | | | | | | | | | | | | | |
| LHHL | (7) | | | | | | | | | | | | | | | |
| LHHH | (8) | | | | | | | | | | | | | | | |
| HLLL | (1) | | | | | | | | | | | | | | | |
| HLLH | (2) | | | | | | | | | | | | | | | |
| HLHL | (3) | | | | | | | | | | | | | | | |
| HLHH | (4) | | | | | | | | | | | | | | | |
| HHLL | (5) | | | | | | | | | | | | | | | |
| HHLH | (6) | | | | | | | | | | | | | | | |
| HHHL | (7) | | | | | | | | | | | | | | | |
| HHHH | (8) | | | | | | | | | | | | | | | |

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| Upper 4bit Lower 4bit | LLLL | LLLH | LLHL | LLHH | LHLL | LHLH | LHHL | LHHH | HLLL | HLLH | HLHL | HLHH | HHLL | HHLH | HHHL | HHHH |
|--------------------------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| LLLL | CG RAM (1) | | | | | | | | | | | | | | | |
| LLLH | (2) | | | | | | | | | | | | | | | |
| LLHL | (3) | | | | | | | | | | | | | | | |
| LLHH | (4) | | | | | | | | | | | | | | | |
| LHLL | (5) | | | | | | | | | | | | | | | |
| LHLH | (6) | | | | | | | | | | | | | | | |
| LHHL | (7) | | | | | | | | | | | | | | | |
| LHHH | (8) | | | | | | | | | | | | | | | |
| HLLL | (1) | | | | | | | | | | | | | | | |
| HLLH | (2) | | | | | | | | | | | | | | | |
| HLHL | (3) | | | | | | | | | | | | | | | |
| HLHH | (4) | | | | | | | | | | | | | | | |
| HHLL | (5) | | | | | | | | | | | | | | | |
| HHLH | (6) | | | | | | | | | | | | | | | |
| HHHL | (7) | | | | | | | | | | | | | | | |
| HHHH | (8) | | | | | | | | | | | | | | | |

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| Absolute Maximum Ratings | | | | | | |
|--------------------------|--------|-----------|------|-----|-------|------|
| Item | Symbol | Condition | Min | Typ | Max | Unit |
| Supply Voltage for Logic | VDDIO | --- | -0.3 | --- | 6.00 | V |
| Input Voltage | VDD | --- | -0.3 | --- | VDDIO | °C |
| Operating Temperature | TOP | --- | -40 | --- | 80 | °C |
| Storage Temperature | TST | --- | -40 | --- | 85 | °C |

| Electronic Characteristics | | | | | | |
|-----------------------------------|---------|-----------|----------|---------|----------|------|
| Item | Symbol | Condition | Minimum | Typical | Maximum | Unit |
| Input High Voltage | VIH | --- | 0.80xVDD | --- | --- | V |
| Input Low Voltage | VIL | --- | --- | --- | 0.20xVDD | V |
| Output High Voltage | VOH | IOH=0.5mA | 0.90xVDD | --- | --- | V |
| Output Low Voltage | VOL | IOL=0.5mA | --- | --- | 0.10xVDD | V |
| Supply Voltage for Logic | VDDIO | --- | 4.80 | 5.00 | 5.30 | V |
| Supply Voltage for I/O | VDD-VSS | --- | 4.80 | 5.00 | 5.30 | V |
| Supply Voltage for Display | VCC | --- | 9.50 | 10.00 | 10.50 | V |
| 50% Checkboard Operating Current. | ICC | VDD=5V | 25 | 28 | 30 | mA |
| CIE _x (Blue) | --- | (CIE1931) | 0.12 | 0.16 | 0.20 | --- |
| CIE _y (Blue) | --- | (CIE1931) | 0.22 | 0.26 | 0.30 | --- |

| OLED Characteristics | | | | | | |
|--|--------------|-----------|---------|---------|---------|-------------------|
| Item | Symbol | Condition | Minimum | Typical | Maximum | Unit |
| Viewing Angle | (V) θ | --- | 160 | --- | --- | Deg |
| | (H) ϕ | --- | 160 | --- | --- | Deg |
| Contrast Ratio | CR | Dark | 2000:1 | --- | --- | --- |
| Response Time | T Rise | --- | --- | 10 | --- | μ s |
| | T Fall | --- | --- | 10 | --- | μ s |
| Display with 50% Checkboard Brightness | | | 60 | 80 | --- | cd/m ² |

| OLED Life Time | | | |
|---------------------|--|--------------|--------|
| Item | Conditions | Typical | Remark |
| Operating Life Time | Ta=25°C. Initial checkboard brightness. 50%. | 50,000 Hours | --- |

| | | | |
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[MC22008B6W-SPR](#) [MC11605A6WR-SPTLY-V2](#) [MCOT048064A1V-YI](#) [MCT101E0CW1280800LMLIPS](#) [MCT104A0W1024768LML](#)
[MCT070Z0W800480LML](#) [MC41605A6W-FPTLA-V2](#) [MC42004A6WK-SPTLY-V2](#) [MCOT128064UA1V-WM](#)
[MCT101E0TW1280800LMLIPS](#) [MCT150B0W1024768LML](#) [MCT050HDMI-A-RTP](#) [MCT050HDMI-A-CTP](#)
[MCT070Z0TW1W800480LML](#) [MCT050ACA0CW800480LML](#) [MC42005A12W-VNMLY](#) [MC42005A12W-VNMLG](#)
[MCT052A6W480128LML](#) [MC21605A6WK-BNMLW-V2](#) [MC21605B6WD-BNMLW-V2](#) [MCOT256064A1A-BM](#) [MCOT22005A1V-EYM](#)
[MCT024L6W240320PML](#) [MC20805A12W-VNMLG](#) [MC22405A6WK-BNMLW-V2](#) [MC41605A6WK-FPTLW-V2](#) [MCT101HDMI-A-RTP](#)
[MCCOG21605D6W-FPTLWI](#) [MC21605A6WD-SPTLY-V2](#) [MC22005A6WK-BNMLW-V2](#) [MC24005AA6W9-BNMLW-V2](#) [MC11609A6W-](#)
[SPTLY-V2](#) [MC21605H6WR-SPTLY-V2](#) [MC128064A6W-BNMLW-V2](#) [MCOT064048A1V-YM](#) [MCOT128064BY-BM](#)
[MCCOG128064B12W-FPTLRGB](#) [MC11609A6W-SPR-V2](#) [MC21605H6WK-BNMLW-V2](#) [MCOT128064E1V-BM](#) [MCT070HDMI-B-RTP](#)
[MDT5000C](#) [MCOT128128AZ-RGBM](#) [MCCOG42005A6W-BNMLWI](#) [MC11605A12W-VNMLB](#)