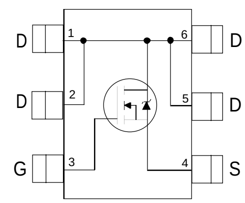
PD - 91508D

International
IOR Rectifier

IRLMS1503

HEXFET® Power MOSFET

- Generation V Technology
- Micro6 Package Style
- Ultra Low $R_{DS(on)}$
- N-Channel MOSFET



Top View

V_{DSS} = 30V

$R_{DS(on)}$ = 0.10Ω


Micro6™

Description

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The Micro6™ package with its customized leadframe produces a HEXFET® power MOSFET with $R_{DS(on)}$ 60% less than a similar size SOT-23. This package is ideal for applications where printed circuit board space is at a premium. It's unique thermal design and $R_{DS(on)}$ reduction enables a current-handling increase of nearly 300% compared to the SOT-23.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	3.2	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	2.6	
I_{DM}	Pulsed Drain Current ①	18	
P_D @T_A = 25°C	Power Dissipation	1.7	W
	Linear Derating Factor	13	mW/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance Ratings

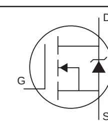
	Parameter	Min.	Typ.	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	——	——	75	°C/W

3/17/04

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.037	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.100	Ω	V_{GS} = 10V, I_D = 2.2A ③
		–––	–––	0.20		V_{GS} = 4.5V, I_D = 1.1A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–––	–––	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	1.1	–––	–––	S	V_{DS} = 10V, I_D = 1.1A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		–––	–––	25		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	–––	–––	100		V_{GS} = 20V
Q_g	Total Gate Charge	–––	6.4	9.6	nC	I_D = 2.2A
Q_{gs}	Gate-to-Source Charge	–––	1.1	1.7		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	1.9	2.8		V_{GS} = 10V, See Fig. 6 and 9 ③
$t_{d(on)}$	Turn-On Delay Time	–––	4.6	–––	ns	V_{DD} = 15V
t_r	Rise Time	–––	4.4	–––		I_D = 2.2A
$t_{d(off)}$	Turn-Off Delay Time	–––	10	–––		R_G = 6.0Ω
t_f	Fall Time	–––	2.0	–––		R_D = 6.7Ω, See Fig. 10 ③
C_{iss}	Input Capacitance	–––	210	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	90	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	32	–––		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	18		
V_{SD}	Diode Forward Voltage	–––	–––	1.2	V	T_J = 25°C, I_S = 2.2A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	–––	36	54	ns	T_J = 25°C, I_F = 2.2A
Q_{rr}	Reverse RecoveryCharge	–––	39	58	nC	di/dt = 100A/µs ③

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $I_{SD} \leq$ 2.2A, di/dt $\leq$ 150A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

③ Pulse width $\leq$ 300µs; duty cycle $\leq$ 2%.

④ Surface mounted on FR-4 board, t $\leq$ 5sec.

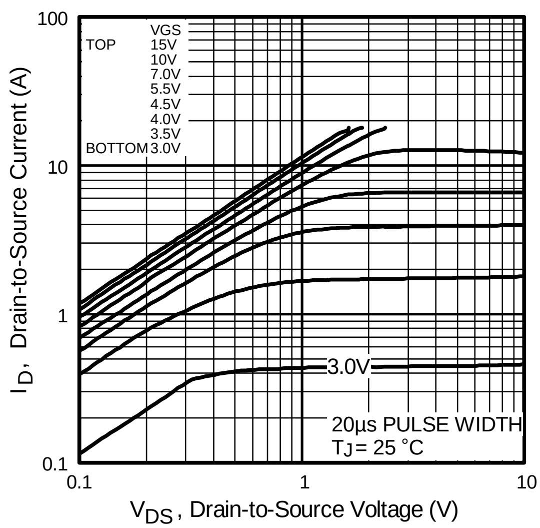


Fig 1. Typical Output Characteristics

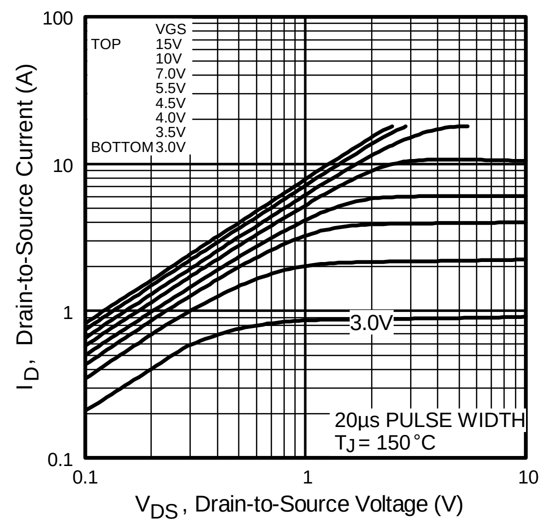


Fig 2. Typical Output Characteristics

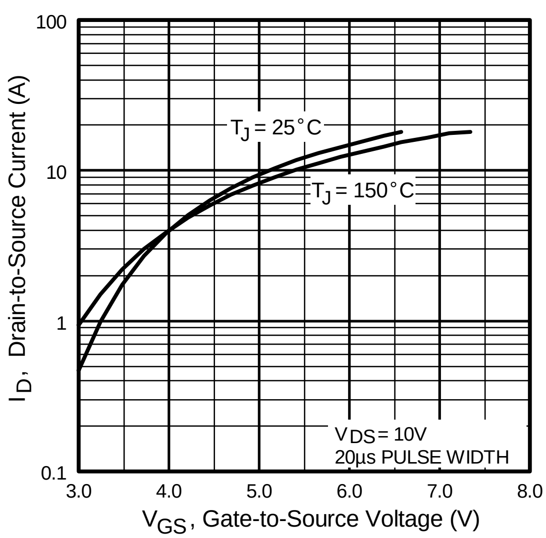


Fig 3. Typical Transfer Characteristics

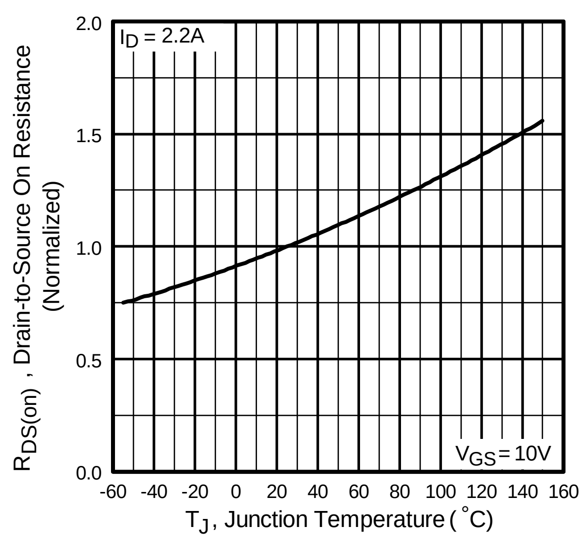


Fig 4. Normalized On-Resistance
Vs. Temperature

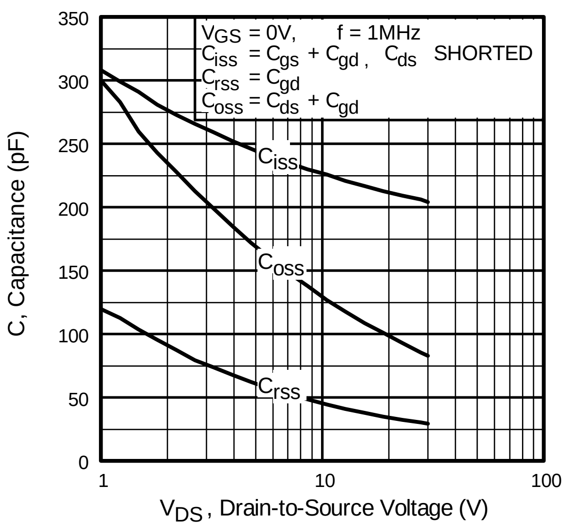


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

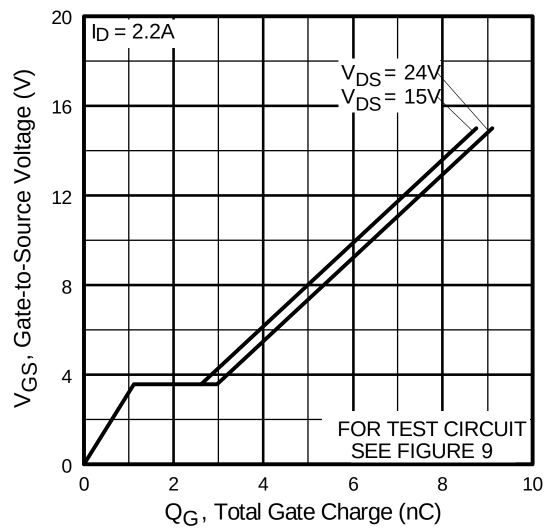


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

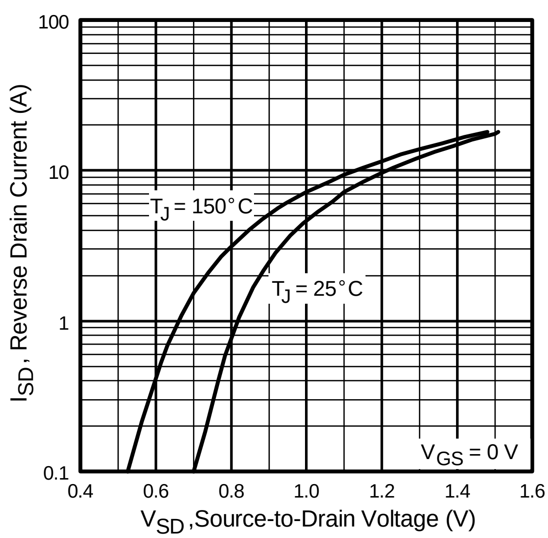


Fig 7. Typical Source-Drain Diode Forward Voltage

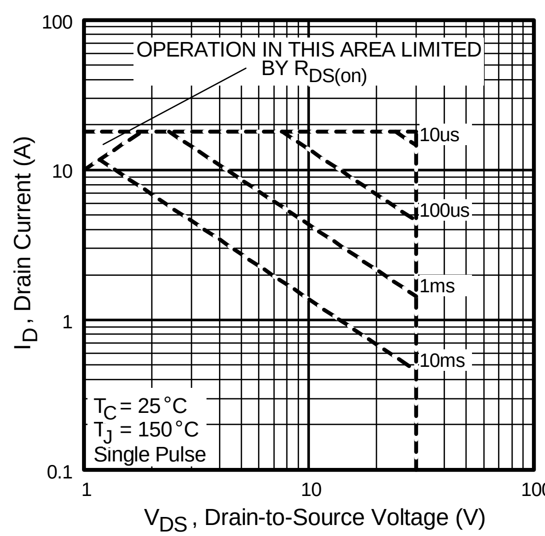


Fig 8. Maximum Safe Operating Area

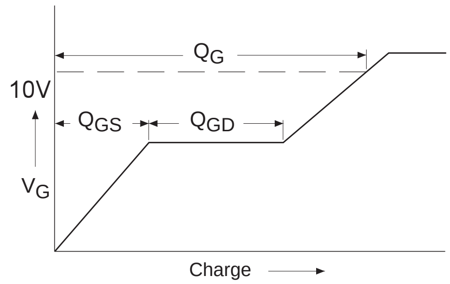


Fig 9a. Basic Gate Charge Waveform

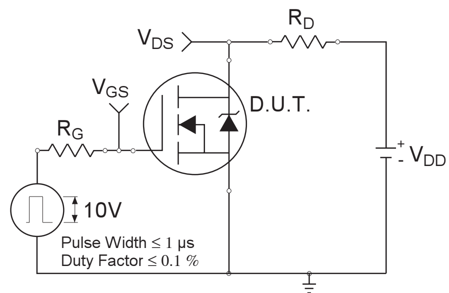


Fig 10a. Switching Time Test Circuit

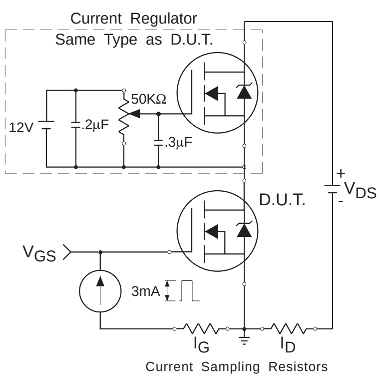


Fig 9b. Gate Charge Test Circuit

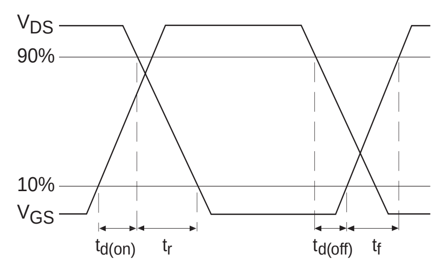


Fig 10b. Switching Time Waveforms

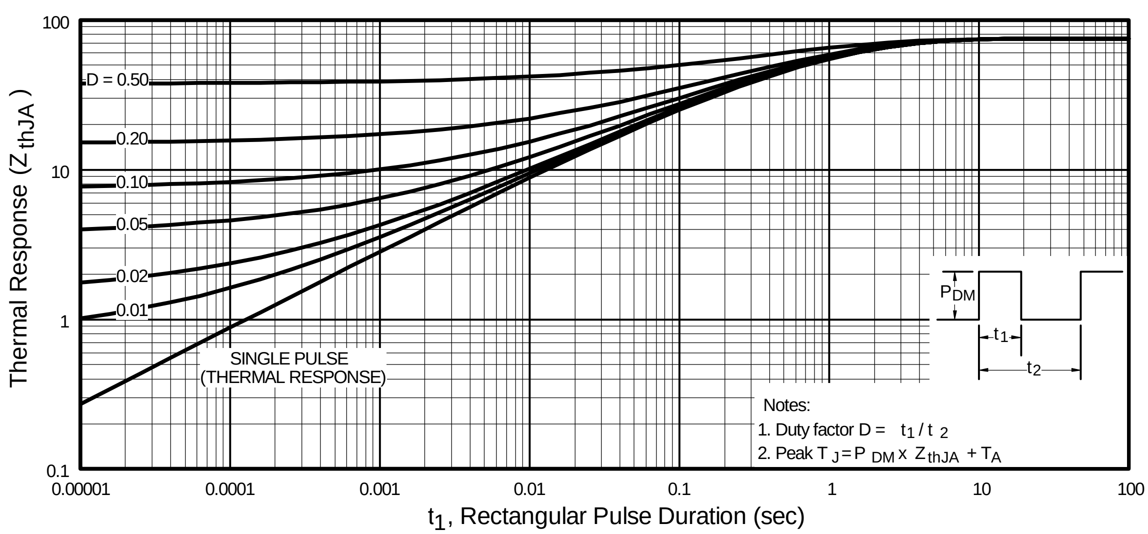
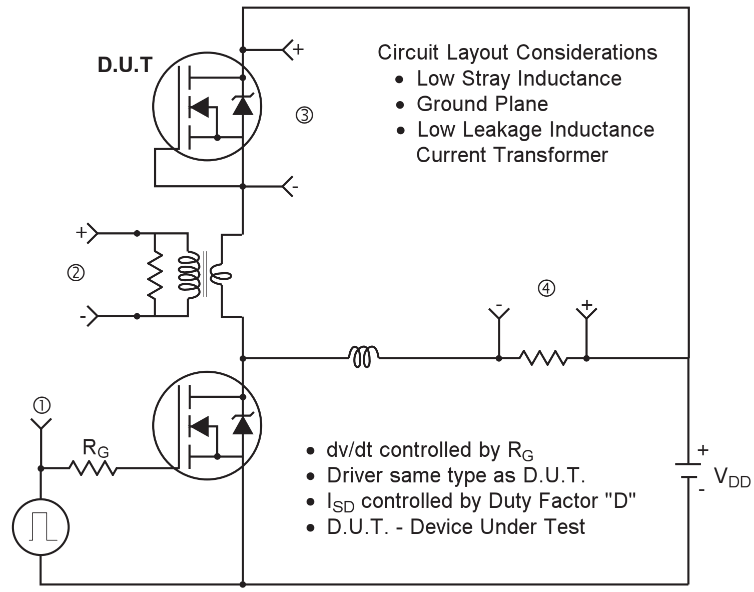
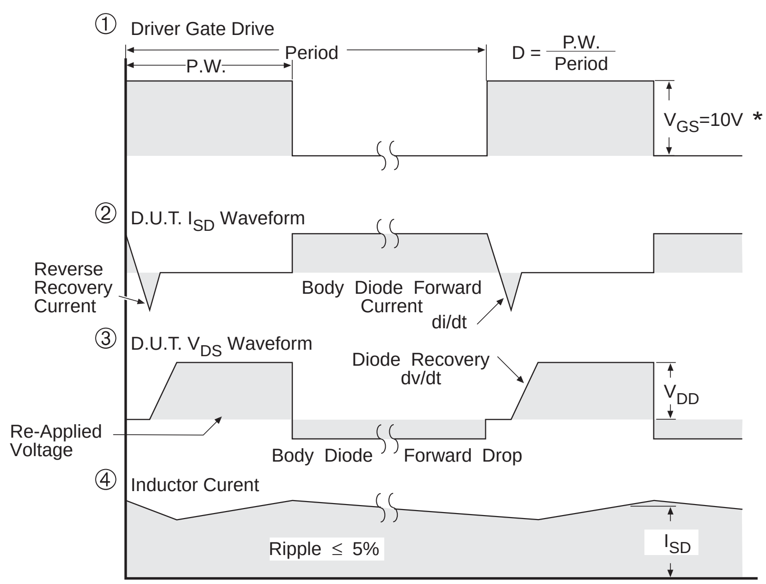


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



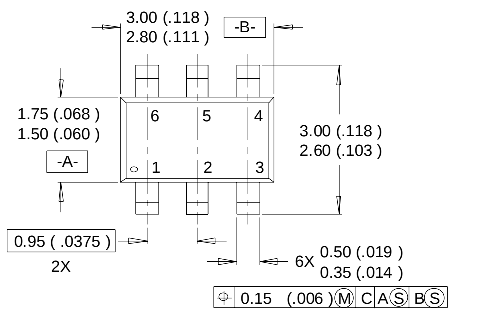


* V_{GS} = 5V for Logic Level Devices

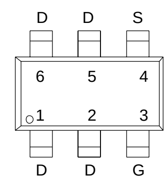
Fig 13. For N-channel HEXFET® power MOSFET s

Package Outline

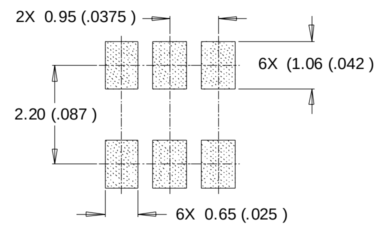
Micro6™

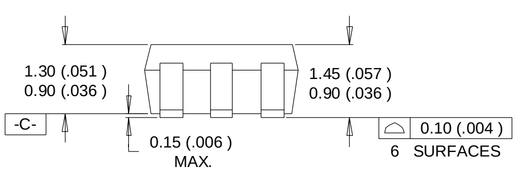


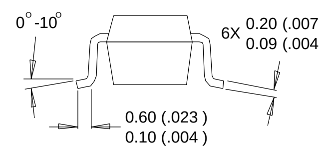
LEAD ASSIGNMENTS



RECOMMENDED FOOTPRINT







NOTES :
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Part Marking Information

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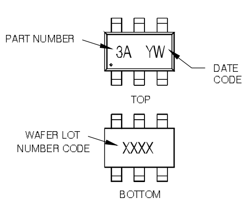
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRLMS6702



PART NUMBER CODE REFERENCE:

2A = IRLMS1902
2B = IRLMS1503
2C = IRLMS6702
2D = IRLMS5703
2E = IRLMS6802
2F = IRLMS4502
2G = IRLMS2002
2H = IRLMS6803

DATE CODE EXAMPLES:
YWW = 9603 = 6C
YWW = 9632 = FF

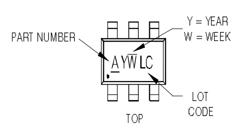
WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

WW = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

Notes: This part marking information applies to devices produced after 02/26/2001



PART NUMBER CODE REFERENCE:

A = IRLMS1902
B = IRLMS1503
C = IRLMS6702
D = IRLMS5703
E = IRLMS6802
F = IRLMS4502
G = IRLMS2002
H = IRLMS6803

Note: A line above the work week (as shown here) indicates Lead-Free.

W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

W = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

Tape & Reel Information

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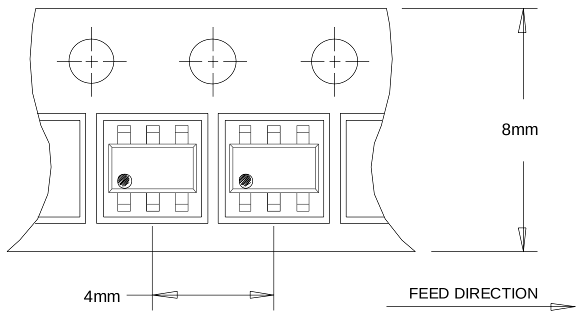
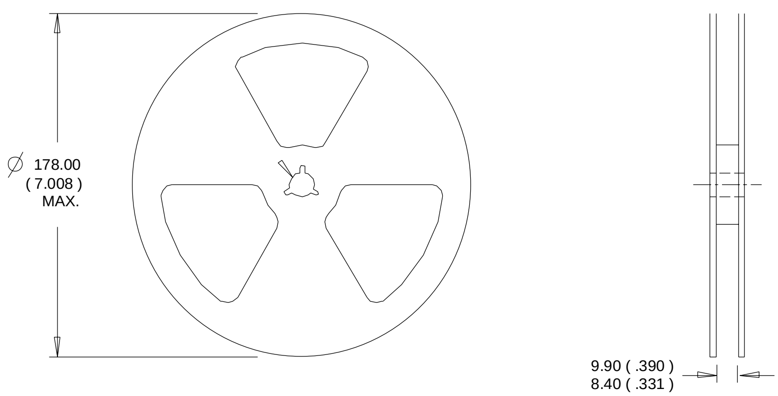


NOTES :
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.

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