CA5420A

0.5MHz, Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers

FN1925
Rev 9.00
February 11, 2015

The CA5420A is an integrated circuit operational amplifier that combines PMOS transistors and bipolar transistors on a single monolithic chip. It is designed and guaranteed to operate in microprocessor logic systems that use V+ = 5V, V- = GND, since it can operate down to ±1V supplies. It will also be suitable for 3.3V logic systems.

The CA5420A BiMOS operational amplifier features gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every +10°C increase in temperature. The CA5420A operates at total supply voltages from 2V to 20V either single or dual supply. This operational amplifier is internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, it has access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45V below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.0mA (Min) is provided by using nonlinear current mirrors.

This device has guaranteed specifications for 5V operation over the full military temperature range of -55°C to +125°C.

The CA5420A has the same 8 lead pinout used for the industry standard 741.

Features

- CA5420A at 5V supply voltage with full military temperature range guaranteed specifications
- CA5420A guaranteed to operate from ±1V to ±10V supplies
- 2V supply at 350µA supply current
- 1pA (Typ) input current (essentially constant to +85°C)
- Rail-to-rail output swing (Drive ±2mA into 1kΩ load)
- Pin compatible with 741 op amp
- Pb-free (RoHS compliant)

Applications

- pH probe amplifiers
- Picoammeters
- Electrometer (High Z) instruments
- Portable equipment
- Inaccessible field equipment
- Battery dependent equipment (medical and military)
- 5V logic systems
- Microprocessor interface

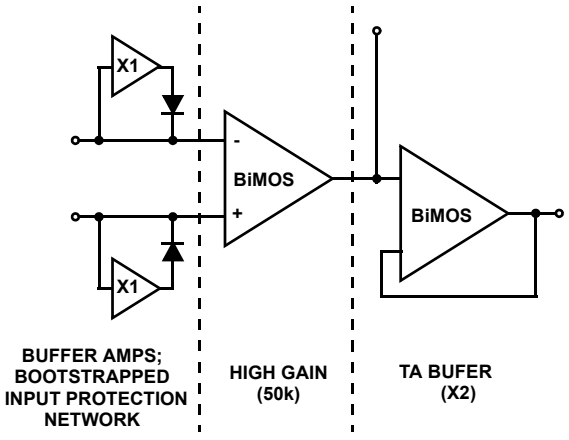


FIGURE 1. FUNCTIONAL DIAGRAM

Ordering Information

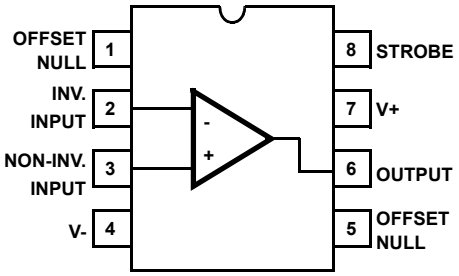
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
CA5420AMZ	5420 AMZ	-55 to +125	8 Ld SOIC	M8.15

NOTES:

1. Add “96” suffix for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for CA5420A. For more information on MSL please see techbrief TB363.

Pin Configuration

CA5420A
(8 LD SOIC)
TOP VIEW



Pin is connected to Case.

Absolute Maximun Ratings

Supply Voltage (Between V+ and V- Terminals) 22V
Differential Input Voltage 15V
Input Voltage . . . . . (V+ + 8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 4) . . . . . Indefinite
Temperature Range . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package	157	N/A

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range (All Types) . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Short circuit may be applied to ground or to either supply.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Typical Values Intended Only for Design Guidance. V+ = +5V; V- = GND, T_A = +25°C

PARAMETER		SYMBOL	TEST CONDITIONS		CA5420A	UNITS
Input Resistance		R_I			150	TΩ
Input Capacitance		C_I			4.9	pF
Output Resistance		R_O			300	Ω
Equivalent Input Noise Voltage		e_N	f = 1kHz	R_S = 100Ω	62	$nV/\sqrt{Hz}$
			f = 10kHz		38	$nV/\sqrt{Hz}$
Short-Circuit Current To Opposite Supply	Source	$I_{OM}+$			2.6	mA
	Sink	$I_{OM}-$			2.4	mA
Gain Bandwidth Product		f_T			0.5	MHz
Slew Rate		SR			0.5	V/µs
Transient Response	Rise Time	t_r	R_L = 2kΩ, C_L = 100pF		0.7	µs
	Overshoot	OS			15	%
Current from Terminal 8 To V-		I_8+			20	µA
Current from Terminal 8 To V+		I_8-			2	mA
Settling Time		0.01%	A_V = 1	$2V_{P-P}$ Input	8	µs
		0.10%	A_V = 1	$2V_{P-P}$ Input	4.5	µs

Electrical Specifications

T_A = +25°C, V+ = 5V, V- = 0, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420A			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	
Input Offset Voltage	V_{IO}	V_O = 2.5V		1	5	mV
Input Offset Current	I_{IO}	V_O = 2.5V		0.02	4	pA
Input Current	I_I	V_O = 2.5V		0.02	5	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.7V, V_O = 2.5V	75	83		dB
Common Mode Input Voltage Range	$V_{ICR}+$	V_O = 2.5V	3.7	4		V
	$V_{ICR}-$			-0.3	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	70	83		dB
Large Signal Voltage Gain	A_{OL}					
V_O = 0.5 to 4V		R_L = ∞	85	87		dB
V_O = 0.5 to 4V		R_L = 10kΩ	85	87		dB
V_O = 0.7 to 3V		R_L = 2kΩ	70	85		dB
Source Current	I_{SOURCE}	V_O = 0V	1.2	2.7		mA

Electrical Specifications T_A = +25°C, V+ = 5V, V- = 0, Unless Otherwise Specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420A			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	
Sink Current	I_{SINK}	V_O = 5V	1.2	2.1		mA
Output Voltage	V_{OM}+	R_L = ∞	4.85	4.94		V
	V_{OM}-			0.13	0.15	V
	V_{OM}+	R_L = 10kΩ	4.7	4.9		V
	V_{OM}-			0.12	0.15	V
	V_{OM}+	R_L = 2kΩ	3.5	4.6		V
	V_{OM}-			0.1	0.15	V
Supply Current	I_{SUPPLY}	V_O = 0V		400	550	µA
		V_O = 2.5V		430	600	µA

Electrical Specifications T_A = -55°C to +125°C, V+ = 5V, V- = 0, Unless Otherwise Specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420A			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	
Input Offset Voltage	V_{IO}	V_O = 2.5V		2	**10**	mV
Input Offset Current	I_{IO}	V_O = 2.5V		1.5	**3**	nA
Up to T_A = +85°C				2	10	pA
Input Current	$\|I_I\|$	V_O = 2.5V		2	**5**	nA
Up to T_A = +85°C				10	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.7V, V_O = 2.5V	**70**	80		dB
Common Mode Input Voltage Range	V_{ICR}+	V_O = 2.5V	**3.7**	4		V
	V_{ICR}-			-0.3	**0**	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	**70**	83		dB
Large Signal Voltage Gain	A_{OL}					
V_O = 0.5 to 4V		R_L = ∞	**65**	75		dB
V_O = 0.7 to 4V		R_L = 10kΩ	**80**	87		dB
V_O = 0.7 to 2.5V		R_L = 2kΩ	**70**	80		dB
Source Current	I_{SOURCE}	V_O = 0V	**1**	2.7		mA
Sink Current	I_{SINK}	V_O = 5V	**1**	2.1		mA
Output Voltage	V_{OM}+	R_L = ∞	**4.8**	4.9		V
	V_{OM}-			0.16	**0.2**	V
	V_{OM}+	R_L = 10kΩ	**4.7**	4.9		V
	V_{OM}-			0.15	**0.2**	V
	V_{OM}+	R_L = 2kΩ	**3**	4		V
	V_{OM}-			0.14	**0.2**	V
Supply Current	I_{SUPPLY}	V_O = 0V		430	**600**	µA
		V_O = 2.5V		480	**650**	µA

Electrical Specifications For Equipment Design at V_{SUPPLY} = ±1V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420A			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	
Input Offset Voltage	V_{IO}			2	5	mV
Input Offset Current	$\|I_{IO}\|$			0.01	4	pA
Input Current	$\|I_I\|$			0.02	5	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	10	100		kV/V
			80	100		dB
Common Mode Rejection Ratio	CMRR			560		µV/V
			50	65		dB
Common Mode Input Voltage Range	V_{ICR}+		0.2	0.5		V
	V_{ICR}-		-1	-1.3		V
Power Supply Rejection Ratio	PSRR			32	425	µV/V
			70	90		dB
Maximum Output Voltage	V_{OM}+	R_L = ∞	0.9	0.95		V
	V_{OM}-		-0.85	-0.91		V
Supply Current	I_{SUPPLY}			350	650	µA
Device Dissipation	P_D			0.7	1.1	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$			4		µV/°C

Electrical Specifications For Equipment Design at V_{SUPPLY} = ±10V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420A			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	
Input Offset Voltage	V_{IO}			2	5	mV
Input Offset Current	$\|I_{IO}\|$			0.03	4	pA
Input Current	$\|I_I\|$			0.05	5	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	20	100		kV/V
			80	100		dB
Common Mode Rejection Ratio	CMRR			100	320	µV/V
			70	80		dB
Common Mode Input Voltage Range	V_{ICR}+		9	9.3		V
	V_{ICR}-		-10	-10.3		V
Power Supply Rejection Ratio	PSRR			32	320	µV/V
			70	90		dB
Maximum Output Voltage	V_{OM}+	R_L = ∞	9.7	9.9		V
	V_{OM}-		-9.7	-9.85		V
Supply Current	I_{SUPPLY}			450	1000	µA
Device Dissipation	P_D			9	14	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$			4		µV/°C

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Applications

Picoammeter Circuit

The exceptionally low input current (typically 0.2pA) makes the CA5420A highly suited for use in a picoammeter circuit. With only a single 10GΩ resistor, this circuit covers the range from ±1.5pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1MΩ resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10MΩ resistor connected to pin 2 of the CA5420A decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

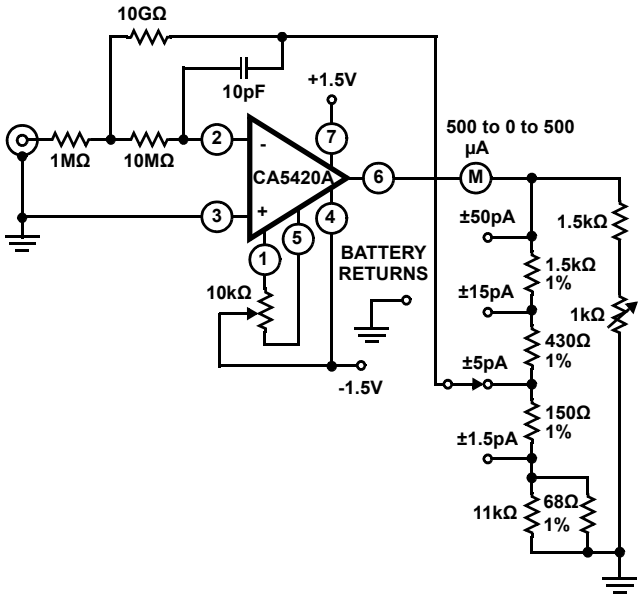


FIGURE 2. PICOAMMETER CIRCUIT

High Input Resistance Voltmeter

Advantage is taken of the high input impedance of the CA5420A in a high input resistance DC voltmeter. Only two 1.5V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000MΩ) DC voltmeter. Full-scale deflection is ±500mV, ±150mV, and ±15mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300µA. At full-scale deflection this current rises to 800µA. Carbon-zinc battery life should be in excess of 1,000 hours.

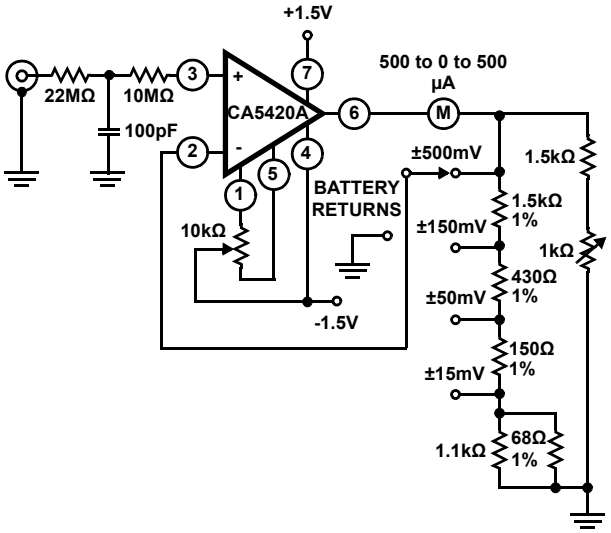


FIGURE 3. HIGH INPUT RESISTANCE VOLTMETER

Typical Performance Curves

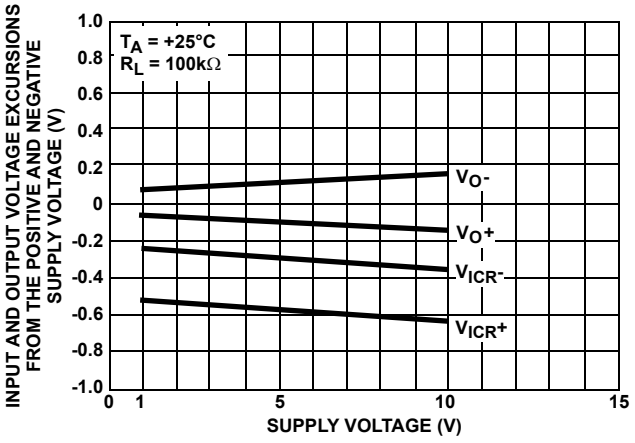


FIGURE 4. OUTPUT VOLTAGE SWING AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

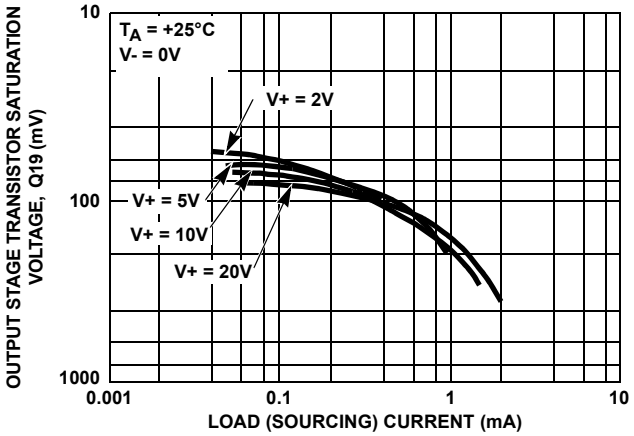


FIGURE 5. OUTPUT VOLTAGE vs LOAD SOURCING CURRENT

Typical Performance Curves (Continued)

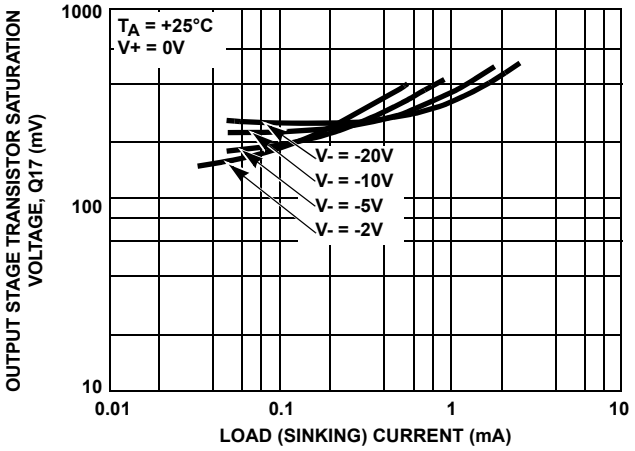


FIGURE 6. OUTPUT VOLTAGE vs LOAD SINKING CURRENT

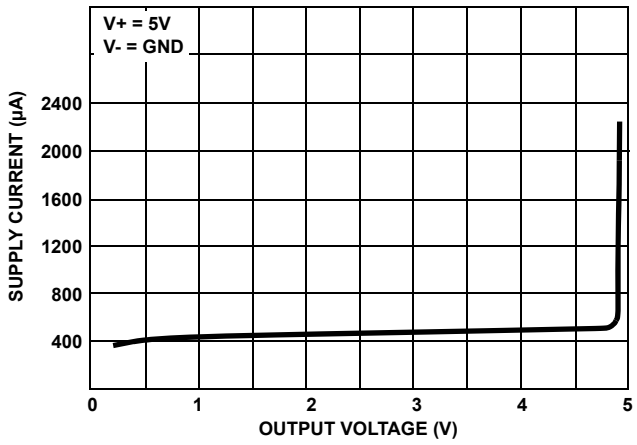


FIGURE 7. SUPPLY CURRENT vs OUTPUT VOLTAGE

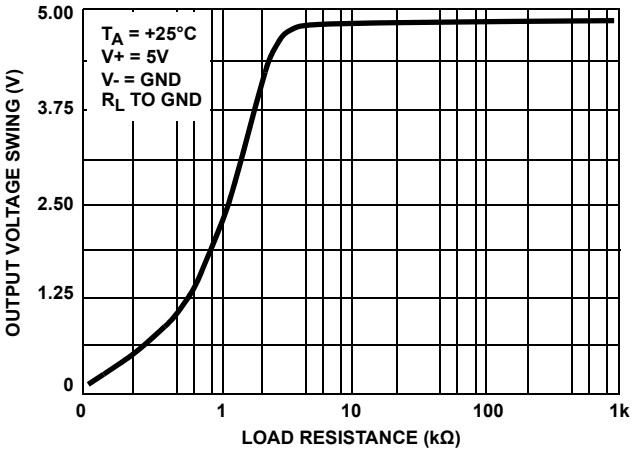


FIGURE 8. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

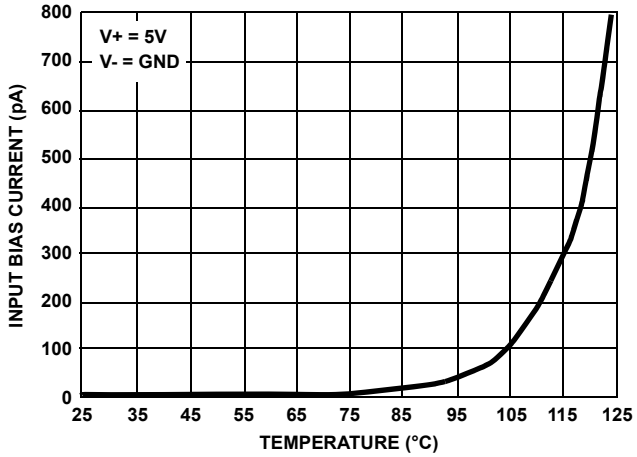


FIGURE 9. INPUT BIAS CURRENT DRIFT ($\Delta I_B/\Delta T$)

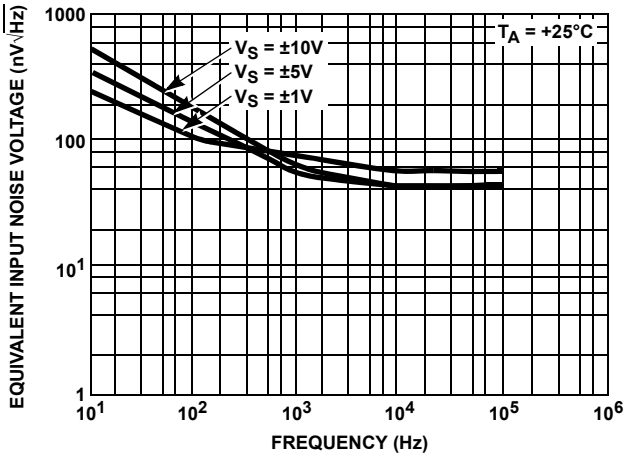


FIGURE 10. INPUT NOISE VOLTAGE vs FREQUENCY

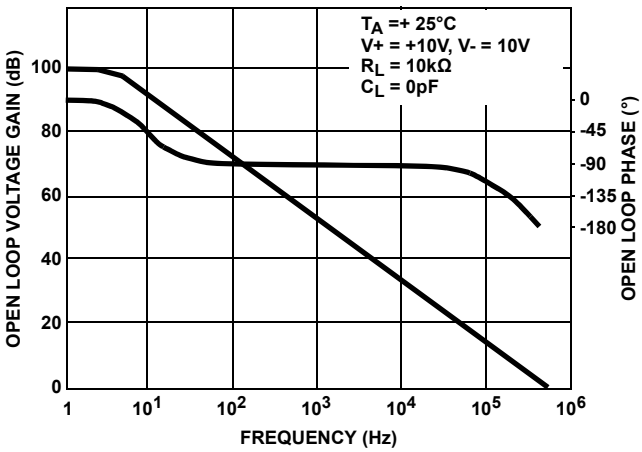


FIGURE 11. OPEN LOOP GAIN AND PHASE SHIFT RESPONSE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
February 11, 2015	FN1925.9	Electrical Specifications Table: On page 3, Large signal voltage gain Vo = 0.7 to 3V Min limit changed from 80 to 70, and page 4 Large signal voltage gain Vo = 0.7 to 2.5V Min limit changed from 75 to 70.
September 25, 2013	FN1925.8	Page 5 - Changed CMRR limits for ±1V spec table from 60dB to 50dB Page 9 - Updated POD to rev 4. Changes from rev 3: Changed Note 1 "1982" to "1994".
July 8, 2011	FN1925.7	page 1 Features: Change "2V Supply at 300µA....." to "2V Supply at 350µA....." page 3 Updated Thermal Resistance note for package. page 3 Electrical Spec Table, V+ = 5V, V- = 0V (lower table): change PSRR min from 75dB to 70dB. page 4 Electrical Spec Table, V+ = 5V, V- = 0V (upper table) Change Supply Current Vo =0V Max from 500µA to 550µA, and V0 = 2.5V change max from 550µA to 600µA. page 4 Electrical Spec Table, TA = -55 to +125 V+ = 5V, V- = 0V (lower table) change Supply Current VO=0V Max from 550µA to 600µA, change Vo=2.5V max from 600uA to 650uA. page 5 Electrical Spec Table Vsupply =+/-1V (upper table) Common Mode Rejection Ratio, delete 1000uV/V MAX spec and leave only a typ spec. PSRR change 320uV/V max to 425µV/V max. page 9 POD M8.15 Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205)
December 08, 2009	FN1925.6	Electrical Specifications Table; TA = 25°C, V+ = 5V, V- = 0V; Change Input Offset Current Max from 0.5pA to 4pA P3, same table as above; Input Current Max from 1pA to 5pA. P4: same table as above; Output Voltage VOM+: Minimum spec for RL = Infinity from 4.9V to 4.85V P5: In Vsupply = +/-1V, Large Signal Voltage Gain spec : Min from 20kV/V to 10kV/V and from 86dB to 80dB P4; Large Signal Voltage Gain RL = inf; change min to 65dB and typ to75dB (was 85dB Min and 87dB Typ) Updated Pb-free bullet in Features and Pb-free note in Ordering Information based on lead finish. Added TB347 link to ordering information for reel specifications. Added MSL link to Order Info Updated Caution statement in Abs Max per legal's new verbiage. Added Pb-Free Reflow link to Thermal Info Added POD to last page Added standard Over Temp note to applicable elec spec tables Corrected Input Offset Current Max from 0.4pA to 4pA
December 21, 2005	FN1925.5	Added redline release FGs to ordering information table.
September 1998	FN1925.4	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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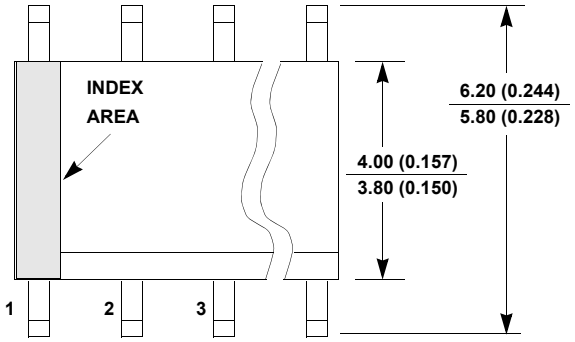
Package Outline Drawing

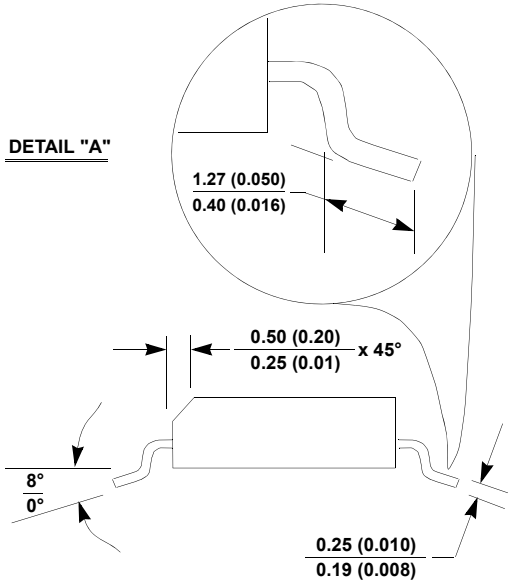
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

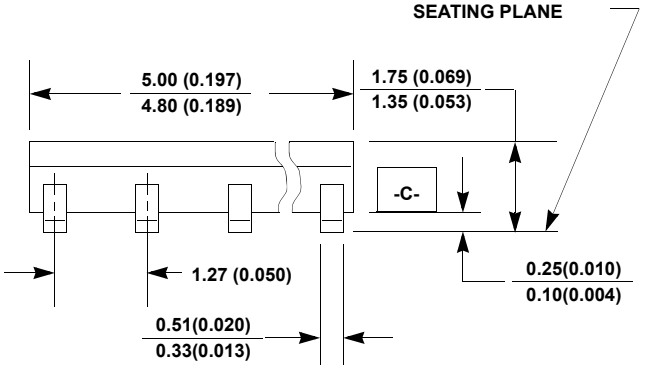
Rev 4, 1/12



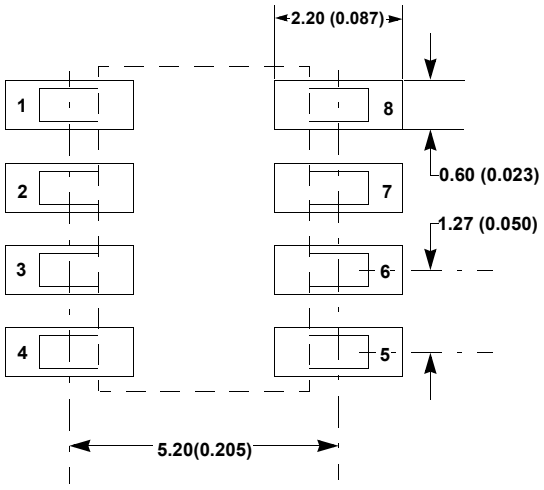
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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