MCP39F521

I²C Power Monitor with Calculation and Energy Accumulation

Features

- Power Monitoring Accuracy Capable of 0.1% Error Across 4000:1 Dynamic Range
- Built-In Calculations on Fast 16-bit Processing Core
  - Active, Reactive, Apparent Power
  - True Root Mean Square (RMS) Current, RMS Voltage
  - Line Frequency, Power Factor
- 64-bit Wide Import and Export Active Energy Accumulation Registers
- 64-bit Four Quadrant Reactive Energy Accumulation Registers
- Signed Active and Reactive Power Outputs
- Dedicated Zero Crossing Detection (ZCD) Pin Output with Less than 100 µs Latency
- Automatic Event Pin Control through Fast Voltage Surge Detection, Less than 5 ms Delay
- I²C Interface, up to 400 kHz Clock Rate
- Two Independent Registers for Minimum and Maximum Output Quantity Tracking
- Fast Calibration Routines and Simplified Command Protocol
- 512 Bytes User-Accessible EEPROM through Page Read/Write Commands
- Low-Drift Internal Voltage Reference, 10 ppm/°C Typical
- 28-lead 5 x 5 mm QFN Package
- Extended Temperature Range -40°C to +125°C

Applications

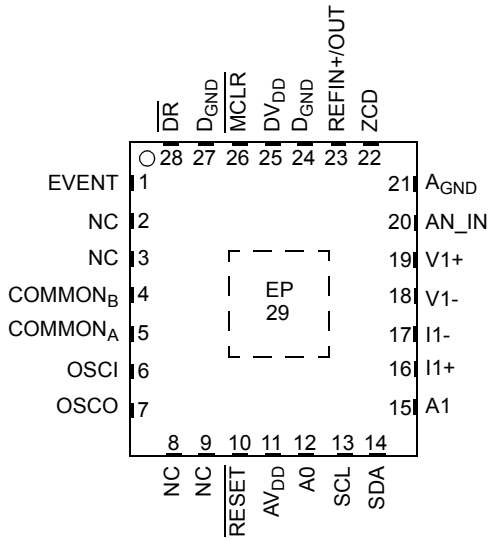
- Power Monitoring for Home Automation
- Industrial Lighting Power Monitoring
- Real-Time Measurement of Input Power for AC/DC Supplies
- Intelligent Power Distribution Units

Description

The MCP39F521 is a highly integrated, complete single-phase power-monitoring device, designed for real-time measurement of input power for AC/DC power supplies, power distribution units, consumer and industrial applications. It includes dual-channel delta-sigma ADCs, a 16-bit calculation engine, EEPROM and a flexible two-wire I²C interface. An integrated low-drift voltage reference with 10 ppm/°C in addition to 94.5 dB of signal-to-noise and distortion ratio (SINAD) performance on each measurement channel allows for better than 0.1% accurate designs across a 4000:1 dynamic range.

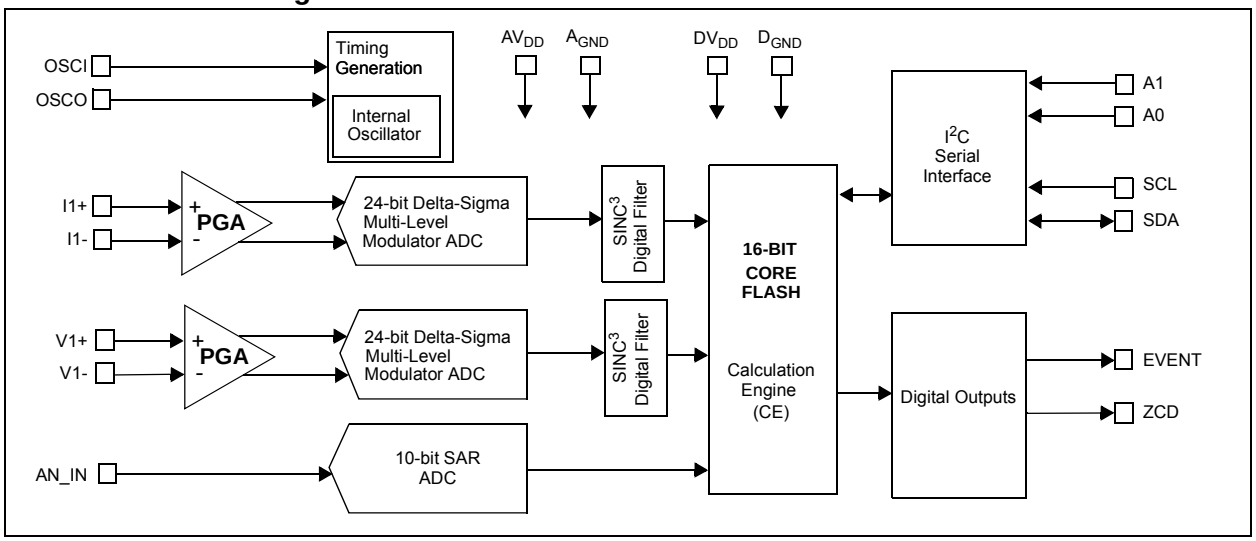
Package Types

MCP39F521
5x5 QFN*

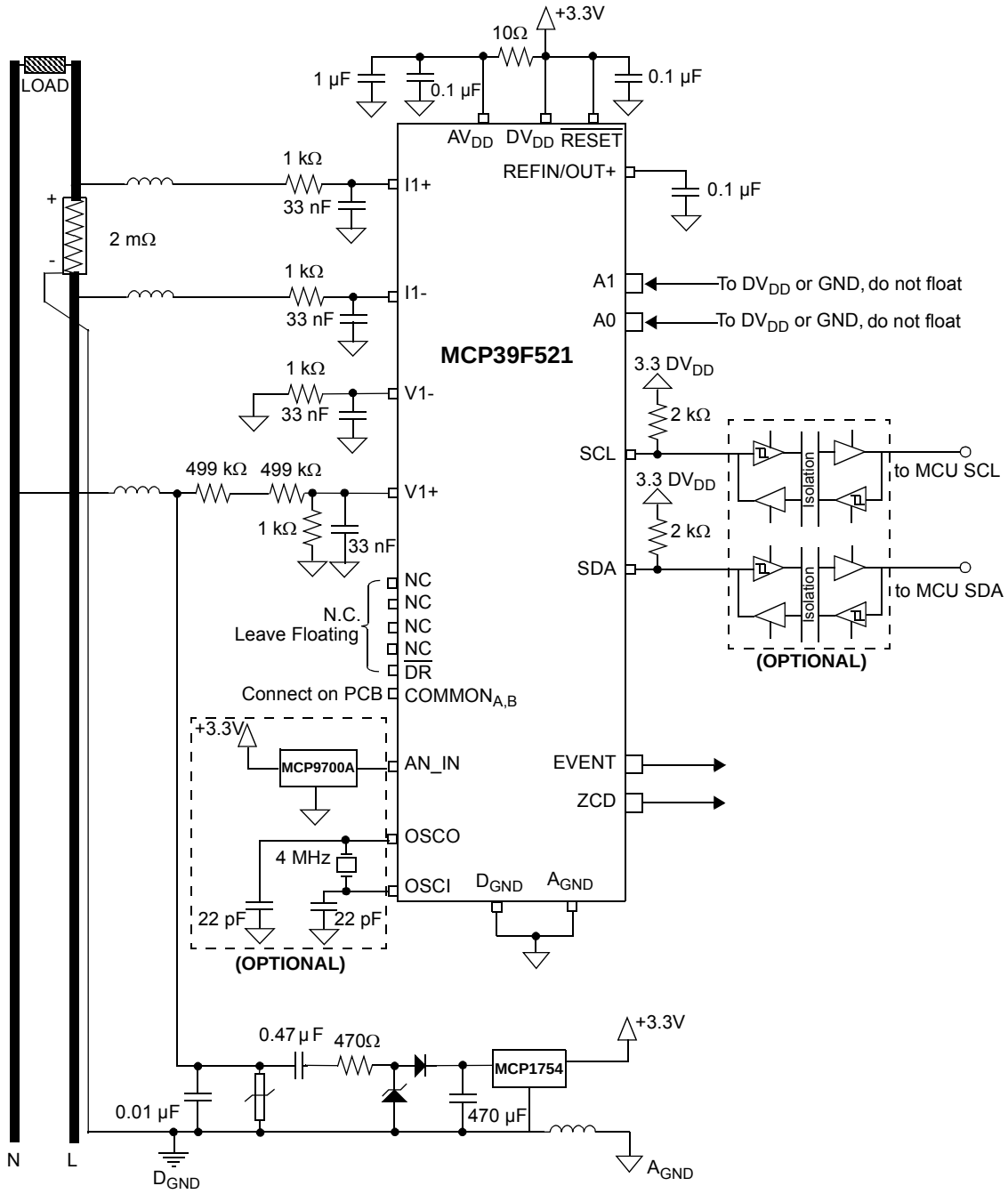


*Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



MCP39F521 Typical Application – Single-Phase, Two-Wire Application Schematic



Note: The external sensing components shown here, a 2 mΩ shunt, two 499 kΩ and 1 kΩ resistors for the 1000:1 voltage divider, are specifically chosen to match the default values for the calibration registers defined in **Section 6.0, Register Descriptions**. By choosing low-tolerance components of these values (e.g. 1% tolerance), measurement accuracy in the 2-3% range can be achieved with zero calibration. See **Section 8.0, MCP39F521 Calibration** for more information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} ..... -0.3 to +4.5V
AV_{DD} ..... -0.3 to +4.0V
Digital inputs and outputs w.r.t. A_{GND} ..... -0.3V to +4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} ..... -2V to +2V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin ..... 300 mA
Maximum Current into DV_{DD} pin ..... 250 mA
Maximum Output Current Sunk by Digital IO ..... 25 mA
Maximum Current Sourced by Digital IO ..... 25 mA
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) ..... 4.0 kV, 200V
ESD on all other pins (HBM,MM) ..... 4.0 kV, 200V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Power Measurement						
Active Power **(Note 1)**	P	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 2)**
Reactive Power **(Note 1)**	Q	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 2)**
Apparent Power **(Note 1)**	S	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 2)**
Current RMS **(Note 1)**	I_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 2)**
Voltage RMS **(Note 1)**	V_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Voltage Channel **(Note 2)**
Power Factor **(Note 1)**	Φ	—	±0.1	—	%	
Line Frequency **(Note 1)**	LF	—	±0.1	—	%	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.
2: Specification by design and characterization; not production tested.
3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.
4: Applies to Voltage Sag and Voltage Surge events only.
5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.
6: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.
7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x ($1/f_{LINE}$)	—	ms	**Note 3**
Minimum Time for Voltage Surge/Sag Detection	t_{AC_SASU}	—	see **Section 7.0**	—	ms	**Note 4**
24-Bit Delta-Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (V1+ – V1-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	**Note 5**
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	**Note 6**
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	**Note 6**
Signal-to-Noise Ratio	SNR	92	95	—	dB	**Note 6**
Spurious Free Dynamic Range	SFDR	—	111	—	dB	**Note 6**
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + 0.6V_{PP}, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.

6: V_{IN} = 1V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
10-Bit SAR ADC Performance for Temperature Measurement						
Resolution	N_R	—	10	—	bits	
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	D_{VDD} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Nonlinearity	I_{NL}	—	±1	±2	LSb	
Differential Nonlinearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Temperature Measurement Rate		—	$f_{LINE}/2^N$	—	sps	**Note 3**
Clock and Timings						
I^2C Clock Frequency	f_{SCL}	—	—	400	kHz	100 kHz and 400 kHz I^2C modes supported
Master Clock and Crystal Frequency	f_{MCLK}	-2%	4	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40 to +85°C only (**Note 7**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	
Temperature Coefficient	TCV_{REF}	—	10	—	ppm/°C	T_A = -40°C to +85°C, V_{REFEXT} = 0
Output Impedance	$ZOUTV_{REF}$	—	2	—	kΩ	
Current, V_{REF}	$AI_{DD}V_{REF}$	—	40	—	µA	
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.3V	V	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.

6: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	
DV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0 – 3.3V in 0.1s, 0 – 2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power On Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms
Operating Current	I_{DD}	—	13	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	Years	Provided no other specifications are violated
Supply Current during Programming	I_{DDPD}	—	7	—	mA	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.

6: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 DV_{DD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
		—	0.050	0.100	µA	Digital Output pins only (ZCD, EVENT)

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	36.9	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

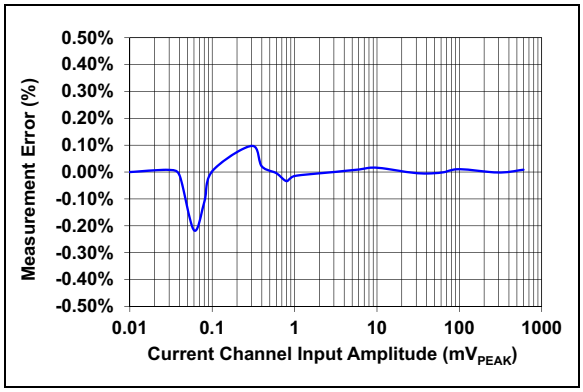


FIGURE 2-1: *Active Power, Gain = 1.*

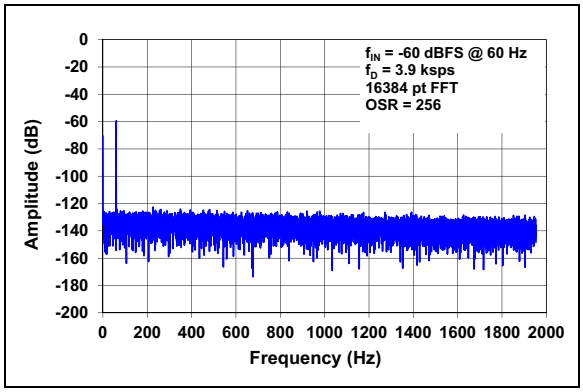


FIGURE 2-4: *Spectral Response.*

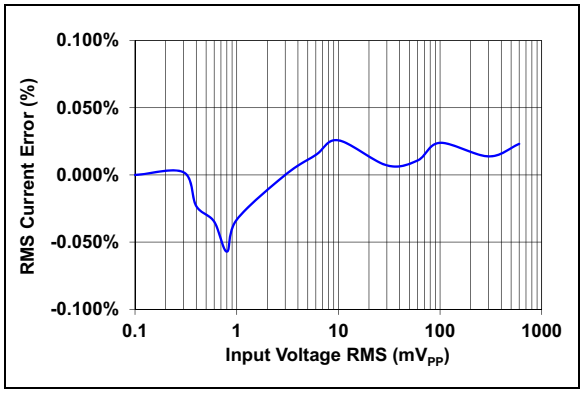


FIGURE 2-2: *RMS Current, Gain = 1.*

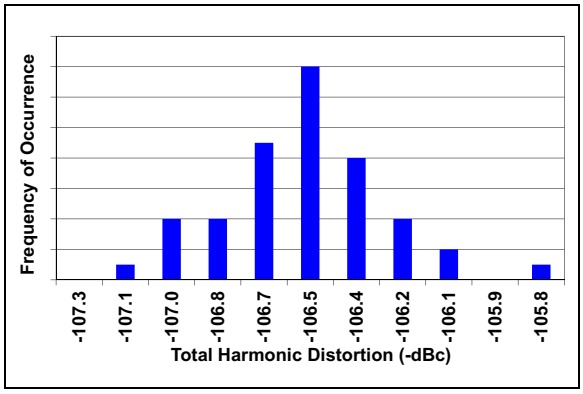


FIGURE 2-5: *THD Histogram.*

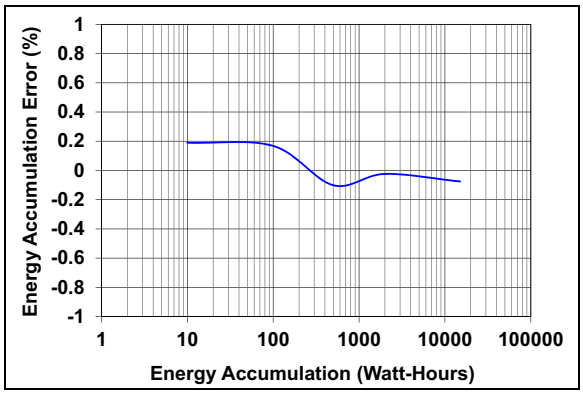


FIGURE 2-3: *Energy, Gain = 8.*

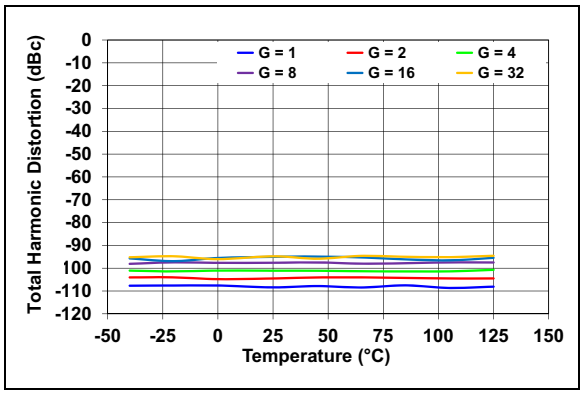


FIGURE 2-6: *THD vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

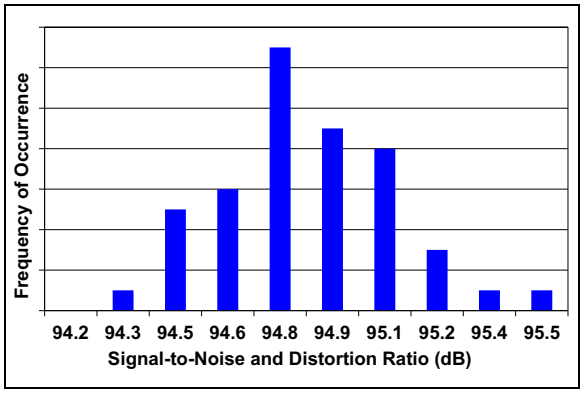


FIGURE 2-7: *SNR Histogram.*

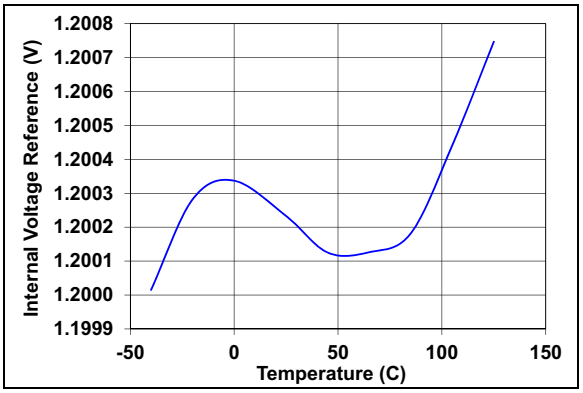


FIGURE 2-10: *Internal Voltage Reference vs. Temperature.*

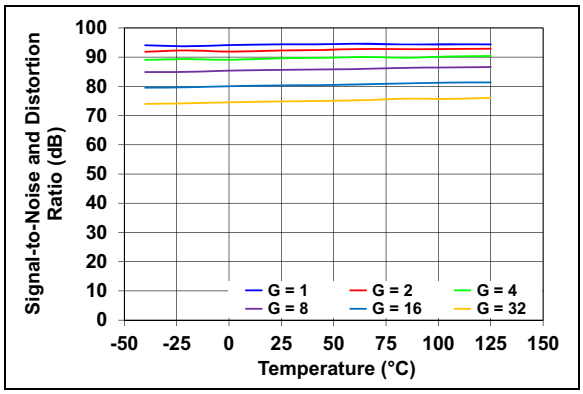


FIGURE 2-8: *SINAD vs. Temperature.*

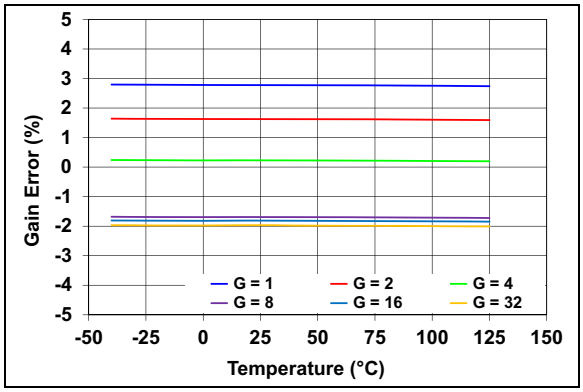


FIGURE 2-9: *Gain Error vs. Temperature.*

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F521 5x5 QFN	Symbol	Function
1	EVENT	Event Output Pin
2, 3, 8, 9	NC	No Connect (must be left floating)
4	$COMMON_B$	Common pin B, to be connected to $COMMON_A$
5	$COMMON_A$	Common pin A, to be connected to $COMMON_B$
6	OSCI	Oscillator Crystal Connection Pin or External Clock Input Pin
7	OSCO	Oscillator Crystal Connection Pin
10	$\overline{RESET}$	Reset Pin for Delta Sigma ADCs
11	AV_{DD}	Analog Power Supply Pin
12	A0	I^2C Address Select Pin A0
13	SCL	I^2C Serial Clock
14	SDA	I^2C Serial Data
15	A1	I^2C Address Select Pin A1
16	I1+	Noninverting Current Channel Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel Input for 24-bit ΔΣ ADC
18	V1-	Inverting Voltage Channel Input for 24-bit ΔΣ ADC
19	V1+	Noninverting Voltage Channel Input for 24-bit ΔΣ ADC
20	AN_IN	Analog Input for SAR ADC
21	A_{GND}	Analog Ground Pin, Return Path for internal analog circuitry
22	ZCD	Zero Crossing Detection Output
23	REFIN+/OUT	Noninverting Voltage Reference Input and Internal Reference Output Pin
24, 27	D_{GND}	Digital Ground Pin, Return Path for internal digital circuitry
25	DV_{DD}	Digital Power Supply Pin
26	$\overline{MCLR}$	Master Clear for Device
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to D_{GND})

3.1 Event Output Pin (EVENT)

This digital output pin can be configured to act as an output flag based on various internal raise conditions. Control is modified through the Event Configuration register.

3.2 Common Pins ($COMMON_A$ and $COMMON_B$)

The $COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F521. These two pins should be connected together in the application.

3.3 Oscillator Pins (OSCI/OSCO)

OSCI and OSCO provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 4 MHz crystal can be connected to these pins. If a crystal of external clock source is not detected, the device will clock from the internal 4 MHz oscillator.

3.4 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the delta-sigma ADCs, PGA, internal V_{REF} and other blocks associated with the analog front-end in a Reset state when pulled low. This input is Schmitt-triggered.

3.5 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F521.

This pin requires appropriate bypass capacitors and should be maintained to 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.6 Chip Address Inputs (A0, A1)

The A0 and A1 inputs are used by the MCP39F521 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four devices may be connected to the same bus by using different combinations. These inputs must be connected to V_{DD} or GND and cannot be left floating.

In most applications, the chip address inputs are hardwired to logic 0 or logic 1. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic 0 or logic 1 before normal device operation can proceed.

3.7 I^2C Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.8 I^2C Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to DV_{DD} (typical 10kΩ for 100kHz, 2kΩ for 400kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Change during SCL high is reserved for indicating the Start and Stop conditions.

3.9 24-Bit Delta Sigma ADC Differential Current Channel Input Pins (I1+/I1-)

I1- and I1+ are the two fully-differential current channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.10 24-Bit Delta Sigma ADC Differential Voltage Channel Inputs (V1-/V1+)

V1- and V1+ are the two fully-differential voltage channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each V_N+/- input pin is ±1V with no distortion and ±2V, with no breaking after continuous voltage.

3.11 Analog Input (AN_IN)

This is the input to the analog-to-digital converter that can be used for temperature measurement and compensation. If temperature compensation is required in the application, it is advised to connect the low-power active thermistor IC MCP9700A to this pin. If temperature compensation is not required, this can be used as a general purpose analog-to-digital converter input.

3.12 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground pin is available on the PCB, it is recommended that this pin be tied to that plane.

3.13 Zero Crossing Detection (ZCD)

This digital output pin is the output of the Zero Crossing Detection circuit of the IC. The output here will be a logic output with edges that transition at each zero crossing of the voltage channel input. For more information see **Section 5.13, Zero Crossing Detection (ZCD)**.

3.14 Noninverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the noninverting side of the differential voltage reference input for the delta sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.15 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry in the system.

3.16 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F521. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.17 Data Ready Pin ($\overline{DR}$)

The data ready pin indicates if a new delta-sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the Data Ready pin to indicate that the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with the line frequency to ensure an integer number of samples for each line cycle.

Note:	This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.18 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to D_{GND}.

NOTES:

4.0 COMMUNICATION PROTOCOL

The I^2C communication protocol is a frame-based protocol, with a complete communication frame occurring between the I^2C start and stop bits.

A command frame is a write transmission from the I^2C master to the MCP39F521 device.

A read response frame is read transmission from the I^2C master to the MCP39F521.

Each command frame consists of a header byte, the number of bytes in the frame, command packet (or command packets) and a checksum.

Each response frame consists of either a ACK, NAK, CSFAIL, or ACK+Data with checksum.

Note:	If a custom communication protocol is desired, please contact a Microchip sales office.

4.1 COMMUNICATION FRAMES

The following two figures represent the command frames and read request frames.

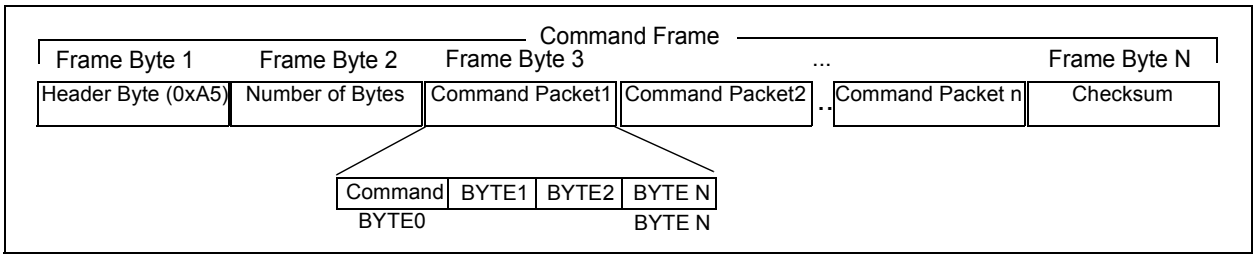


FIGURE 4-1: *MCP39F521 Command Write Frame.*

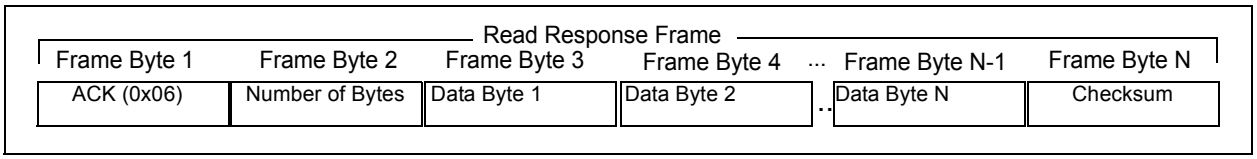


FIGURE 4-2: *MCP39F521 Read Response Frame (ACK with Data).*

The following two figures represent I^2C command frame writes and read frame responses.

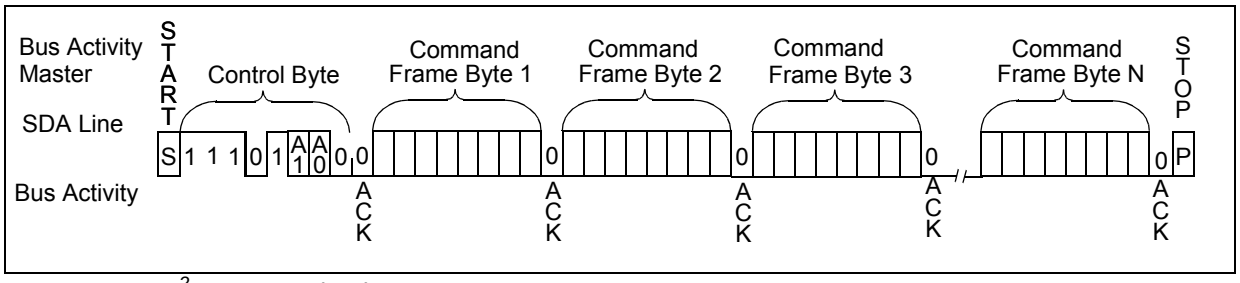


FIGURE 4-3: *I^2C Command Write Frame.*

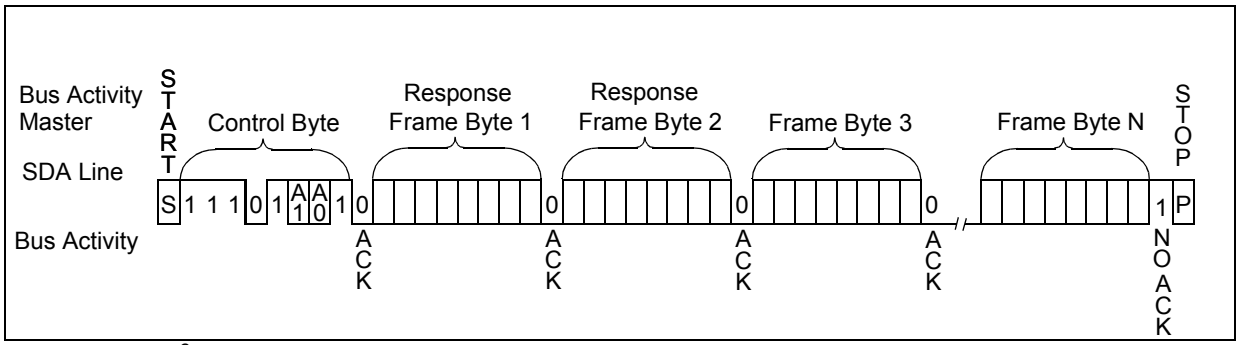


FIGURE 4-4: *I^2C Read Response Frame.*

This approach allows for single, secure transmission from the host processor to the MCP39F521 with either a single command, or multiple commands. No command in a frame is processed until the frame is complete and the checksum and number of bytes are validated after the stop bit.

The number of bytes in an individual *command packet* depends on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

4.2 I²C CONTROL BYTE

A Control byte is the first byte received following the Start condition from the master device. The Control byte consists of a 4-bit control code. For the MCP39F521 the control code is '1110' for all read and write operations. The following three bits are chip-select address bits, A2, A1, and A0. For the MCP39F521, A2 is always set to binary '1'. A1 and A0 are controlled by the logic pins A1 and A0, which allows up to 4 different devices on the I²C bus.

The last bit of the Control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected.

Following a Start condition, the MCP39F521 monitors the SDA bus checking for the 4-bit control code ('1110') and proper address bits. Upon receiving the correct control code and address bits, the slave (MCP39F521) outputs an acknowledge signal on the SDA line, and depending on the state of the R/W bit, will either respond with data or wait to receive additional bytes prior to the Stop condition. The Control byte is defined in the following figure.

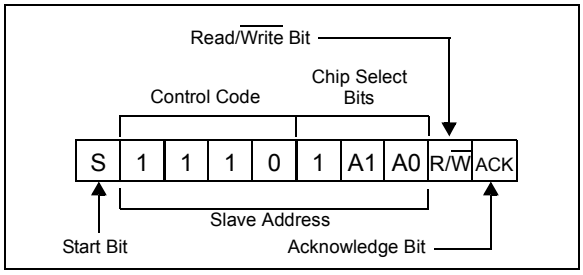


FIGURE 4-5: *MCP39F521 Control Byte Format.*

4.3 I²C Time Out and Clock Stretching

Time out is when an I²C slave resets its interface if the I²C clock is low for longer than a specified time. The MCP39F521 offers a set 2 ms I²C time out that can be disabled through the Time-out Disable bit in the System Configuration Register (Register 6-2).

In addition, the device includes a clock stretching feature which allows the master to know when a frame has been processed. Clock stretching is when a slave device can not cooperate with the clock speed or needs to slow down the bus. In the case of the MCP39F521, after a frame is received, the device will hold the clock low until the frame has been processed. The maximum clock stretching duration is less than 10 milliseconds.

4.4 Checksum

The checksum is generated using simple byte addition and taking the modulus to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F521 will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F521, the frame and checksum are created in the same way, with the header byte becoming an acknowledge (0x06). Communication examples are given in **Section 4.6, Example Communication Frames and MCP39F521 Responses**.

4.5 Command List

The following table is a list of all accepted command bytes for the MCP39F521. There are **10** possible accepted commands for the MCP39F521.

TABLE 4-1: MCP39F521 INSTRUCTION SET

Command #	Command	Command ID	Instruction Parameter	Number of Bytes	Successful Response
1	`Register Read, N bytes`	0x4E	Number of Bytes	2	ACK, Data, Checksum
2	`Register Write, N bytes`	0x4D	Number of Bytes	1+N	ACK
3	`Set Address Pointer`	0x41	ADDRESS	3	ACK
4	`Save Registers To Flash`	0x53	None	2	ACK
5	`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, Checksum
6	`Page Write EEPROM`	0x50	PAGE	18	ACK
7	`Bulk Erase EEPROM`	0x4F	None	2	ACK
8	`Auto-Calibrate Gain`	0x5A	None	**Note 1**	
9	`Auto-Calibrate Reactive Gain`	0x7A	None	**Note 1**	
10	`Auto-Calibrate Frequency`	0x76	None	**Note 1**	

Note 1: See **Section 8.0, MCP39F521 Calibration** for more information on calibration.

4.6 Example Communication Frames and MCP39F521 Responses

Tables 4-2 to 4-11 show exact hexadecimal communication frames as they should be sent to the MCP39F521 from the system MCU. The values here can be used as direct examples for writing your code to communicate to the MCP39F521.

TABLE 4-2: REGISTER READ, N BYTES COMMAND (Note 1)

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x08	Number of Bytes in Frame	
3	0x41	Command (Set Address Pointer)	
4	0x00	Address High	
5	0x02	Address Low	
6	0x4E	Command (`Register Read, N bytes`)	
7	0x20	Number of Bytes to Read (32)	
8	0x5E	Checksum	ACK + Number of Bytes (35) + 32 bytes, + Checksum

Note 1: This example `Register Read, N bytes` frame, as written here, can be used to poll a subset of the output data, starting at the top, address 0x02, and reading 32 data bytes back or 35 bytes total in the frame.

TABLE 4-3: REGISTER WRITE, N- BYTES COMMAND (Note 1)

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x25	Number of Bytes in Frame	
3	0x41	Command (Set Address Pointer)	
4	0x00	Address High	
5	0x48	Address Low	
6	0x4D	Command (`Register Write, N Bytes`)	
7	0x1C	Number of Bytes to Write (28)	
8-36	*Data*	Data Bytes (28 total data bytes)	
37	Checksum	Checksum	ACK

Note 1: This `Register Write, N Bytes` frame, as written here, can be used to write the entire set of calibration target data, starting at the top, address 0x7A, and continuing to write until the end of this set of registers, 28 bytes later, register 0x94. Note these are not the calibration registers, but the calibration targets which need to be written prior to issuing the auto-calibration target commands. See **Section 8.0, MCP39F521 Calibration** for more information.

TABLE 4-4: SET ADDRESS POINTER COMMAND (Note 1)

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x06	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0xEE	Checksum	ACK

Note 1: The `Set Address Pointer` command is typically included inside of a frame that includes a read or write command, as shown in Table 4-2 and Table 4-3. There is typically no reason for this command to have its own frame, but is shown here as an example.

TABLE 4-5: SAVE TO FLASH COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x53	Command (`Save To Flash`)	
4	0xFC	Checksum	ACK

TABLE 4-6: PAGE READ EEPROM COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x42	Command (`Page Read EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5	0xED	Checksum	ACK + EEPROM Page Data + Checksum

TABLE 4-7: PAGE WRITE EEPROM COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x15	Number of Bytes in Frame	
3	0x50	Command (`Page Write EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5-20	*Data*	EEPROM Data (16 bytes/Page)	
21	Checksum	Checksum	ACK

TABLE 4-8: BULK ERASE EEPROM COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x4F	Command (`Bulk Erase EEPROM`)	
4	0xF8	Checksum	ACK

TABLE 4-9: AUTO-CALIBRATE GAIN COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x5A	Command (`Auto-Calibrate Gain`)	
4	0x03	Checksum	ACK (or NAK if unable to calibrate), see **Section 8.0, MCP39F521 Calibration** for more information.

TABLE 4-10: AUTO-CALIBRATE REACTIVE GAIN COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x7A	Command (`Auto-Calibrate Reactive Gain`)	
4	0x23	Checksum	ACK (or NAK if unable to calibrate), see **Section 8.0, MCP39F521 Calibration** for more information.

TABLE 4-11: AUTO-CALIBRATE FREQUENCY COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x76	Command (`Auto-Calibrate Frequency`)	
4	0x1F	Checksum	ACK (or NAK if unable to calibrate), see **Section 8.0, MCP39F521 Calibration** for more information.

4.7 Command Descriptions

4.7.1 REGISTER READ, N BYTES (0x4E)

The `Register Read, N bytes` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. The maximum number of bytes that can be read with this command is 32. If there are other read commands within a frame, the maximum number of bytes that can be read is 32 minus the number of bytes being read in the frame. With this command, the data is returned LSB first.

4.7.2 REGISTER WRITE, N BYTES (0x4D)

The `Register Write, N bytes` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other write commands. An acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 32. If there are other write commands within a frame, the maximum number of bytes that can be written is 32 minus the number of bytes being written in the frame. With this command, the data is written LSB first.

4.7.3 SET ADDRESS POINTER (0x41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes, address high byte followed by address low byte. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an acknowledge will be returned.

4.7.4 SAVE REGISTERS TO FLASH (0x53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to flash. This includes all R/W registers in the register set. The response to this command is an acknowledge.

4.7.5 PAGE READ EEPROM (0x42)

The `Read Page EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F521. A more complete description of the memory organization of the EEPROM can be found in **Section 9.0, EEPROM**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an acknowledge, 16-bytes of data and CRC checksum.

4.7.6 PAGE WRITE EEPROM (0x50)

The `Page Write EEPROM` command is expecting 17 additional bytes in the command parameters, which are the EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 9.0, EEPROM** The response to this command is an acknowledge.

4.7.7 BULK ERASE EEPROM (0x4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 9.0, EEPROM**. The response to this command is acknowledge.

4.7.8 AUTO-CALIBRATE GAIN (0x5A)

The `Auto-Calibrate Gain` command initiates the single-point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and active power based on the target values written in the corresponding registers. See **Section 8.0, MCP39F521 Calibration** for more information on device calibration. The response to this command is acknowledge.

4.7.9 AUTO-CALIBRATE REACTIVE GAIN (0X7A)

The `Auto-Calibrate Reactive Gain` command initiates a single-point calibration to match the measured reactive power to the target reactive power. This is typically done at PF = 0.5. See section **Section 8.0, MCP39F521 Calibration** for more information on device calibration.

4.7.10 AUTO-CALIBRATE FREQUENCY (0x76)

For applications not using an external crystal and running the MCP39F521 off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency (0x00AE) register is set such that the frequency indication matches what is set in the Line Frequency Reference (0x0094) register. See **Section 8.0, MCP39F521 Calibration** for more information on device calibration.

4.8 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F521:

TABLE 4-12: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
u64	Unsigned, 64-bit register
u32	Unsigned, 32-bit register
s32	Signed, 32-bit register
u16	Unsigned, 16-bit register
s16	Signed, 16-bit register
b32	32-bit register containing discrete Boolean bit settings

5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F521 uses a coherent sampling algorithm to phase lock the sampling rate to the line frequency with an integer number of samples per line cycle, and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the output power quantities.

5.2 Accumulation Interval Parameter

The accumulation interval is defined as an 2^N number of line cycles, where N is the value in the Accumulation Interval Parameter register.

5.3 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F521 is shown in Figure 5-1. All conditions set in this diagram effect all of the output registers (RMS current, RMS voltage, active power, reactive power, apparent power, etc.). The gain of the PGA, the Shutdown and Reset status of the 24-bit ADCs are all controlled through the System Configuration register (Register 6-2).

For DC applications, offset can be removed by using the DC Offset Current register. To compensate for any external phase error between the current and voltage channels, the Phase Compensation register can be used.

See **Section 8.0, MCP39F521 Calibration** for more information on device calibration.

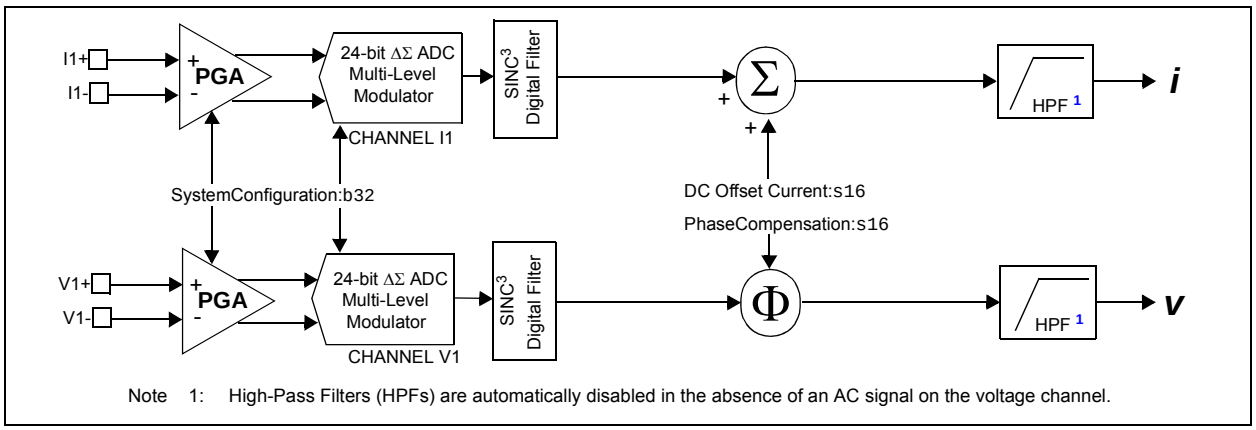


FIGURE 5-1: *Channel I1 and V1 Signal Flow.*

5.4 RMS Current and RMS Voltage

The MCP39F521 device provides true RMS measurements. The MCP39F521 device has two simultaneous sampling 24-bit A/D converters for the current and voltage measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (v_n)^2}{2^N}}$$

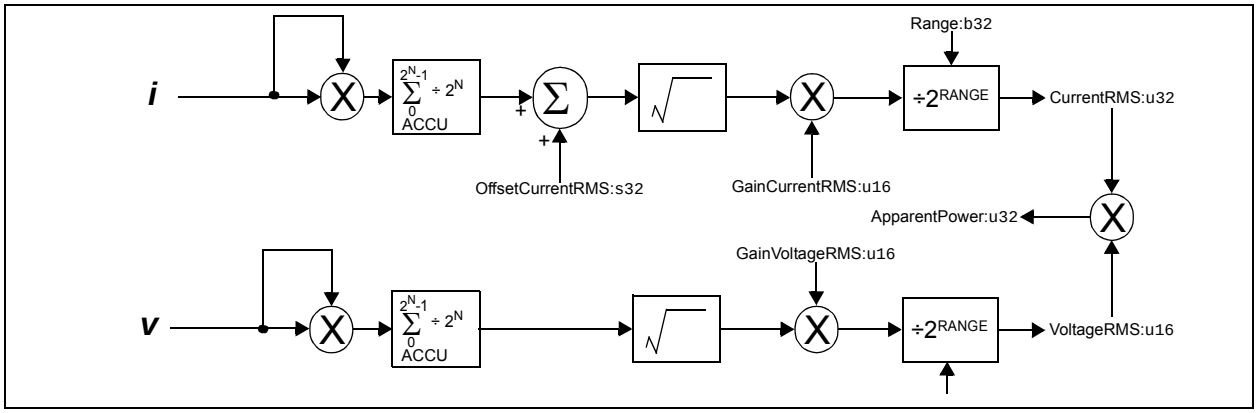


FIGURE 5-2: *RMS Current and Voltage Calculation Signal Flow.*

5.5 Power and Energy

The MCP39F521 offers signed power numbers for active and reactive power, import and export registers for active energy, and four-quadrant reactive power measurement. For this device, import power or energy is considered positive (power or energy being consumed by the load), and export power or energy is considered negative (power or energy being delivered by the load). The following figure represents the measurements obtained by the MCP39F521.

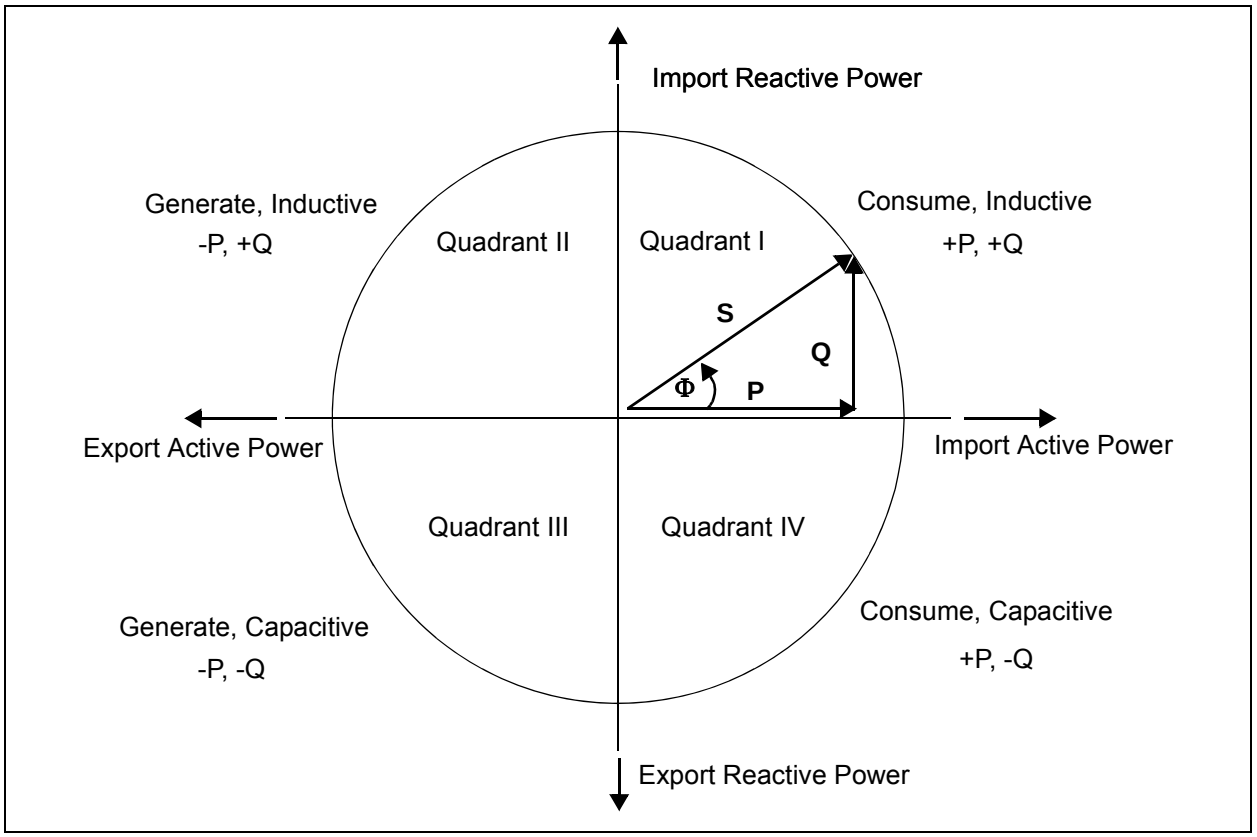


FIGURE 5-3: *The Power Circle and Triangle (S = Apparent, P = Active, Q = Reactive).*

5.6 Energy Accumulation

Energy accumulation for all four energy registers (import/export, active/reactive) occurs at the end of each computation cycle, if the energy accumulation has been turned on. See **Section 6.3, System Status Register** on the Energy Control register. A no-load threshold test is done to make sure the measured energy is not below the no-load threshold; if it is above the no-load threshold, the accumulation occurs with a default energy resolution of 1mWh for all of the energy registers.

5.6.1 NO-LOAD THRESHOLD

The no-load threshold is set by modifying the value in the No-Load Threshold register. The unit for this register is power with a default resolution of 0.01W. The default value is 100 or 1.00W. Any power that is below 1W will not be accumulated into any of the energy registers.

5.7 Apparent Power (S)

This 32-bit register is the output register for the final apparent power indication. It is the product of RMS current and RMS voltage as shown in Equation 5-2.

EQUATION 5-2: APPARENT POWER (S)

$$S = I_{RMS} \times V_{RMS}$$

For scaling of the apparent power indication, the calculation engine uses the register Apparent Power Divisor. This is described in the following register operations, per Equation 5-3.

EQUATION 5-3: APPARENT POWER (S)

$$S = \frac{CurrentRMS \times VoltageRMS}{10^{ApparentPowerDivisor}}$$

5.8 Active Power (P)

The MCP39F521 has two simultaneous sampling A/D converters. For the active power calculation, the instantaneous current and instantaneous voltages are multiplied together to create instantaneous power. This instantaneous power is then converted to active power by averaging or calculating the DC component.

Equation 5-4 controls the number of samples used in this accumulation prior to updating the Active Power output register.

Please note that although this register is unsigned, the direction of the active power (import or export) can be determined by the Active Power Sign bit (SIGN_PA) located in the System Status register (Register 6-1).

EQUATION 5-4: ACTIVE POWER

$$P = \frac{1}{2^N} \sum_{k=0}^{k=2^N-1} V_k \times I_k$$

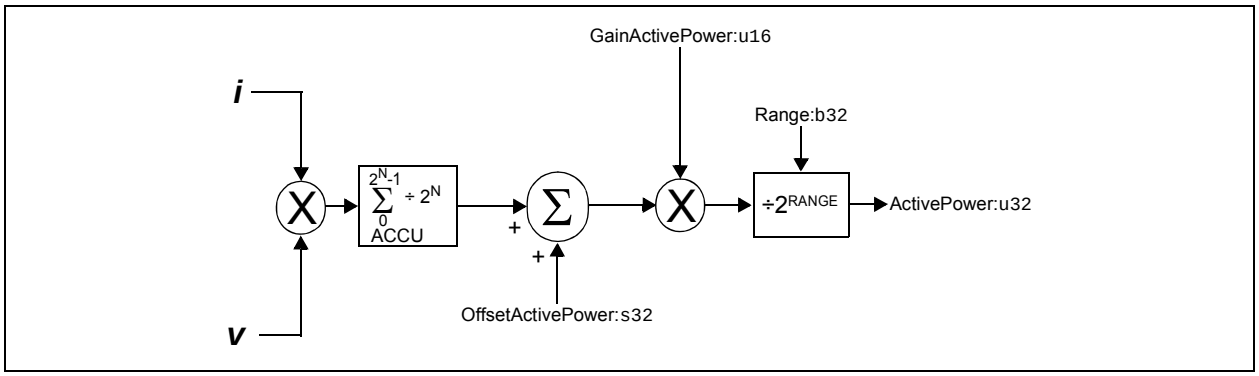


FIGURE 5-4: *Active Power Calculation Signal Flow.*

5.9 Power Factor (PF)

Power factor is calculated by the ratio of P to S or active power divided by apparent power.

EQUATION 5-5: POWER FACTOR

$$PF = \frac{P}{S}$$

The Power Factor Reading is stored in a signed 16-bit register (Power Factor). This register is a signed, two's complement register with the MSB representing the polarity of the power factor. Positive means inductive load, negative means capacitive load. Each LSB is then equivalent to a weight of 2^{-15}. A maximum register value of 0x7FFF corresponds to a power factor of 1. The minimum register value of 0x8000 corresponds to a power factor of -1.

5.10 Reactive Power (Q)

In the MCP39F521, Reactive Power is calculated using a 90 degree phase shift in the voltage channel. The same accumulation principles apply as with active power where ACCU acts as an accumulator. Any light load or residual power can be removed by using the Offset Reactive Power register. Gain is corrected by the Gain Reactive Power register. The final output is an unsigned 32-bit value located in the Reactive Power register.

Please note that although this register is unsigned, the direction of the power can be determined by the Reactive Power Sign bit (SIGN_PR) in the System Status register (Register 6-1).

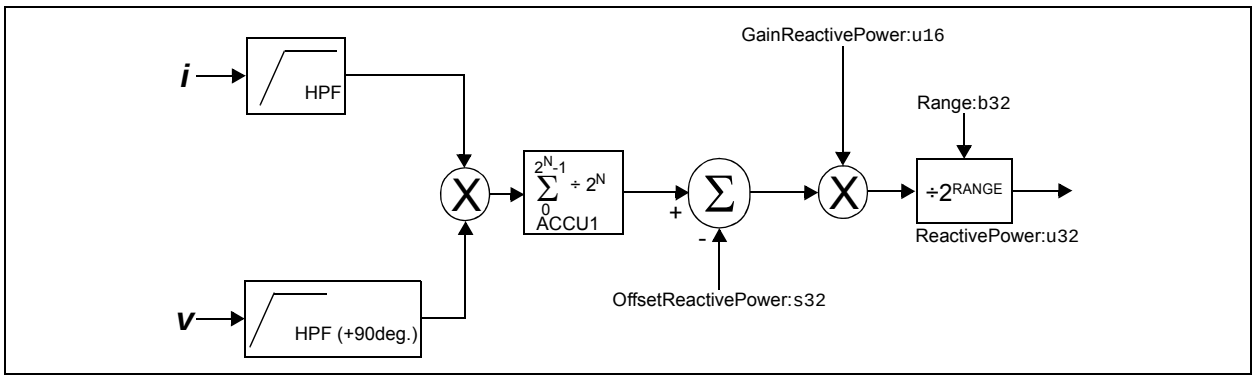


FIGURE 5-5: *Reactive Power Calculation Signal Flow.*

5.11 10-Bit Analog Input

The least 10 significant bits of the 16-bit Analog Input register contain the output of the 10-bit ADC. The conversion rate of the analog input occurs once every computation cycle.

The Thermistor Voltage can be used for temperature compensation of the calculation engine. See **Section 8.7, Temperature Compensation** for more information.

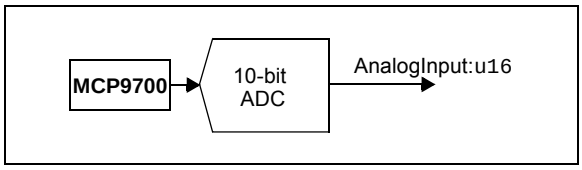


FIGURE 5-6: *Using an Analog Out-Temperature Sensor for Automatic Temperature Compensation.*

5.12 Minimum and Maximum Recordings

The MCP39F521 has the ability to record minimum and maximum outputs and keep them in a total of four registers (two minimum and two maximum) based on the value of address pointers located in the four registers listed below.

A minimum and maximum test is done after each calculation interval. If the current measurement value of the value directed to by the pointer is smaller or larger than the value in the Minimum or Maximum register, the record is updated appropriately.

The registers are listed as follows:

- MinMaxPointer1 → MinimumRecord1, MaximumRecord1
- MinMaxPointer2 → MinimumRecord2, MaximumRecord2

Only the output quantity register addresses can be tracked by the Min/Max pointers. Output quantity registers are defined as those from Voltage RMS to Apparent Power (addresses 0x0006 to 0x001A). All other addresses will be ignored by the calculation engine.

Please note that the 64-bit energy registers can not be tracked through the Minimum and Maximum recording registers.

5.13 Zero Crossing Detection (ZCD)

The Zero Crossing Detection block generates a logic pulse output on the ZCD pin that is coherent with the zero crossing of the input AC signal present on voltage input pins (V1+, V1-). The ZCD pin can be enabled and disabled by the corresponding bit (ZCD_OUTPUT_DIS) in the System Configuration register (Register 6-2). When enabled, this produces a square wave with a frequency that is twice that of the AC signal present on the voltage input. Figure 5-7 represents the signal on the ZCD pin superimposed with the AC signal present on the voltage input in this mode.

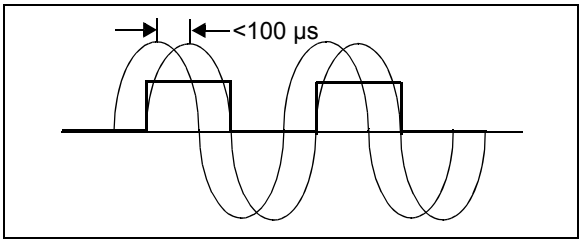


FIGURE 5-7: *Zero Crossing Detection Operation (Noninverted, Non-Pulsed).*

A second mode is available that produces a 100 µs pulse (ZCD_PULS) at each zero crossing, shown in Figure 5-8.

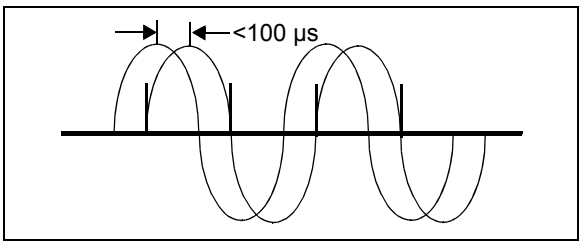


FIGURE 5-8: *Zero Crossing Detection Operation (Noninverted, Pulsed).*

Switching modes is done by setting the corresponding bit in the System Configuration register (Register 6-2). In addition, either the toggling of this pin, or the pulse, can be inverted. The ZCD Inversion bit (ZCD_INV) is also in the System Configuration register (Register 6-2).

There are two bits in the System Configuration register that can be used to modify the zero crossing. The zero crossing output can be inverted by setting the Inversion bit, or the zero crossing can be a 100 µs pulse at each zero crossing, by setting the Pulse Bit.

Note that a low-pass filter is included in the signal path that allows the zero crossing detection circuit to filter out the fundamental frequency. An internal compensation circuit is then used to gain back the phase delay introduced by the low-pass filter resulting in a latency of less than 100 µs.

6.0 REGISTER DESCRIPTIONS

6.1 Complete Register Map

The following table describes the registers for the MCP39F521 device.

TABLE 6-1: MCP39F521 REGISTER MAP

Address	Register Name	Section Number	Read/ Write	Data Type	Description
Output Registers					
0x0000	Instruction Pointer	6.2	R	u16	Address pointer for read or write commands
0x0002	System Status	6.3	R	b16	System Status Register
0x0004	System Version	6.4	R	u16	System version date code information for MCP39F521, set at Microchip factory; format YMDD
0x0006	Voltage RMS	5.4	R	u16	RMS Voltage output
0x0008	Line Frequency	8.6	R	u16	Line Frequency output
0x000A	Analog Input Voltage	5.11	R	u16	Output of the 10-bit SAR ADC
0x000C	Power Factor	5.9	R	s16	Power Factor output
0x000E	Current RMS	5.4	R	u32	RMS Current output
0x0012	Active Power (Note 1)	5.8	R	u32	Active Power output
0x0016	Reactive Power (Note 1)	5.10	R	u32	Reactive Power output
0x001A	Apparent Power	5.7	R	u32	Apparent Power output
0x001E	Import Active Energy Counter	5.6	R	u64	Accumulator for Active Energy, Import
0x0026	Export Active Energy Counter	5.6	R	u64	Accumulator for Active Energy, Export
0x002E	Import Reactive Energy Counter	5.6	R	u64	Accumulator for Reactive Energy, Import
0x0036	Export Reactive Energy Counter	5.6	R	u64	Accumulator for Reactive Energy, Export
0x003E	Minimum Record 1	5.12	R	u32	Minimum Value of the Output Quantity Address in Min/Max Pointer 1 Register
0x0042	Minimum Record 2	5.12	R	u32	Minimum Value of the Output Quantity Address in Min/Max Pointer 2 Register
0x0046	Reserved	—	R	u32	Reserved
0x004A	Reserved	—	R	u32	Reserved
0x004E	Maximum Record 1	5.12	R	u32	Maximum Value of the Output Quantity Address in Min/Max Pointer 1 Register
0x0052	Maximum Record 2	5.12	R	u32	Maximum Value of the Output Quantity Address in Min/Max Pointer 2 Register
0x0056	Reserved	—	R	u32	Reserved
0x005A	Reserved	—	R	u32	Reserved

Note 1: The registers are unsigned, however their sign is kept as a separate bit in the System Status Register (Register 6-1).

2: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters; please contact the local Microchip office for further support.

TABLE 6-1: MCP39F521 REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data Type	Description
Calibration Registers					
0x005E	Calibration Register Delimiter	8.8	R/W	u16	May be used to initiate loading of the default calibration coefficients at start-up
0x0060	Gain Current RMS	8.3	R/W	u16	Gain Calibration Factor for RMS Current
0x0062	Gain Voltage RMS	8.3	R/W	u16	Gain Calibration Factor for RMS Voltage
0x0064	Gain Active Power	8.3	R/W	u16	Gain Calibration Factor for Active Power
0x0066	Gain Reactive Power	8.3	R/W	u16	Gain Calibration Factor for Reactive Power
0x0068	Offset Current RMS	8.5.1	R/W	s32	Offset Calibration Factor for RMS Current
0x006C	Offset Active Power	8.5.1	R/W	s32	Offset Calibration Factor for Active Power
0x0070	Offset Reactive Power	8.5.1	R/W	s32	Offset Calibration Factor for Reactive Power
0x0074	DC Offset Current	8.5.2	R/W	s16	Offset Calibration Factor for DC Current
0x0076	Phase Compensation	8.5	R/W	s16	Phase Compensation
0x0078	Apparent Power Divisor	5.7	R/W	u16	Number of Digits for apparent power divisor to match I_{RMS} and V_{RMS} resolution
Design Configuration Registers					
0x007A	System Configuration	6.5	R/W	b32	Control for device configuration, including ADC configuration
0x007E	Event Configuration	7.0	R/W	b16	Settings for the Event pin
0x0082	Range	6.6	R/W	b32	Scaling factor for Outputs
0x0086	Calibration Current	8.3.1	R/W	u32	Target Current to be used during single-point calibration
0x008A	Calibration Voltage	8.3.1	R/W	u16	Target Voltage to be used during single-point calibration
0x008C	Calibration Power Active	8.3.1	R/W	u32	Target Active Power to be used during single-point calibration
0x0090	Calibration Power Reactive	8.3.1	R/W	u32	Target Reactive Power to be used during single-point calibration
0x0094	Line Frequency Reference	8.6.1	R/W	u16	Reference Value for the nominal line frequency
0x0096	Reserved	—	R/W	u32	Reserved
0x009A	Reserved	—	R/W	u32	Reserved
0x009E	Accumulation Interval Parameter	5.2	R/W	u16	N for 2^N number of line cycles to be used during a single computation cycle
0x00A0	Voltage Sag Limit	7.2	R/W	u16	RMS Voltage threshold at which an event flag is recorded
0x00A2	Voltage Surge Limit	7.2	R/W	u16	RMS Voltage threshold at which an event flag is recorded
0x00A4	Over Current Limit	7.2	R/W	u32	RMS Current threshold at which an event flag is recorded
0x00A8	Over Power Limit	7.2	R/W	u32	Active Power Limit at which an event flag is recorded

Note 1: The registers are unsigned, however their sign is kept as a separate bit in the System Status Register (Register 6-1).

2: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters; please contact the local Microchip office for further support.

TABLE 6-1: MCP39F521 REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data Type	Description
EMI Filter Compensation Registers (Note 2)					
0x00AC	Reserved	—	R	u16	Reserved
0x00AE	Reserved	—	R	u16	Reserved
0x00B0	Reserved	—	R	u16	Reserved
0x00B2	Reserved	—	R	u16	Reserved
0x00B4	Reserved	—	R	u16	Reserved
0x00B6	Reserved	—	R	u16	Reserved
0x00B8	Reserved	—	R	u16	Reserved
0x00BA	Reserved	—	R	u16	Reserved
0x00BC	Reserved	—	R	u16	Reserved
0x00BE	Reserved	—	R	u16	Reserved
0x00C0	Reserved	—	R	u16	Reserved
0x00C2	Reserved	—	R	u16	Reserved
0x00C4	Reserved	—	R	u16	Reserved
Temperature Compensation Registers					
0x00C6	Temperature Compensation for Frequency	8.7	R/W	u16	Correction factor for compensating the line frequency indication over temperature
0x00C8	Temperature Compensation for Current	8.7	R/W	u16	Correction factor for compensating the Current RMS indication over temperature
0x00CA	Temperature Compensation for Power	8.7	R/W	u16	Correction factor for compensating the active power indication over temperature
0x00CC	Ambient Temperature Reference Voltage	8.7	R/W	u16	Register for storing the reference temperature during calibration
Control Registers for Peripherals					
0x00CE	Reserved	—	R/W	u16	Reserved
0x00D0	Reserved	—	R/W	u16	Reserved
0x00D2	Reserved	—	R/W	u16	Reserved
0x00D4	MinMaxPointer1	5.12	R/W	u16	Address Pointer for Min/Max 1 Outputs
0x00D6	MinMaxPointer2	5.12	R/W	u16	Address Pointer for Min/Max 2 Outputs
0x00D8	Reserved	—	R/W	u16	Reserved
0x00DA	Reserved	—	R/W	u16	Reserved
0x00DC	Energy Control	5.6	R/W	u16	Input register for reset/start of Energy Accumulation
0x00DE	Reserved	—	R/W	u16	Reserved
0x00E0	No-Load Threshold	5.6.1	R/W	u16	No-Load Threshold for Energy Counting

Note 1: The registers are unsigned, however their sign is kept as a separate bit in the System Status Register (Register 6-1).

2: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters; please contact the local Microchip office for further support.

6.2 Address Pointer Register

This unsigned 16-bit register contains the address to which all read and write instructions occur. This register is only written through the `Set Address Pointer` command and is otherwise outside the writable range of register addresses.

6.3 System Status Register

The System Status register is a read-only register and can be used to detect the various states of pin levels as defined below.

REGISTER 6-1: SYSTEM STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-x	U-0	U-0
—	—	—	—	—	EVENT	—	—
bit 15							bit 8

U-0	U-0	R-x	R-x	R-x	R-x	R-x	R-x
—	—	SIGN_PR	SIGN_PA	OVERPOW	OVERCUR	VSURGE	VSAG
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented**: Read as ‘0’

bit 11 **Unimplemented**: Read as ‘0’

bit 10 **EVENT:** State of Event Detection algorithm. This bit is latched and must be cleared.
1 = Event has occurred
0 = Event has not occurred

bit 9-8 **Unimplemented**: Read as ‘0’

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5 **SIGN_PR:** Sign of Reactive Power
1 = Reactive Power is positive, inductive and is in quadrants 1,2
0 = Reactive Power is negative, is capacitive and is in quadrants 3,4

bit 4 **SIGN_PA:** Sign of Active Power (import/export sign of active power)
1 = Active Power is positive (import) and is in quadrants 1,4
0 = Active Power is negative (export) and is in quadrants 2,3

bit 3 **OVERPOW:** State of Over Power detection algorithm
1 = Over Power threshold has been broken
0 = Over Power threshold has not been broken

bit 2 **OVERCUR:** State of the Over Current detection algorithm
1 = Over Current threshold has been broken
0 = Over Current threshold has not been broken

bit 1 **VSURGE:** State of Voltage Surge Detection algorithm. This bit is latched and must be cleared.
1 = Surge threshold has been broken
0 = Surge threshold has not been broken

bit 0 **VSAG:** State of Voltage Sag Detection algorithm. This bit is latched and must be cleared.
1 = Sag threshold has been broken
0 = Sag threshold has not been broken

6.4 System Version Register

The System Version register is hard-coded by Microchip Technology Inc. and contains calculation engine date code information. The System Version register is a date code in the YMDD format, with year and month in hex, day in decimal (e.g. 0xF316 = 2015, Feb. 16th).

6.5 System Configuration

The System Configuration register (Register 6-2) contains bits for controlling the following:

- PGA setting
- ADC Reset State
- ADC Shutdown State
- Voltage Reference Trim
- Single Wire Auto-Transmission

These options are described in the following sections.

6.5.1 PROGRAMMABLE GAIN AMPLIFIERS (PGA)

The two Programmable Gain Amplifiers (PGAs) reside at the front-end of each 24-bit Delta-Sigma ADC. They have two functions:

- Translate the Common mode of the input from A_{GND} to an internal level between A_{GND} and A_{VDD}
- Amplify the input differential signal

The translation of the Common mode does not change the differential signal but enters the Common mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the delta-sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn<2:0> bits in Register 6-2 the System Configuration register. Table 6-2 represents the gain settings for the PGAs.

TABLE 6-2: PGA CONFIGURATION SETTING (Note 1)

Gain PGA_CHn<2:0>			Gain (V/V)	Gain (dB)	V_{IN} Range (V)
0	0	0	1	0	±0.5
0	0	1	2	6	±0.25
0	1	0	4	12	±0.125
0	1	1	8	18	±0.0625
1	0	0	16	24	±0.03125
1	0	1	32	30	±0.015625

Note 1: The two undefined settings (110, 111) are G = 1.

6.5.2 24-BIT ADC RESET MODE (SOFT RESET MODE)

24-bit ADC Reset mode (also called Soft Reset) can only be entered through setting high the RESET<1:0> bits in the System Configuration register (Register 6-2). This mode is defined as the condition where the converters are active but their output is forced to '0'.

6.5.3 ADC SHUTDOWN MODE

ADC Shutdown mode is defined as a state where the converters and their biases are OFF, consuming only leakage current. When the Shutdown bit (SHUTDOWN <1:0>) is reset to '0', the analog biases will be enabled, as well as the clock and the digital circuitry.

Each converter can be placed in Shutdown mode independently. This mode is only available through programming of the SHUTDOWN<1:0> bits in the System Configuration register (Register 6-2).

6.5.4 V_{REF} TEMPERATURE COMPENSATION

If desired, the user can calibrate out the temperature drift for ultra-low V_{REF} drift.

The internal voltage reference comprises a proprietary circuit and algorithm to compensate first-order and second-order temperature coefficients. The compensation allows very low temperature coefficients (typically 10 ppm/°C) on the entire range of temperatures from -40°C to +125°C. This temperature coefficient varies from part to part.

The temperature coefficient can be adjusted on each part through the System Configuration register (0x0042) (Register 6-2). The default value of this register is set to 0x42. The typical variation of the temperature coefficient of the internal voltage reference, with respect to VREFCAL register code, is shown in Figure 6-1.

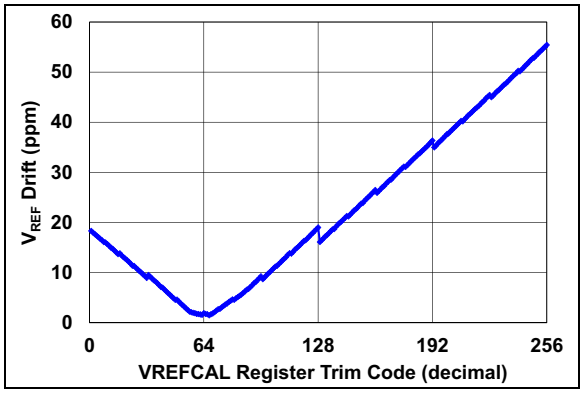


FIGURE 6-1: *V_{REF} Tempco vs. VREFCAL Trimcode Chart.*

REGISTER 6-2: SYSTEM CONFIGURATION REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	PGA_CH1<2:0>			PGA_CH0<2:0>		
bit 31							bit 24

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
VREFCAL<7:0>							
bit 23							bit 16

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0
TIMEOUT_DIS	—	—	ZCD_INV	ZCD_PULS	ZCD_OUTPUT_ DIS	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
TEMPCOMP	RESET<1:0>		SHUTDOWN<1:0>		VREFEXT	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented**: Read as '0'

bit 29-27 **PGA_CH1 <2:0>:** PGA Setting for Channel 1
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1 **(DEFAULT)**

bit 26-24 **PGA_CH0 <2:0>:** PGA Setting for Channel 0
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8 **(Default)**
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1

bit 23-16 **VREFCAL<n>:** Internal voltage reference temperature coefficient register value (See **Section 6.5.4, V_{REF} Temperature Compensation** for complete description)

bit 15 **TIMEOUT_DIS:** Time Out Disable
1 = I^2C Time Out is Disabled
0 = I^2C Time Out is Enabled **(DEFAULT)**

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **ZCD_INV:** Zero Crossing Detection Output Inverse
1 = ZCD is inverted
0 = ZCD is not inverted **(DEFAULT)**

REGISTER 6-2: SYSTEM CONFIGURATION REGISTER (CONTINUED)

bit 11 **ZCD_PULS:** Zero Crossing Detection Pulse mode
1 = ZCD output is 100 µs pulses on zero crossings
0 = ZCD Output changes logic state on zero crossings **(DEFAULT)**

bit 10 **ZCD_OUTPUT_DIS:** Disable the Zero Crossing output pin
1 = ZCD output is disabled
0 = ZCD output is enabled (Default)

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **TEMPCOMP:** temperaure compensation enable bit
1 = Temperature compensation is enabled
0 = Temperature compensation is disabled **(DEFAULT)**

bit 6-5 **RESET <1:0>:** Reset mode setting for ADCs
11 = Both I1 and V1 are in Reset mode
10 = V1 ADC is in Reset mode
01 = I1 ADC is in Reset mode
00 = Neither ADC is in Reset mode **(DEFAULT)**

bit 4-3 **SHUTDOWN <1:0>:** Shutdown mode setting for ADCs
11 = Both I1 and V1 are in Shutdown
10 = V1 ADC is in Shutdown
01 = I1 ADC is in Shutdown
00 = Neither ADC is in Shutdown **(DEFAULT)**

bit 2 **VREFEXT:** Internal Voltage Reference Shutdown Control
1 = Internal Voltage Reference Disabled
0 = Internal Voltage Reference Enabled **(DEFAULT)**

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 6-3: ENERGY ACCUMULATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ENRG_CNTRL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bits 15-1 **Unimplemented:** Read as '0'

bit 0 **ENRG_CNTRL:** Energy Accumulation Control bit
1 = Energy Accumulation is tuned on and all registers are accumulating
0 = Energy Accumulation is turned off and all energy accumulation registers are reset to 0 **(DEFAULT)**

6.6 Range Register

The Range register (Register 6-4) is a 32-bit register that contains the number of right-bit shifts for the following outputs, divided into separate bytes as defined below:

- RMS Current
- RMS Voltage
- Power (Active, Reactive, Apparent)

Note that the power range byte operates across both the active and reactive output registers and sets the same scale.

The purpose of this register is two-fold: the number of right-bit shifting (division by 2^{RANGE}) must be high enough to prevent overflow in the output register, and low enough to allow for the desired output resolution. It is the user's responsibility to set this register correctly to ensure proper output operation for a given meter design.

For further information and example usage, see **Section 8.3, Single-Point Gain Calibrations at Unity Power Factor**.

REGISTER 6-4: RANGE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
POWER<7:0>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
CURRENT<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
VOLTAGE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24	**Unimplemented:** Read as '0'
bit 23-16	**POWER<7:0>:** Sets the number of right-bit shifts for the Active and Reactive Power output registers
bit 15-8	**CURRENT<7:0>:** Sets the number of right-bit shifts for the Current RMS output register
bit 7-0	**VOLTAGE<7:0>:** Sets the number of right-bit shifts for the Voltage RMS output register

7.0 EVENT OUTPUT PIN/EVENT CONFIGURATION REGISTER

7.1 Event Pin

The MCP39F521 device has one Event pin that can be configured in three possible configurations. These configurations are:

1. No event is mapped to the pin
2. Voltage Surge, Voltage Sag, Over Current, or Over Power event is mapped to the pin. More than one event can be mapped to the Event pin.
3. Manual control of the Event pin.

These three configurations allow for the control of external interrupts or hardware that is dependent on the measured power, current or voltage. The Event configuration register (Register 7-1) below describes how these events and pins can be configured.

7.2 Voltage Sag and Voltage Surge Detection

The event alarms for Voltage Sag and Voltage Surge work differently compared to the Over Current and Over Power events, which are tested against every computation cycle. These two event alarms are designed to provide a much faster interrupt if the condition occurs. Note that neither of these two events have a respective Hold register associated with them, since the detection time is less than one line cycle.

The calculation engine keeps track of a trailing mean square of the input voltage, as defined by the following equation:

EQUATION 7-1:

$$V_{SA} = \frac{2 \times f_{LINE}}{f_{SAMPLE}} \times \left[\sum_{n = -\frac{f_{SAMPLE}}{2 \times f_{LINE}} - 1}^{0} V_n \right]^2$$

Therefore, at each data-ready occurrence, the value of V_{SA} is compared to the programmable threshold set in the Voltage Sag Limit register and Voltage Surge Limit register to determine if a flag should be set. If either of these events are masked to either the Event pin, a logic-high interrupt will be given on these pins.

The Sag or Surge events can be used to quickly determine if a power failure has occurred in the system.

REGISTER 7-1: EVENT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	OVERPOW_PIN	OVERCUR_PIN	VSURGE_PIN	VSAG_PIN
bit 23							bit 16
U-0	R/W-0	U-0	U-0	R/W	R/W	R/W-0	R/W-0
—	EVENT_MANU	—	—	OVERCUR_CL	OVERPOW_CL	VSUR_CL	VSAG_CL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VSUR_LA	VSAG_LA	OVERPOW_LA	OVERCUR_LA	VSUR_TST	VSAG_TST	OVERPOW_TST	OVERCUR_TST
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23 **Unimplemented:** Read as ‘0’

bit 22 **Unimplemented:** Read as ‘0’

bit 21 **Unimplemented:** Read as ‘0’

bit 20 **Unimplemented:** Read as ‘0’

bit 19 **OVERPOW_PIN:** Pin Operation for the Over Power event
1 = Event mapped to Event pin only
0 = Event not mapped to a pin **(Default)**

bit 18 **OVERCUR_PIN:** Pin Operation for the Over Current event
1 = Event mapped to Event pin only
0 = Event not mapped to a pin **(Default)**

bit 17 **VSURGE_PIN:** Pin Operation for the Voltage Surge event
1 = Event mapped to Event pin only
0 = Event not mapped to a pin **(Default)**

bit 16 **VSAG_PIN:** Pin Operation for the Voltage Sag event
1 = Event mapped to Event pin only
0 = Event not mapped to a pin **(Default)**

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **EVENT_MANU:** Manual Control of the Event pin
1 = Pin is logic high
0 = Pin is logic low **(Default)**

bit 13-12 **Unimplemented:** Read as ‘0’

bit 11 **OVERCUR_CL:** Reset or clear bit for the Over Current event
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 10 **OVERPOW_CL:** Reset or clear bit for the Over Power event
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 9 **VSUR_CL:** Reset or clear bit for the Voltage Surge event
1 = Event is cleared
0 = Event is not cleared **(Default)**

REGISTER 7-1: EVENT CONFIGURATION REGISTER (CONTINUED)

bit 8 **VSAG_CL:** Reset or clear bit for the Voltage Sag event
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 7 **VSUR_LA:** Latching control of the Voltage Surge event
1 = Event is latched and needs to be cleared
0 = Event does not latch

bit 6 **VSAG_LA:** Latching control of the Voltage Sag event
1 = Event is latched and needs to be cleared
0 = Event does not latch

bit 5 **OVERPOW_LA:** Latching control of the Over Power event
1 = Event is latched and needs to be cleared
0 = Event does not latch

bit 4 **OVERCUR_LA:** Latching control of the Over Current event
1 = Event is latched and needs to be cleared
0 = Event does not latch

bit 3 **VSUR_TST:** Test control of the Voltage Surge event
1 = Simulated event is turned on
0 = Simulated Event is turned off

bit 2 **VSAG_TST:** Test control of the Voltage Sag event
1 = Simulated event is turned on
0 = Simulated Event is turned off

bit 1 **OVERPOW_TST:** Test control of the Over Power event
1 = Simulated Event is turned on
0 = Simulated Event is turned off

bit 0 **OVERCUR_TST:** Test control of the Over Current event
1 = Simulated Event is turned on
0 = Simulated Event is turned off

Note: Writing a 1 to the Clear bit, clears the event, either real or simulated through test bits, and then returns to a state of 0.

8.0 MCP39F521 CALIBRATION

8.1 Overview

Calibration compensates for ADC gain error, component tolerances and overall noise in the system. The device provides an on-chip calibration algorithm that allows simple system calibration to be performed quickly. The excellent analog performance of the A/D converters on the MCP39F521 allows for a single point calibration and a single calibration command to achieve accurate measurements.

Calibration can be done by either using the predefined auto-calibration commands, or by writing directly to the calibration registers. If additional calibration points are required (AC offset, Phase Compensation, DC offset), the corresponding calibration registers are available to the user and will be described separately in this section.

8.2 Calibration Order

The proper steps for calibration need to be observed.

If the device has an external temperature sensor attached, temperature calibration should be done first by reading the value from the Thermistor Voltage register and copying the value by writing to the Ambient Temperature Reference Voltage register.

If the device runs on the internal oscillator, the line frequency must be calibrated next using the `Auto-Calibration Frequency` command.

The single-point gain calibration at unity power factor should be performed next.

If non-unity displacement power factor measurements are a concern, then the next step should be phase calibration, followed by reactive power gain calibration.

To summarize the order of calibration:

1. Temperature Calibration (optional)
2. Line Frequency Calibration (optional)
3. Gain Calibration at PF = 1
4. Phase Calibration at PF ≠ 1 (optional)
5. Reactive Gain Calibration at PF ≠ 1(optional)

8.3 Single-Point Gain Calibrations at Unity Power Factor

When using the device in AC mode with the high-pass filters turned on, most offset errors are removed and only a single-point gain calibration is required.

Setting the gain registers to properly produce the desired outputs can be done manually by writing to the appropriate register. The alternative method is to use the auto-calibration commands described in this section.

8.3.1 USING THE AUTO-CALIBRATION GAIN COMMAND

By applying stable reference voltages and currents that are equivalent to the values that reside in the target Calibration Current, Calibration Voltage and Calibration Active Power registers, the `Auto-Calibration Gain` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following registers are set when the `Auto-Calibration Gain` command is issued:

- Gain Current RMS
- Gain Voltage RMS
- Gain Active Power

When this command is issued, the MCP39F521 attempts to match the expected values to the measured values for all three output quantities by changing the gain register based on the following formula:

EQUATION 8-1:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured}$$

The same formula applies for voltage RMS, current RMS and active power. Since the gain registers for all three quantities are 16-bit numbers, the ratio of the expected value to the measured value (which can be modified by changing the Range register) and the previous gain must be such that the equation yields a valid number. Here the limits are set to be from 25,000 to 65,535. A new gain within this range for all three limits will return an ACK for a successful calibration, otherwise the command returns a NAK for a failed calibration attempt.

It is the user's responsibility to ensure that the proper range settings, PGA settings and hardware design settings are correct to allow for successful calibration using this command.

8.3.2 EXAMPLE OF RANGE SELECTION FOR VALID CALIBRATION

In this example, the user applies a calibration current of 1A to an uncalibrated system. The indicated value in the Current RMS register is 2300 with the system's specific shunt value, PGA gain, etc. The user expects to see a value of 1000 in the Current RMS register when 1A current is applied, meaning 1.000A with 1 mA resolution. Other given values are:

- The existing value for Gain Current RMS is 33480
- The existing value for Range is 12

By using Equation 8-2, the calculation for $Gain_{NEW}$ yields:

EQUATION 8-2:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{2300} = 14556$$

$$14556 < 25,000$$

When using the `Auto-Calibration Gain` command, the result would be a failed calibration or a NAK returned form the MCP39F521, because the resulting $Gain_{NEW}$ is less than 25,000.

The solution is to use the Range register to bring the measured value closer to the expected value, such that a new gain value can be calculated within the limits specified above.

The Range register specifies the number of right-bit shifts (equivalent to divisions by 2) after the multiplication with the Gain Current RMS register. Refer to **Section 5.0, Calculation Engine (CE) Description** for information on the Range register.

Incrementing the Range register by 1 unit, an additional right-bit shift or ÷2 is included in the calculation. Increasing the current range from 12 to 13 yields the new measured Current RMS register value of 2300/2 = 1150. The expected (1000) and measured (1150) are much closer now, so the expected new gain should be within the limits:

EQUATION 8-3:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{1150} = 29113$$

$$25,000 < 29113 < 65535$$

The resulting new gain is within the limits and the device successfully calibrates Current RMS and returns an ACK.

It can be observed that the range can be set to 14 and the resulting new gain will still be within limits ($Gain_{NEW}$ = 58226). However, since this gain value is close to the limit of the 16-bit Gain register, variations from system to system (component tolerances, etc.) might create a scenario where the calibration is not successful on some units and there would be a yield issue. The best approach is to choose a range value that places the new gain in the middle of the bounds of the gain registers described above.

In a second example, when applying 1A, the user expects an output of 1.0000A with 0.1 mA resolution. The example is starting with the same initial values:

EQUATION 8-4:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{10000}{2300} = 145565$$

$$145565 > 65535$$

The $Gain_{NEW}$ is much larger than the 16-bit limit of 65535, so fewer right-bit shifts must be introduced to get the measured value closer to the expected value. The user needs to compute the number of bit shifts that will give a value lower than 65535. To estimate this number:

EQUATION 8-5:

$$\frac{145565}{65535} = 2.2$$

2.2 rounds to the closest integer value of 2. The range value changes to 12 – 2 = 10; there are 2 less right-bit shifts.

The new measured value will be 2300 x 2^2 = 9200.

EQUATION 8-6:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{10000}{9200} = 36391$$

$$25,000 < 36391 < 65535$$

The resulting new gain is within the limits and the device successfully calibrates Current RMS and returns an ACK.

8.4 Calibrating the Phase Compensation Register

Phase compensation is provided to adjust for any phase delay between the current and voltage path. This procedure requires sinusoidal current and voltage waveforms, with a significant phase shift between them, and significant amplitudes. The recommended displacement power factor for calibration is 0.5. The procedure for calculating the phase compensation register is as follows:

1. Determine what the difference is between the angle corresponding to the measured power factor (PF_{MEAS}) and the angle corresponding to the expected power factor (PF_{EXP}), in degrees.

EQUATION 8-7:

$$PF_{MEAS} = \frac{Value\ in\ PowerFactor\ Register}{32768}$$

$$ANGLE_{MEAS}(^\circ) = acos(PF_{MEAS}) \times \frac{180}{\Pi}$$

$$ANGLE_{EXP}(^\circ) = acos(PF_{EXP}) \times \frac{180}{\Pi}$$

2. Convert this from degrees to the resolution provided in Equation 8-8:

EQUATION 8-8:

$$\Phi = (ANGLE_{MEAS} - ANGLE_{EXP}) \times 40$$

3. Combine this additional phase compensation to whatever value is currently in the phase compensation, and update the register. Equation 8-9 should be computed in terms of an 8-bit two's complement signed value. The 8-bit result is placed in the least significant byte of the 16-bit Phase Compensation register.

EQUATION 8-9:

$$PhaseCompensation_{NEW} = PhaseCompensation_{OLD} + \Phi$$

Based on Equation 8-9, the maximum angle in degrees that can be compensated is ±3.2 degrees. If a larger phase shift is required, contact your local Microchip sales office.

8.5 Offset/No-Load Calibrations

During offset calibrations, no line voltage or current should be applied to the system. The system should be in a No-Load condition.

8.5.1 AC OFFSET CALIBRATION

There are three registers associated with the AC Offset Calibration:

- Offset Current RMS
- Offset Active Power
- Offset Reactive Power

When computing the AC offset values, the respective Gain and Range registers should be taken into consideration according to the block diagrams in Figures 5-2 and 5-4.

After a successful offset calibration, a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

8.5.2 DC OFFSET CALIBRATION

In DC applications, the high-pass filter on the current and voltage channels is turned off. To remove any residual DC value on the current, the DC Offset Current register adds to the A/D conversion immediately after the ADC and prior to any other function.

8.6 Calibrating the Line Frequency Register

The Line Frequency register contains a 16-bit number with a value equivalent to the input line frequency as it is measured on the voltage channel. When in DC mode, this calculation is turned off and the register will be equal to zero.

The measurement of the line frequency is only valid from 45 to 65 Hz.

8.6.1 USING THE AUTO-CALIBRATION FREQUENCY COMMAND

By applying a stable reference voltage with a constant line frequency that is equivalent to the value that resides in the Line Frequency Ref, the `Auto-Calibration Frequency` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following register is set when the `Auto-Calibration Frequency` command is issued:

• Gain Line Frequency

Note that the command is only required when running off the internal oscillator. The formula used to calculate the new gain is shown in Equation 8-1.

8.7 Temperature Compensation

The MCP39F521 measures the indication of the temperature sensor and uses the value to compensate the temperature variation of the shunt resistance and the frequency of the internal RC oscillator.

The same formula applies for Line Frequency, Current RMS, Active Power and Reactive Power. The temperature compensation coefficient depends on the 16-bit signed integer value of the corresponding compensation register.

EQUATION 8-10:

$$y = x \times (1 + c \times (T - T_{CAL}))$$

$$c = \frac{Temperature Compensation\ Register}{2^M}$$

Where:

- x = Uncompensated Output (corresponding to Line Frequency, Current RMS, Active Power and Reactive Power)
- y = Compensated Output
- c = Temperature Compensation Coefficient (depending on the shunt's Temperature Coefficient of Resistance or on the internal RC oscillator temperature frequency drift). There are three registers: one for Line Frequency compensation, one for Current compensation, and one for power compensation (Active and Reactive)
- T = Thermistor Voltage (in 10-bit ADC units)
- T_{CAL} = Ambient Temperature Reference Voltage. It should be set at the beginning of the calibration procedure, by reading the thermistor voltage and writing its value to the ambient temperature reference voltage register.
- M = 26 (for Line Frequency compensation)
  = 27 (for Current, Active Power and Reactive Power)

When calibrating the temperature, the effect of the compensation coefficients is minimal. The coefficients need to be tuned when the difference between the calibration temperature and the device temperature is significant. It is recommended to use the default values as starting points.

8.8 Retrieving Factory Default Calibration Values

After user calibration and a `Save to Flash` command has been issued, it is possible to retrieve the factory default calibration values. This can be done by writing 0xA5A5 to the Calibration Register Delimiter, issuing a `Save to Flash`, and then resetting the part. This procedure will retrieve all factory default calibration values and will remain in this state until calibration has been performed again, and a `Save to Flash` command has been issued.

9.0 EEPROM

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable across the entire V_{DD} range. The MCP39F521 has 256 16-bit words of EEPROM that is organized in 32 pages for a total of 512 bytes.

There are three commands that support access to the EEPROM array.

- `EEPROM Page Read` (0x42)
- `EEPROM Page Write` (0x50)
- `EEPROM Bulk Erase` (0x4F)

TABLE 9-1: EXAMPLE EEPROM COMMANDS AND DEVICE RESPONSE

Command	Command ID BYTE 0	BYTE 1-N	# Bytes	Successful Response
`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, Checksum
`Page Write EEPROM`	0x50	PAGE + 16 BYTES OF DATA	18	ACK
`Bulk Erase EEPROM`	0x4F	---------	1	ACK

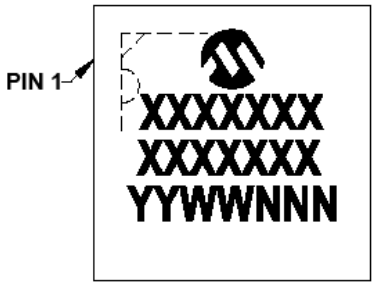
TABLE 9-2: MCP39F521 EEPROM ORGANIZATION

Page		00	02	04	06	08	0A	0C	0E
0	0000	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
1	0010	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
2	0020	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
3	0030	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
4	0040	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
5	0050	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
6	0060	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
7	0070	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
8	0080	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
9	0090	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
10	00A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
11	00B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
12	00C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
13	00D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
14	00E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
15	00F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
16	0100	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
17	0110	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
18	0120	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
19	0130	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
20	0140	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
21	0150	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
22	0160	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
23	0170	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
24	0180	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
25	0190	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
26	01A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
27	01B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
28	01C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
29	01D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
30	01E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
31	01F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF

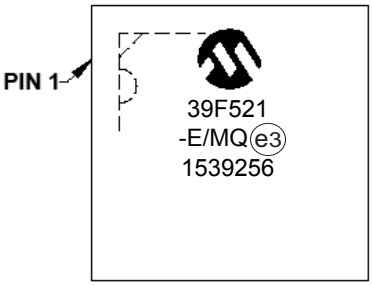
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

28-Lead QFN (5x5x0.9 mm)



Example

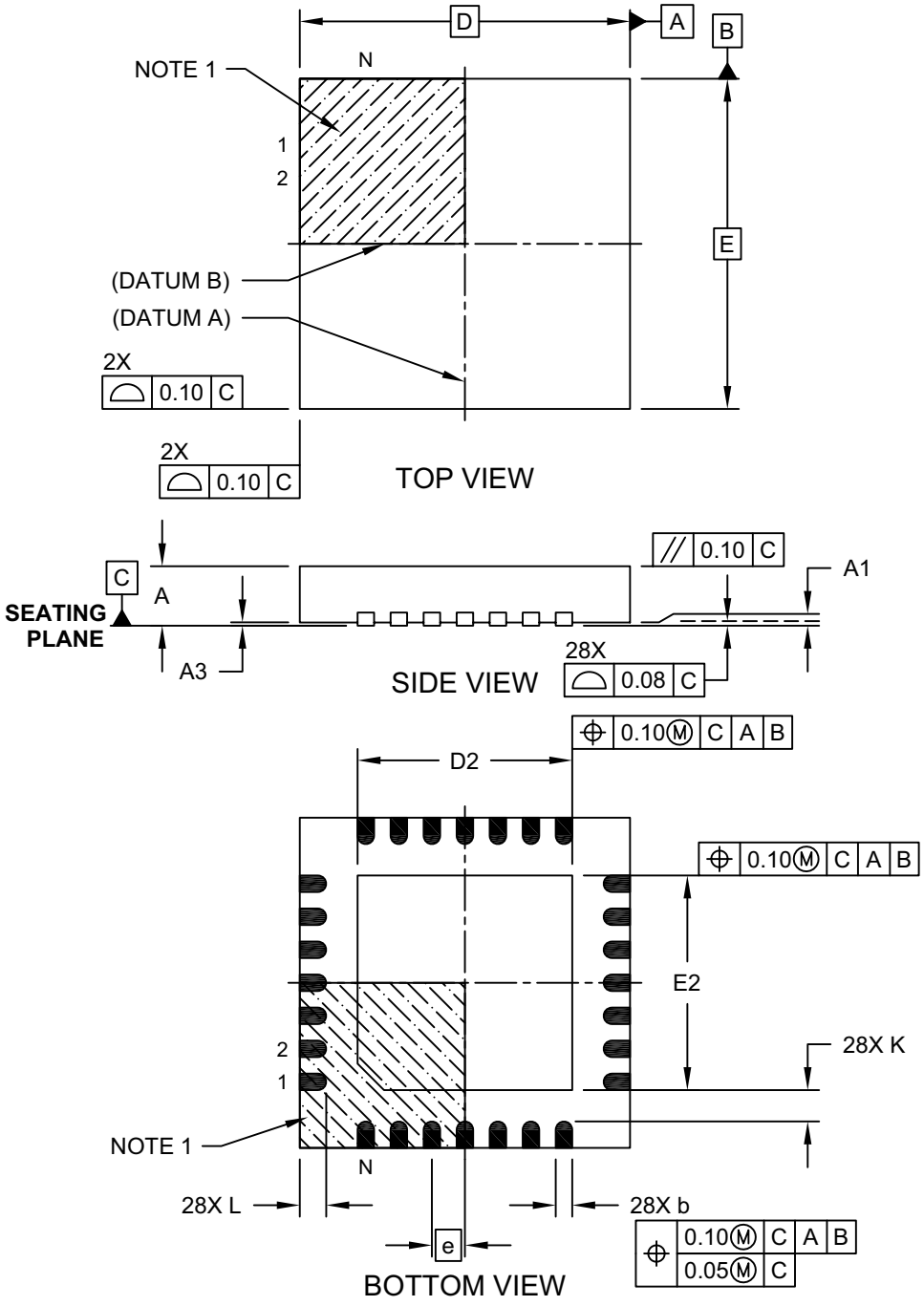


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

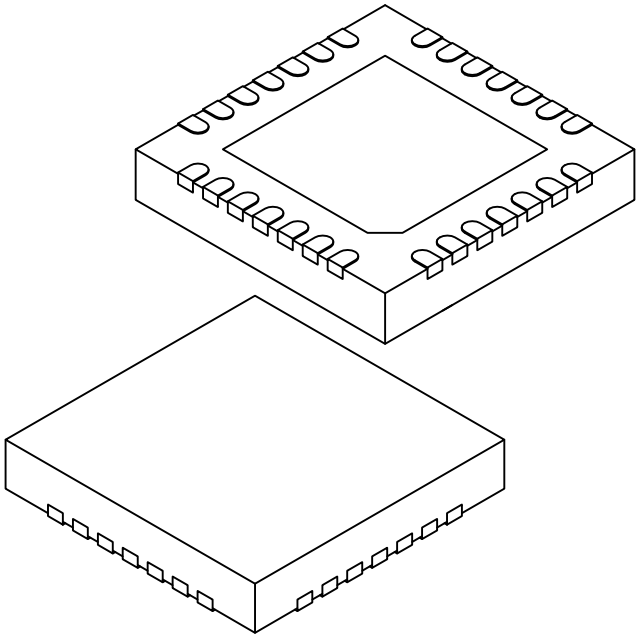
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-140C Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

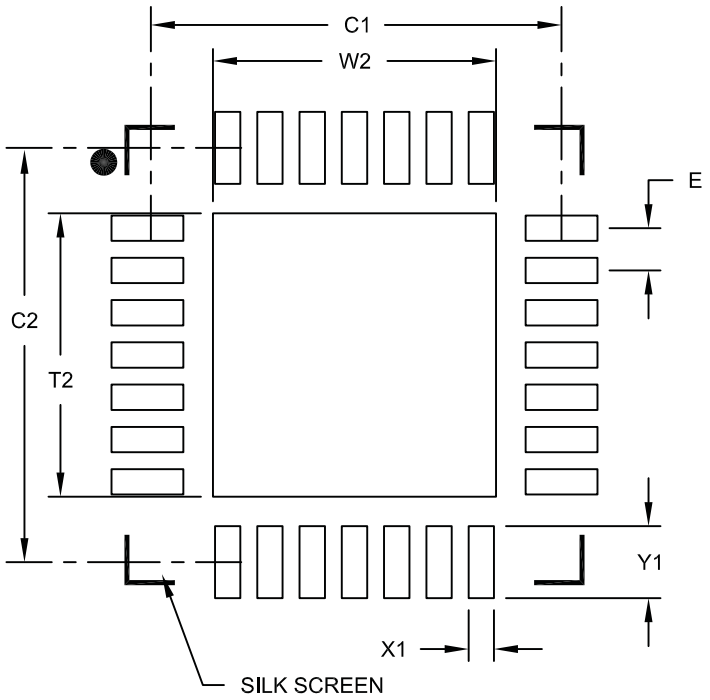
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-140C Sheet 2 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5 mm Body [QFN] Land Pattern With 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			0.85

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2140A

APPENDIX A: REVISION HISTORY

Revision A (September 2015)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP39F521:	I^2C Power-Monitor with Calculation and Energy Accumulation
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T =	Tape and Reel(1)
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	MQ =	Plastic Quad Flat, No Lead Package – 5x5x0.9 mm body (QFN), 28-lead

Examples:

a) MCP39F521-E/MQ: Extended temperature, 28LD 5x5 QFN package

b) MCP39F521T-E/MQ: Tape and Reel, Extended temperature, 28LD 5x5 QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

NOTES:

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