HV748

4-Channel High-Speed Bipolar ±75V 1.25A Ultrasound Pulser

Features

- High-Density Integrated Ultrasound Transmitter
- 0V to ±75V Output Voltage
- 1.25A Source and Sink Current in Pulse Mode
- ±300 mA Current in CW Mode
- Up to 20 MHz Operating Frequency
- Matched Delay Times
- 2.5V to 3.3V CMOS Logic Interface
- Built-in Output Drain Bleed Resistors

Applications

- Portable Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-Destructive Testing
- Pulse Waveform Generator

General Description

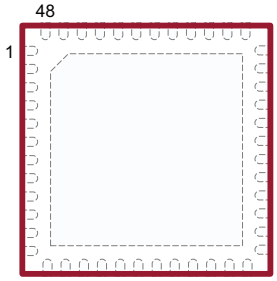
The HV748 is a 4-channel high-voltage high-speed pulse generator. It is designed for portable medical ultrasound applications. This high-voltage and high-speed integrated circuit can also be used for piezoelectric, capacitive or MEMS sensing in ultrasonic non-destructive detection and sonar ranger applications.

The HV748 consists of a controller logic interface circuit, level translators, MOSFET gate drivers and high-power P-channel and N-channel MOSFETs as the output stages for each channel.

The output stages of each channel are designed to provide peak output currents of over ±1.8A for pulsing, when in Mode 4, with up to ±75 volt swings. When in Mode 1, all the output stages drop the peak current to ±400 mA for low-voltage CW mode operation to decrease the power consumption of the IC. The drivers are supplied by two floating power supplies referenced to V_{PP} and V_{NN}. This direct coupling topology of the gate drivers not only eliminates two high-voltage capacitors per channel but also makes the PCB layout easier.

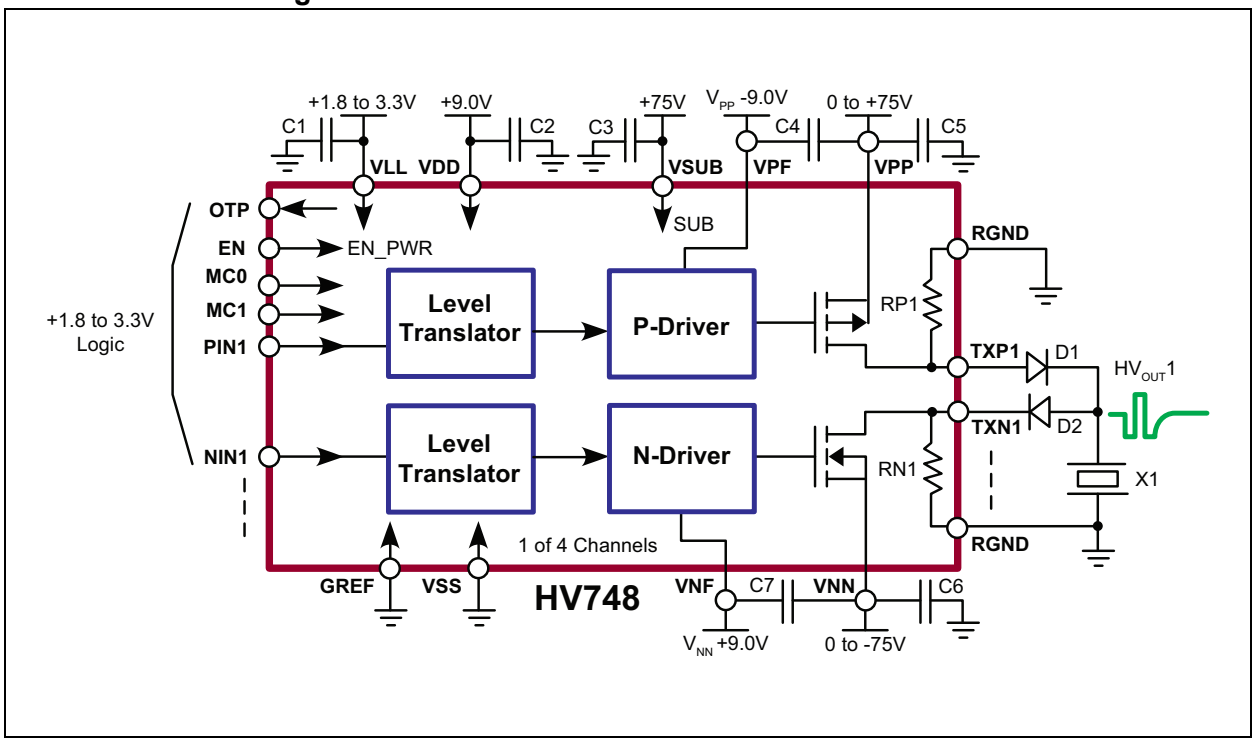
Package Type

48-lead (7 X 7) VQFN
(Top view)

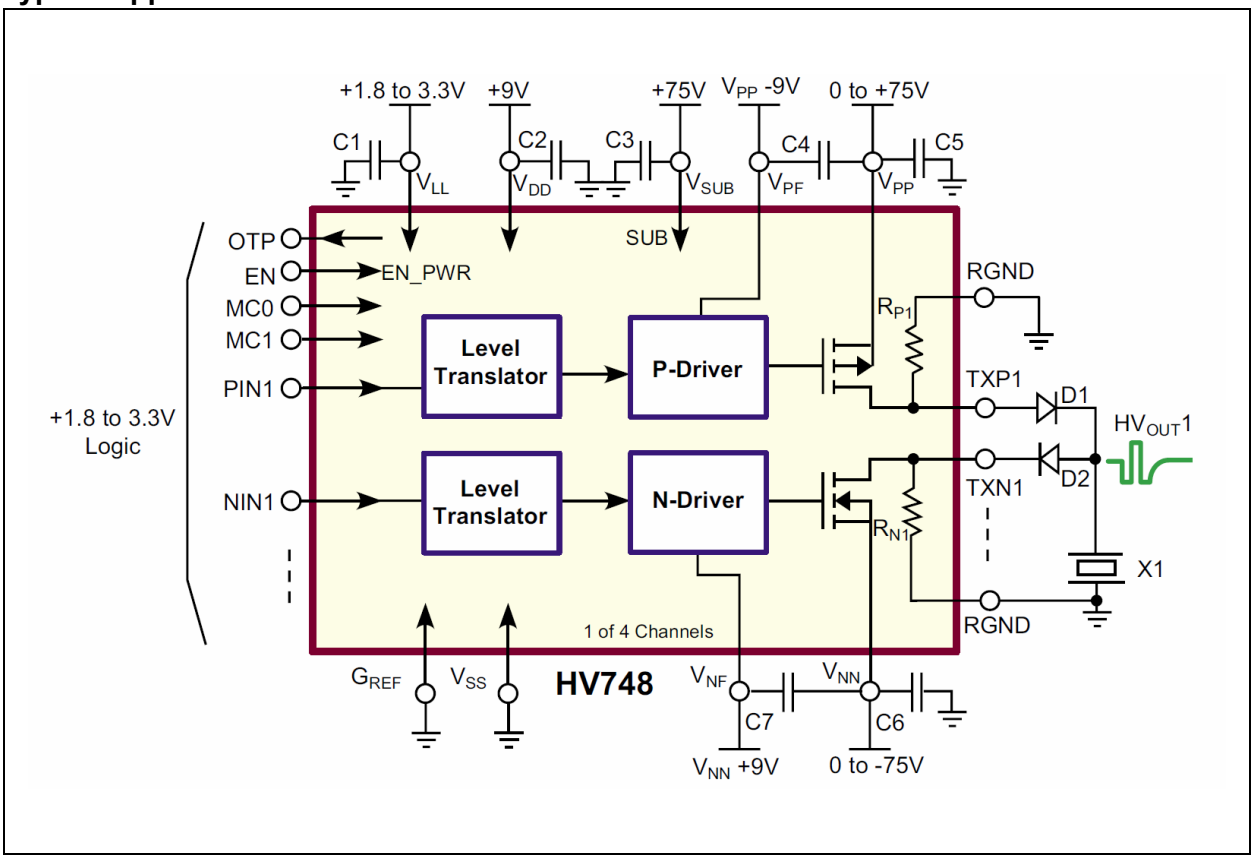


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Power Supply Reference, V_{SS} 0V
Positive Logic Supply, V_{LL} ..... –0.5V to +7V
Positive Logic and Level Translator Supply, V_{DD} ..... –0.5V to +14V
Positive Floating Gate Drive Supply, $V_{PP}–V_{PF}$ ..... –0.5V to +14V
Negative Floating Gate Drive Supply, $V_{NF}–V_{NN}$ ..... –0.5V to +14V
Differential High-Voltage Supply, $V_{PP}–V_{NN}$ ..... +170V
High-Voltage Positive Supply, V_{PP} ..... –0.5V to +85V
High-Voltage Negative Supply, V_{NN} ..... –0.5V to –85V
Overtemperature Protection Output, OTP ..... –0.5V to +7V
All Logic Input PIN_X, NIN_X and EN Voltages ..... –0.5V to +7V
Substrate to V_{SS} Voltage Difference, $V_{SUB}–V_{SS}$ ..... +170V
V_{PP} to TXP_X Voltage Difference, $V_{PP}–TXP_X$ ..... +170V
Substrate to TXP_X Voltage Difference, $V_{SUB}–TXP_X$ ..... +170V
TXN_X to V_{NN} Voltage Difference, $TXN_X–V_{NN}$ ..... +170V
Operating Junction Temperature, T_J ..... –40°C to +125°C
Storage Temperature, T_S ..... –65°C to +150°C
ESD Rating (**Note 1**) ..... ESD Sensitive

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

OPERATING SUPPLY VOLTAGES AND CURRENT (FOUR ACTIVE CHANNELS)

Electrical Specifications: V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +9V, $V_{PP}–V_{PF}$ = +9V, $V_{NN}–V_{NF}$ = –9V, V_{PP} =+75V, V_{NN} = –75V, T_A = 25°C unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Voltage Reference	V_{LL}	1.2	1.8 to 3.3	5	V	
Internal Voltage Supply	V_{DD}	8	9	12	V	
Positive Gate Driver Supply	V_{PF}	(V_{PP}–12)	(V_{PP}–9)	(VPP–8)	V	Floating driver voltage supplies
Negative Gate Drive Supply	V_{NF}	(V_{NN}+8)	(V_{NN}+9)	(V_{NN}+12)	V	
IC Substrate Voltage	V_{SUB}	V_{DD}	V_{PP}	+75	V	Must be the most positive potential of the IC
Positive High-Voltage Supply	V_{PP}	0	—	+75	V	
Negative High-Voltage Supply	V_{NN}	–75	—	0	V	
Slew Rate Limit of V_{PP}, V_{NN}	SR_{MAX}	—	—	25	V/µs	Built-in slew rate detection protection (**Note 1**)
V_{LL} Current EN = Low	I_{LL}	—	35	120	µA	
V_{DD} Current EN = Low	I_{DDQ}	—	15	—	µA	
V_{DD} Current EN = High	I_{DDEN}	—	0.75	2	mA	f = 0 MHz
V_{DD} Current MODE = 4	I_{DDEN}	—	0.75	—	mA	f = 5 MHz, continuous, no load
V_{DD} Current MODE = 1	I_{DDENCW}	—	2	—	mA	
V_{PP} Current EN = Low	I_{PPQ}	—	10	25	µA	f = 0 MHz

Note 1: Design guidance only

OPERATING SUPPLY VOLTAGES AND CURRENT (FOUR ACTIVE CHANNELS) (CONTINUED)

Electrical Specifications: V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +9V, V_{PP}–V_{PF} = +9V, V_{NN}–V_{NF} = –9V, V_{PP} =+75V, V_{NN} = –75V, T_A = 25°C unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{PP} Current MODE = 4	I_{PPEN}	—	250	—	mA	f = 5 MHz, continuous no load
V_{PP} Current MODE = 1	I_{PPENCW}	—	170	—	mA	
V_{NN} Current EN = Low	I_{NNQ}	—	15	30	µA	f = 0 MHz
V_{NN} Current MODE = 4	I_{NNEN}	—	250	—	mA	f = 5 MHz, continuous, No load
V_{NN} Current MODE = 1	I_{NNENCW}	—	170	—	mA	
V_{PF} Current EN = Low	I_{PFQ}	—	10	25	µA	f = 0 MHz
V_{PF} Current MODE = 4	I_{PFEN}	—	50	—	mA	f = 5 MHz, continuous, No load
V_{PF} Current MODE = 1	I_{PFENCW}	—	12	—	mA	
V_{NF} Current EN = Low	I_{NFQ}	—	20	30	µA	f = 0 MHz
V_{NF} Current MODE = 4	I_{NFEN}	—	25	—	mA	f = 5 MHz, continuous, No load
V_{NF} Current MODE = 1	I_{NFENCW}	—	12	—	mA	

Note 1: Design guidance only

UNDERVOLTAGE AND OVERTEMPERATURE PROTECTION

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Open Drain Pull-Up Voltage	V_{PULL_UP}	—	—	5	V	
V_{DD} Threshold	V_{UVDD}	3.5	—	6.5	V	
V_{LL} Threshold	V_{UVLL}	0.7	—	1	V	
V_{PF}, V_{NF} Threshold	V_{UVVF}	3.5	—	6.5	V	
OTP Flag Output Low Voltage	V_{OL_OTP}	—	—	1	V	V_{LL} = 3.3V, OTP = Active, I_{PULL_UP} = 1 mA
Maximum Open-Drain Output Current	I_{OTP}	—	1	—	mA	
Overtemperature Threshold	T_{OTP}	95	110	125	°C	If overtemperature occurred, OTP low and all TX outputs will be High-Z.
OTP Output Reset Hysteresis	T_{HYS}	—	7	—		

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +9V, V_{PP}–V_{PF} = +9V, V_{NN}–V_{NF} = –9V, V_{PP} = +75V, V_{NN} = –75V, T_A = 25°C unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
P-CHANNEL MOSFET OUTPUT, TXP1-4 (MC [1:0] = 11b)						
Output Saturation Current	I_{OUT}	1.25	1.8	—	A	
Channel Resistance	R_{ON}	—	8	—	Ω	I_{SD} = 100 mA
Output Capacitance	C_{OSS}	—	100	—	pF	V_{DS} = 25V, f = 1 MHz (**Note 1**)
N-CHANNEL MOSFET OUTPUT, TXN1-4 (MC [1:0] = 11b)						
Output Saturation Current	I_{OUT}	1.25	1.8	—	A	
Channel Resistance	R_{ON}	—	7.5	—	Ω	I_{SD} = 100 mA
Output Capacitance	C_{OSS}	—	40	—	pF	V_{DS} = 25V, f = 1 MHz (**Note 1**)
MOSFET DRAIN BLEED RESISTOR						

Note 1: Design guidance only

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +9V, V_{PP}–V_{PF} = +9V, V_{NN}–V_{NF} = –9V, V_{PP} = +75V, V_{NN} = –75V, T_A = 25°C unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Output Bleed Resistance	$R_{P/N1\sim4}$	10	15	30	kΩ	
Bleed Resistors Power Limit	P_{RO}	—	—	40	mW	**Note 1**
LOGIC INPUT						
Input Logic High Voltage	V_{IH}	(V_{LL}–0.4)	—	V_{LL}	V	
Input Logic Low Voltage	V_{IL}	0	—	0.4	V	
Input Logic High Current	I_{IH}	—	—	10	µA	
Input Logic Low Current	I_{IL}	–10	—	—	µA	
Input Logic Capacitance	C_{IN}	—	—	5	pF	**Note 1**

Note 1: Design guidance only

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +9V, V_{PP}–V_{PF} = +9V, V_{NN}–V_{NF} = –9V, V_{PP} = +75V, V_{NN} = –75V, T_A = 25°C unless otherwise specified.

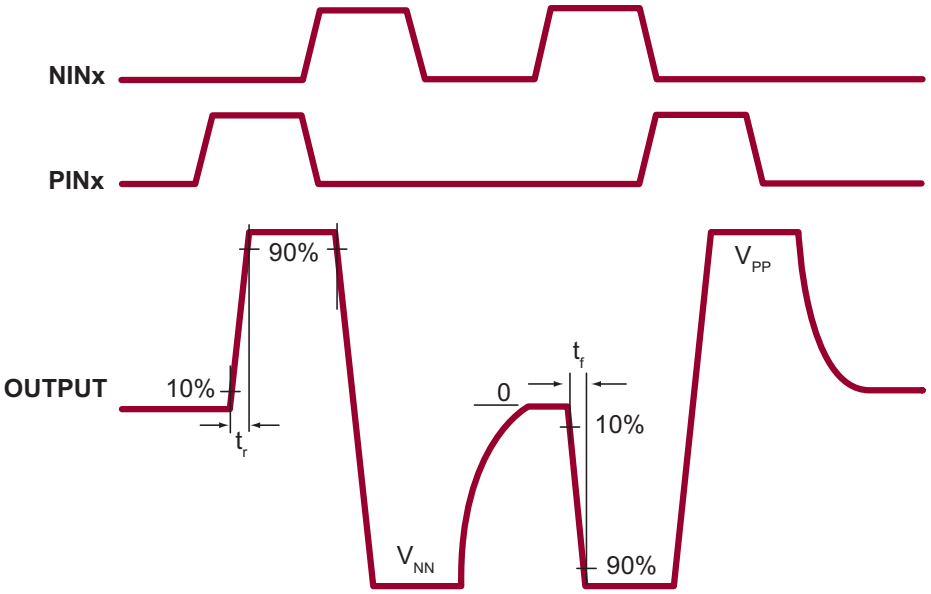
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Output Rise Time	t_r	—	35	—	ns	330 pF//2.5 kΩ load
Output Fall Time	t_f	—	43	—	ns	
Output Frequency Range	f_{OUT}	—	—	20	MHz	100Ω resistor load
Second Harmonic Distortion	HD2	—	–40	—	dB	100Ω resistor load (**Note 1**)
Enable Time	t_{EN}	—	180	500	µs	100Ω resistor load
Disable Time	t_{DIS}	—	2.8	10	µs	100Ω resistor load
Delay Time on Inputs Rise	t_{dr}	—	18	—	ns	3.9Ω resistor load (See **Timing Waveforms**.)
Delay Time on Inputs Fall	t_{df}	—	18	—	ns	
Delay Time Matching	Δt_{DELAY}	—	±2	—	ns	P to N, channel to channel
Delay on Mode Change	t_{dm}	—	2.5	10	µs	100Ω resistor load
Delay Jitter on Rise or Fall	t_j	—	15	—	ps	V_{PP}/V_{NN} = ±25V, input t_r 50% to HV_{OUT} t_r or t_f 50%, with 330 pF//2.5 kΩ load (**Note 1**)

Note 1: Design guidance only

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
48-lead VQFN	θ_{JA}	—	18	—	°C/W	
48-lead VQFN (Junction to Thermal Pad)	θ_{JC}	—	2	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV748 are listed in Table 2-1.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VDD	Positive internal voltage supply (+9V)
2	VSS	Power supply return (0V)
3	PIN1	Input logic control of high-voltage output P-FET of channel 1, High = on, Low = off
4	NIN1	Input logic control of high-voltage output N-FET of channel 1, High = on, Low = off
5	PIN2	Input logic control of high-voltage output P-FET of channel 2, High = on, Low = off
6	NIN2	Input logic control of high-voltage output N-FET of channel 2, High = on, Low = off
7	PIN3	Input logic control of high-voltage output P-FET of channel 3, High = on, Low = off
8	NIN3	Input logic control of high-voltage output N-FET of channel 3, High = on, Low = off
9	PIN4	Input logic control of high-voltage output P-FET of channel 4, High = on, Low = off
10	NIN4	Input logic control of high-voltage output N-FET of channel 4, High = on, Low = off
11	VSS	Power supply return (0V)
12	VDD	Positive internal voltage supply (+9V)
13	OTP	Overtemperature protection output, open N-FET drain, active low if IC temperature >110°C.
14	MC1	Output Current mode control pins (See Table 3-3.)
15	MC0	
16	Thermal Pad (VSUB)	Substrate of the IC. Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.
17	VPF	P-FET drive floating power supply, (VPP–VPF) = +9V
18	VPP	Positive high-voltage power supply (+75V)
19		
20		
21	VNN	Negative high-voltage power supply (–75V)
22		
23		
24	VNF	N-FET drive floating power supply, (VNF–VNN) = +9V
25	Thermal Pad (VSUB)	Substrate of the IC. Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.
26	RGND	Bleed resistors common return ground. (Both pins must be used.)
27	TXN4	Output N-FET drain (open drain output) for Channel 4
28	TXP4	Output P-FET drain (open drain output) for Channel 4
29	TXN3	Output N-FET drain (open drain output) for Channel 3
30	TXP3	Output P-FET drain (open drain output) for Channel 3
31	TXN2	Output N-FET drain (open drain output) for Channel 2
32	TXP2	Output P-FET drain (open drain output) for Channel 2
33	TXN1	Output N-FET drain (open drain output) for Channel 1
34	TXP1	Output P-FET drain (open drain output) for Channel 1
35	RGND	Bleed resistors common return ground. (Both pins must be used.)

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
36	Thermal Pad (VSUB)	Substrate of the IC. Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.
37	VNF	N-FET drive floating power supply, (VNF–VNN) = +9V
38	VNN	Negative high-voltage power supply (–75V)
39		
40		
41	VPP	Positive high-voltage power supply (+75V)
42		
43		
44	VPF	P-FET drive floating power supply, (VPP–VPF) = +9V
45	Thermal Pad (VSUB)	Substrate of the IC. Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.
46	EN	Chip power enable High = on, Low = off
47	GREF	Logic Low reference, logic ground (0V)
48	VLL	Logic High-voltage reference input (+3.3V)

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV748:

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-Up		Power-Down	
Step	**Description**	**Step**	**Description**
1	V_{SUB}	1	All logic signals go to low
2	V_{LL} with logic signal low	2	V_{PP} and V_{NN}
3	V_{DD}	3	(V_{PP}–V_{PF}) and (V_{NF}–V_{NN})
4	(V_{PP}–V_{PF}) and (V_{NF} –V_{NN})	4	V_{DD}
5	V_{PP} and V_{NN}	5	V_{LL}
6	Logic control signals	6	V_{SUB}

Note: Powering up or powering down in any arbitrary sequence will not damage the device. The power-up sequence and power-down sequence are only recommended to minimize possible inrush current.

TABLE 3-2: TRUTH FUNCTION TABLE (ALL MODES)

Logic Inputs			Outputs	
$\overline{EN}$	PIN_X	NIN_X	TXP_X	TXN_X
1	0	0	OFF	OFF
1	1	0	ON	OFF
1	0	1	OFF	ON
1	1	1	ON (**Note 1**)	ON (**Note 1**)
0	X	X	OFF	OFF

Note 1: Not allowed. May damage IC.

TABLE 3-3: DRIVE MODE CONTROL TABLE

Mode	MC1	MC0	I_{SC} (A) (**Note 2**)	R_{ONP} (Ω)	R_{ON} (Ω) (**Note 3**)
1	0	0	0.41	35	33
2	0	1	0.58	25	23
3	1	0	0.97	15	14
4	1	1	1.8	8	7.5

Note 1: V_{PP}/V_{NN} = +/–75V, V_{DD} = (V_{PP}–V_{PF}) = (V_{NF}–V_{NN}) = +9V

2: I_{SC} is current into 1Ω to GND.

3: R_{ON} is calculated from V_{OUT} into 100Ω load.

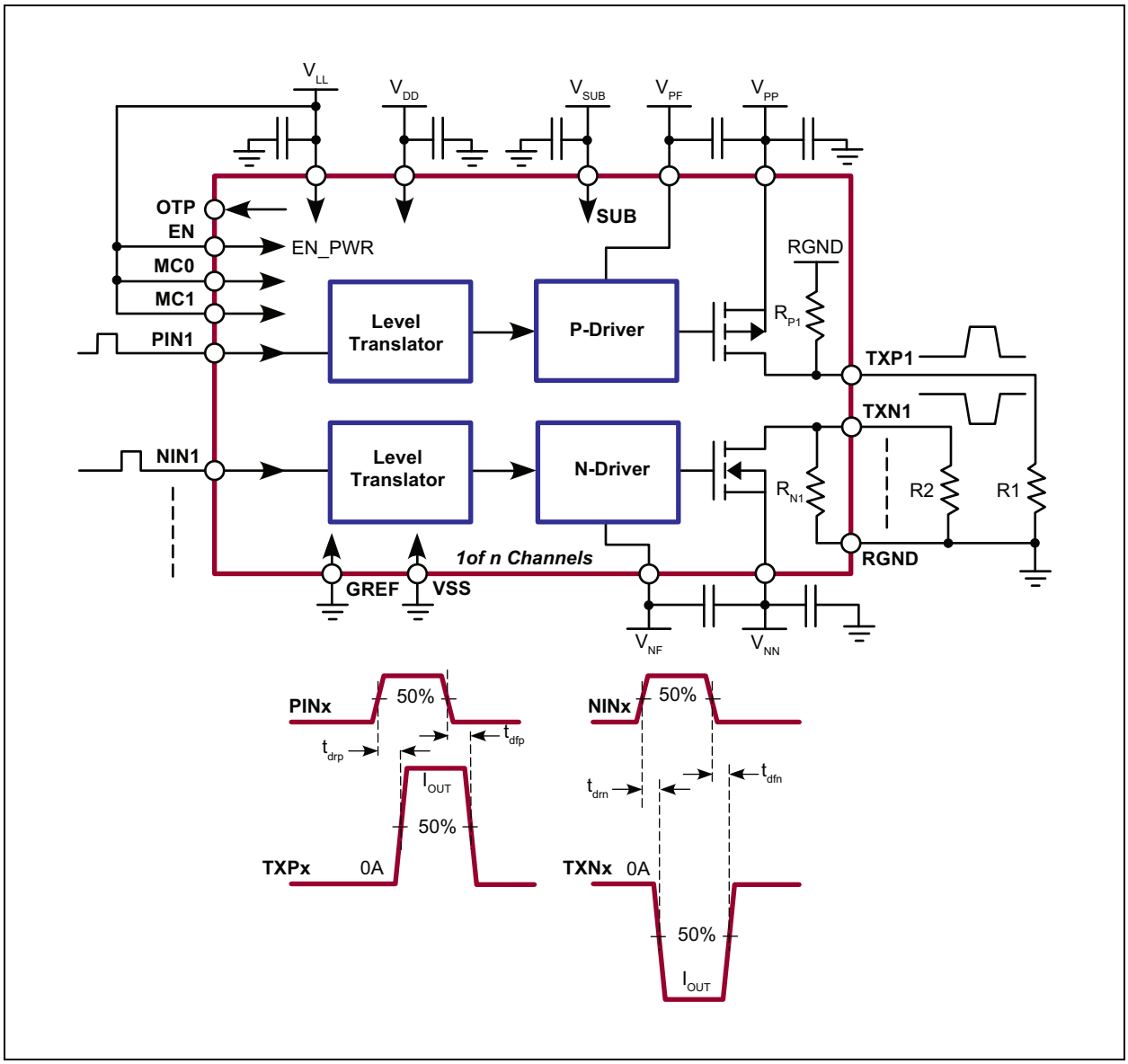


FIGURE 3-1: *Switch Test Timing Diagram.*

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

48-lead QFN

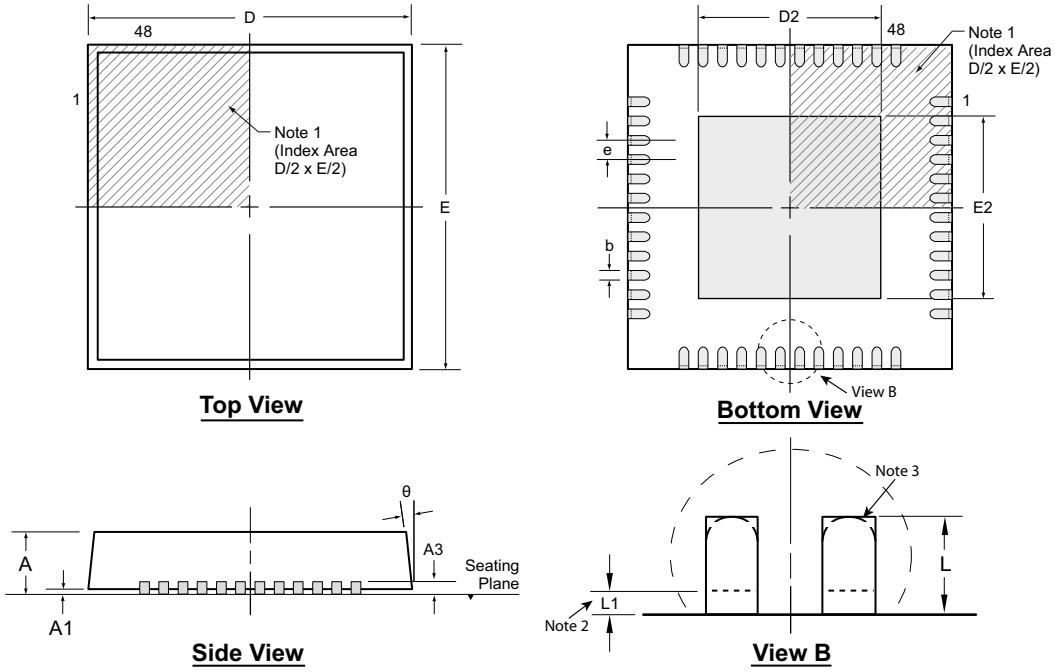
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

48-Lead QFN Package Outline (K6)

7.00x7.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	6.85*	1.25	6.85*	1.25	0.50 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.25	7.00	-	7.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	7.15*	5.45	7.15*	5.45		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VKKD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (November 2018)

- Converted Supertex Doc# DSFP-HV748 to Microchip DS20005898A
- Removed “HVCMOS® Technology for high performance” in the Features section
- Changed the package marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV748	=	4-Channel High-Speed Bipolar ±75V 1.25A Ultrasound Pulser
Package:	K6	=	48-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	260/Tray for a K6 Package

Example:

a) HV748K6-G: 4-Channel High-Speed Bipolar ±75V1.25A Ultrasound Pulser, 48-lead VQFN, 260/Tray

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