

Product Summary (Typ. @ $V_{GS} = -4.5V$, $T_A = +25^\circ C$)

V_{DSS}	$R_{DS(on)}$	Q_g	Q_{gd}	I_D
-8V	8.2m Ω	8.1nC	1.8nC	-10A

Description

This 3rd generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal $R_{DS(on)}$ per footprint area.

Applications

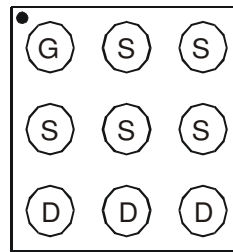
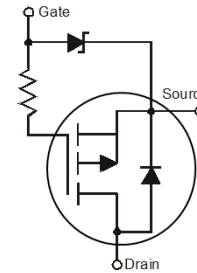
- DC-DC Converters
- Battery Management
- Load Switch

Features

- LD-MOS Technology with the Lowest Figure of Merit:
 $R_{DS(on)} = 8.2m\Omega$ to Minimize On-State Losses
 $Q_g = 8.1nC$ for Ultra-Fast Switching
- $V_{GS(th)} = -0.8V$ typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm x 1.5mm
- Height = 0.62mm for Low Profile
- ESD = 6kV HBM Protection of Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: U-WLB1515-9
- Terminal Connections: See Diagram Below

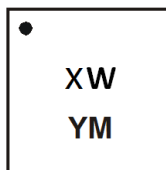
U-WLB1515-9

 Top-View
Pin Configuration


Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMP1012UCB9-7	U-WLB1515-9	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information
U-WLB1515-9


XW = Product Type Marking Code
 YM = Date Code Marking
 Y or \bar{Y} = Year (ex: B = 2014)
 M or \bar{M} = Month (ex: 9 = September)

Date Code Key

Year	2012	2013	2014	2015	2016	2017	2018
Code	Z	A	B	C	D	E	F

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units	
Drain-Source Voltage	V_{DSS}	-8	V	
Gate-Source Voltage	V_{GSS}	-6	V	
Continuous Drain Current (Note 5) $V_{GS} = -4.5\text{V}$	I_D	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	-10 -8	A
Continuous Drain Current (Note 6) $V_{GS} = -4.5\text{V}$		$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	-7.4 -6.0	A
Pulsed Drain Current (Pulse duration $10\mu\text{s}$, duty cycle $\leq 1\%$)	I_{DM}	-50	A	
Continuous Source Pin Current (Note 6)	I_S	-2	—	
Pulsed Source Pin Current (Pulse duration $10\mu\text{s}$, duty cycle $\leq 1\%$)	I_{SM}	-15	—	
Continuous Gate Current	I_G	-0.5	A	

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	0.89	W
Total Power Dissipation (Note 6)	P_D	1.57	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	+142.1	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	+80.5	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-8	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Gate to Source Voltage	BV_{SGS}	-6	—	—	V	$V_{DS} = 0\text{V}, I_G = -250\mu\text{A}$
Zero Gate Voltage Drain Current @ $T_C = +25^\circ\text{C}$	I_{DSS}	—	—	-1	μA	$V_{DS} = -4.0\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	-100	nA	$V_{GS} = -4.0\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-0.8	-1.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	8.2	10	m Ω	$V_{GS} = -4.5\text{V}, I_D = -2\text{A}$
			10	13		$V_{GS} = -3.0\text{V}, I_D = -2\text{A}$
			11	14		$V_{GS} = -2.5\text{V}, I_D = -2\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	16.8	—	S	$V_{DS} = -4\text{V}, I_D = -2\text{A}$
Diode Forward Voltage (Note 6)	V_{SD}	—	-0.7	-1	V	$V_{GS} = 0\text{V}, I_S = -2\text{A}$
Reverse Recovery Charge	Q_{rr}	—	6.3	—	nC	$V_{dd} = -5\text{V}, I_F = -2\text{A}$
Reverse Recovery Time	t_{rr}	—	18.5	—	ns	$di/dt = 200\text{A}/\mu\text{s}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	817	1060	pF	$V_{DS} = -4\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	595	770	pF	
Reverse Transfer Capacitance	C_{rss}	—	269	350	pF	
Series Gate Resistance	R_G	—	1.9	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge (4.5V)	Q_g	—	8.1	10.5	nC	$V_{GS} = -4.5\text{V}, V_{DS} = -4\text{V}, I_D = -2\text{A}$
Gate-Source Charge	Q_{gs}	—	0.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.8	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	6.2	10	ns	$V_{DD} = -4\text{V}, V_{GS} = -4.5\text{V}, I_{DS} = -2\text{A}, R_G = 10\Omega$
Turn-On Rise Time	t_r	—	22.6	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	30.1	48	ns	
Turn-Off Fall Time	t_f	—	22.7	—	ns	

- Notes:
- Device mounted on FR-4 PCB with minimum recommended pad layout.
 - Device mounted on FR4 material with 1-inch² (6.45cm²), 2oz (0.071mm thick) Cu.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

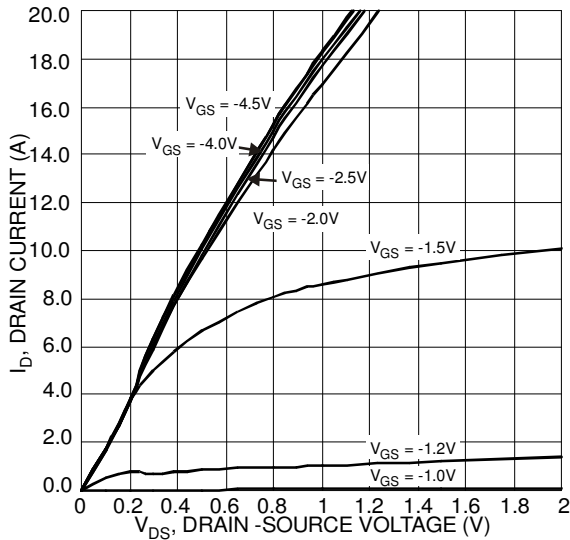


Figure 1 Typical Output Characteristics

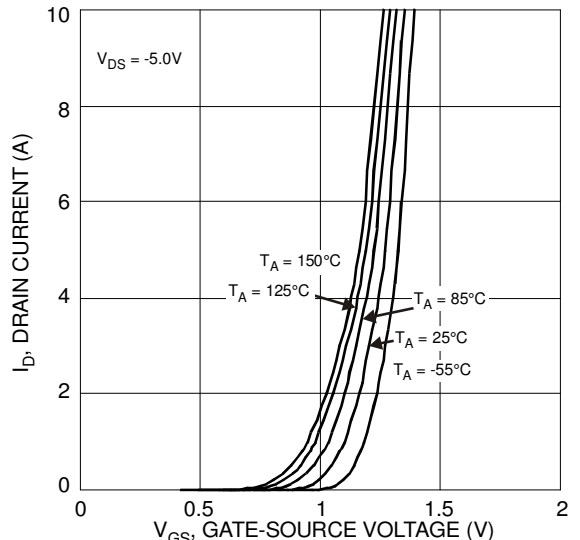


Figure 2 Typical Transfer Characteristics

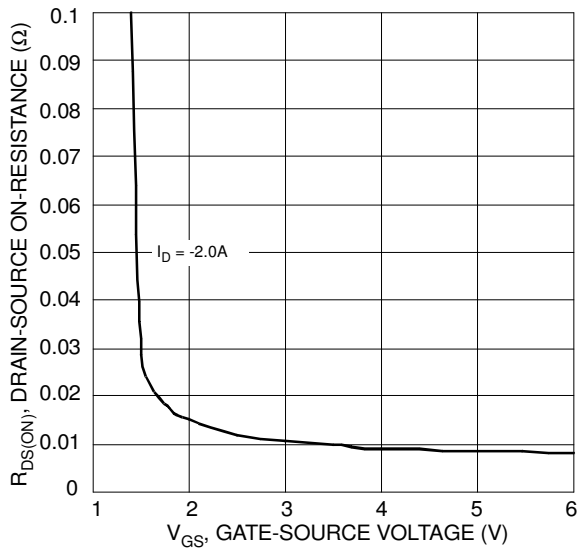


Figure 3 Typical Transfer Characteristic

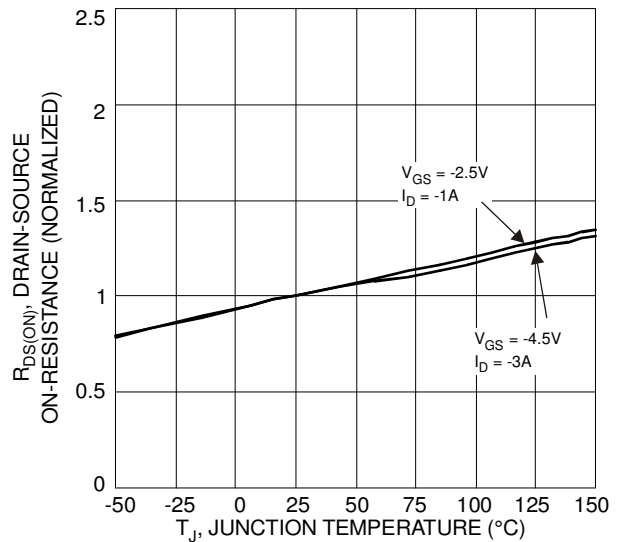


Figure 4 On-Resistance Variation with Temperature

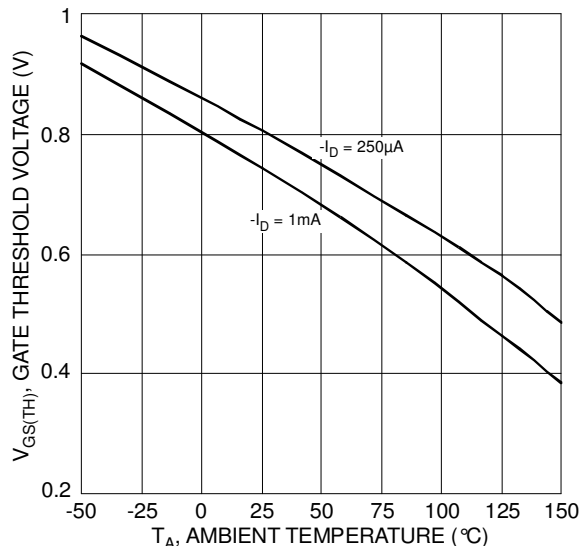


Figure 5 Gate Threshold Variation vs. Ambient Temperature

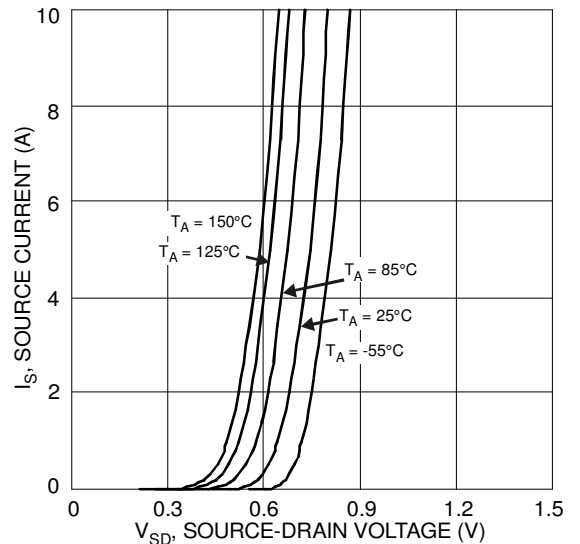


Figure 6 Diode Forward Voltage vs. Current

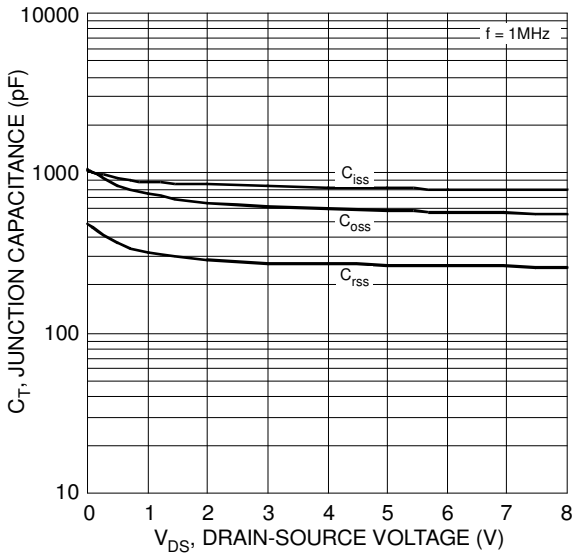


Figure 7 Typical Junction Capacitance

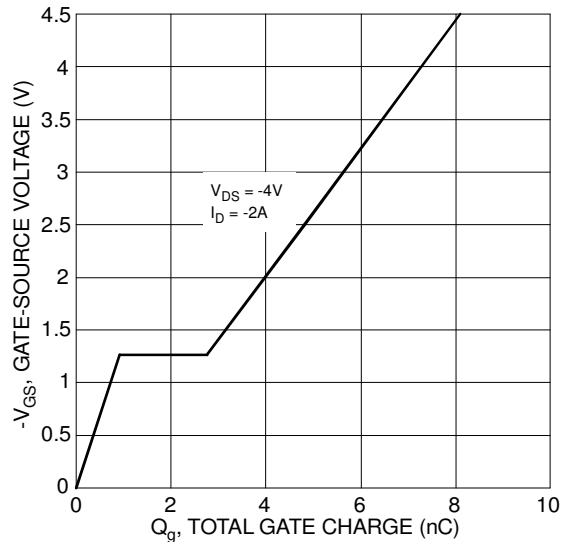


Figure 8 Gate-Charge Characteristics

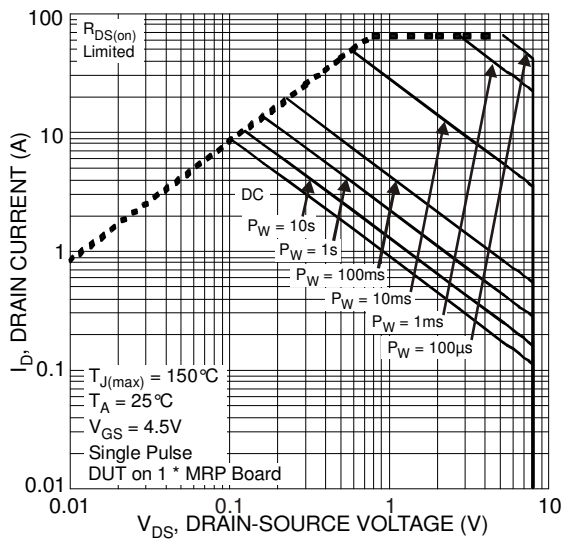


Figure 9 SOA, Safe Operation Area

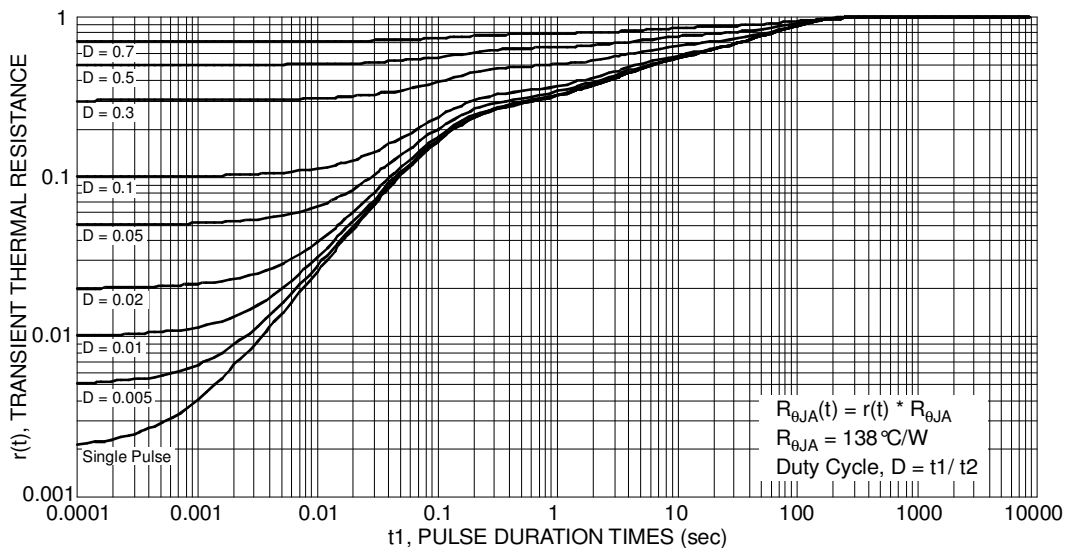
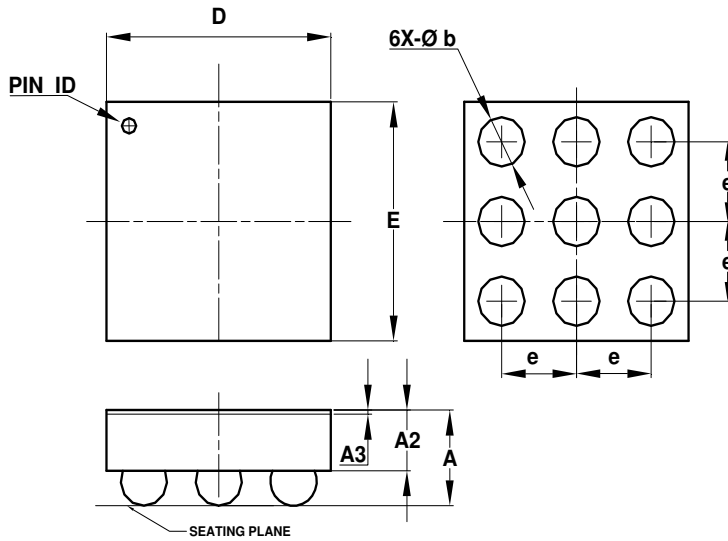


Figure 10 Transient Thermal Resistance

Package Outline Dimensions

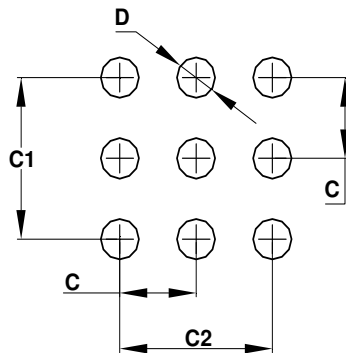
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



U-WLB1515-9			
Dim	Min	Max	Typ
A	-	0.62	-
A2	-	0.36	0.36
A3	0.020	0.030	0.025
b	0.27	0.37	0.32
D	1.47		1.49
E	1.47		1.49
e	-	-	0.50
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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