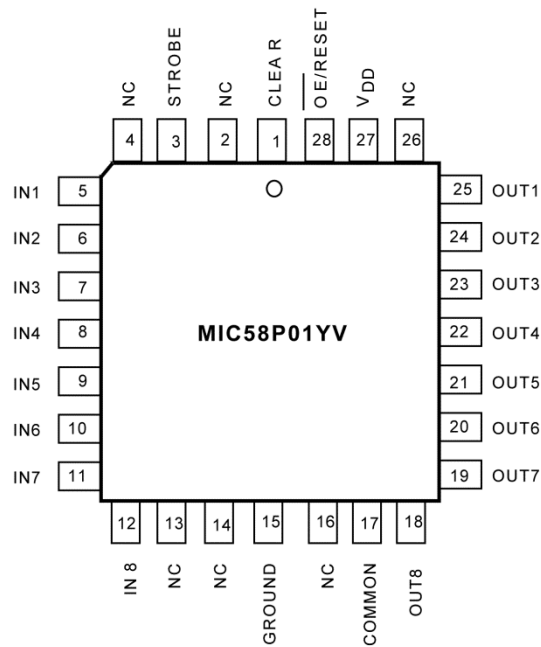


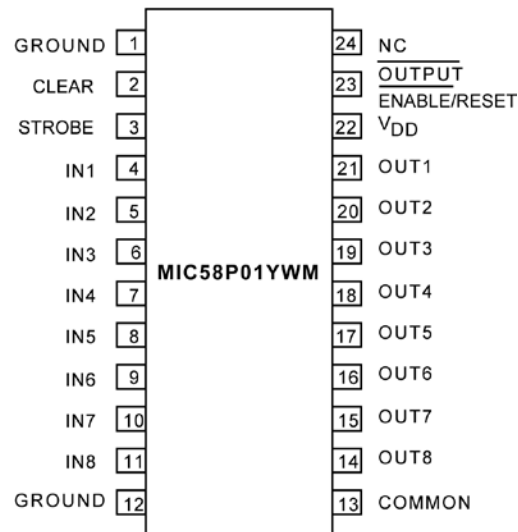
Ordering Information

Part Number	Junction Temperature Range	Package	Pb-Free
MIC58P01YV	-40°C to +85°C	28-Pin PLCC	√
MIC58P01YWM	-40°C to +85°C	28-Pin Wide SOIC	√

Pin Configuration

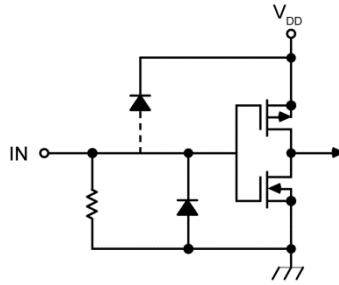


**28-Pin PLLC (V)
(Top View)**



**24-Pin SOIC (WM)
(not pin compatible with MIC5801YWM)**

Typical Input



Pin Description

Pin Number (PLCC)	Pin Number (SOIC)	Pin Name	Pin Function
1	2	CLEAR	Resets all Latches and turns all outputs OFF (open).
3	3	STROBE	Input Strobe Pin. Loads output latches when High.
5 – 12	4 – 11	IN _N	Parallel Inputs, 1 through 8.
15	1, 12	GROUND	Logic and Output Ground pin.
17	13	COMMON	Transient suppression diode common cathode pin.
18 – 25	14 – 21	OUT _N	Parallel Outputs, 8 through 1.
27	22	V _{DD}	Logic Supply voltage.
28	23	<u>OUTPUT ENABLE / RESET</u>	When Low, Outputs are active. When High, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE output.

Absolute Maximum Ratings⁽¹⁾

Output Voltage (V_{CE})	+80V
Logic Supply Voltage (V_{DD})	+15V
Input Voltage Range (V_{IN})	-0.3V to V_{DD} +0.3V
Operating Temperature Range (T_A)	-55°C to +85°C
Storage Temperature Range (T_S)	-65°C to +125°C
ESD Rating ⁽³⁾	ESD Sensitive

Operating Ratings⁽²⁾

Package Power Dissipation, P_D	
MIC58P01YV	1.6W
Derate above $T_A = +25^\circ\text{C}$	16mW/°C
MIC58P01YWM	1.4W
Derate above $T_A = +25^\circ\text{C}$	14mW/°C
Operating Temperature Range (T_A)	-40°C to +85°C

Electrical Characteristics⁽⁴⁾

$V_{DD} = 5V$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CEX}	Output Leakage Current	$V_{CE} = 80V$, $T_A = +25^\circ\text{C}$			50	μA
		$V_{CE} = 80V$, $T_A = +70^\circ\text{C}$			100	
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	$I_C = 100\text{mA}$		0.9	1.1	V
		$I_C = 200\text{mA}$		1.1	1.3	
		$I_C = 350\text{mA}$		1.3	1.6	
$V_{IN(0)}$	Input Voltage (Low)				1.0	V
$V_{IN(1)}$	Input Voltage (High)	$V_{DD} = 12V$	10.5			
		$V_{DD} = 10V$	8.5			
		$V_{DD} = 5V$, Note 5	3.5			
R_{IN}	Input Resistance	$V_{DD} = 12V$	50	200		k Ω
		$V_{DD} = 10V$	50	300		
		$V_{DD} = 5V$	50	600		
$I_{DD(1ON)}$	Supply Current	One Driver ON, $V_{DD} = 12V$, Outputs Open		3.3	4.5	mA
		One Driver ON, $V_{DD} = 10V$, Outputs Open		3.1	4.5	
		One Driver ON, $V_{DD} = 5V$, Outputs Open		2.4	3.6	
$I_{DD(ON)}$		All Drivers ON, $V_{DD} = 12V$, Outputs Open		6.4	10.0	mA
		All Drivers ON, $V_{DD} = 10V$, Outputs Open		6.0	9.0	
		All Drivers ON, $V_{DD} = 5V$, Outputs Open		4.7	7.5	
$I_{DD(OFF)}$		All Drivers OFF, $V_{DD} = 12V$, Outputs Open, Inputs = 0V		3.0	4.5	mA
		All Drivers OFF, $V_{DD} = 5V$, Outputs Open, Inputs = 0V		2.2	3.6	
I_R		Clamp Diode Leakage Current	$V_R = 80V$, $T_A = +25^\circ\text{C}$			50
	$V_R = 80V$, $T_A = +70^\circ\text{C}$				100	
I_{LIM}	Overcurrent Threshold	Per Output		500		mA
V_{SU}	Start-Up Voltage	Note 6	3.5	4.0	4.5	V

Notes:

- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.
- Specification for packaged product only.
- Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
- Under-Voltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

Electrical Characteristics⁽⁴⁾ (Continued)

$V_{DD} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD\ MIN}$	Minimum Operating V_{DD}		3.0	3.5	4.0	V
V_F	Clamp Diode Forward Voltage	$I_F = 350mA$		1.7	2.0	V
	Thermal Shutdown			165		$^\circ C$
	Thermal Shutdown Hysteresis			10		$^\circ C$

Truth Table

IN_N	Strobe	Clear	Output Enable	OUT_N	
				$t - 1$	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

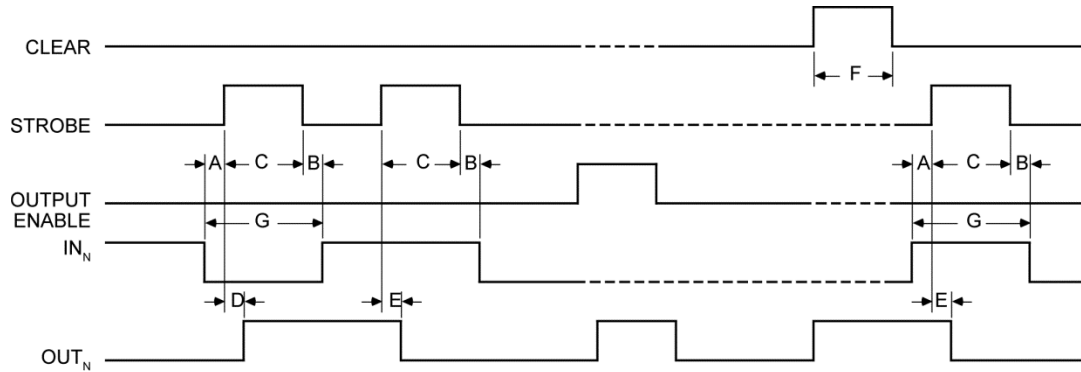
X = Irrelevant

$t - 1$ = Previous output state

t = Present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the Data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current shutdown is activated, the OUTPUT ENABLE must be pulsed high to restore operation. Over temperature faults are not latched and require no reset pulse.

Timing

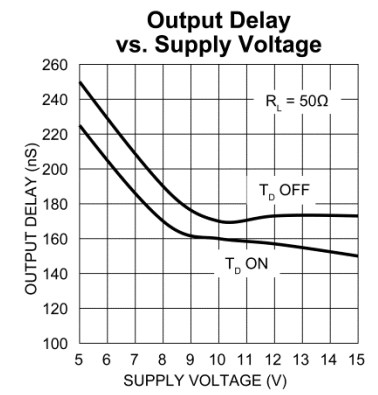
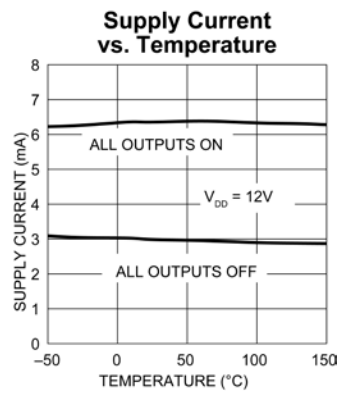
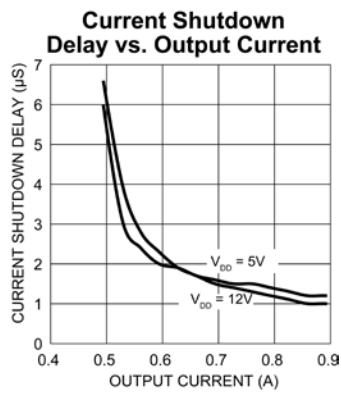
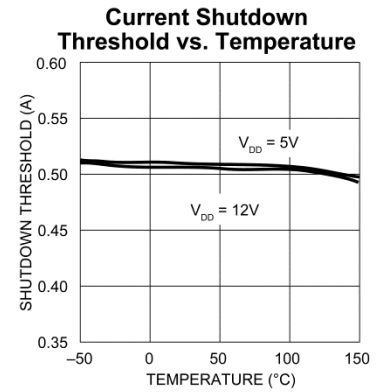
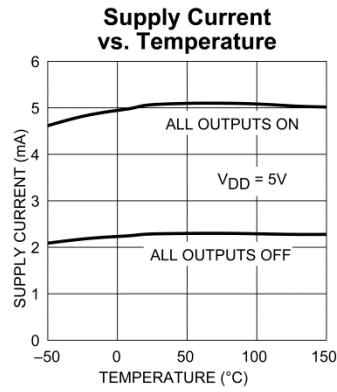
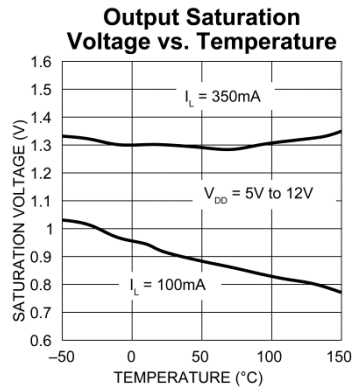


Timing Conditions

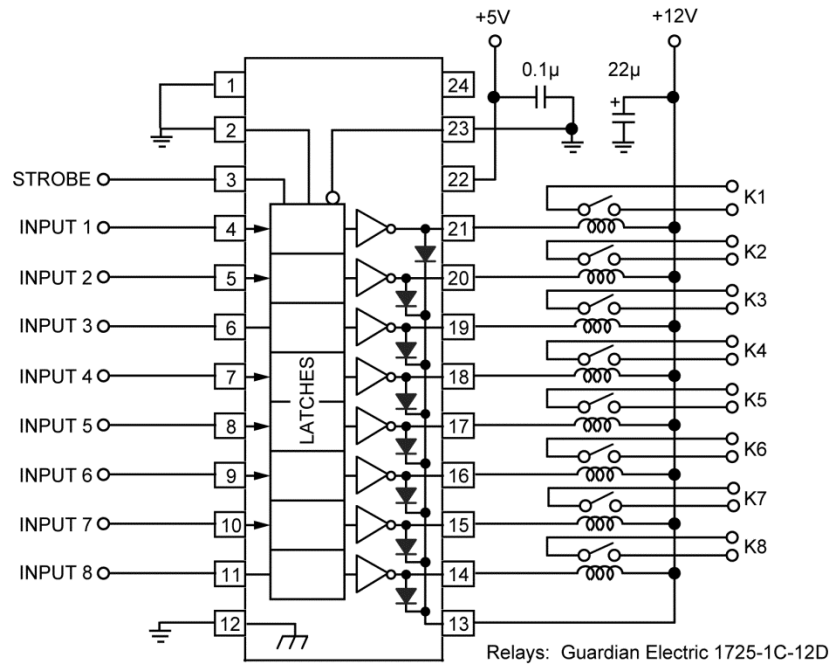
(T_A = +25°C, Logic Levels are V_{DD} and Ground, V_{DD} = 5V)

A. Minimum data active time before strobe enabled (data set-up time)	50ns
B. Minimum data active time after strobe disabled (data hold time)	50ns
C. Minimum strobe pulse width	125ns
D. Typical time between strobe activation and output on to off transition	500ns
E. Typical time between strobe activation and output off to on transition.....	500ns
F. Minimum clear pulse width	300ns
G. Minimum data pulse width	225ns

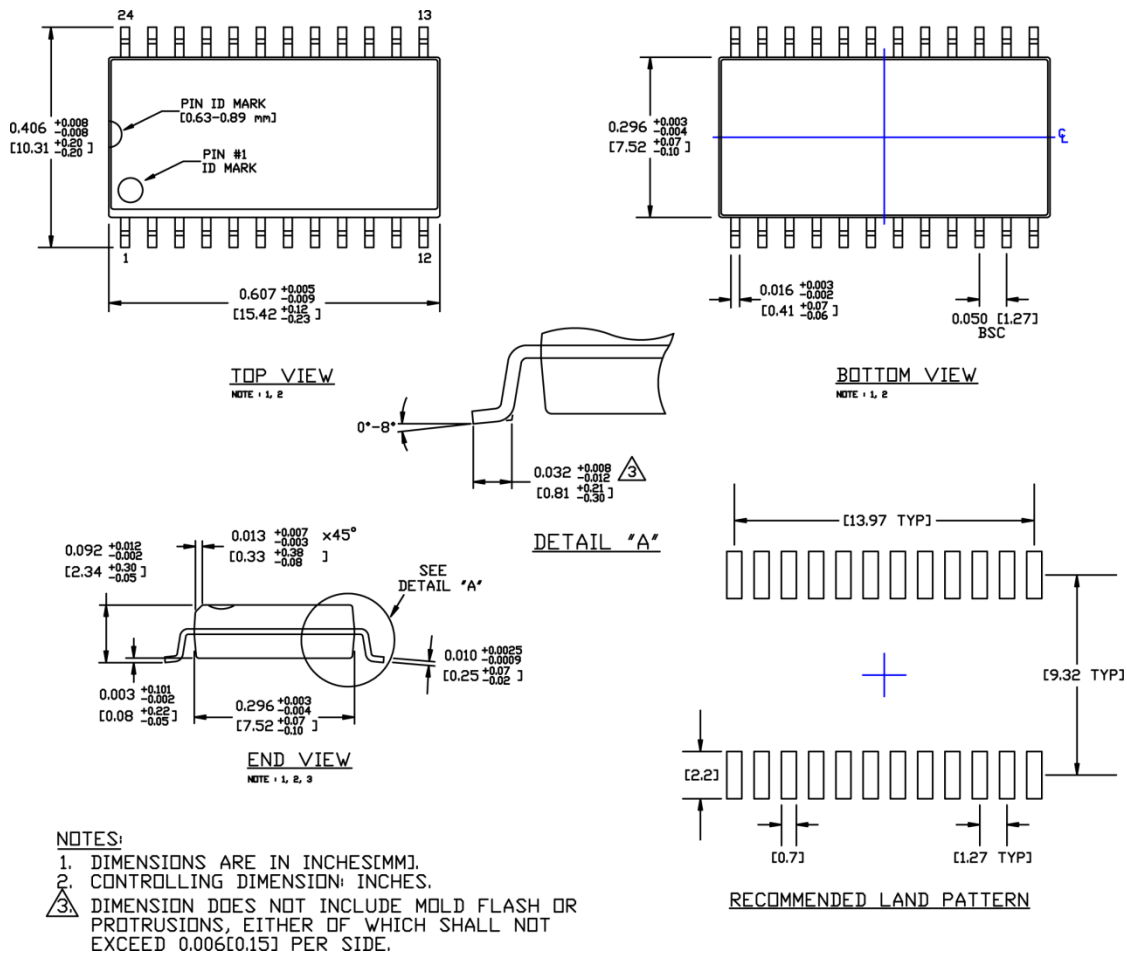
Typical Characteristics



Typical Application Schematic



Package Information and Recommended Landing Pattern⁽⁵⁾

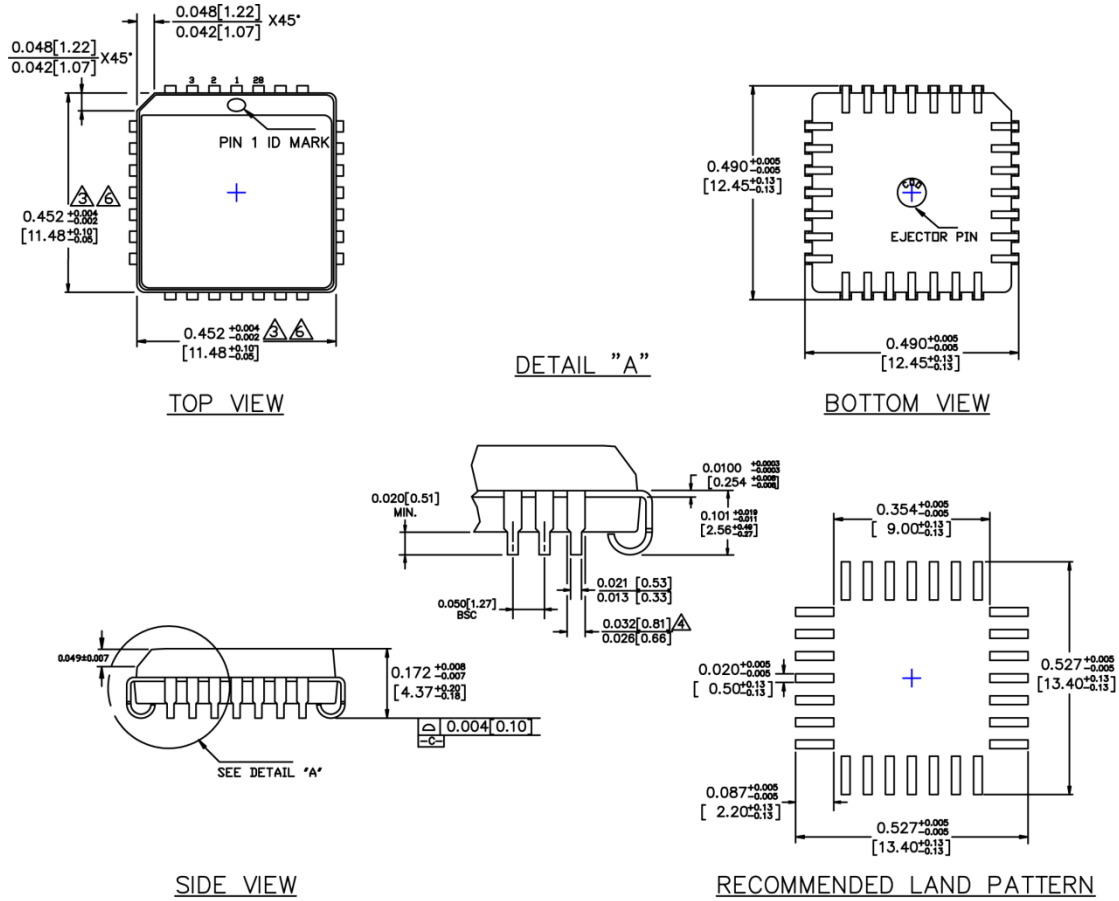


24-Pin Wide SOIC (WM)

Note:

7. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Landing Pattern⁽⁵⁾ (Continued)



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS : MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

28-Pin PLCC (V)

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