

## Features

- Supply Voltage: 2.7V to 5.5V
- Low Supply Current: typical 600µA per channel
- Rail to Rail Input and Output
- Bandwidth: typical 6 MHz
- Slew Rate: typical 4.5V/µs
- Excellent EMI Suppress Performance
- Offset Voltage: maximum ±3mV
- Offset Voltage Temperature Drift: typical 1 µV/°C
- Low Noise: typical 19 nV/√Hz at 1kHz
- High Output Capability: typical 100mA
- -40°C to 125°C Operation Temperature Range
- AEC-Q100 Qualification: TP1561AL1-S5TR-S, TP1562AL1-SO1R-S, TP1564AL1-SO2R-S

## Applications

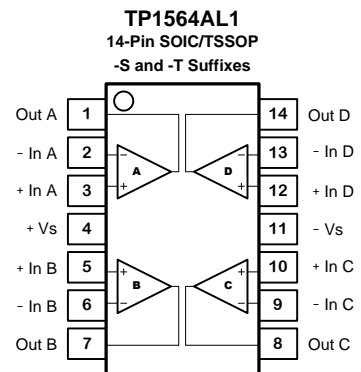
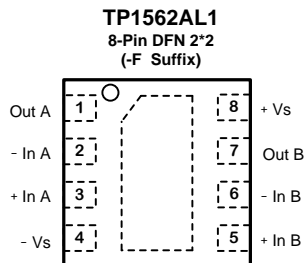
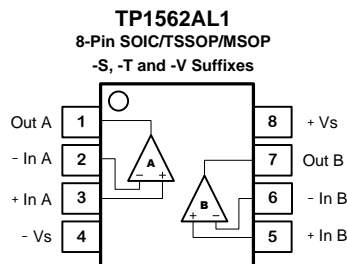
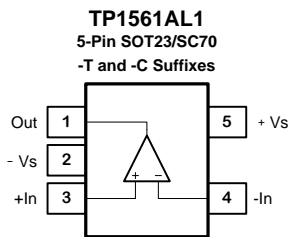
- White Goods
- Motor Control

## Description

The TP156XAL1 series are CMOS dual, and quad RRIO op-amps with low offset, low power and stable high frequency response. They incorporate 3PEAK's proprietary and patented design techniques to achieve very good AC performance with 6MHz bandwidth, 4.5V/µs slew rate and low distortion while drawing only 600µA of quiescent current per amplifier. The input common-mode voltage range extends 300mV beyond V<sub>-</sub> and V<sub>+</sub>, and the outputs swing rail-to-rail. The TP156XAL1 family can be used as plug-in replacements for many commercially available op-amps to reduce power and improve input/output range and performance.

The combination of features makes the TP156XAL1 ideal choices for motor control and portable audio amplification, sound ports, and other consumer Audio. The TP156XAL1 Op-amp is very stable, and it is capable of driving heavy capacitive loads such as those found in LCDs. The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

## Pin Configuration



The thermal pad of DFN package is recommended to be left float or connected to -Vs

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## Revision History

Date	Revision	Notes
2021/12/12	Rev.Pre.0	Pre-Release Version
2022/2/17	Rev.Pre.1	Update MSL Level
2022/3/10	Rev.Pre.2	Update MSL Level to MSL 1
2022/4/28	Rev.Pre.3	Correct some typo

**Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TP1561AL1-S5TR-S	-40 to 125°C	5-Pin SOT23	61S	MSL 1	Tape and Reel, 3000
TP1562AL1-SO1R-S	-40 to 125°C	8-Pin SOIC	1562S	MSL 1	Tape and Reel, 4000
TP1562AL1-VS1R-S	-40 to 125°C	8-Pin MSOP	1562S	MSL 1	Tape and Reel, 3000
TP1564AL1-SO2R-S	-40 to 125°C	14-Pin SOIC	1564S	MSL 1	Tape and Reel, 2500

## Absolute Maximum Ratings <sup>Note 1</sup>

Parameters	Rating
Supply Voltage, (+V <sub>S</sub> )– (-V <sub>S</sub> )	6.5 V
Input Voltage	(-V <sub>S</sub> ) – 0.3 to (+V <sub>S</sub> ) + 0.3
Differential Input Voltage	±7V
Input Current: +IN, –IN <sup>Note 2</sup>	±10mA
Output Short-Circuit Duration <sup>Note 3</sup>	Infinite
Maximum Junction Temperature	150°C
Operating Temperature Range	–40 to 125°C
Storage Temperature Range	–65 to 150°C
Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

## ESD Rating

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV

## Thermal Information

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-Pin SOT23	250	81	°C/W
8-Pin SOIC	158	43	°C/W
8-Pin MSOP	210	45	°C/W
14-Pin SOIC	120	36	°C/W

## Electrical Characteristics

All test condition is  $V_S = 5V$ ,  $T_A = 25^\circ C$ ,  $R_L = 2k\Omega$ ,  $C_L = 100pF$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Power Supply</b>						
$V_S$	Supply Voltage Range		2.7		5.5	V
$I_Q$	Quiescent Current per Amplifier			600	900	$\mu A$
		$T_A = -40^\circ C$ to $125^\circ C$			1200	$\mu A$
PSRR	Power Supply Rejection Ratio	$V_S = 2.7V$ to $5.5V$ , $V_{CM} = 0$	75	90		dB
		$V_S = 2.7V$ to $5.5V$ , $V_{CM} = 0$ , $T_A = -40^\circ C$ to $125^\circ C$	65			dB
<b>Input Characteristics</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 0V$ to $3V$	-3		3	mV
$V_{OS}$	Input Offset Voltage	$V_{CM} = 0V$ to $3V$ , $T_A = -40^\circ C$ to $125^\circ C$	-5		5	mV
$V_{OS\ TC}$	Input Offset Voltage Drift	$T_A = -40^\circ C$ to $125^\circ C$		1		$\mu V/^\circ C$
$I_B$	Input Bias Current	$T_A = 25^\circ C$	-200	1	200	$\mu A$
		$T_A = 125^\circ C$	-2000	25	2000	$\mu A$
$I_{OS}$	Input Offset Current			10		$\mu A$
$C_{IN}$	Input Capacitance	Differential Mode		8		pF
		Common Mode		7		pF
$A_V$	Open-loop Voltage Gain	$V_{OUT} = 0.1V$ to $4.9V$ , $R_{LOAD} = 100k\Omega$	80	100		dB
		$V_{OUT} = 0.1V$ to $4.9V$ , $R_{LOAD} = 100k\Omega$ , $T_A = -40^\circ C$ to $125^\circ C$	70			dB
$V_{CMR}$	Common-mode Input Voltage Range		(V-) - 0.1		(V+) + 0.1	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0V$ to $2.5V$	70	100		dB
		$V_{CM} = 0V$ to $2.5V$ , $T_A = -40^\circ C$ to $125^\circ C$	60			dB
Xtalk	Channel Separation	$f = 1kHz$ , $R_L = 2k\Omega$		110		dB
<b>Output Characteristics</b>						
	Maximum Output Voltage Swing	$R_{LOAD} = 10k\Omega$		3	15	mV
		$R_{LOAD} = 10k\Omega$ , $T_A = -40^\circ C$ to $125^\circ C$			30	mV
$I_{SC}$	Output Short-Circuit Current		90	100		mA
		$T_A = -40^\circ C$ to $125^\circ C$	50			mA
<b>AC Specifications</b>						
GBW	Gain-Bandwidth Product			6		MHz
SR	Slew Rate	$A_V = 1$ , $V_{OUT} = 1.5V$ to $3.5V$ , $C_{LOAD} = 60pF$ , $R_{LOAD} = 1k\Omega$		4.5		V/ $\mu s$
$t_s$	Settling Time, 0.1%	$A_V = 1$ , $2V$ Step, $C_{LOAD} = 60pF$ ,		0.8		$\mu s$

	Settling Time, 0.01%	$R_{LOAD} = 1k\Omega$		1		$\mu s$
PM	Phase Margin	$R_{LOAD} = 1k\Omega, C_{LOAD} = 60pF$		60		$^{\circ}$
GM	Gain Margin	$R_{LOAD} = 1k\Omega, C_{LOAD} = 60pF$		15		dB
Noise Performance						
$E_N$	Input Voltage Noise	$f = 0.1Hz \text{ to } 10Hz$		8		$\mu V_{PP}$
$e_N$	Input Voltage Noise Density	$f = 1kHz$		19		nV/ $\sqrt{Hz}$
$i_N$	Input Current Noise	$f = 1kHz$		2		fA/ $\sqrt{Hz}$

## Typical Performance Characteristics

V<sub>s</sub> = 5V, V<sub>CM</sub> = 2.5V, R<sub>L</sub> = Open, unless otherwise specified.

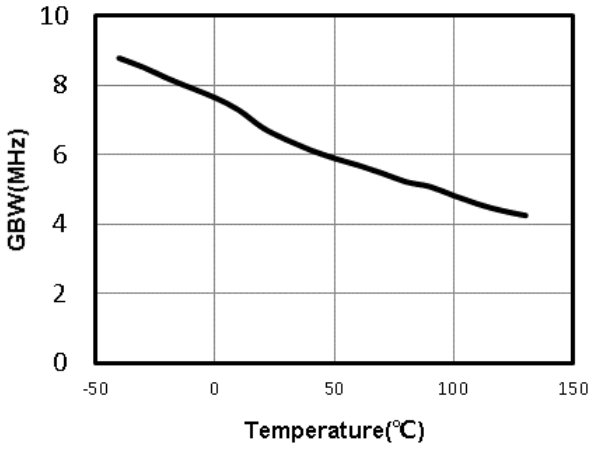


Figure 1. Unity Gain Bandwidth vs. Temperature

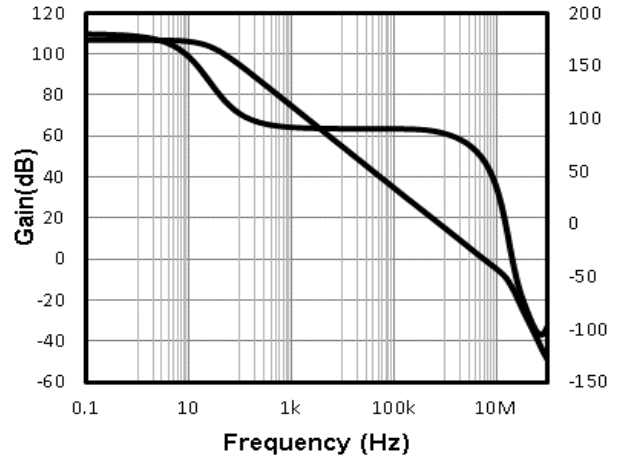


Figure 2. Open-Loop Gain and Phase

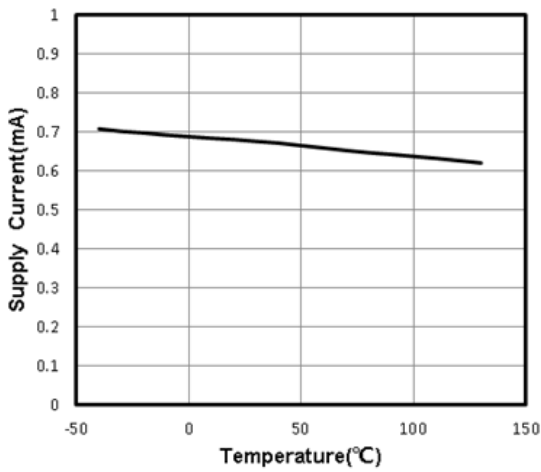


Figure 3. Supply Current vs. Temperature

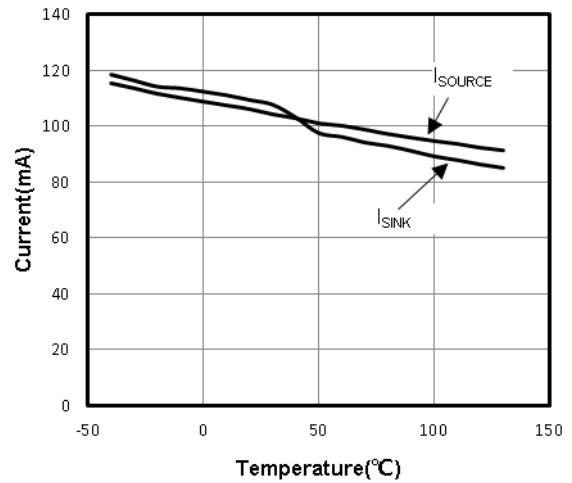


Figure 4. Short Circuit Current vs. Temperature

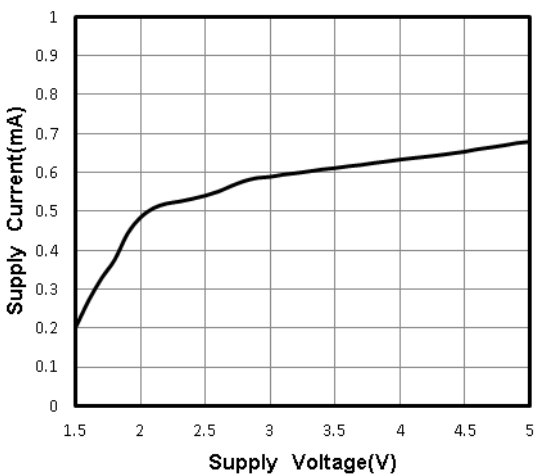


Figure 5. Quiescent Current vs. Supply Voltage

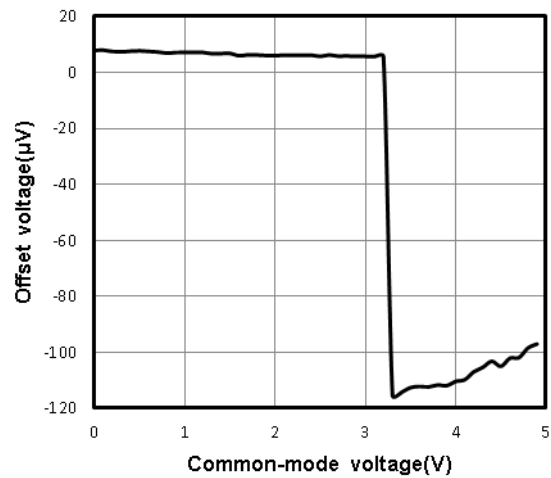


Figure 6. Offset Voltage vs. Common-Mode Voltage

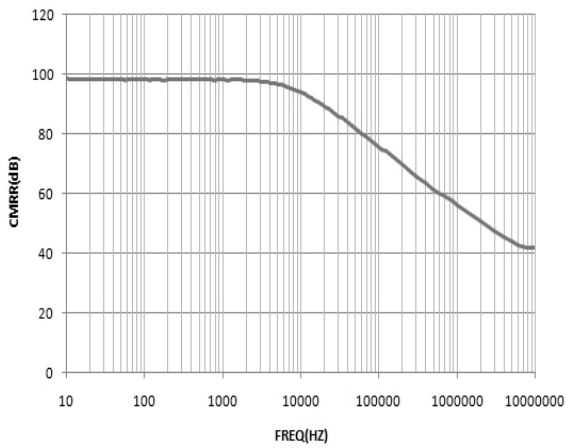


Figure 7. CMRR vs. Frequency

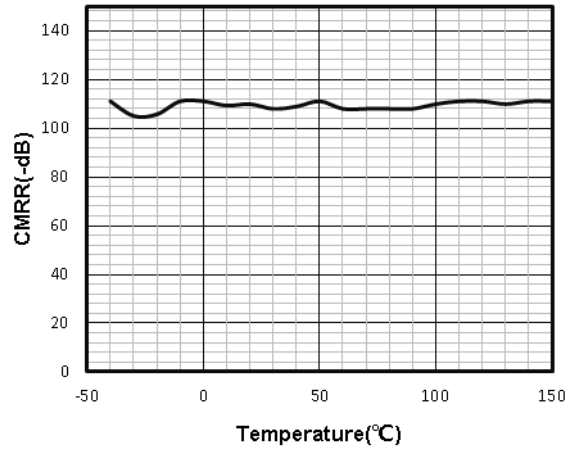


Figure 8. CMRR vs. Temperature

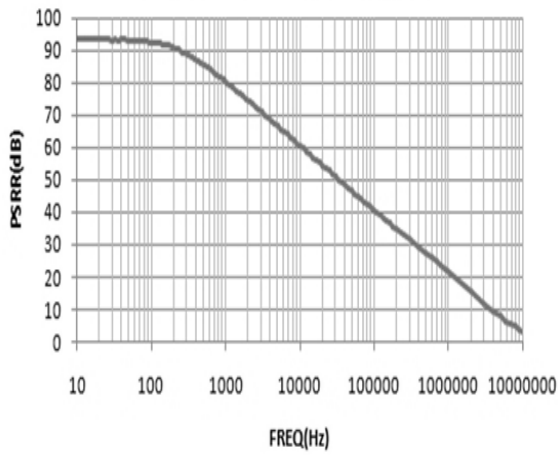


Figure 9. PSRR vs. Frequency

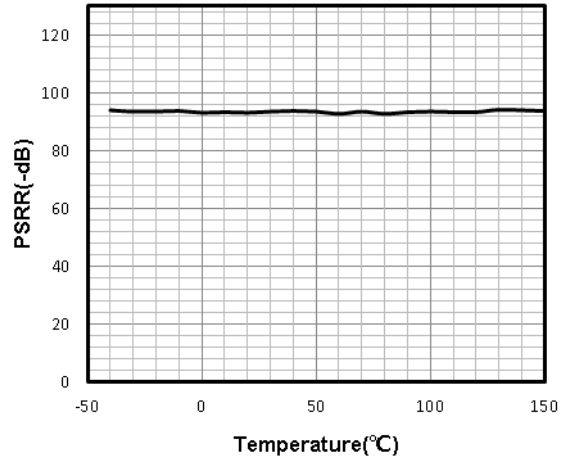


Figure 10. PSRR vs. Temperature

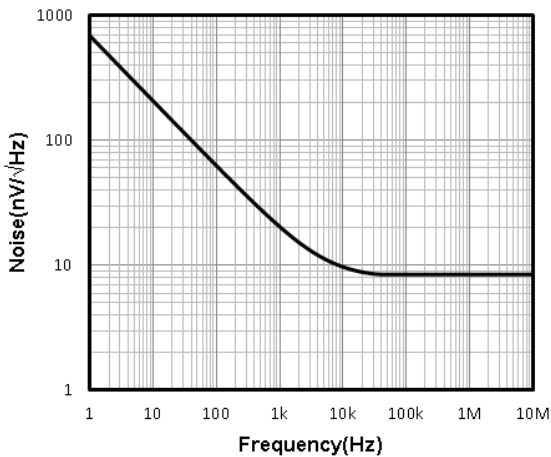


Figure 11. Input Voltage Noise Spectral Density

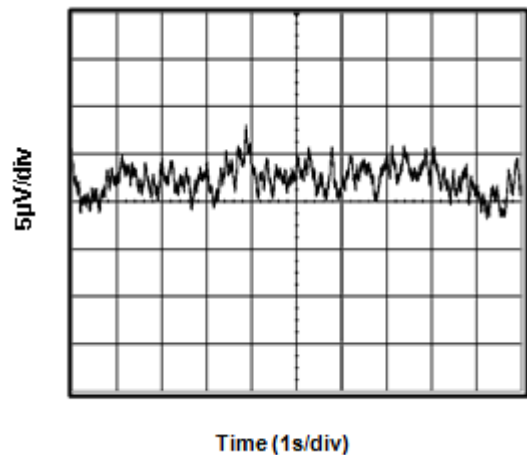


Figure 12. 0.1 Hz to 10 Hz Input Voltage Noise



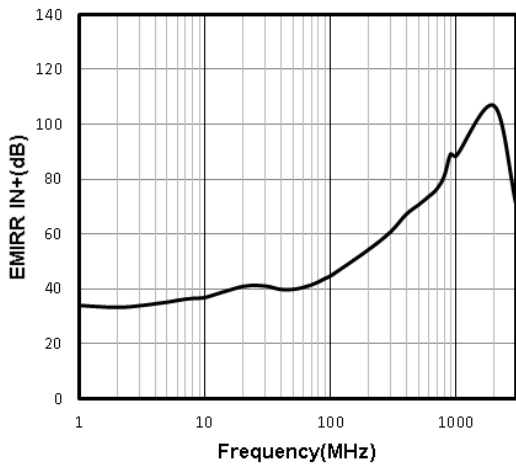
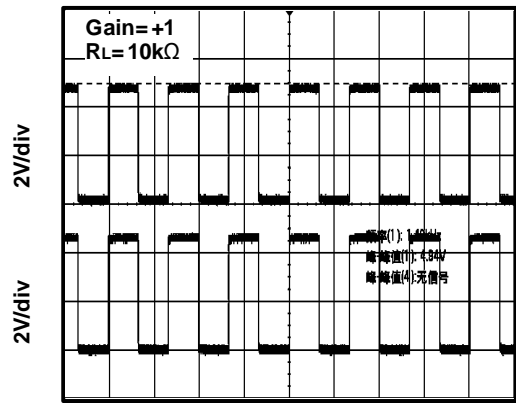
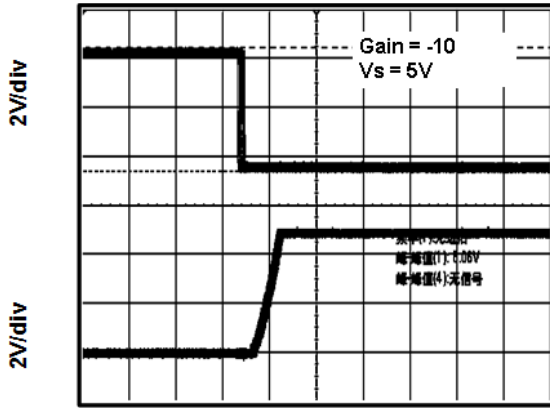


Figure 13. EMIRR IN+ vs. Frequency



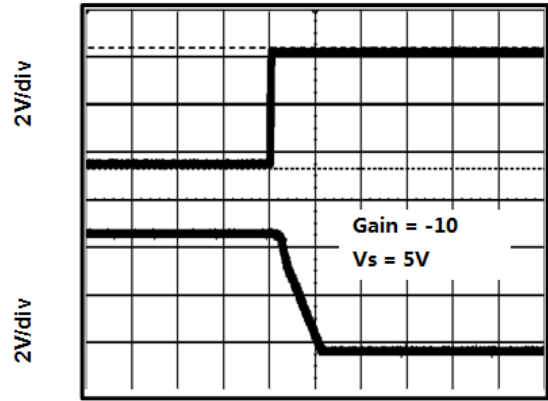
Time (500 $\mu$ s/div)

Figure 14. Large-Scale Step Response



Time (2 $\mu$ s/div)

Figure 15. Negative Over-Voltage Recovery



Time (1 $\mu$ s/div)

Figure 16. Positive Over-Voltage Recovery

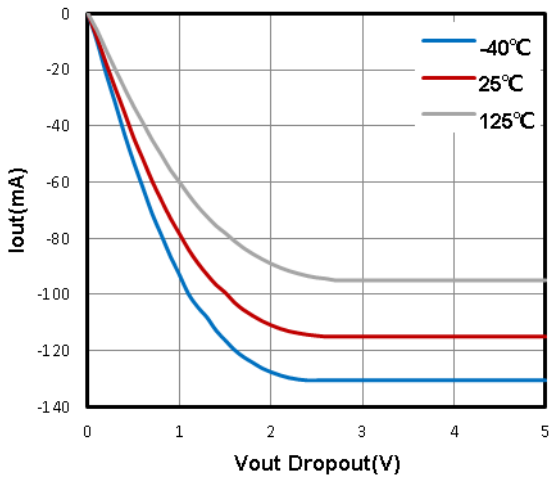


Figure 17. Negative Output Swing vs. Load Current

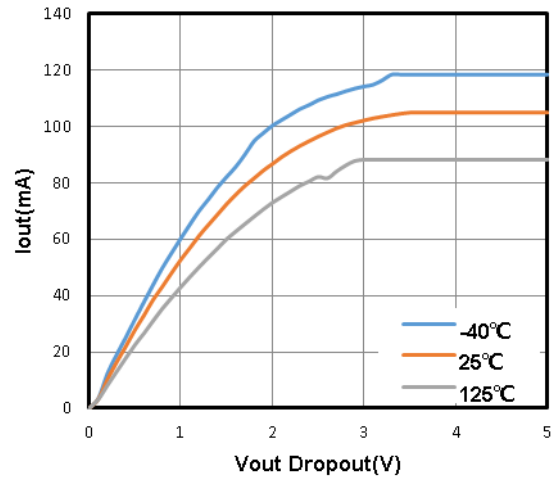


Figure 18. Positive Output Swing vs. Load Current

## Application Information

### Low Supply Voltage and Low Power Consumption

The TP156XAL1 family of operational amplifiers can operate with power supply voltages from 2.7 V to 5.5 V. Each amplifier draws only 600  $\mu$ A quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding high capacitive load driving capability and stable wide bandwidth. The TP156XAL1 family is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable for any capacitive load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

### Ground Sensing and Rail to Rail Output

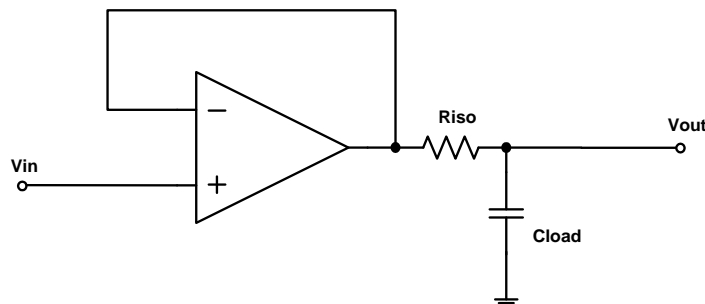
The TP156XAL1 family has excellent output drive capability, delivering over 100 mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300 mV beyond either rail, the op-amp can easily perform ‘true ground’ sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

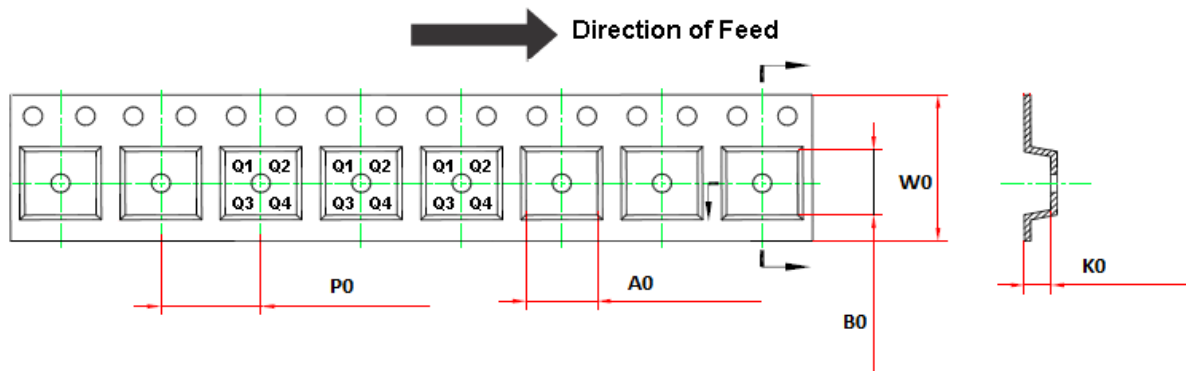
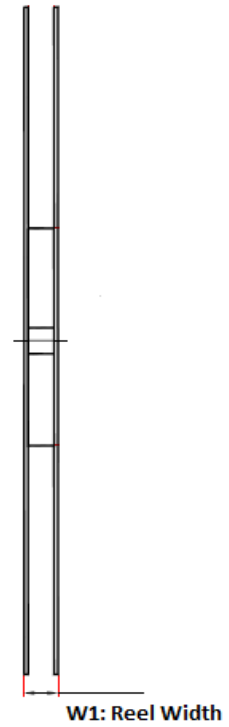
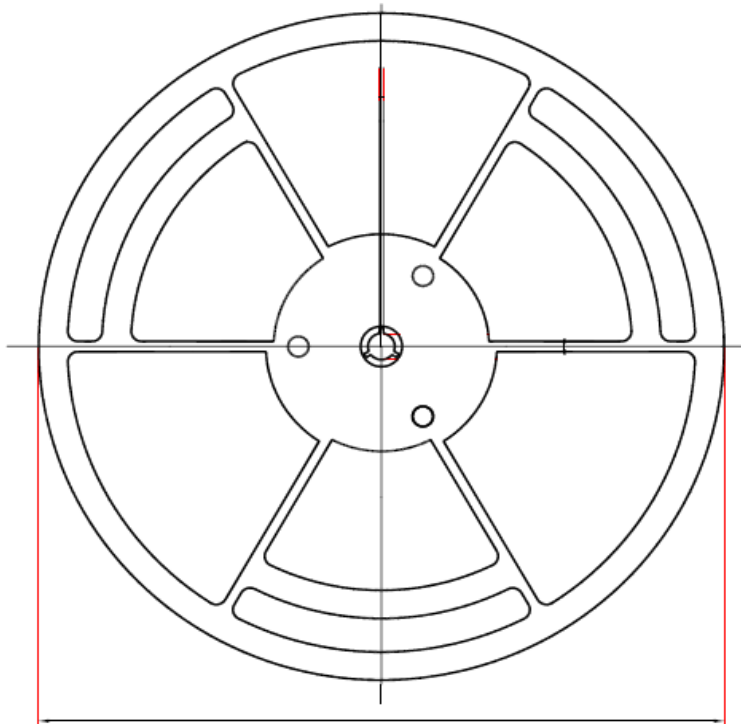
### Driving Large Capacitive Load

The TP156XAL1 family of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for “Phase Margin vs. Load Capacitance”. As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop’s phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer ( $G = +1V/V$ ) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP156XAL1 OPA family (e.g., > 200 pF when  $G = +1V/V$ ), a small series resistor at the output (RISO in Figure 3) improves the feedback loop’s phase margin and stability by making the output load resistive at higher frequencies.



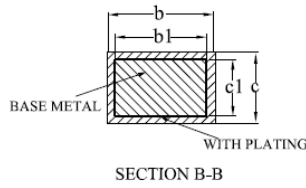
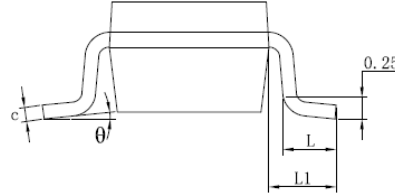
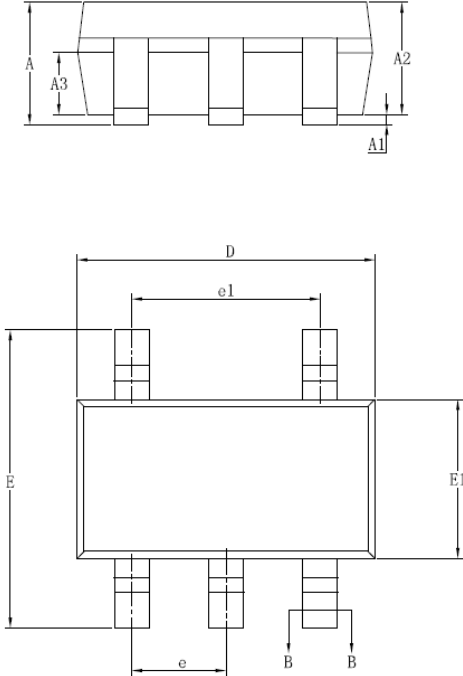
Tape and Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TP1561AL1-S5TR-S	5-Pin SOT23	180.0	13.1	3.2	3.2	1.4	4.0	8.0	Q3
TP1562AL1-SO1R-S	8-Pin SOIC	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TP1562AL1-VS1R-S	8-Pin MSOP	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
TP1564AL1-SO2R-S	14-Pin SOIC	330.0	21.6	6.5	9.0	2.1	8.0	16.0	Q1

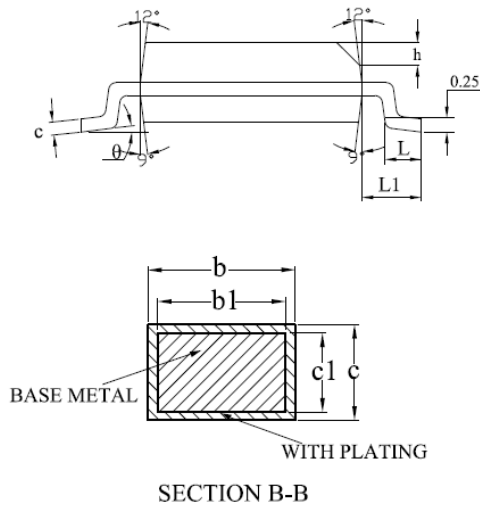
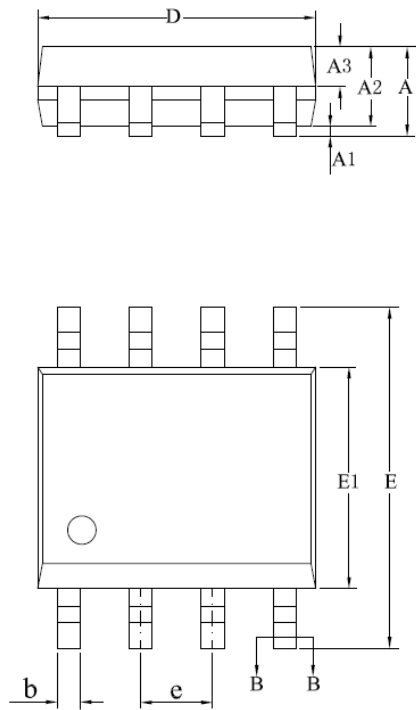
Package Outline Dimensions

SOT23-5



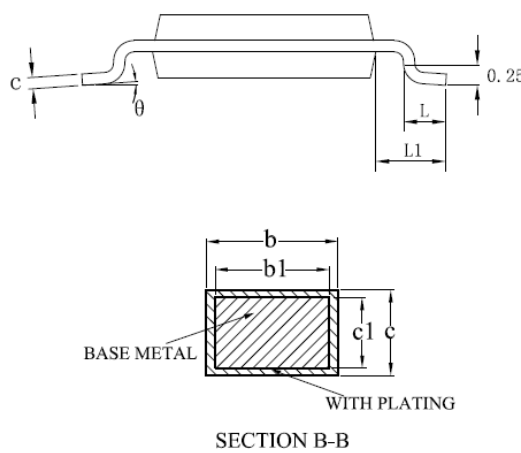
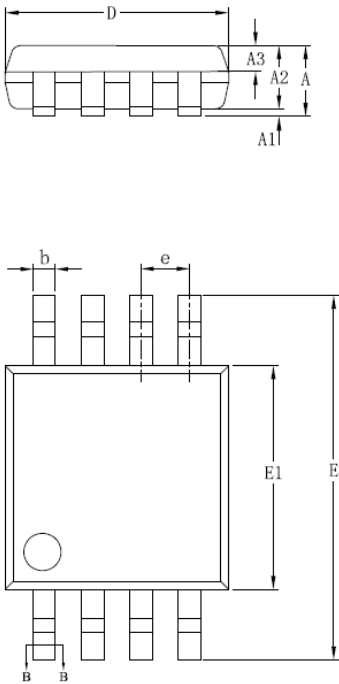
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.25
A1	0.04	—	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
e1	1.90BSC		
L	0.30	—	0.60
L1	0.60REF		
θ	0	—	8°

## SOIC-8



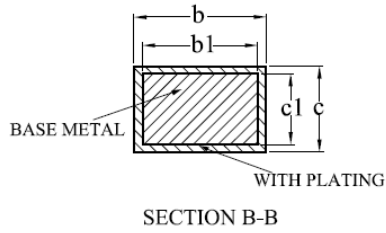
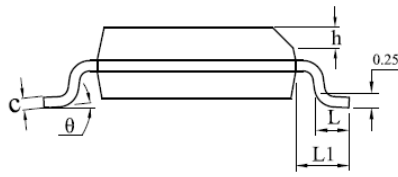
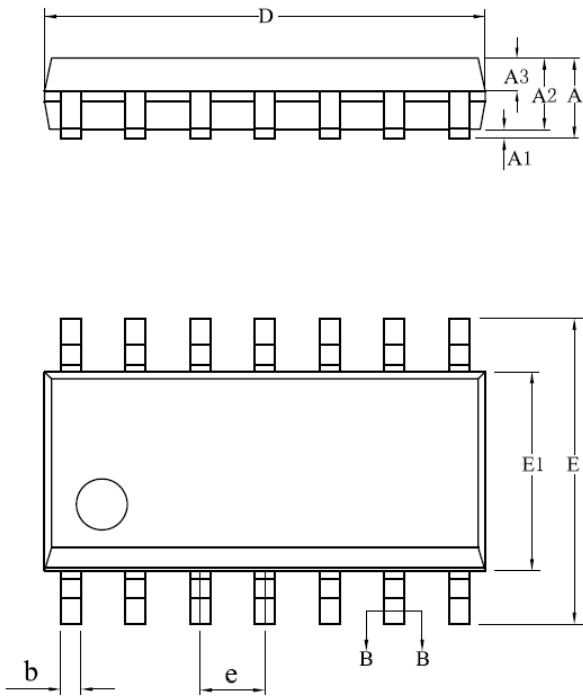
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

## MSOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

SOIC-14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

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[430227FB](#) [UPC451G2-A](#) [UPC824G2-A](#) [LT1678IS8](#) [UPC258G2-A](#) [NCV33202DMR2G](#) [NJM324E](#) [NTE925](#) [AZV358MTR-G1](#)  
[AP4310AUMTR-AG1](#) [AZV358MMTR-G1](#) [SCY33178DR2G](#) [NCV5652MUTWG](#) [NCV20034DR2G](#) [NTE778S](#) [NTE871](#) [NTE937](#)  
[MCP6V16UT-E/OT](#) [SCY6358ADR2G](#) [UPC4570G2-E1-A](#) [NCS20282FCTTAG](#) [UPC834G2-E1-A](#) [UPC1458G2-E2-A](#) [UPC813G2-E2-A](#)  
[UPC458G2-E1-A](#) [UPC824G2-E2-A](#) [UPC4574G2-E2-A](#) [UPC4558G2-E2-A](#) [UPC4560G2-E1-A](#) [UPC4062G2-E1-A](#) [UPC258G2-E1-A](#)  
[UPC4742GR-9LG-E1-A](#) [UPC4742G2-E1-A](#) [UPC832G2-E2-A](#) [UPC842G2-E1-A](#) [UPC802G2-E1-A](#) [UPC4741G2-E2-A](#) [UPC4572G2-E2-A](#)  
[UPC844GR-9LG-E2-A](#) [UPC259G2-E1-A](#) [UPC4741G2-E1-A](#) [UPC4558G2-E1-A](#) [UPC4574GR-9LG-E1-A](#) [UPC1251GR-9LG-E1-A](#)  
[UPC4744G2-E1-A](#) [UPC4092G2-E1-A](#) [UPC4574G2-E1-A](#) [UPC4062G2-E2-A](#) [UPC451G2-E2-A](#) [UPC832G2-E1-A](#)