Features

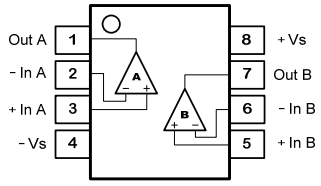
- **Ultra-low Distortion: 0.0001% at 1 kHz**
- **Low Noise: 17 nV/√Hz**
- **High Slew Rate: 6.5 V/μs**
- **Wide Bandwidth: 10 MHz**
- **Low Supply Current: 1.2mA per Amplifier**
- **Wide Supply Range: 2.7 V to 36 V, or Dual-Supply ±1.35 V to ±18 V**
- **Low Input Offset Voltage: 0.5 mV Typical**
- **Low V_{OS} TC: 2.0 μV/°C**
- **Low Input Bias Current: 0.04 pA Typical**
- **Rail-to-Rail Output Voltage Range**
- **Unity Gain Stable for 220pF Capacitive Load**
- **Drive 600 Ω Load**
- **–40°C to 125°C Operation Range**
- **Green, Popular Type Package**

Applications

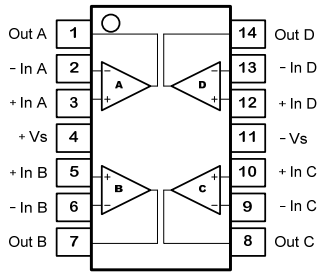
- Professional Audio Equipments
- Line Drivers or Line Receivers
- Pre-amplification and Filtering
- PCM DAC I/V Converter
- Transducer Amplifier
- Data Acquisition

Pin Configuration (Top View)

TP2604
8-Pin SOIC/MSOP
(-S and -V Suffixes)



TP2608
14-Pin SOIC/TSSOP
(-S and -T Suffixes)



Description

The TP2604/2608 are ultra-low distortion, high-voltage CMOS op-amps featuring THD+N of 0.0001% at 1kHz. This feature along with its low noise, very high PSRR makes TP260x ideal choices for professional audio equipments.

The TP2604/2608 are unity gain stable with 220pF capacitive load with a wide 10MHz bandwidth, 6.5V/μs high slew rate, which makes the device appropriate for current-to-voltage converters.

The TP2604/2608 can operate from a single-supply voltage of +2.7V to +36.0V or a dual-supply voltage of ±1.35V to ±18.0V. Rail-to-rail output characteristics allow the full power-supply voltage to be used for signal range.

The TP2604 is dual channel version available in 8-pin SOIC and MSOP package. The TP2608 is quad channel version available in 14-pin SOIC and TSSOP package.

Related 36V RRO Op-amps

Supply Voltage	Single 2.7V to 36V or Dual ±1.35V to ±18V		
Supply Current	125 μA	350 μA	1.2 mA
GBWP	1.5 MHz	3 MHz	10 MHz
Slew Rate	0.8 V/μs	3 V/μs	6.5 V/μs
Dual	**TP2614**	**TP2634**	**TP2604**
Quad	**TP2618**	**TP2638**	**TP2608**

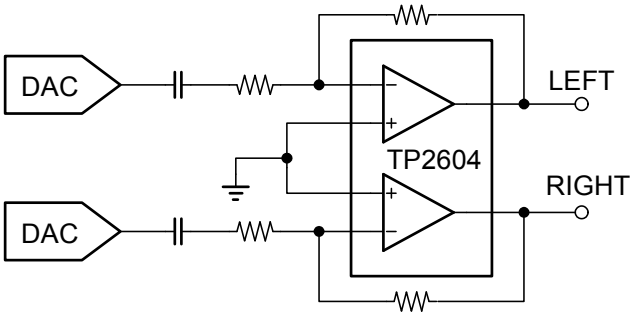


Figure 1. TP2604 in Audio Equipment

Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP2604	TP2604-SR	8-Pin SOIC	Tape and Reel, 4,000	2604S
	TP2604-VR	8-Pin MSOP	Tape and Reel, 3,000	2604V
TP2608	TP2608-SR	14-Pin SOIC	Tape and Reel, 2,500	2608S
	TP2608-TR	14-Pin TSSOP	Tape and Reel, 3,000	2608T

Note (1): 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ - V^-$.....48.0V
Input Voltage..... V^- – 0.3 to V^+ + 0.3
Input Current: +IN, –IN Note 2..... ±20mA
Output Current: OUT..... ±25mA
Output Short-Circuit Duration Note 3..... Indefinite
Current at Supply Pins……..... ±60mA
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	3	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Electrical Characteristics

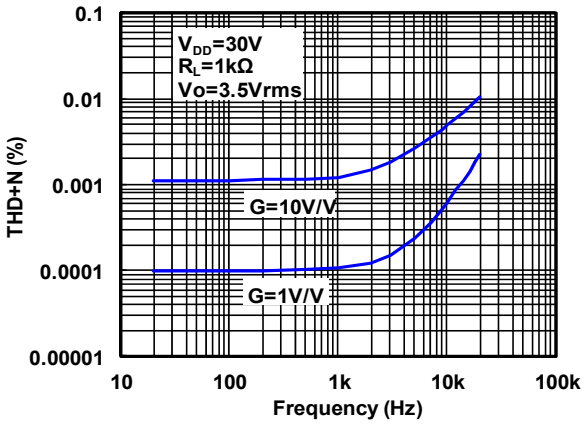
The specifications are at T_A = 27°C. V_{SUPPLY} = ±15V, V_{CM} = V_{OUT} =0V, R_L = 100kΩ, C_L =100pF.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V_{DD}/2	-4.0	±0.5	+4.0	mV
V_{OS} TC	Input Offset Voltage Drift	-40°C to 125°C		2.0		μV/°C
I_B	Input Bias Current	T_A = 27 °C		0.04		pA
		T_A = 85 °C		100		pA
		T_A = 125 °C		5.7		nA
I_{OS}	Input Offset Current			0.001		pA
V_N	Input Voltage Noise	f = 0.1Hz to 10Hz		3.2		μV_{RMS}
		f = 20Hz to 20kHz		2.0		μV_{RMS}
e_N	Input Voltage Noise Density	f = 1kHz		17		nV/√Hz
C_{IN}	Input Capacitance	Differential Common Mode		2.9 5		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = -14.6V to 13V		126		dB
V_{CM}	Common-mode Input Voltage Range		V^-		V^+-2.0	V
PSRR	Power Supply Rejection Ratio			130		dB
A_{VOL}	Open-Loop Large Signal Gain	V_{OUT} = 0V, R_{LOAD} = 100kΩ	110	130		dB
		V_{OUT} = -14.9V to 14.9V, R_{LOAD} = 100kΩ	110	130		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 100kΩ		50		mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f = 1kHz, I_{OUT} = 0		0.01		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, I_{OUT} = 0		125		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current		25		mA
V_{DD}	Supply Voltage		2.7		36	V
I_Q	Quiescent Current per Amplifier			1.2		mA
PM	Phase Margin	R_{LOAD} = 100kΩ, C_{LOAD} = 100pF		56		°
GM	Gain Margin	R_{LOAD} = 100kΩ, C_{LOAD} = 100pF		8		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		10		MHz
SR	Slew Rate	A_V = 1, V_{OUT} = 0V to 10V, C_{LOAD} = 100pF, R_{LOAD} = 100kΩ		6.5		V/μs
FPBW	Full Power Bandwidth Note 1			70		kHz
t_S	Settling Time, 0.1% Settling Time, 0.01%	A_V = –1, 10V Step		1.5 1.6		μs
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, A_V =1, R_L = 1kΩ, V_{OUT} = 3.5V_{RMS}		0.0001		%
X_{talk}	Channel Separation	f = 1kHz, R_L = 1kΩ		110		dB

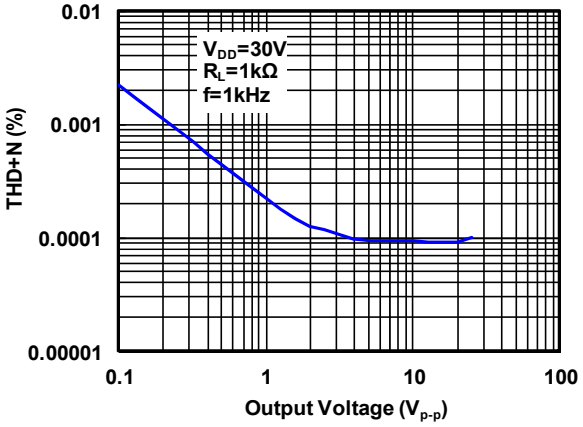
Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • VP-P

Typical Performance Characteristics

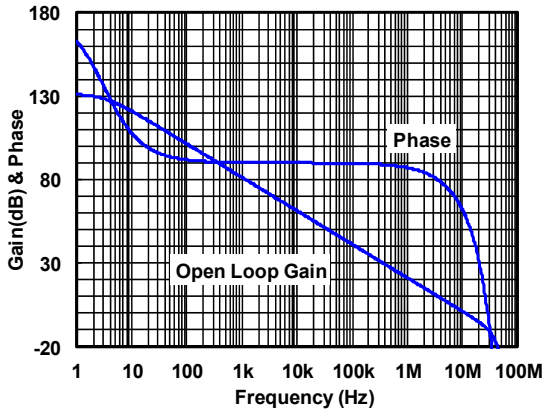
Total Harmonic Distortion + Noise vs. Frequency



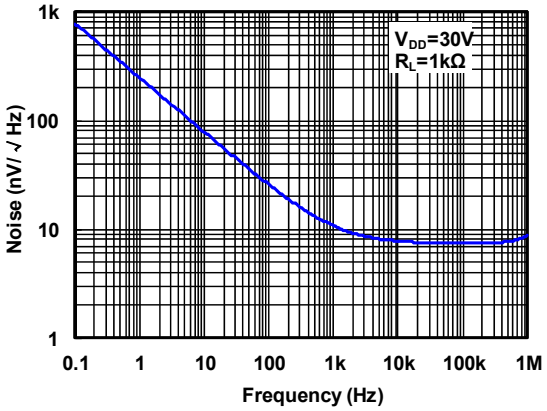
Total Harmonic Distortion + Noise vs. Output Voltage



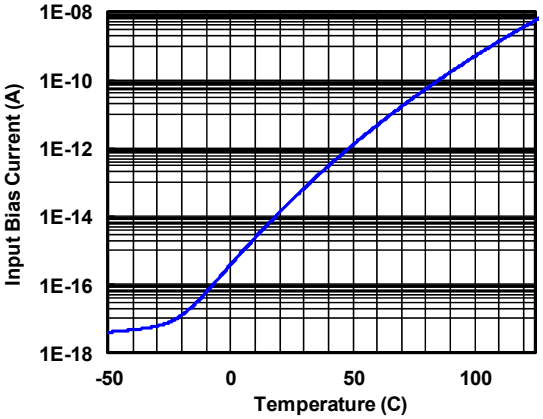
Open-Loop Gain and Phase



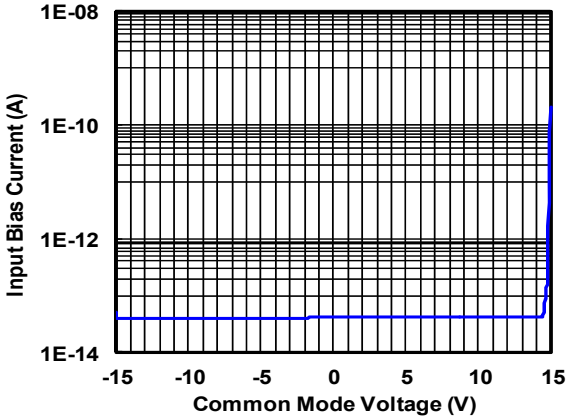
Input Voltage Noise Spectral Density



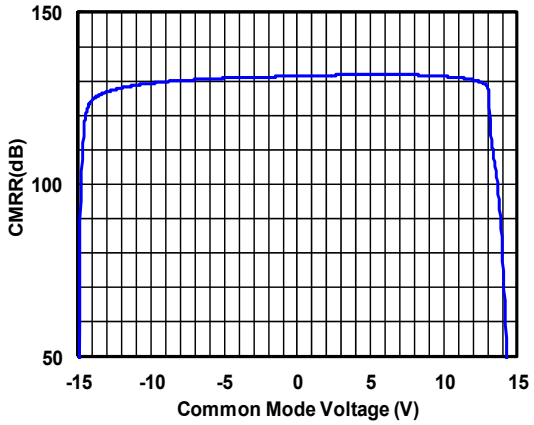
Input Bias Current vs. Temperature



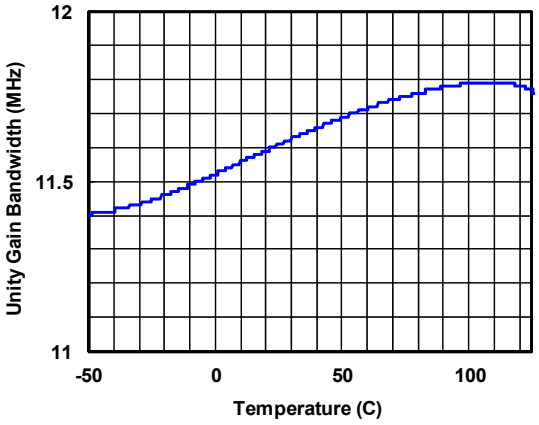
Input Bias Current vs. Input Common Mode Voltage



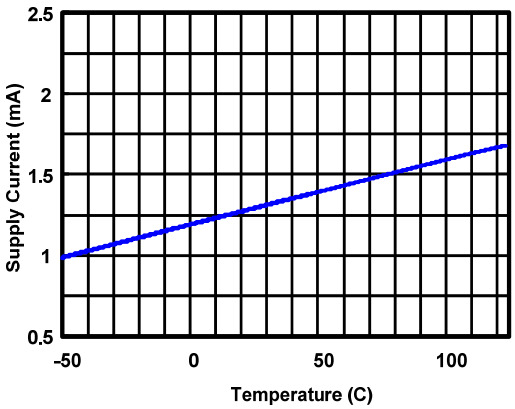
Common Mode Rejection Ratio



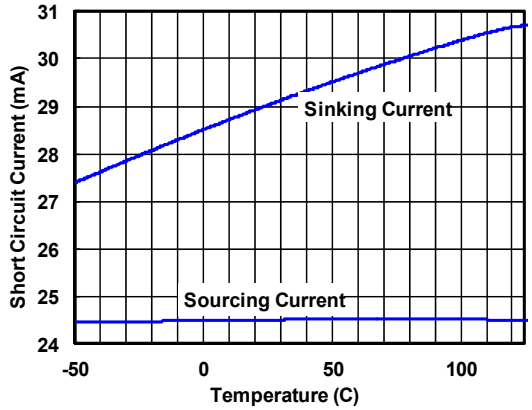
Unity Gain Bandwidth vs. Temperature



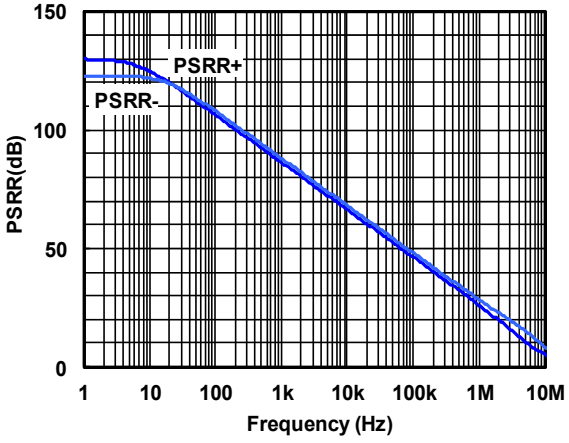
Quiescent Current vs. Temperature



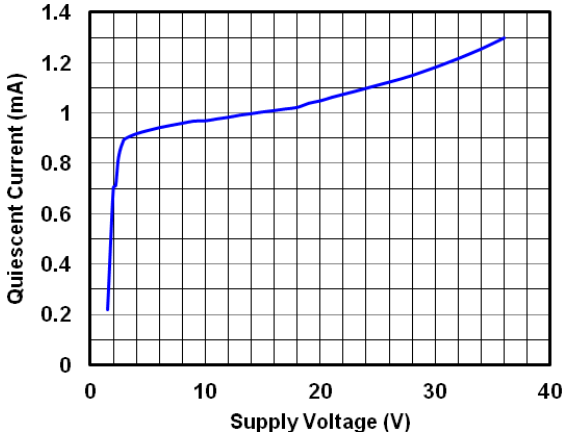
Short Circuit Current vs. Temperature



Power-Supply Rejection Ratio



Quiescent Current vs. Supply Voltage



Pin Functions

-IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- to (V^+ - 2.0V).

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

OUT: Amplifier Output. The voltage range extends to within milli-volts of each supply rail.

V+ or $+V_S$: Positive Power Supply. Typically the voltage is from 2.7V to 36V. Split supplies are possible as long as the voltage between V+ and V– is between 2.7V and 36V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^- or ^-V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.7V to 36V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

Operation

The TP2604 and TP2608 have input signal range from V^- to (V^+ – 2.0V). The output can extend all the way to the supply rails. The input stage is comprised of a PMOS differential amplifier for best noise and THD performance. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

Wide Supply Voltage

The TP2604/2608 operational amplifiers can operate with power supply voltages from 2.7V to 36V. Each amplifier draws 1.2mA quiescent current at 30V supply voltage. The TP2604/2608 is optimized for wide bandwidth low power applications. They have an industry leading high GBW to power ratio and the GBW remains nearly constant over specified temperature range.

Low Input Referred Noise

The TP2604/2608 provides a low input referred noise density of 17nV/ √Hz at 1kHz. The voltage noise will grow slowly with the frequency in wideband range, and the input voltage noise is typically 2.0µV_{RMS} at the frequency of 20Hz to 20kHz.

Ultra Low Distortion

The TP2604/2608 has an ultra low distortion of less than 0.0001% at 1kHz. Along with its low voltage noise, TP2604/2608 is ideal for high-fidelity audio signal amplification or filtering.

Low Input Bias Current

The TP2604/2608 is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP2604/2608 OPA’s input bias current at +27°C (±1pA, typical). It is recommended to use multi-layer PCB layout and route the OPA’s -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 2 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

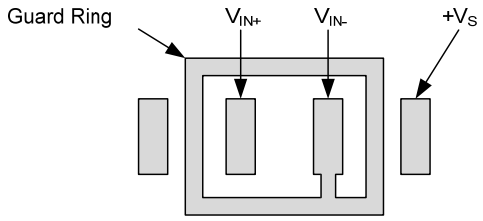


Figure 2 The Layout of Guard Ring

Ground Sensing and Rail to Rail Output

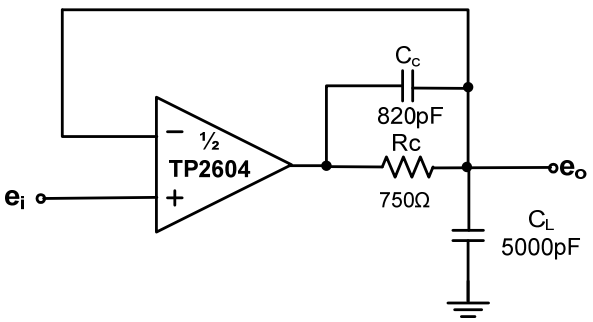
The TP2604/2608 family has excellent output drive capability. It drives 600Ω load directly with good THD performance. The output stage is a rail-to-rail topology that is capable of swinging to within 50mV of either rail.

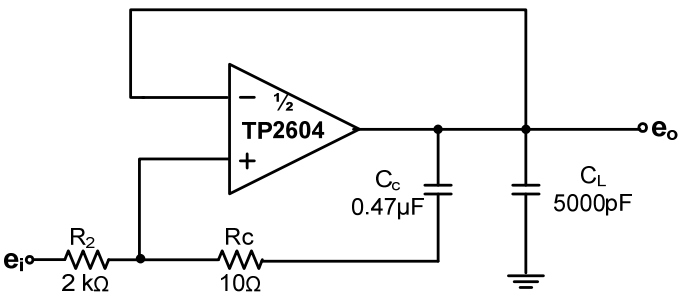
The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

Driving Large Capacitive Load

The TP2604/2608 op-amp family is designed to drive large capacitive loads. As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

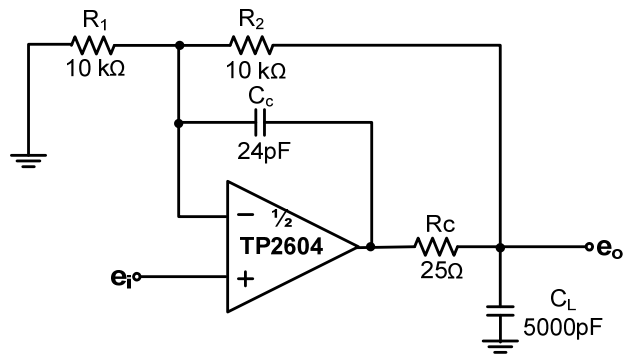
When driving large capacitive loads with the TP2604/2608 op-amp family (e.g., > 1,000 pF), different compensation schemes (Figure 3) improve the feedback loop's phase margin and stability.



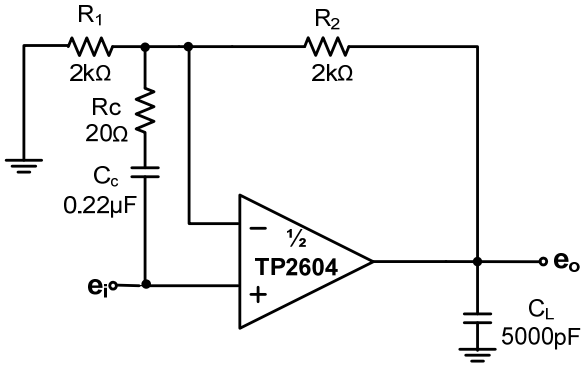


$$C_C = \sqrt{120 \times 10^{-12} C_L}$$

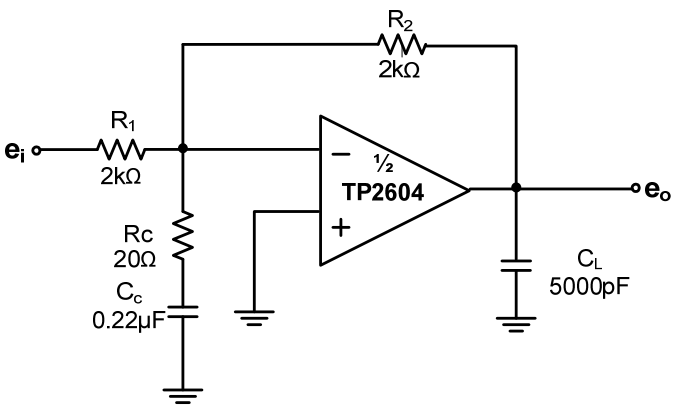
$$R_C = \frac{R_2}{4C_L \times 10^{-10} - 1} \qquad C_C = \frac{C_L \times 10^3}{R_C}$$



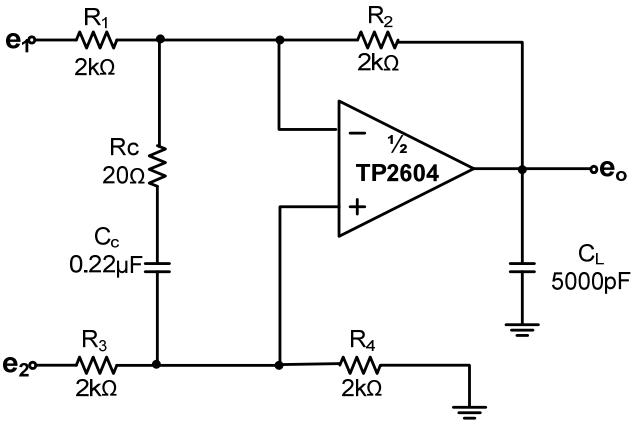
$$C_C = \frac{50}{R_2} C_L$$



$$R_C = \frac{R_2}{2C_L \times 10^{10} - (1 + R_2/R_1)} \qquad C_C = \frac{C_L \times 10^3}{R_C}$$



$$R_C = \frac{R_2}{2C_L \times 10^{10} - (1 + R_2/R_1)} \qquad C_C = \frac{C_L \times 10^3}{R_C}$$



$$R_C = \frac{R_2}{2C_L \times 10^{10} - (1 + R_2/R_1)} \qquad C_C = \frac{C_L \times 10^3}{R_C}$$

NOTE : Design equations and component values are approximate, User adjustment is required for optimum performance.

Figure 3 Driving Large Capacitive Loads

Power Supply Layout and Bypass

The TP2604/2608 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

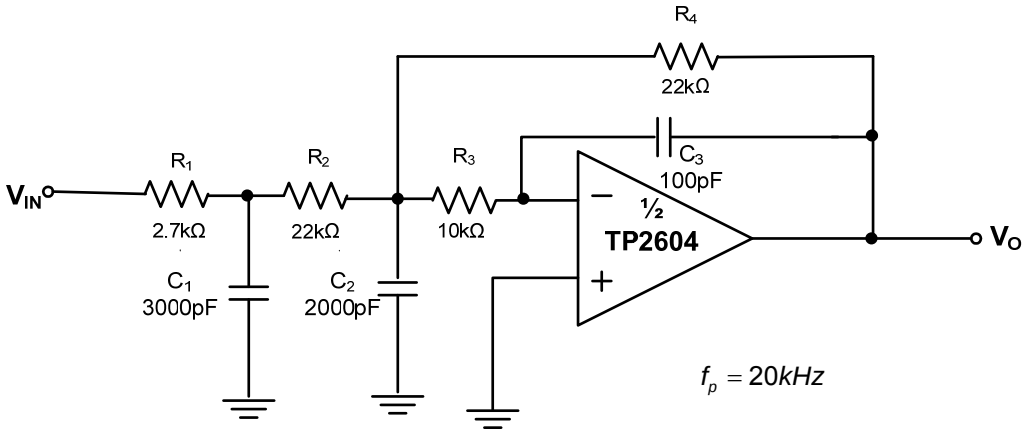
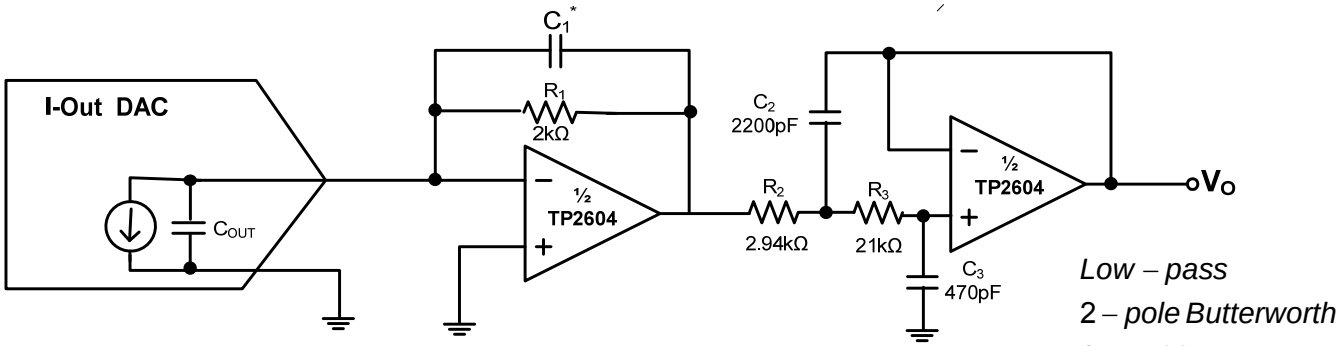


Figure 4 Three-Pole Low-Pass Filter

DAC I/V Amplifier and Low-Pass Filter



$$C_1^* = \sqrt{\frac{C_{OUT}}{2\pi R_1 f_c}}$$

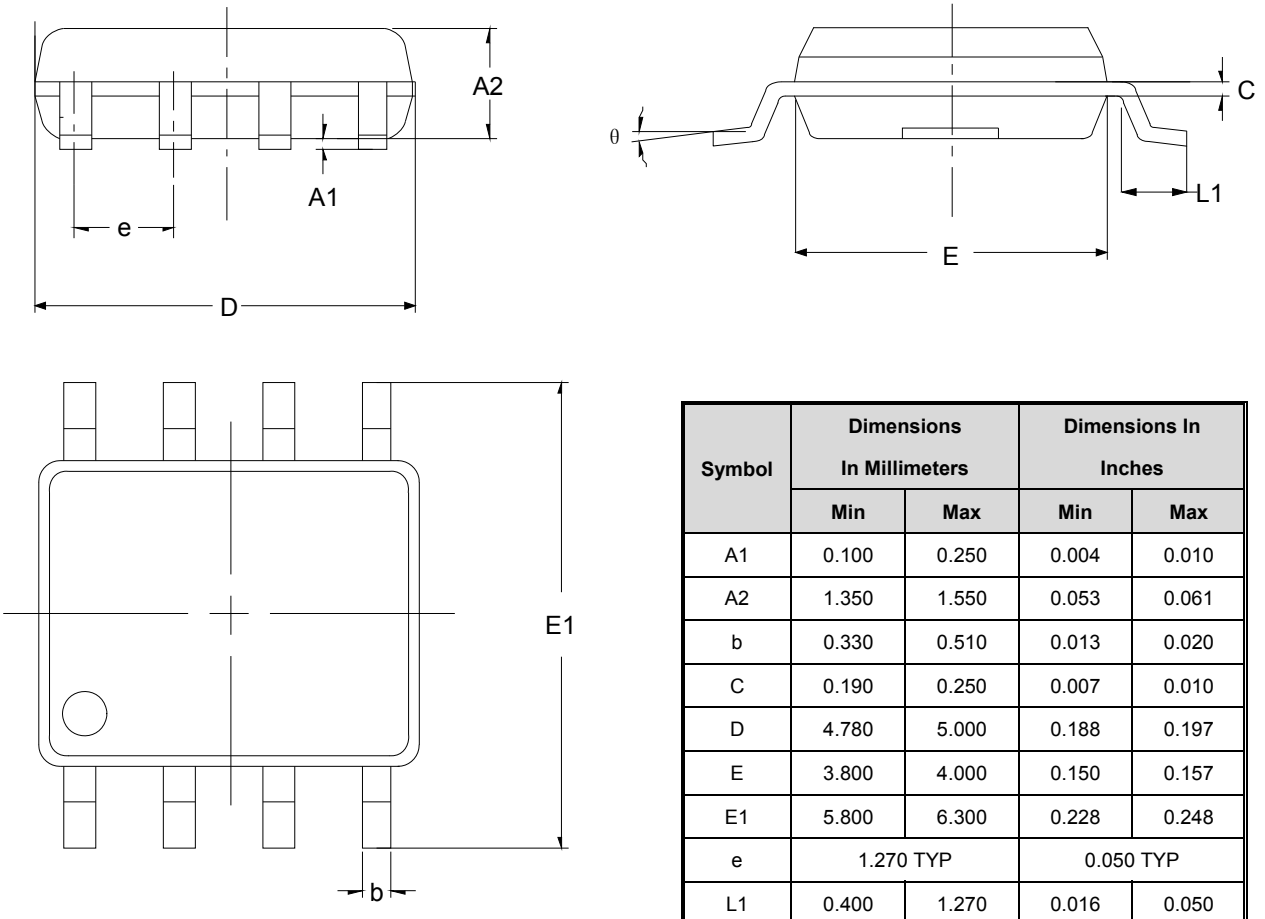
$R_1 = Feedback\ \ resistance = 2k\Omega$

$f_c = Crossover\ \ frequency = 8MHz$

Figure 5 DAC I/V Amplifier and Low-Pass Filter

Package Outline Dimensions

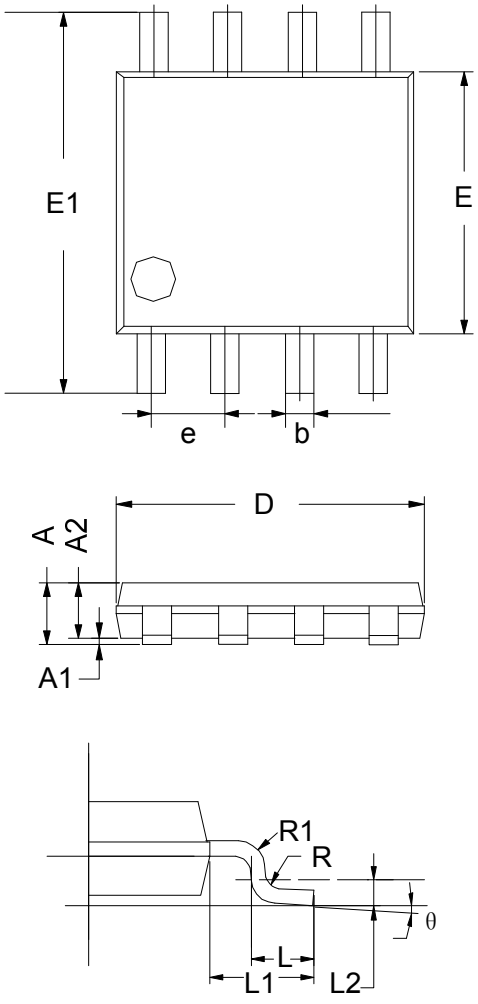
SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

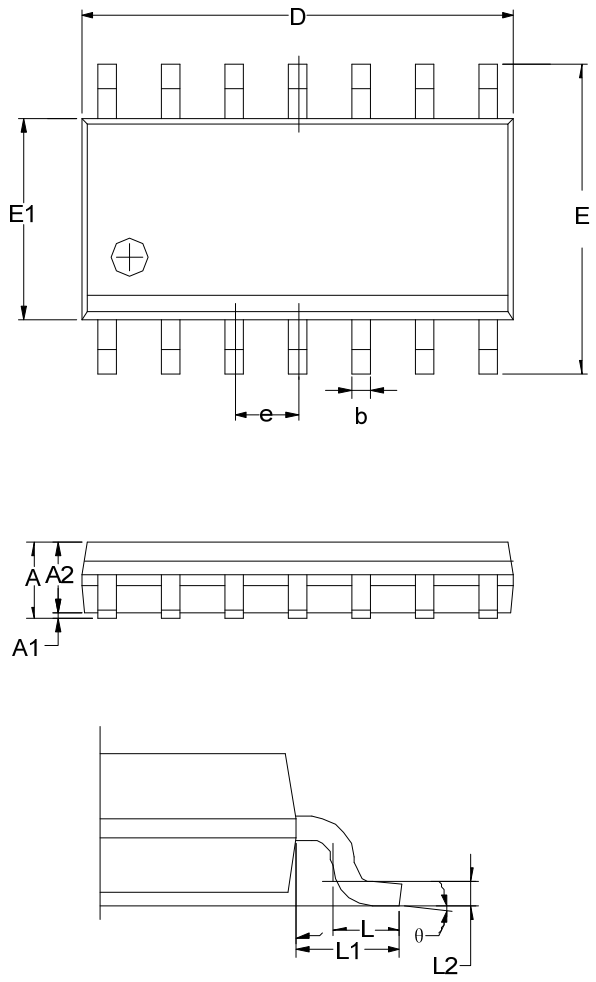
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

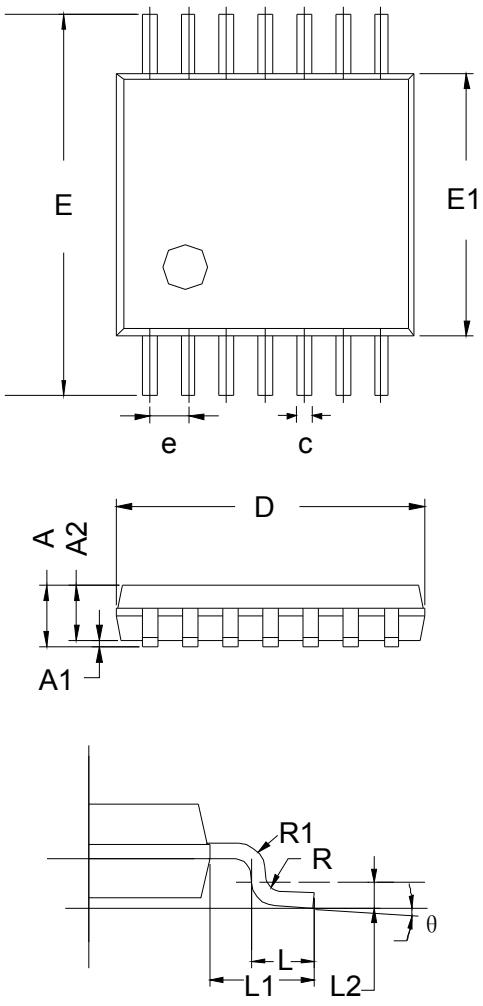
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°

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