



# BUK7Y3R0-40H

N-channel 40 V, 3.0 mΩ standard level MOSFET in LFPAK56

14 September 2017

Product data sheet

## 1. General description

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Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

## 2. Features and benefits

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- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower  $R_{DSon}$  in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight  $V_{GS(th)}$  limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced  $R_{th}$  and  $R_{DSon}$
  - Increases maximum current capability and improved current spreading

## 3. Applications

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- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

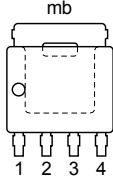
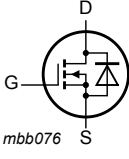
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	172	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 10</a>	1.8	2.55	3	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	6.3	15.8	nC
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V}$	-	19.5	-	nC
S	softness factor	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V}; T_j = 25\text{ °C};$ <a href="#">Fig. 16</a>	-	0.8	-	

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LFPAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y3R0-40H	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals; 4.9 mm x 4.45 mm x 1 mm body	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y3R0-40H	73H040

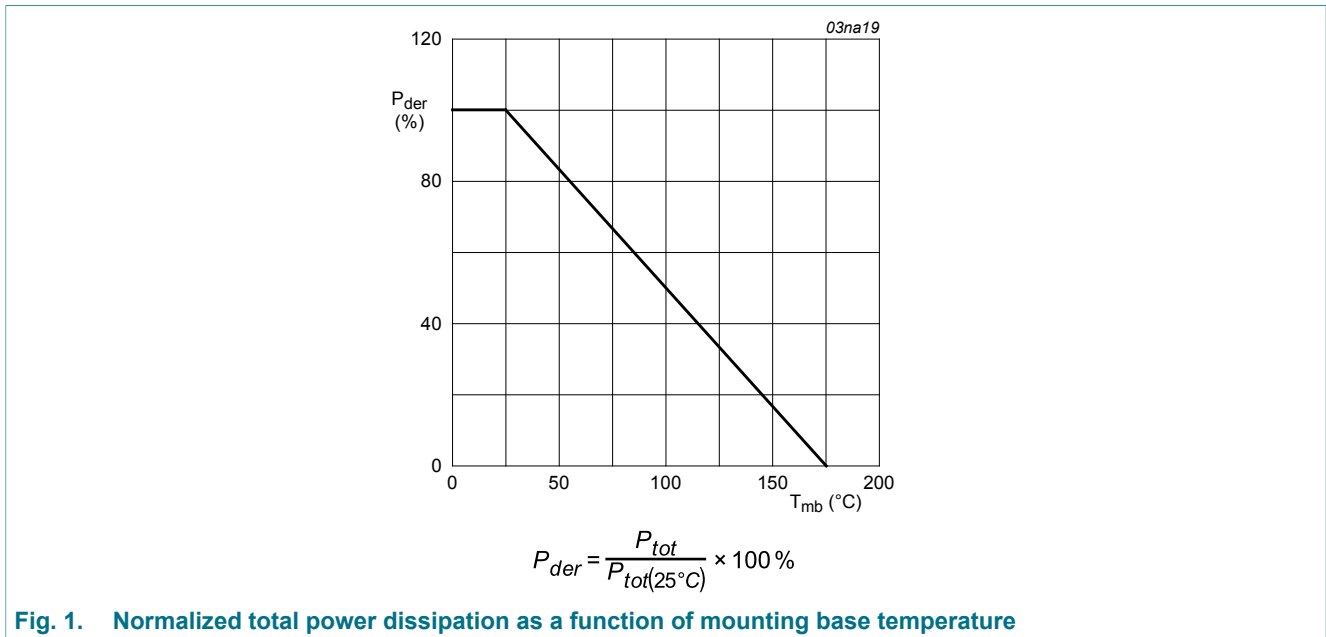
## 8. Limiting values

**Table 5. Limiting values**

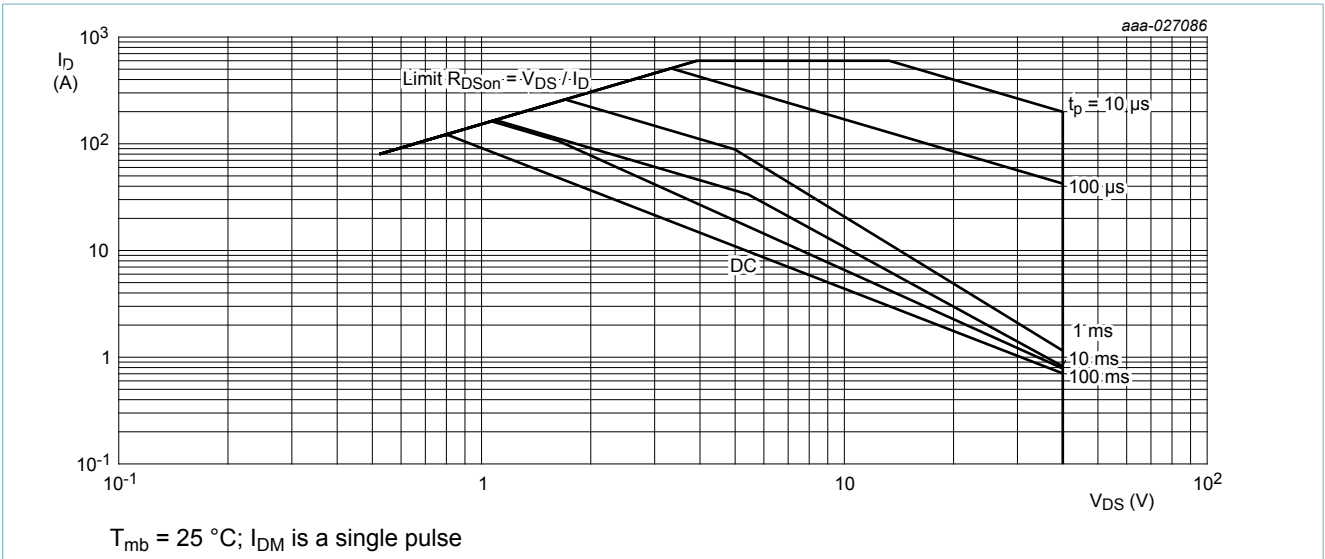
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	172	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C		-	120	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	600	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	<a href="#">[1]</a>	-	120	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	600	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; <a href="#">Fig. 3</a>	<a href="#">[2]</a> <a href="#">[3]</a>	-	50	mJ

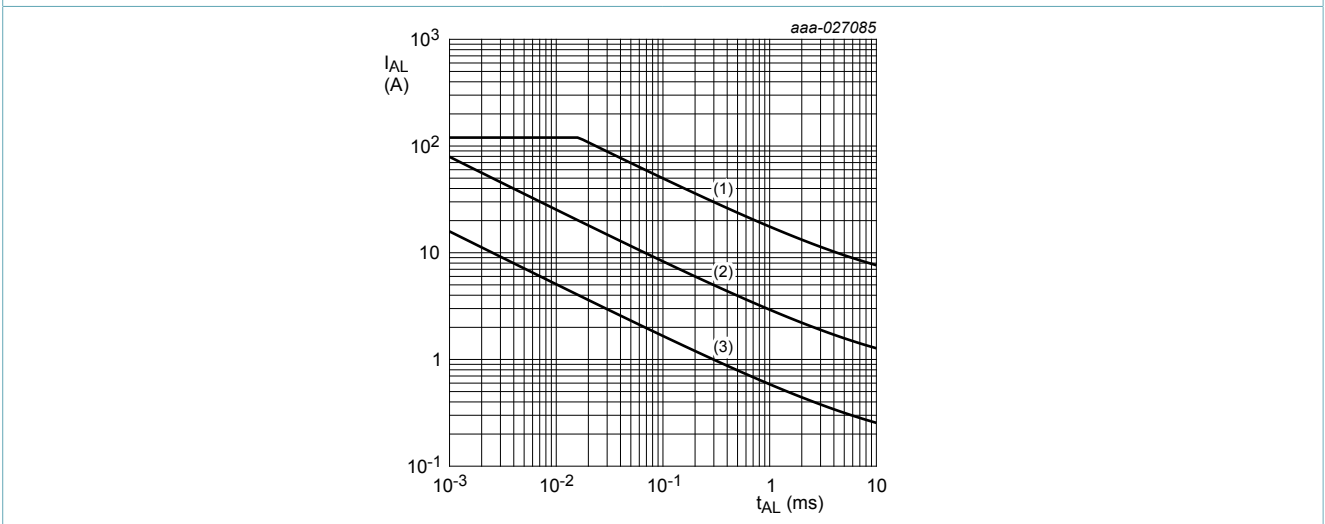
- [1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



**Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



**Fig. 3. Avalanche rating; avalanche current as a function of avalanche time**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	0.77	0.87	K/W

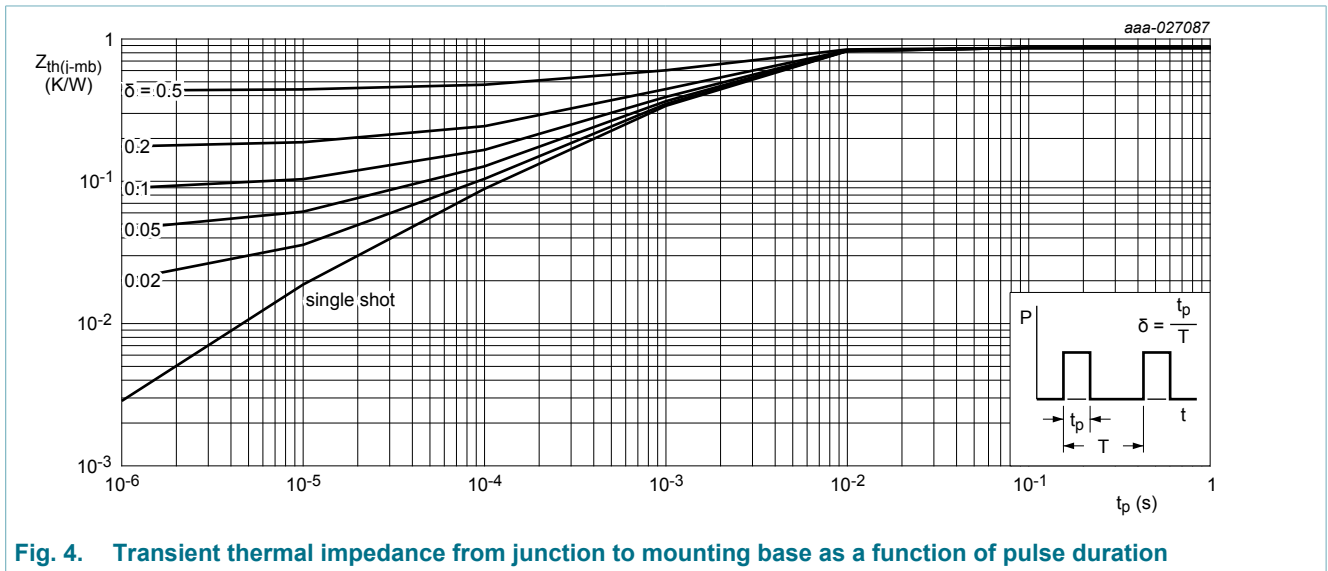


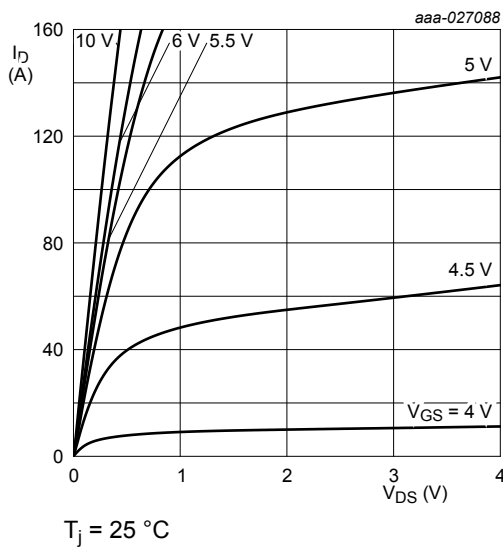
Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

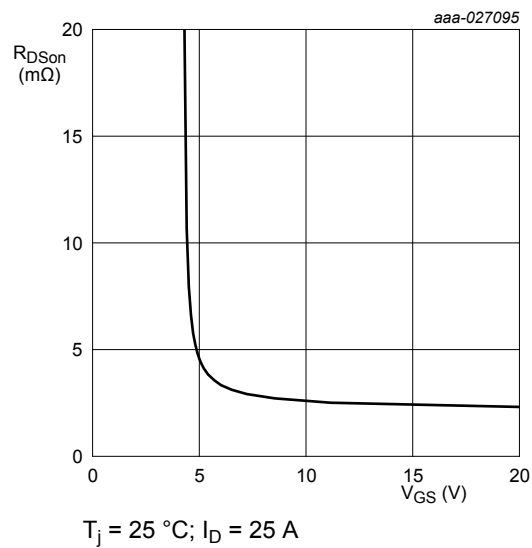
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	40	43	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -40 \text{ }^\circ\text{C}$	-	40.5	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 8</a> ; <a href="#">Fig. 9</a>	2.4	3	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.06	1	$\mu\text{A}$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	0.8	10	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	80	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	1.8	2.55	3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	2.5	3.6	4.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	2.8	4	5.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	3.5	5	6.5	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	0.34	0.85	2.12	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	34	59	nC
$Q_{GS}$	gate-source charge		-	9.8	15	nC
$Q_{GD}$	gate-drain charge		-	6.3	15.8	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	-	2417	5449	pF
$C_{oss}$	output capacitance		-	688	1377	pF
$C_{rss}$	reverse transfer capacitance		-	108	415	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5 \text{ } \Omega$	-	10	-
$t_r$	rise time	-		8.1	-	ns
$t_{d(off)}$	turn-off delay time	-		21.4	-	ns
$t_f$	fall time	-		10	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	0.8	1.2	V

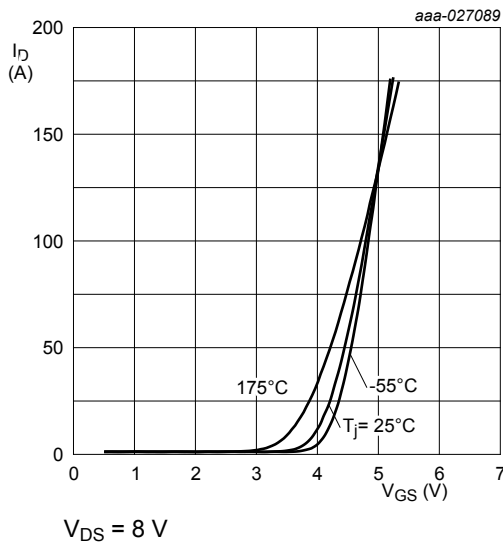
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$	-	27	-	ns
$Q_r$	recovered charge		-	19.5	-	nC
S	softness factor	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 16</a>	-	0.8	-	
		$I_S = 25\text{ A}$ ; $dI_S/dt = -500\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 16</a>	-	0.7	-	



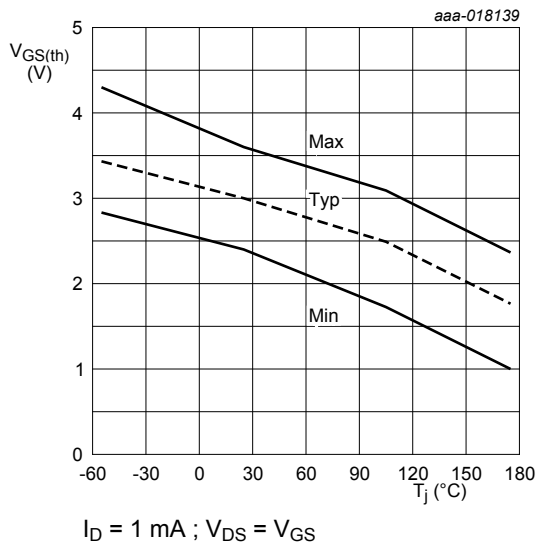
**Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values**



**Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**

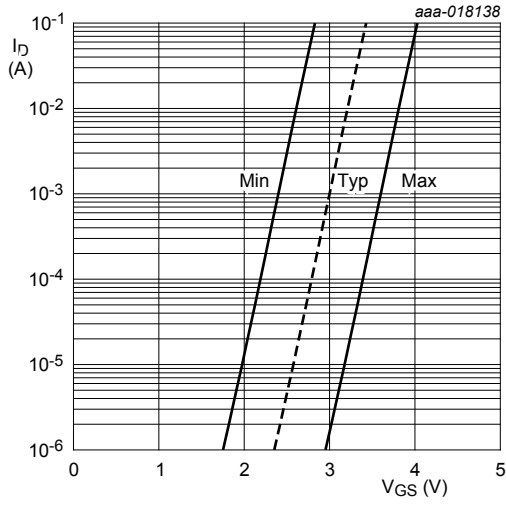


**Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



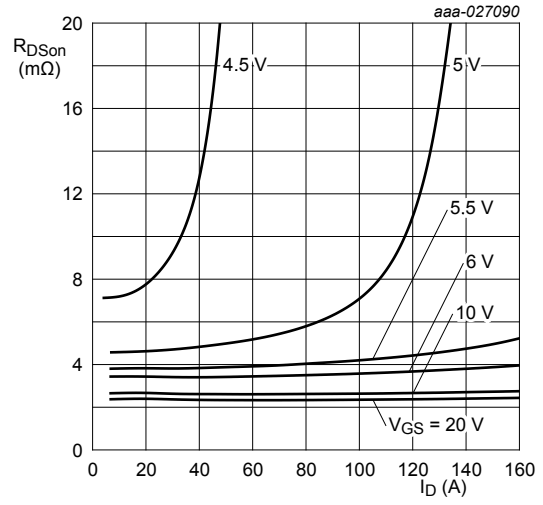
**Fig. 8. Gate-source threshold voltage as a function of junction temperature**





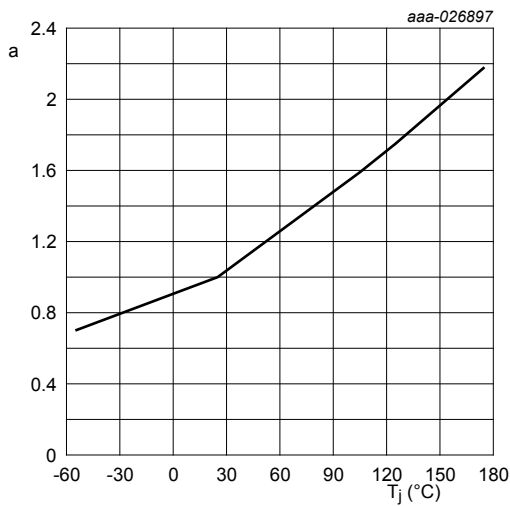
$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

**Fig. 9.** Sub-threshold drain current as a function of gate-source voltage



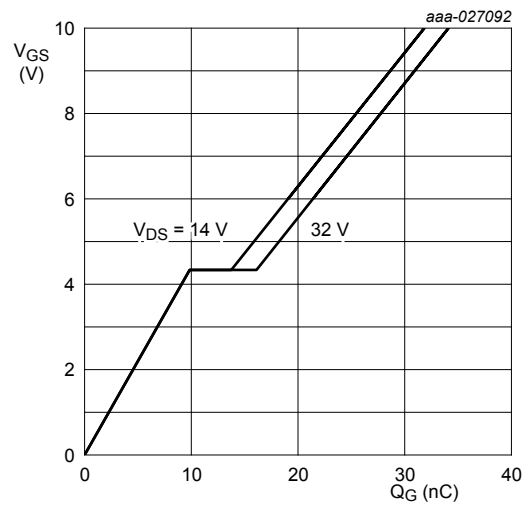
$T_j = 25\text{ °C}$

**Fig. 10.** Drain-source on-state resistance as a function of drain current; typical values



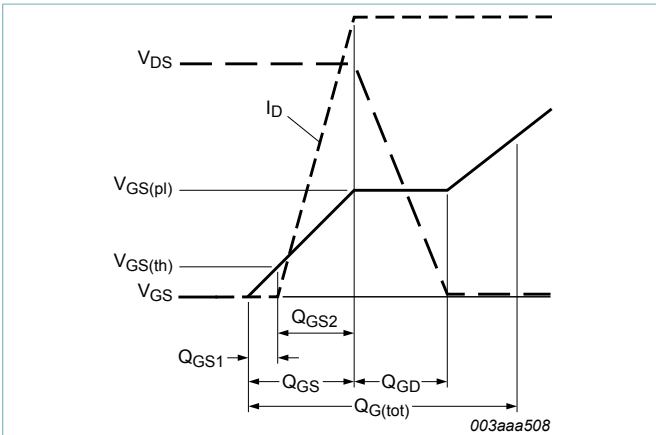
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ °C})}$$

**Fig. 11.** Normalized drain-source on-state resistance factor as a function of junction temperature

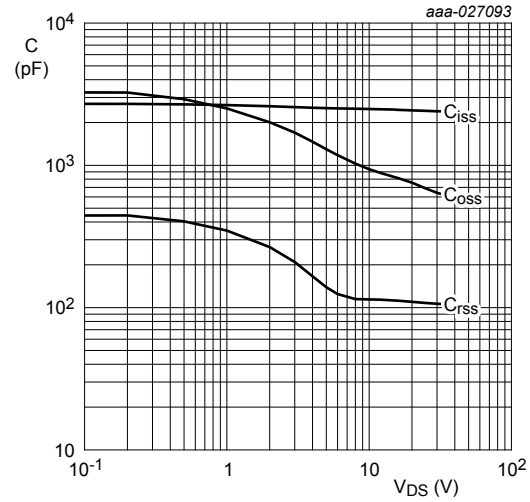


$T_j = 25\text{ °C}; I_D = 25\text{ A}$

**Fig. 12.** Gate-source voltage as a function of gate charge; typical values

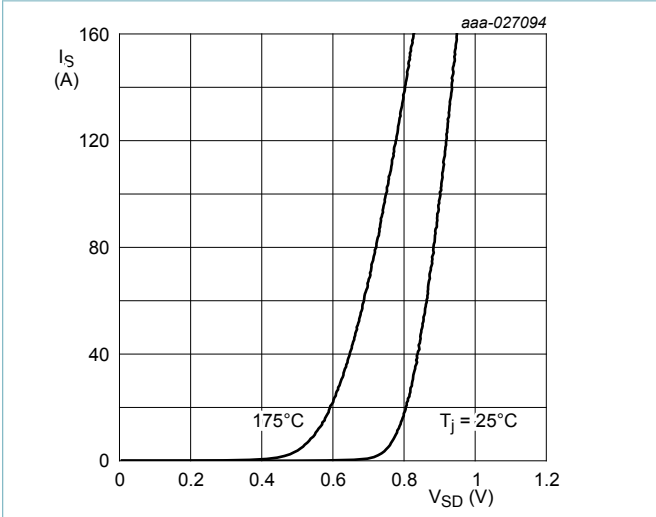


**Fig. 13. Gate charge waveform definitions**

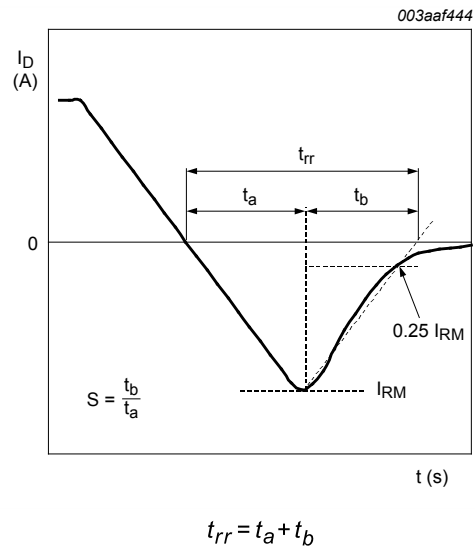


$V_{GS} = 0$  V;  $f = 1$  MHz

**Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

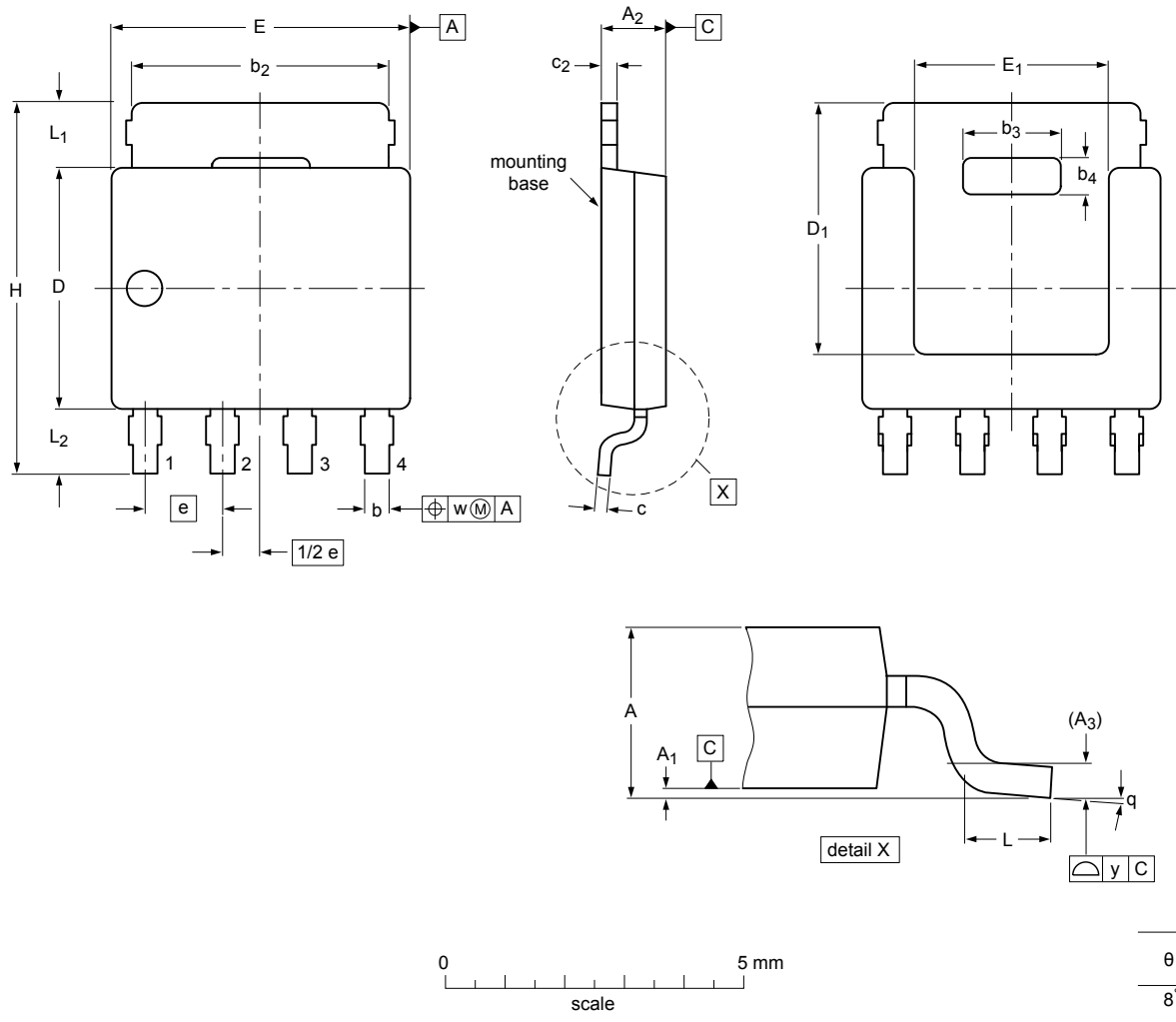


$$t_{rr} = t_a + t_b$$

**Fig. 16. Reverse recovery waveform definitions**

### 11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3	1.27	6.2	0.85	1.3	1.3		
nom				0.25																0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT669		MO-235			-11-03-25- 13-02-27

Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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