GENERAL DESCRIPTION

OB6663L integrates a transition mode power factor correction (TM PFC) controller and a Quasi-Resonant (QR) controller in one chip. The controller provides a cost effective solution for optimizing the power factor. QR provides higher efficiency and lower EMI compared to conventional PWM system.

OB6663L provides high level integration and high performance than conventional PFC/PWM system. The built-in dual output control for TM PFC optimizes power conversion efficiency with reduced system cost. Separated analog ground (AGND) and power ground (PGND) provide better noise immunity.

OB6663L features many built-in green functions to optimize power conversion efficiency at all power levels. This holds for QR operation at high power levels, as well as PFM operation at lower power levels, and 'Extended Burst Mode' operation at very low power or zero power (Standby) levels. At low power levels, OB6663L automatically turns off the PFC stage. In this way, low standby (<0.2W) together with low system cost can be achieved.

OB6663L offers comprehensive protection coverage including VCC Under Voltage Lockout (UVLO), Cycle-by-Cycle Current Limiting for PFC and QR Stage (OCP), Output Over Voltage Protection for PFC and QR Stage (OVP), Open Loop Protection for PFC and QR Stage (OLP), Programmable Brownout Protection (BOP), Programmable Over Temperature Protection (OTP), Built-in Soft Start in QR Stage, VCC Zener Clamp, Gate Clamp, Pin Floating Protection, and External Latch Triggering, etc.

OB6663L is offered in SOP-16 packages.

FEATURES

- Integrated Transition Mode (TM) PFC Controller and Quasi-Resonant (QR) PWM Controller
- Built-in Dual Output PFC Control
- Multi-Mode Operation for QR Stage
- Separated AGND and PGND Provide Better Noise Immunity
- Analog Multiplier with Built-in THD Optimizer for PFC Stage
- Line Feed-forward Compensation for PFC Stage
- Enhanced Dynamic Response for PFC Stage
- Less than 200mW Standby Power Consumption
- Minimum QR Short Circuit Power Consumption
- Audio Noise Free Operation
- External Latch Triggering for Both Converters
- Minimum OFF time for Ringing Suppression
- Maximum ON Time Limit for QR Converter
- Built-in 4ms Soft Start for QR Converter
- Internal Leading Edge Blanking for Both Converters

PROTECTIONS

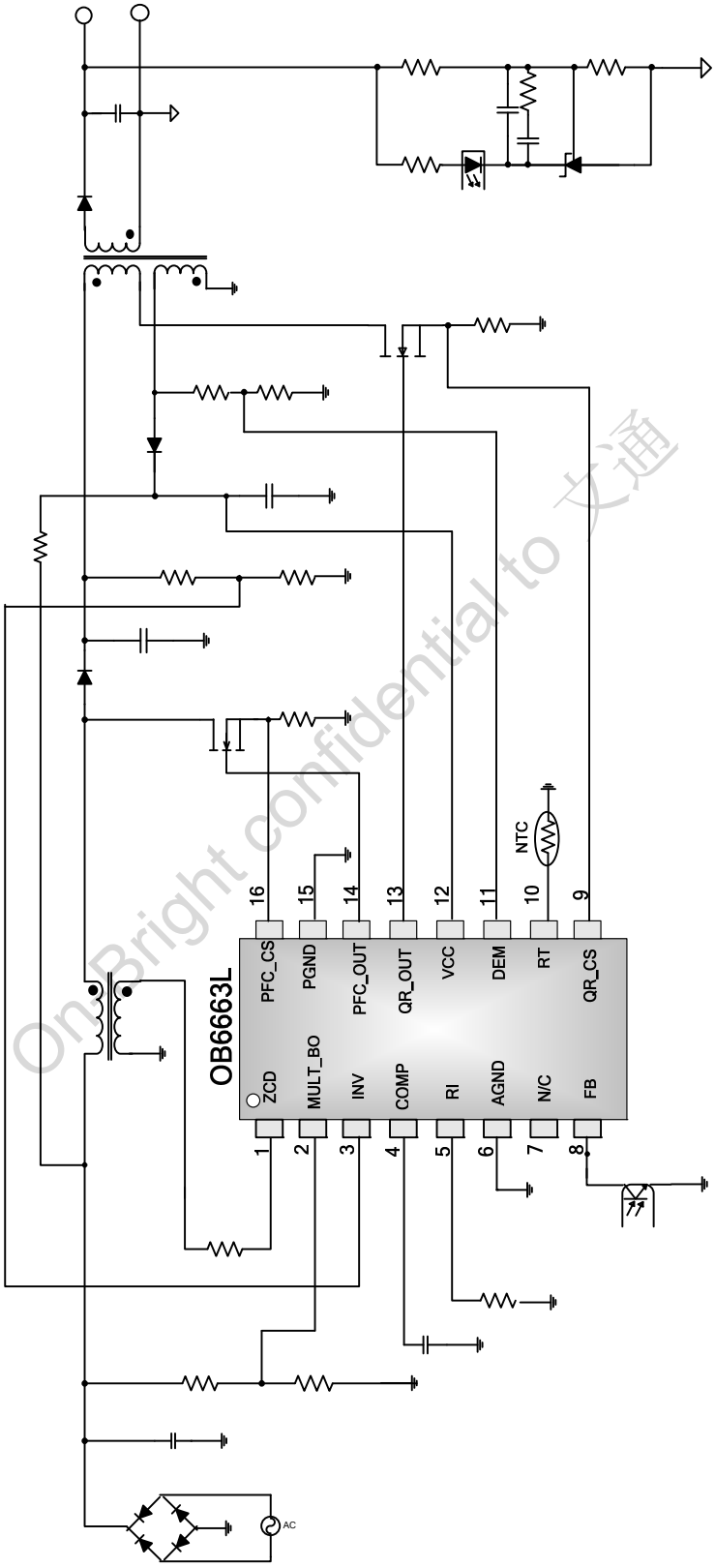
- Precise Output Over Voltage Protection (OVP) for Both Converters
- Open Loop Protection (OLP) for Both Converters
- Cycle-by-Cycle Current Limiting for Both Converters
- Programmable Brownout Protection (BOP)
- External Programmable Over Temperature Protection (OTP)
- All Pin Floating Protection

APPLICATIONS

Offline AC/DC flyback converter for

- General LED Lighting
- LCD Monitor/TV/PC
- Notebook

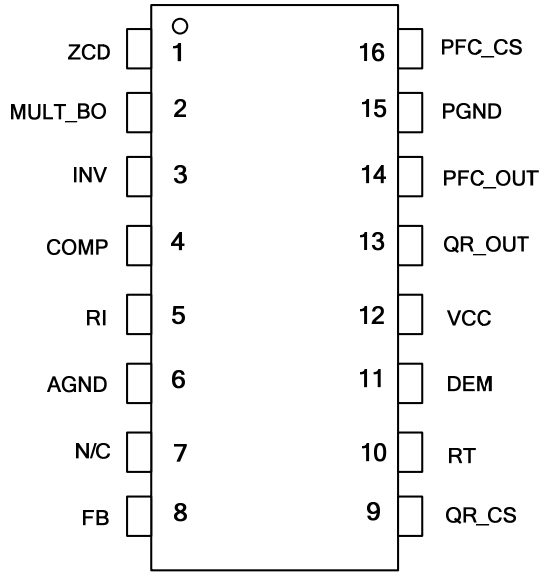
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map of OB6663L SOP16 package is shown as below.



Ordering Information

Part Number	Description
OB6663LQP	16 Pin SOP, Pb free in Tube
OB6663LQPA	16 Pin SOP, Pb free in T&R

Note: All Devices are offered in Pb-free Package if not otherwise noted.

Package Dissipation Rating

Package	RθJA (℃/W)
SOP16	85

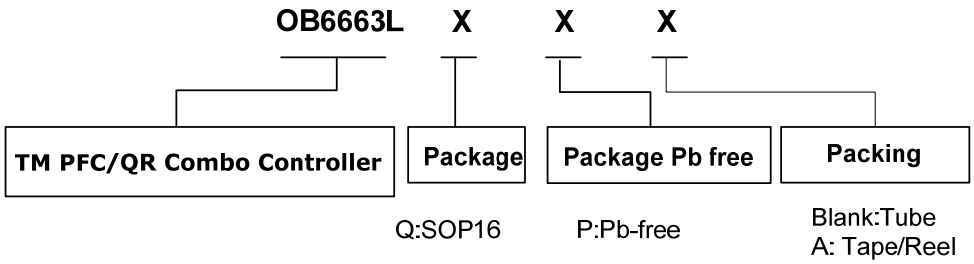
Absolute Maximum Ratings

Parameter	Value
VCC Zener Clamp Voltage	33 V
VCC Clamp Continuous Current	15 mA
ZCD Input Voltage	-0.3 to 7V
MULT_BO Input Voltage	-0.3 to 7V
INV Input Voltage	-0.3 to 7V
COMP Input Voltage	-0.3 to 7V
RI Input Voltage	-0.3 to 7V
N/C Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
QR_CS Input Voltage	-0.3 to 7V
RT Input Voltage	-0.3 to 7V
DEM Input Voltage	-0.3 to 7V
PFC_CS Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

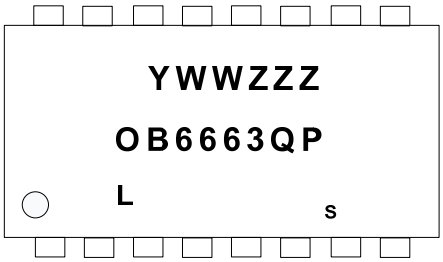
Recommended operating condition

Symbol	Parameter	Range
VCC	VCC Supply Voltage	12 to 28V
T_A	Operating Ambient Temperature	-20 to 85 ℃



Marking Information

SOP16



Y: Year Code

WW: Week Code (01-52)

ZZZ: Lot Code

Q: SOP16

P:Pb-free

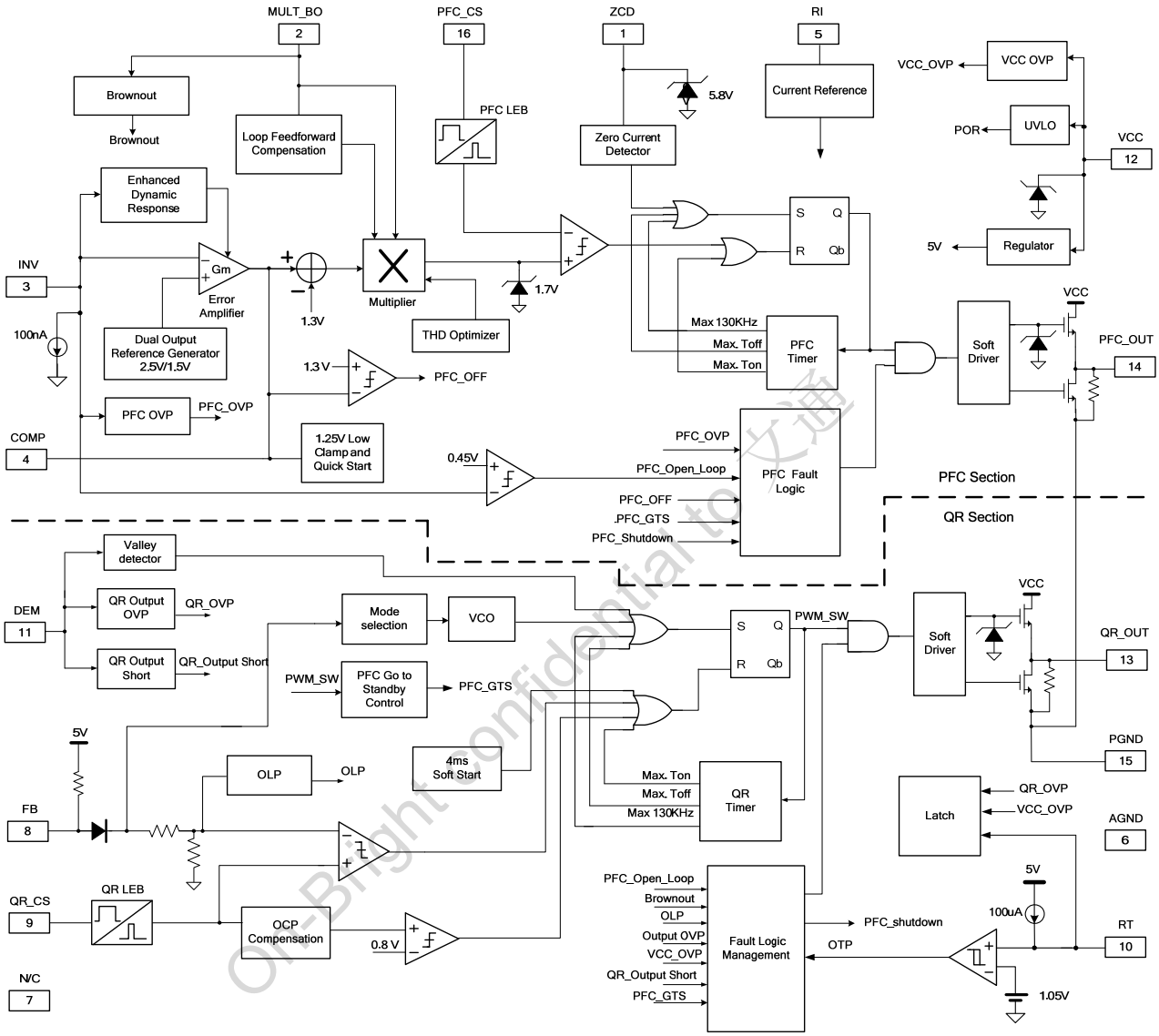
L: Character Code

s: Internal code

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	ZCD	I	Zero current detection input. When activated, a new PFC switching cycle starts.
2	MULT_BO	I/O	Input of multiplier. Connected to line voltage after bridge diodes via a resistor divider to provide sinusoidal reference voltage to the PFC current loop. This pin is also used for brownout detection.
3	INV	I	Inverting input of the error amplifier (EA). The information at the output of the PFC stage is fed to the pin through a resistor divider.
4	COMP	I/O	Output of EA. A compensation network is placed between COMP and AGND to achieve stability of the voltage control loop and ensure high power factor and low THD.
5	RI	O	This pin is connected to AGND via a 20K Ohm resistor.
6	AGND	P	Chip analog ground.
7	N/C		
8	FB	I/O	QR stage feedback input from the opto-coupler. The voltage of this pin controls the mode of QR operation in one of the three modes: Quasi-Resonant (QR), Pulse Frequency Modulation (PFM), and Burst Mode (BM).
9	QR_CS	I	QR stage current sense input pin.
10	RT	I/O	This pin is connected to ground via a NTC resistor, external over temperature protection.
11	DEM	I	Input from QR auxiliary winding for demagnetization timing. This pin is also used for QR over voltage protection and PFC stage control during startup. .
12	VCC	P	Chip power supply pin.
13	QR_OUT	O	QR stage totem pole gate driver output.
14	PFC_OUT	O	PFC stage totem pole gate driver output.
15	PGND	P	Chip power ground pin for PFC and QR gate driver
16	PFC_CS	I	PFC current sense input.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(T_A = 25℃, VCC=18V, RI=20K Ohm if not otherwise noted)

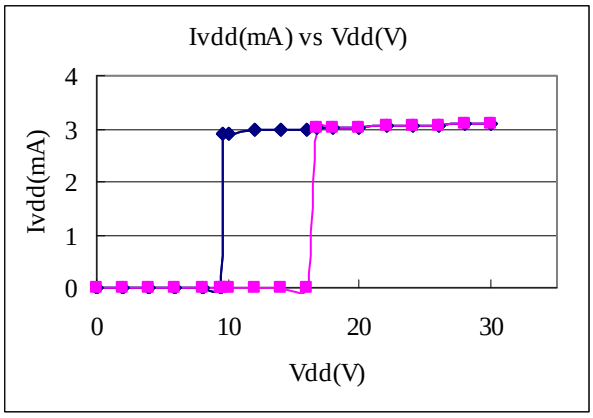
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VCC pin)						
I_VCC_Startup	VCC start up current	VCC =13.5V, Measure current into VCC		5	20	uA
I_VCC_quiet	Operation current without switching	FB=3V, no switching,		2.1		mA
I_VCC_op	Operation current with switching	FB=3V, Fsw=40KHz, 1nF load at GATE		6.0	10	mA
UVLO(ON)	VCC under voltage Lockout Enter		8.5	9.5	10.5	V
UVLO(OFF)	VCC under voltage lockout exit		17.2	18.2	19.2	V
VCC_OVP	VCC over voltage protection enter			31.5		V
VCC_latch_release	VCC latch release voltage			6.3		V
Ivcc(latch)	VCC current when latch off	VCC=V_latch_release+1V		45		uA
Vz	VCC zener clamp voltage	I(VCC) = 15 mA		33		V
RI Voltage (RI pin)						
V_RI_open	RI open load voltage			2.0		V
Over Temperature Protection (RT pin)						
I_RT	Output current of RT pin		95	100	105	uA
V_{TH_OTP}	Over Temperature Protection (OTP) voltage		1.00	1.05	1.10	V
V_RT_Open	RT Pin Open Voltage			3.7		V
AC Line Brown out Protection (MULT_BO pin)						
Vth_bop	MULT_BO threshold. AC Brownout voltage		0.85	0.90	0.95	V
I_bop_hys	Brownout hysteresis current			2		uA
Tbop	Brownout debounce time			45		msec
Vsel_ea_ref	Threshold for PFC EA reference selection		1.7	1.8	1.9	V
Vsel_hys	PFC A reference selection hysteresis			0.2		V
TD_sel	PFC output conversion debounce time			40		mS
PFC Section						
Error Amplifier						
Vea_ref1	EA reference voltage 1		2.46	2.50	2.54	V
Vea_ref2	EA reference voltage 2		1.45	1.50	1.55	V
Gm	EA transconductance		90	115	140	uS
Isource	Max. EA output source current under normal operation			30		uA
Isink	Max. EA output sink current under normal operation			30		uA
Veao(Z)	EA output voltage when			1.3		V

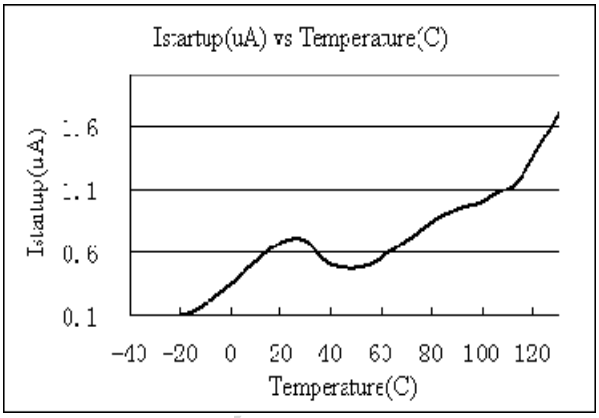
	zero duty cycle					
Vcomp_clamp	COMP pin upper clamping voltage			4.9		V
	COMP pin lower clamping voltage			1.25		V
Current Sense Comparator (PFC_CS pin)						
Vth_OCP	Maximum current sense threshold voltage		1.6	1.7	1.8	V
T_PFC_LEB	PFC leading edge blanking time			300		nsec
Multiplier (MULT_BO pin)						
Vmult	Multiplier maximum linear operating range			3.5	3.8	V
K	Multiplier gain	Vmult=1V, Vcomp=2.8V EA reference = Vea_ref2	0.30	0.45	0.70	1/V
		Vmult=1V, Vcomp=2.8V EA reference = Vea_ref1	0.15	0.25	0.35	1/V
Zero Current Detection (ZCD pin)						
Vth_ZCD	ZCD demagnetization threshold voltage			1.3		V
Vzcd_hys	ZCD detection hysteresis voltage			0.2		V
T_ZCD_OUT	Timeout after last ZCD transition			5		usec
Timer						
Ton_pfc_max	Maximum on time		30	45	60	usec
Toff_pfc_max	Maximum off time		40	60	80	usec
F_PFC_max	Maximum PFC switching frequency		190	240	290	KHz
PFC Over Voltage Protection (PFC OVP)						
Vth_pfc_ovp	INV threshold, PFC output over voltage protection (OVP)		2.590	2.625	2.660	V
Vpfc_ovp_hys	PFC OVP hysteresis			50		mV
PFC Open Loop Protection (PFC OLP)						
Iinv	INV pin sink current	COMP=2.5V		100	500	nA
V_{OLP}	INV threshold, open loop protection (OLP)		0.40	0.50	0.60	V
PFC Enhanced Dynamic Response (PFC EDR)						
V_{EDR}	INV threshold, below which EDR occurs	PFC EA reference = Vea_ref1		2.30		V
		PFC EA reference = Vea_ref2		1.30		V
$I_{EDR(max)}$	Maximum EA source current under EDR operation	INV=2.1V		400		uA
Gate Driver for PFC (PFC_OUT pin)						
VOL_PFC	PFC_OUT low level	Io = 30 mA			1	V
VOH_PFC	PFC_OUT high level	Io = 30 mA	7			V
V_Clamp_pfc	PFC_OUT clamping voltage	VCC=25V		15		V
Tr_pfc	PFC_OUT rising time	CL= 1nF at PFC_OUT		80		nsec
Tf_pfc	PFC_OUT falling time	CL= 1nF at PFC_OUT		20		nsec
QR Section						

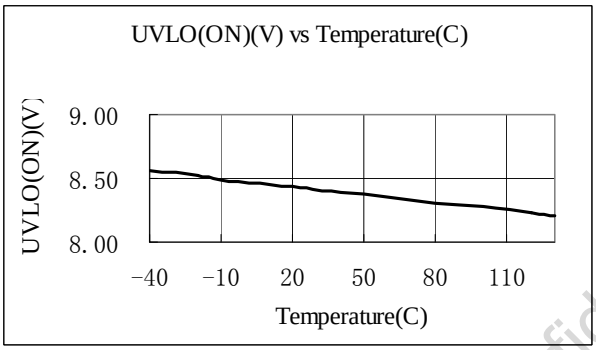
Feedback Input(FB pin)						
VFB gain	VFB/VCS			4.5		V/V
VFB_Open	FB open loop voltage		4.8	5.5	6.0	V
ZFB_IN	Input impedance			10		K Ohm
VFB_pfm	FB voltage in which system works in QR PFM mode			0.85 ~ 1.85		V
Fsw_pfc_off	QR switch frequency threshold, below which PFC will be shutdown			70		KHz
Fsw_pfc_on	QR switch frequency threshold, higher than which PFC will be turn on			86		KHz
Tpfc_off	PFC turn off debounce time			100		msec
Tpfc_on	PFC turn on debounce time			1		msec
QR Current Sense Comparator (QR_CS pin)						
V_{TH}_OCP_min	Min. internal current limiting threshold		0.42	0.45	0.48	V
V_{TH}_OCP_max	Max. internal current limiting threshold			0.80		V
T_D_OC	QR OCP control delay	CL=1nF at QR_OUT		100		nsec
T_QR_LEB	QR leading edge blanking time			300		nsec
Demagnetization Detection (DEM pin)						
V_{TH}_DEM	Demagnetization comparator threshold voltage		10	75	150	mV
V_{TH}_DEM_hyst	Hysteresis for DEM comparator			20		mV
T_{supp}	Suppression of the transformer ringing at start of QR secondary stroke			2		usec
V_{DEM}_clamp_n	DEM pin negative clamp voltage			-0.7		V
V_{DEM}_clamp_p	DEM pin positive clamp voltage			5.8		V
T_DEM_$_{OUT}$	Timeout after last demag transition			5		usec
T_{DEM_delay}	Demag propagation delay			250		nsec
Vth_PFC_en	Enable PFC threshold at startup			1.5		V
Timer						
F_QR_burst	Burst mode switching frequency			20		KHz
F_QR_high	Maximum QR frequency		100	125	145	KHz
Ton_qr_max	Maximum on time		32	47	62	usec
Toff_qr_max	Maximum off time		65	95	125	usec
QR Soft Start						
Tss	QR soft startup time			4.0		msec
QR Over Load Protection (QR OLP)						
V_{TH}_PL	Power Limiting FB			4.2		V

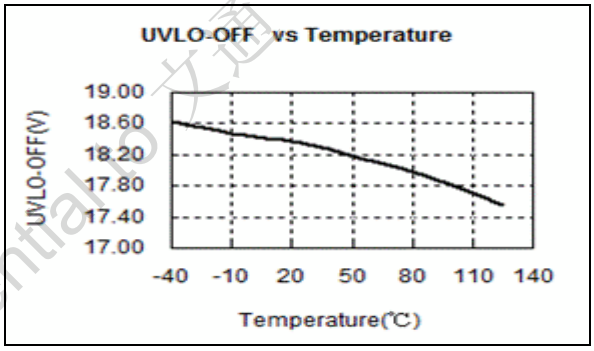
	Threshold Voltage					
T_D_PL	Power limiting Debounce Time			90		msec
QR Output Over Voltage Protection (QR OVP)						
V_{TH}_qr_OVP	Output OVP trigger point			3.75		V
T_ovp_plateau	QR output OVP plateau sampling after switching off			2.0		usec
Ntrue_qr_OVP	Number of subsequent cycles to be true QR OVP			4		Cycle
Gate Driver for QR (QR_OUT pin)						
VOL_QR	QR_OUT low level	Io = 30 mA			1	V
VOH_QR	QR_OUT high level	Io = 30 mA	7			V
V_Clamp_qr	QR_OUT clamping voltage	VCC=25V		15		V
Tr_qr	QR_OUT rising time	CL = 1nF at QR_OUT		80		nsec
Tf_qr	QR_OUT falling time	CL= 1nF at QR_OUT		20		nsec

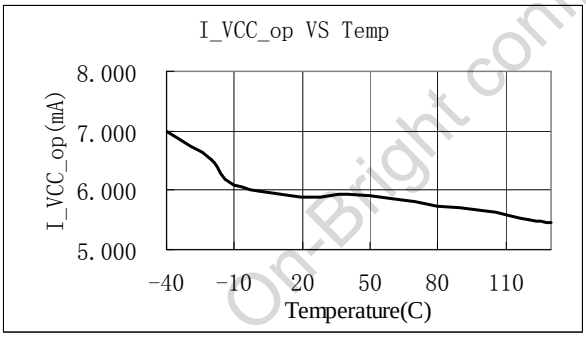
CHARACTERIZATION PLOTS

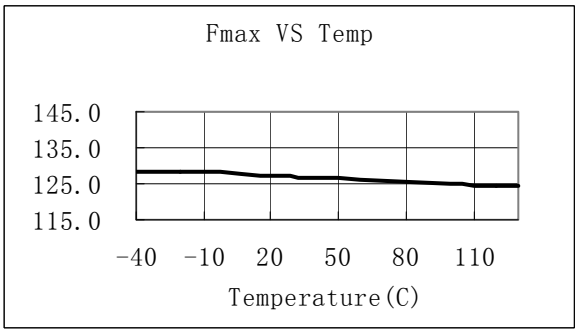


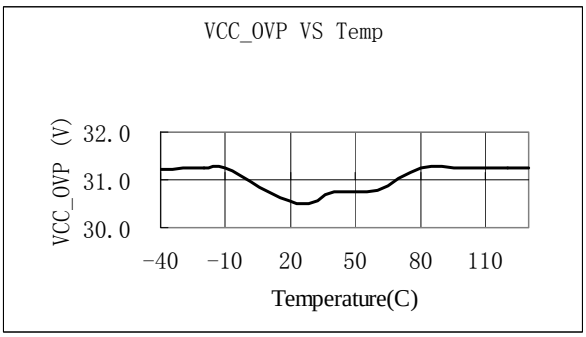


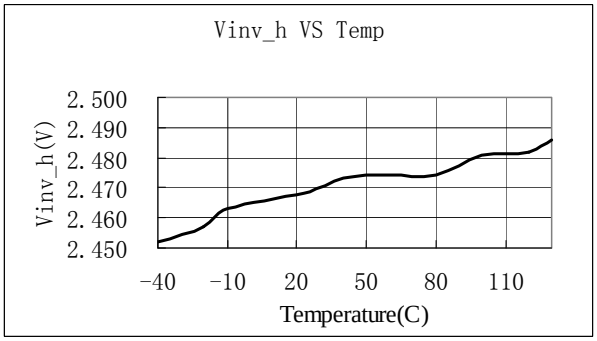


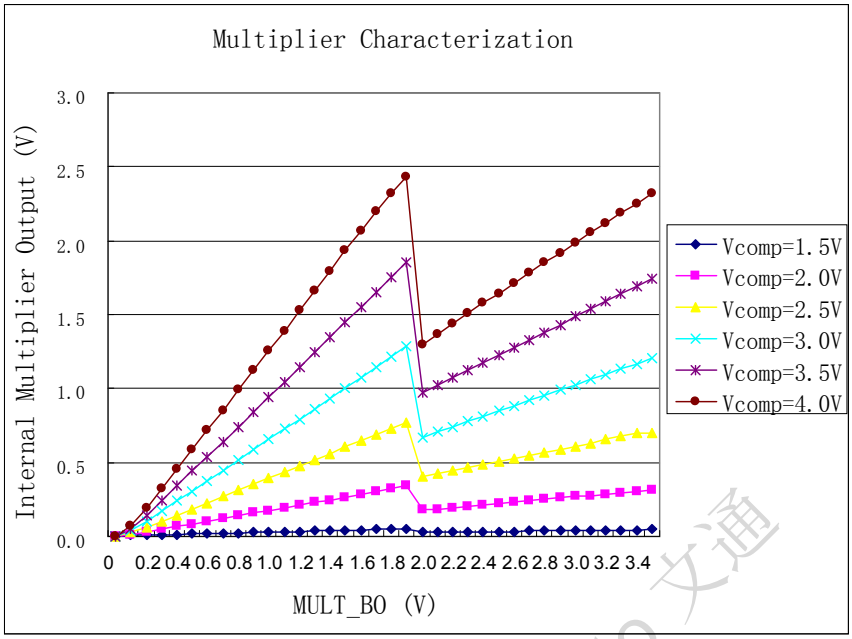












OPERATION DESCRIPTION

GENERAL CONTROL AND FEATURE

- **Integrated TM PFC Controller and QR Controller in One Chip**

OB6663L integrates a transition mode power factor collection (TM PFC) controller and a quasi-resonant (QR) controller in one chip.
In TM PFC control, the inductor current is allowed to completely go to zero before the next switching cycle of the power MOSFET is initiated. Therefore, the reverse recovery loss of output boost diode is minimized. Also TM PFC can provide low harmonic distortion and high power factor.
Quasi-Resonant (QR) control can provide lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency.
The built-in advanced energy saving with high level protection features of OB6663L provide simple and cost effective solutions for the power supplies of 75 Watts or greater.

- **Separate AGND and PGND Provide Better Noise Immunity**

Noise interference is always a problem in power system design. Situations become worse in TM PFC/QR system since TM PFC and QR are both frequency variation systems and there is no synchronization between them. To alleviate this problem, OB6663L uses two separated ground pins, one is analog ground (AGND), and the other one is power ground (PGND). In this way, system noise immunity is enhanced and PCB layout requirement can be relaxed.

- **Over Temperature Protection with Latch Shutdown (RT pin)**

A NTC resistor in series with a regular resistor should be connected between RT and AGND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal 100uA current source (RI=20K Ohm) flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shuts down the MOSFET when the sensed input voltage is lower than 1.05V. OTP is a latched shutdown.

- **External latch trip point**

By externally forcing a level on pin RT (e.g.., with a signal coming from a temperature sensor) less than 1.05V, OB6663L can be permanently latched-off. To resume normal operation, VCC voltage should go below 6.3V (typical), which implies to unplug the SMPS from the mains.

- **Brownout Protection (MULT_BO Pin)**

By monitoring the level on pin MULT_BO during normal operation, the controller protects the SMPS against low line voltage condition. When peak voltage of MULT_BO level falls below 0.9V, and lasts for about 45ms, the controller stops pulsing until this level goes back and resumes operation, as shown in Fig.1. By adjusting the resistor divider connected between the high input voltage and this pin, start and stop levels are programmable.

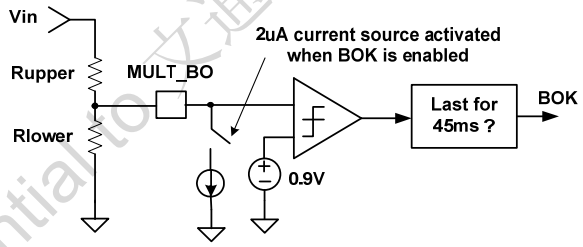


Figure 1

- **RI for Operating Current and Timer (RI Pin)**

A resistor connected between RI and AGND sets the internal current source and thus the chip operating current. The timing of internal timer is also related to this resistor. It is strongly recommended that the resistor is set to be 20K Ohm.

- **Pin Floating Protection**

OB6663L features all pins floating protection. When pin floating occurs, no system damage is guaranteed.

FUNCTIONAL DESCRIPTION for TM PFC

- **Built-in Dual Output Control for PFC**

OB6663L integrates dual output control function according to the AC line voltage. Because the input voltage of the boost converter after the diode bridge is proportional to the peak voltage of the input AC line voltage, the MULT_BO pin voltage represents the peak AC line voltage. If it is lower than 1.8V, OB6663L sets the reference voltage of EA to 1.5V. When MULT_BO pin voltage is larger than 2.0V, the reference voltage will be set to 2.5V, as show in Fig 2. This means that if the output voltage of the boost converter is set to 400V at high line voltage, the output voltage will be 240V (400V*1.5/2.5) at low line voltage. 0.2V

hysteresis window and 40mS debounce time is added for PFC output selection.

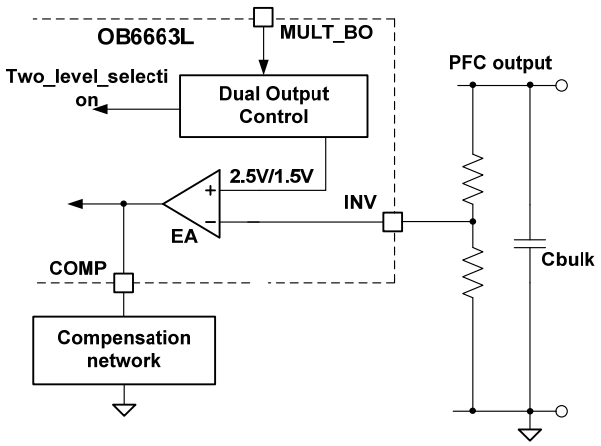


Figure 2

- **PFC Error Amplifier**

PFC Error Amplifier (EA) provides regulation for the PFC voltage loop. Connected to a resistor divider from PFC output, the inverting input of the EA (INV pin voltage) is compared to an internal reference voltage (2.5/1.5V) to set the regulation on output voltage. The EA consists of a transconductance amplifier with a typical transconductance value of 115 uS. The sink and source capability of the EA is approximately 30uA during normal operation. The EA output voltage (COMP pin voltage) is subtracted by 1.3V and then is internally connected to the multiplier input (as shown in Fig 3). PFC loop compensation is realized by connecting a compensation network between COMP and AGND. The system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage.

- **PFC Open Loop Protection (PFC OLP)**

If PFC feedback loop is abnormal, such as INV is shorted to ground or upper voltage feedback resistor is open, INV pin will be pulled low by internal 100nA current source, the IC will then enter into shutdown mode.

- **Enhanced Dynamic Response (INV pin)**

Due to the low frequency bandwidth of the PFC voltage loop, the PFC dynamic response is very slow. This may cause additional stress to the PFC output bulk capacitor and the switching transistor of the PFC in the event of heavy load changes.
OB6663L provides enhanced dynamic response for the PFC loop by detecting the feedback voltage INV at pin3. Whenever INV voltage falls below the reference value by 5%, it will increase EA transconductance in turn increase the PFC_OUT duty cycle directly. This change in duty cycle is bypassing the slow change of COMP voltage, thus results in a fast dynamic response for the PFC stage.

- **Highly Linear PFC Multiplier with THD Optimizer (MULT_BO pin)**

In OB6663L, a highly linear one quadrant analog multiplier for TM PFC control is integrated with THD (Total Harmonic Distortion) Optimizer, as shown in Figure 3. The multiplier output limits the PFC MOSFET peak current with respect to the AC half wave rectified input voltage to achieve TM PFC control. In OB6663L, the two inputs for the multiplier are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion. The output of multiplier can be represented using the following equation:

$$\text{Multiplier\_output} = K \times (V_{COMP} - 1.3) \times V_{MULT\_BO}$$

Where K is a design constant, in low line input range, K is about 0.7; in high line input range, K is about 0.3.
In OB6663L, the multiplier output is internally clamped to 1.7V.

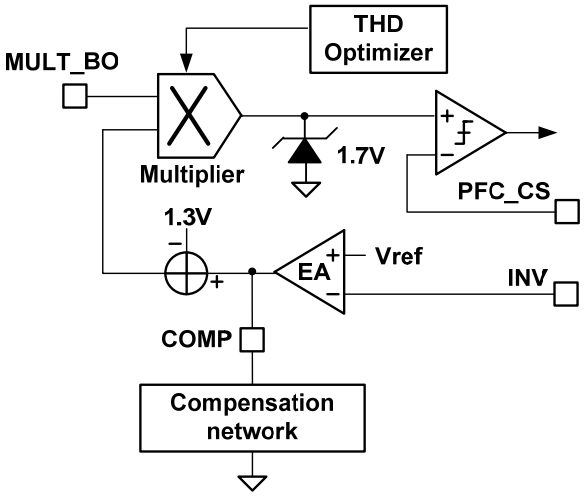


Figure 3

- **Zero Current Detection (ZCD pin)**

OB6663L performs zero current detection (ZCD) by using an auxiliary winding of the PFC boost inductor in series with an external resistor. When the stored energy of the PFC boost inductor is fully released to the output, the voltage at ZCD pin decreases. When ZCD pin voltage falls below 1.3V, an internal ZCD comparator is triggered and a new PFC switching cycle is initiated following the ZCD triggering. If no zero current triggering signal is detected on ZCD pin, OB6663L will generate a restart signal in 60 usec (typ.) after the

last PFC_OUT signal. The maximum and minimum voltage of ZCD pin is internally clamped to 5.8V and -0.7V respectively.

- **Max. and Min. Frequency Clamp in PFC**

In OB6663L, the maximum switching frequency of PFC stage is limited to be below 240KHz for optimizing the transformer and minimizing the switching losses. The minimum switching frequency of PFC is limited to be above 20KHz for audio free noise operation.

- **PFC Quick Start (COMP Pin)**

A Quick Start block is implemented in OB6663L to optimize PFC startup. During initial startup, PFC EA compensation capacitor is discharged, the Quick Start circuit is designed to pre-charge the compensation capacitor at the COMP pin to 1.25V, allowing immediate output switching.

- **PFC Loop Feedforward Compensation**

The power stage gain of PFC pre-regulators varies with AC line input voltage, so does the crossover frequency of the overall voltage open-loop gain. OB6663L integrates PFC loop feedforward compensation block to minimize PFC voltage regulation loop bandwidth variation over the full line input range.

- **PFC Current Sensing and Leading Edge Blanking (PFC_CS pin)**

Cycle-by-Cycle current limiting for the PFC stage is offered in OB6663L. The switch current is detected by a sense resistor into the PFC_CS pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state, the PFC current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period.

- **PFC Go-to-Standby Power Level**

When light/zero loading occurs, OB6663L detects and confirms the presence of the light/zero loading by monitoring SMPS switch frequency. As shown in Fig 4, whether PFC stages is shut down or not is based on SMPS switch frequency.
When the SMPS switch frequency lower than 70K, PFC stages turn off after 100mS debounce. When the SMPS switch frequency higher than 86K, PFC stages goes back to normal operation state after 1mS debounce. The PFC Go-to-Standby control diagram is shown in Fig 4.
During startup PFC stages is shut down. After detecting the DEM voltage is higher than the Vth_PFC_en threshold, the PFC stages can be enabled. Under normal operating conditions, the DEM pin does not control the PFC stage on or off any more.

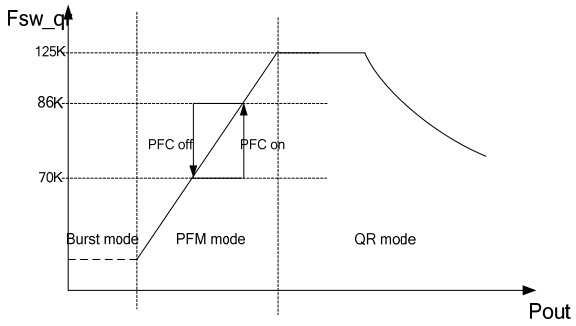


Figure 4

- **PFC Gate Driver (PFC_OUT Pin)**

The PFC_OUT pin is connected to the gate of an external PFC power switch with 1A capability. An internal 15V clamp is added for MOSFET gate protection at high VCC voltage. When VCC voltage drops below UVLO(ON), the PFC_OUT pin is internally pull low to maintain the off state.

FUNCTIONAL DESCRIPTION for QR

- **Multi-Mode Operation for QR**

OB6663L integrates a multi-mode QR controller. The QR controller changes the mode of operation according to FB voltage, which reflects the line and load conditions, as shown in Fig.5.

■ Under normal operating conditions (FB>Vth2, Figure 1), the system operates in QR mode. The frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when 125KHz frequency clamping is reached. System design should be optimized such that the operation frequency is within the range specified at full loading conditions and in universal AC line input range.

■ At light load condition (Vth1<VFB<Vth2, Figure 1), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. In PFM mode, the “ON” time in a switching cycle is fixed and the system modulates the frequency according to the load conditions. Generally, in flyback converter, the decreasing of loading results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when loading decreases, the system automatically skip more and more valleys and the switching frequency is thus

reduced. In such way, a smooth frequency foldback is realized and high power conversion efficiency is achieved.

■ At zero load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In this condition, voltage at FB is below burst mode threshold level, Vth1. The Gate drive output switches only when VCC voltage drops below a preset level or FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. In extended burst mode, the switching frequency is fixed to 20KHz, in this way, possible audio noise is eliminated.

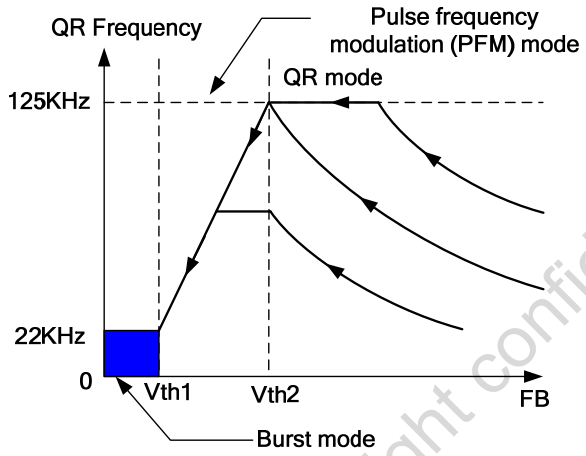


Figure 5

- **QR Demagnetization Detection (DEM pin)**

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. This voltage features a flyback polarity. A new cycle starts when the power switch is activated, as shown in Fig.6. After the on time (determined by the QR_CS voltage and FB), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_pC_d}$, where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.

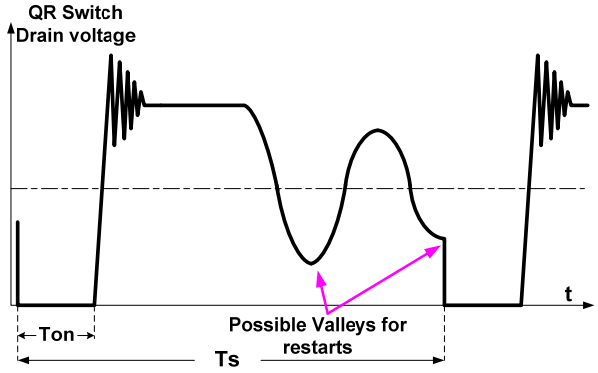


Figure 6

The typical detection level is fixed at 75mV at the DEM pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at DEM is below 75mV in falling edge. DEM detection is suppressed during the ringing suppression time Tsupp (please refer to "**Ringing Suppression Timer**" section).

- **QR Current Sensing and Leading Edge Blanking (QR_CS pin)**

Cycle-by-Cycle current limiting for the QR stage is offered in OB6663L. The switch current is detected by a sense resistor into the QR_CS pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state, the QR current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period.

- **Built-in Soft Start for QR**

The QR controller of OB6663L features a built-in 4ms soft start to soften the constraints occurring in the power supply during startup. It is activated after QR stage is enabled. As soon as QR stage begins to work after power on, the threshold voltage at QR_CS pin is gradually increased from nearly zero to the maximum clamping level 0.45V in 4ms. Every system restart attempt is followed by a QR soft start sequence.

- **Ringing Suppression Timer**

A ringing suppression timer Tsupp is implemented in the QR controller of OB6663L. In normal operation, Tsupp starts when QR_CS reaches the feedback voltage FB, the gate drive QR_OUT is set to low. During Tsupp, gate drive QR_OUT remains in low state and cannot turn power switch on gain. The ringing suppression is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup. In OB6663L, the ringing suppression timer Tsupp is set to 2us internally.

- **Maximum Frequency Clamp in QR operation**

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, when the output power decreases, the switching frequency can become rather high without limiting. To meet EMI limit starting at 150KHz, the maximum switching frequency in OB6663L is internally limited to 125KHz.

- **QR OCP Compensation**

A proprietary OCP compensation for QR stage is provided for better OCP performance in the universal input range. In this way, OCP point difference between high line input and low line input is minimized.

- **QR Output Over Voltage Protection (DEM pin)**

An output over voltage protection is implemented by sensing the auxiliary winding voltage at DEM pin during the flyback phase. The auxiliary winding voltage is a well-defined replica of the output voltage. The QR OVP works by sampling the plateau voltage at DEM pin during the flyback phase, as shown in Fig.7. A 2 us internal delay (plateau sampling) guarantees a clean plateau, provided that the leakage inductance ringing has been fully damped.

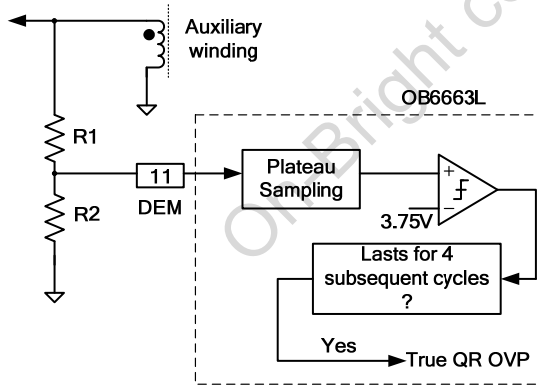


Figure 7

If the sampled plateau voltage exceeds the OVP trip level (3.75V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 4 cycles, the controller assumes a true OVP and it enters a latch off mode and stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level less than 4 successive cycles, the internal counter will be cleared and no fault is asserted.

- **QR Output Short Circuit Protection (DEM pin)**

An output short circuit protection is implemented by sensing the auxiliary winding voltage at DEM pin during the flyback phase. The QR output short detection start working after delay 10mS when QR controller starts working. The QR output short protection works by sampling the plateau voltage at DEM pin during the flyback phase. If the sampled plateau voltage less than 1V and lasting successive 4 cycles, the controller assumes a true output short occurrence and it enters restart mode and stops all switching operations. The special output short protection can minimize output short power consumption.

- **QR Over Load Operation (OLP)**

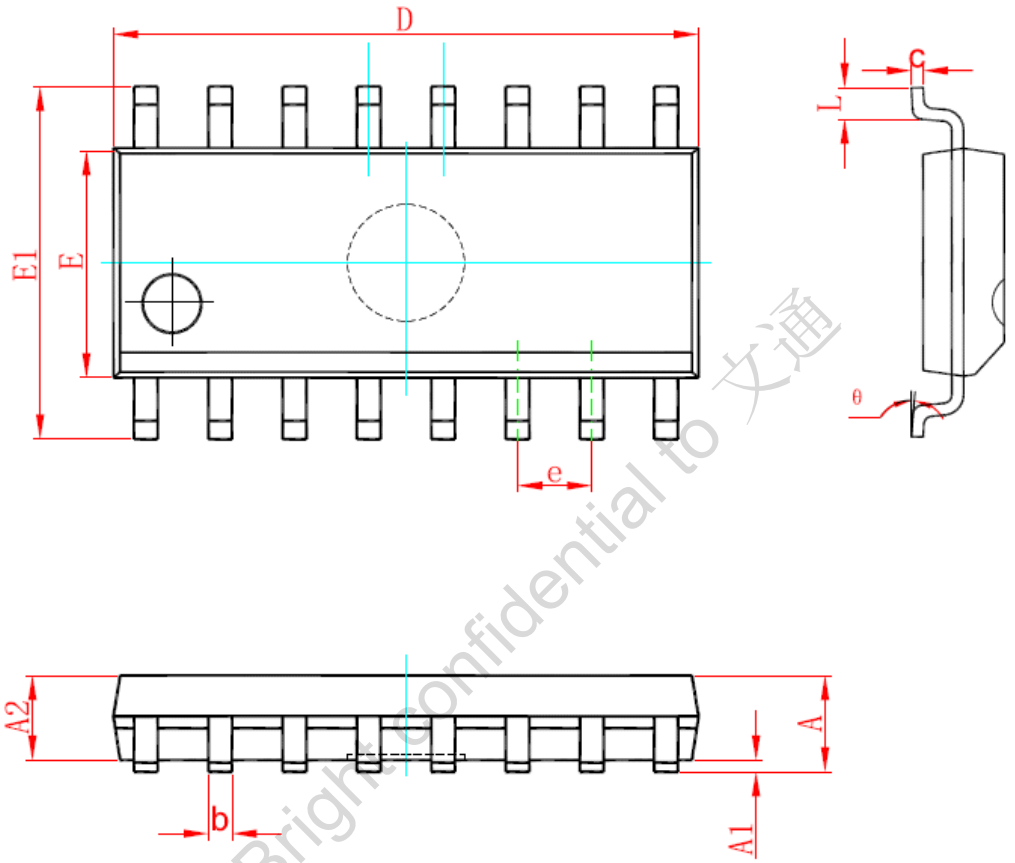
When over load (for example, short circuit or open loop) in the QR stage occurs, the feedback current for QR FB pin is below minimum value and a fault is detected. If this fault is present for more than 90ms, the controller enters an auto-recovery soft burst mode. All pulses for PFC and QR are stopped, VCC will drops below UVLO(ON) and the controller will try to restart with the power on soft start. The SMPS enters the burst sequence and it resumes operation once the fault disappears.

- **QR Gate Driver (QR_OUT Pin)**

The QR_OUT pin is connected to the gate of an external QR power switch with 1A capability. An internal 15V clamp is added for MOSFET gate protection at high VCC voltage. When VCC voltage drops below UVLO(ON), the QR_OUT pin is internally pull low to maintain the off state.

16-Pin Plastic SOP (SOP16)

SOP16 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	9.800	10.400	0.386	0.409
E	3.800	4.040	0.150	0.159
E1	5.800	6.240	0.228	0.246
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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